Mobile Diamondville Single Core Processor for Napa Small Form Factor with Intel 945GSE Express Chipset

Customer Reference Schematics

For Malata 81004

February 2008

Revision 1.4

Intel Confidential

MALATA		
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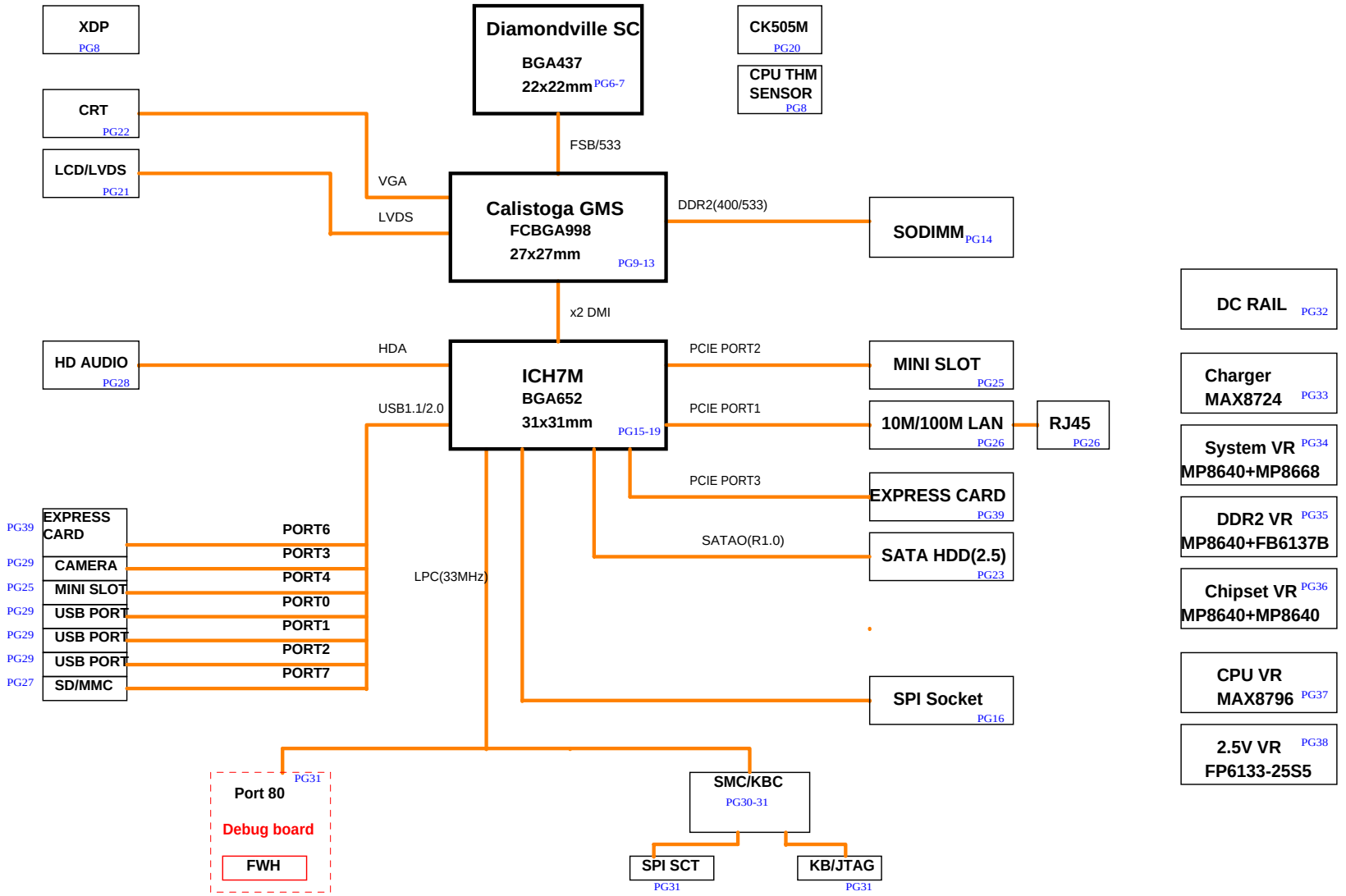
Mobile Diamondville SC with Intel 945GMS Express Chipset
Custormer Reference Board

FAB A **PB# E23308-002**
REV 1.2 **PBA# E23306-200**



MALATA		
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Voltage Rails

Power Plane	Description	Voltage	S0	S3	S4	S5
DCIN	Adapter power supply	19V	✓	✓	✓	✓
+VBATA	Battery power	6-8.4V	✓	✓	✓	✓
+VCC_CORE	Core voltage for CPU	0.5-1.2V	✓	✗	✗	✗
+V1.05S	Chipset Power Rail	1.05V	✓	✗	✗	✗
+V0.9	0.9V Reserved for DDR2 SSTL Term and COMP	0.9V	✓	✓	✗	✗
+V1.8	DDR2 SM	1.8V	✓	✓	✗	✗
+V1.5S	Chipset Power Rail	1.5V	✓	✗	✗	✗
+V2.5S	Chipset Int Gfx Power Rail	2.5V	✓	✗	✗	✗
+V3.3A_KSC	For EC	3.3V	✓	✓	✓	✓
+V3.3A	Peripheral Circuit	3.3V	✓	✓	✓	✗
+V3.3S	Peripheral Circuit	3.3V	✓	✗	✗	✗
+V5A	Peripheral Circuit	5V	✓	✓	✓	✗
+V5S	Peripheral Circuit	5V	✓	✗	✗	✗
+V15A	3.3V and 5V power rail gate power	15V	✓	✓	✓	✗

✓ ON
✗ OFF

CPU Core Power VID

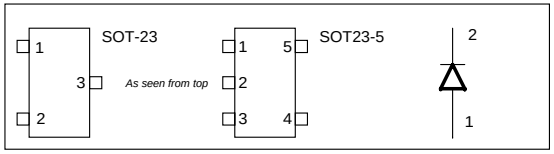
Vcc Boot Voltage typical is 1.1V							
VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vcc(V)
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
~	~	~	~	~	~	~	~
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000

Net Naming Conventions

Suffix
= Active Low Signal

Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



I 2 C / SMB Addresses

Device	Address	Hex	Bus
Clock Generator	1101 001x	D2	SMB_ICH_S
SO-DIMM0	1010 000x	A0	SMB_ICH_S
PCIE Mini Slot	TBD	TBD	SMB_ICH_A
CPU Thermal Sensor	1001 100x	98	SMB_EC_S
CPU Thermal Sensor*	1001 100b	4C	SMB_EC_A
Battery	TBD	TBD	SMB_EC_A
TPM Header	TBD	TBD	SMB_ICH_S
XDP	TBD	TBD	SMB_GMS_S

Jumper / Switch Settings

Jumper	Default	Description
PG1	Open	+V3.3S to LCD VDD
PG2	Short	DC IN
PG3	Short	DC IN
PG4	Short	+V3.3A Source
PG5	Short	+V3.3A Source
PG6	Short	+V5A Source
PG7	Short	+V5A Source
PG8	Short	+V1.05 Source(+V5A input)
PG9	Short	+V0.9 Source(+V1.8)
PG10	Open	+V0.9 Source(+V1.05S)
PG11	Short	+VCC_CORE Source(+VBAT)
PG12,PG15	Open	+VCC_CORE Source(+V5A)
PG13	Open	CMOS Clear
PG14	Open	Revserved for the LCD Gama power source
PG16,PG17	Open	Reserved for the Wimax card with PCI ECN Power input change
PG18	Short	For older version Mini card
PG19/PG20	Open	Reserved for the Mic Refrence input
PS1	Open	+V5S to LCD LED back light
PS2	Short	+VBAT to LCD CCFL Inverter
PS3	Short	+VBAT Input
PS4	Short	+VBAT Input
PS5	Short	+V3.3A Output
PS6	Short	+V5A Output
PS7	Short	+V1.05S Output
PS8	Short	+V1.5S Output
PS9	Short	+V1.8 Output
PS10	Short	+VCC_CORE Output
PS11	Short	+VCC_CORE Output
J35	All Open	CPU VID Selection
J37	1-x	Boot BIOS selection
J43	1-x	EC test mode select, if short 1-2, all IO should force to floating

Power States

SIGNAL / STATE	PM_EN_5VA_3VA#	PM_SLP_S4#	PM_SLP_S3#	+V*A	+V*	+V*S	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	HIGH	HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend To Disk)	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	OFF	OFF	OFF	OFF

LEDs and Switches

LED	Page	Reference
VID0	37	CR30
VID1	37	CR31
VID2	37	CR32
VID3	37	CR33
VID4	37	CR34
VID5	37	CR35
VID6	37	CR36
Num Lock	30	CR13
Caps Lock	30	CR12
Power on	30	CR29
Battery full	30	CR11
Batter charging	30	CR11
HDD	30	CR14
WL	30	CR15

Switch	Default	Description	Page
SW1		Power Button	31
SW2		Touchpad Left Button	31
SW3		Touchpad Right Button	31
U26		Lid SW	30

MALATA

Title: Notes

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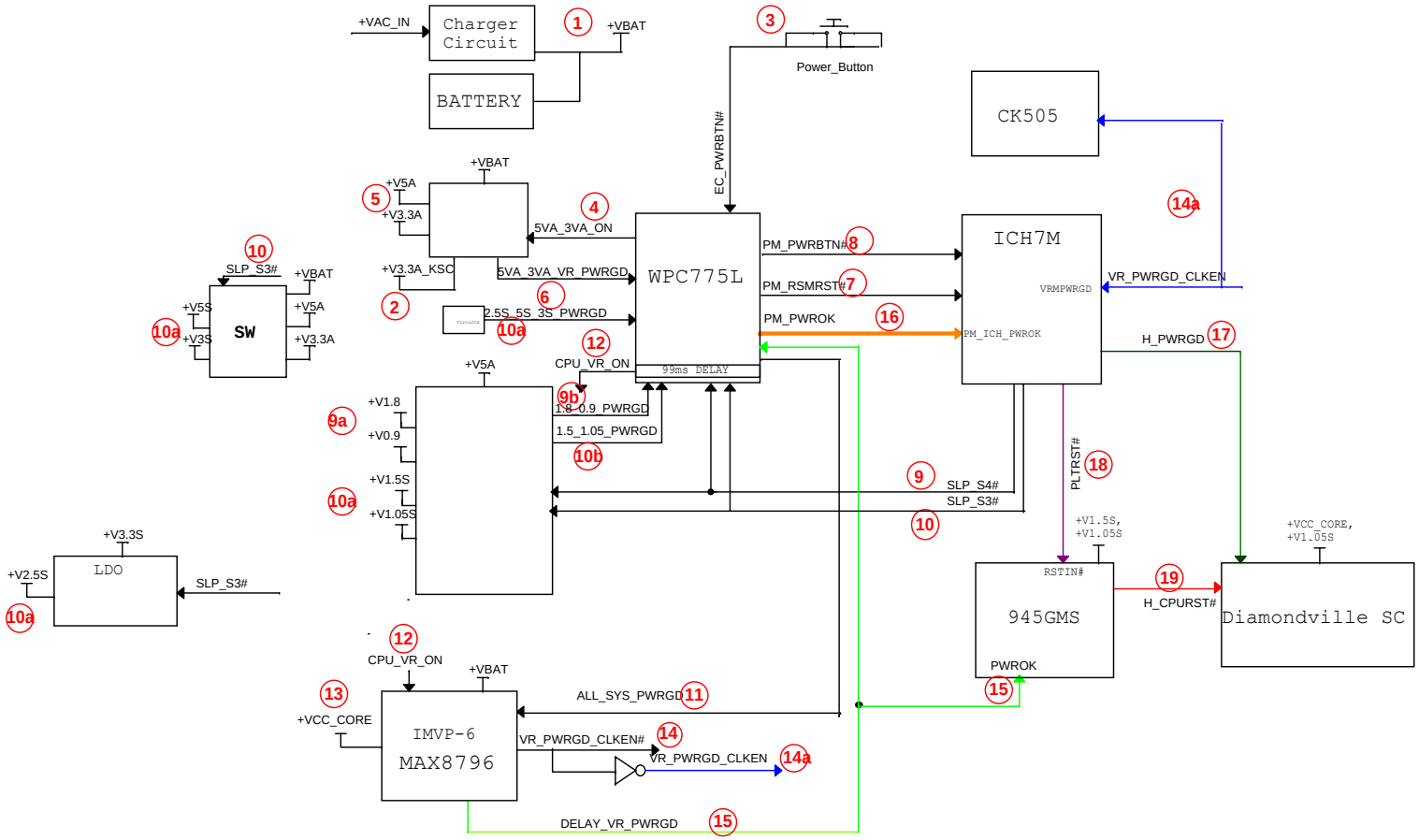

MALATA		
Title: Power on block		
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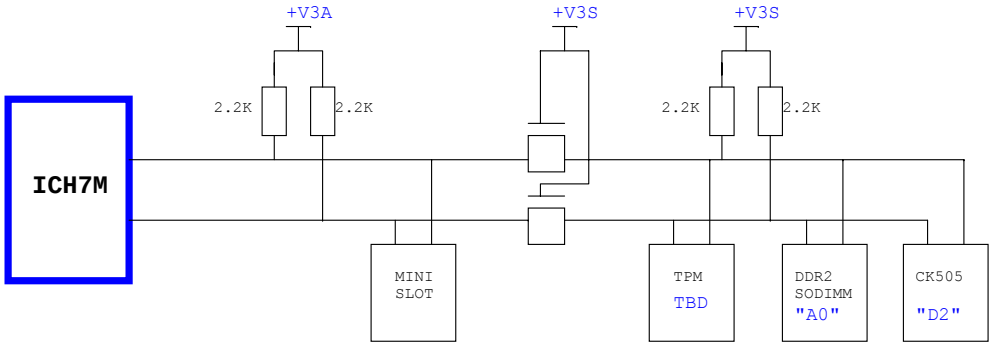

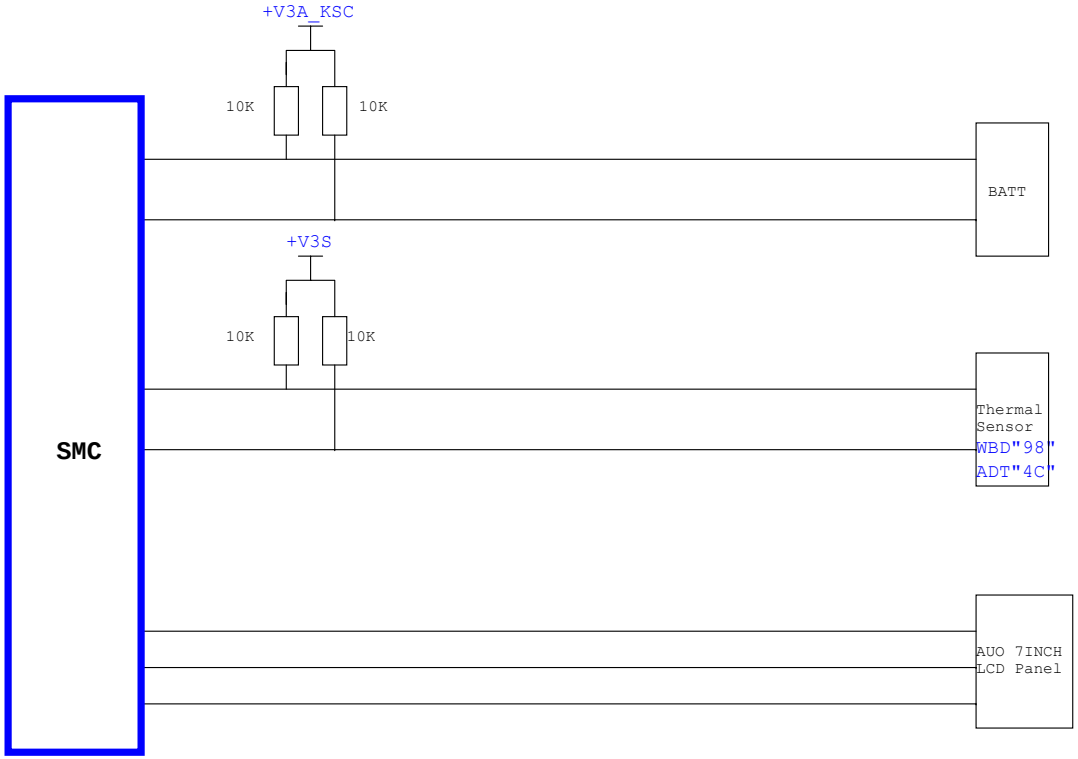

MALATA		
Title: SMBus topology		
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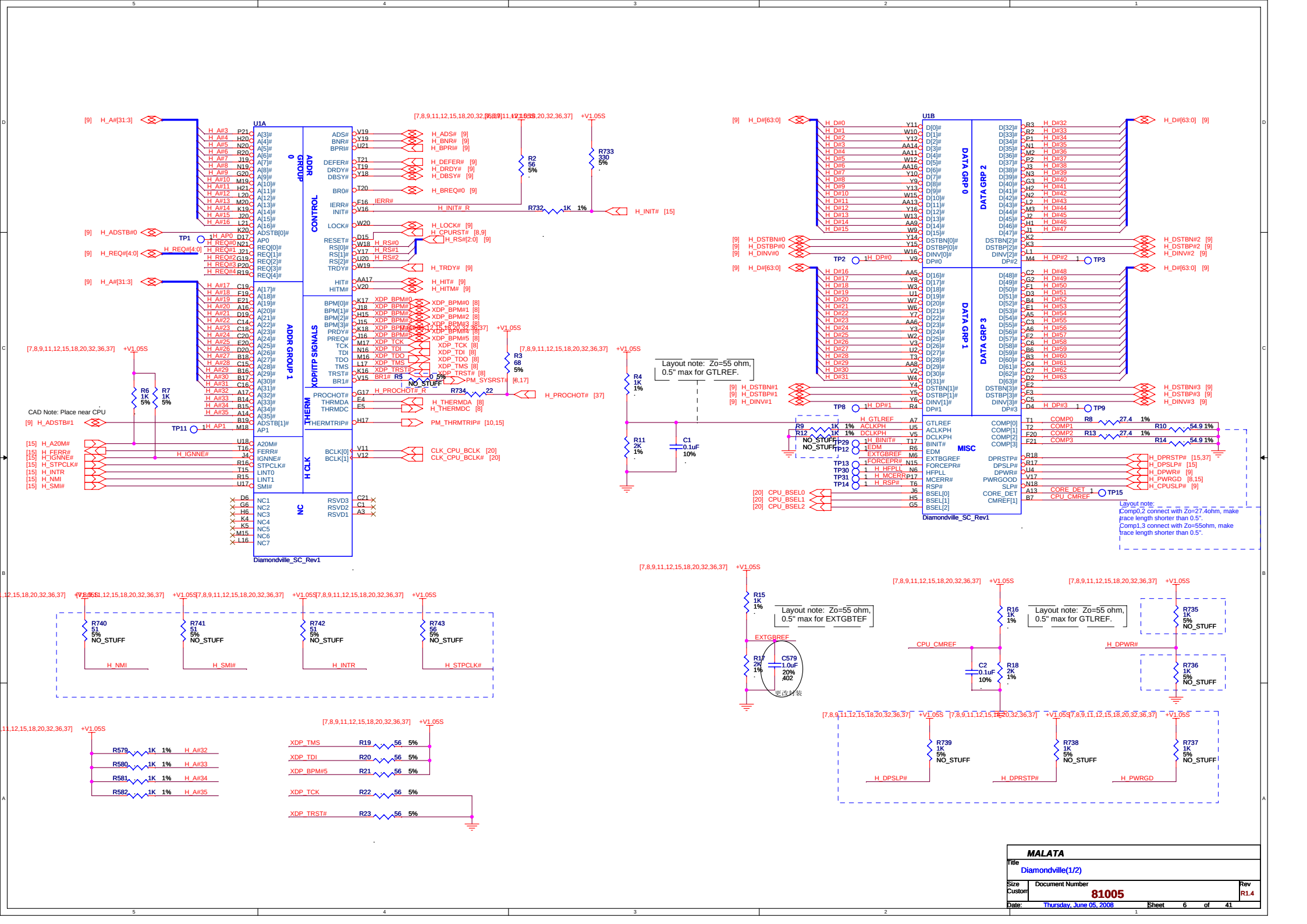
U1A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
NC
Diamondville_SC_Rev1
U1B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Diamondville_SC_Rev1
CAD Note: Place near CPU
Layout note: Zo=55 ohm, 0.5" max for GTLREF.
Layout note: Zo=55 ohm, 0.5" max for EXTGBTEF
Layout note: Zo=55 ohm, 0.5" max for GTLREF.
Layout note:
Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5".
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5".
MALATA
Title
Diamondville(1/2)
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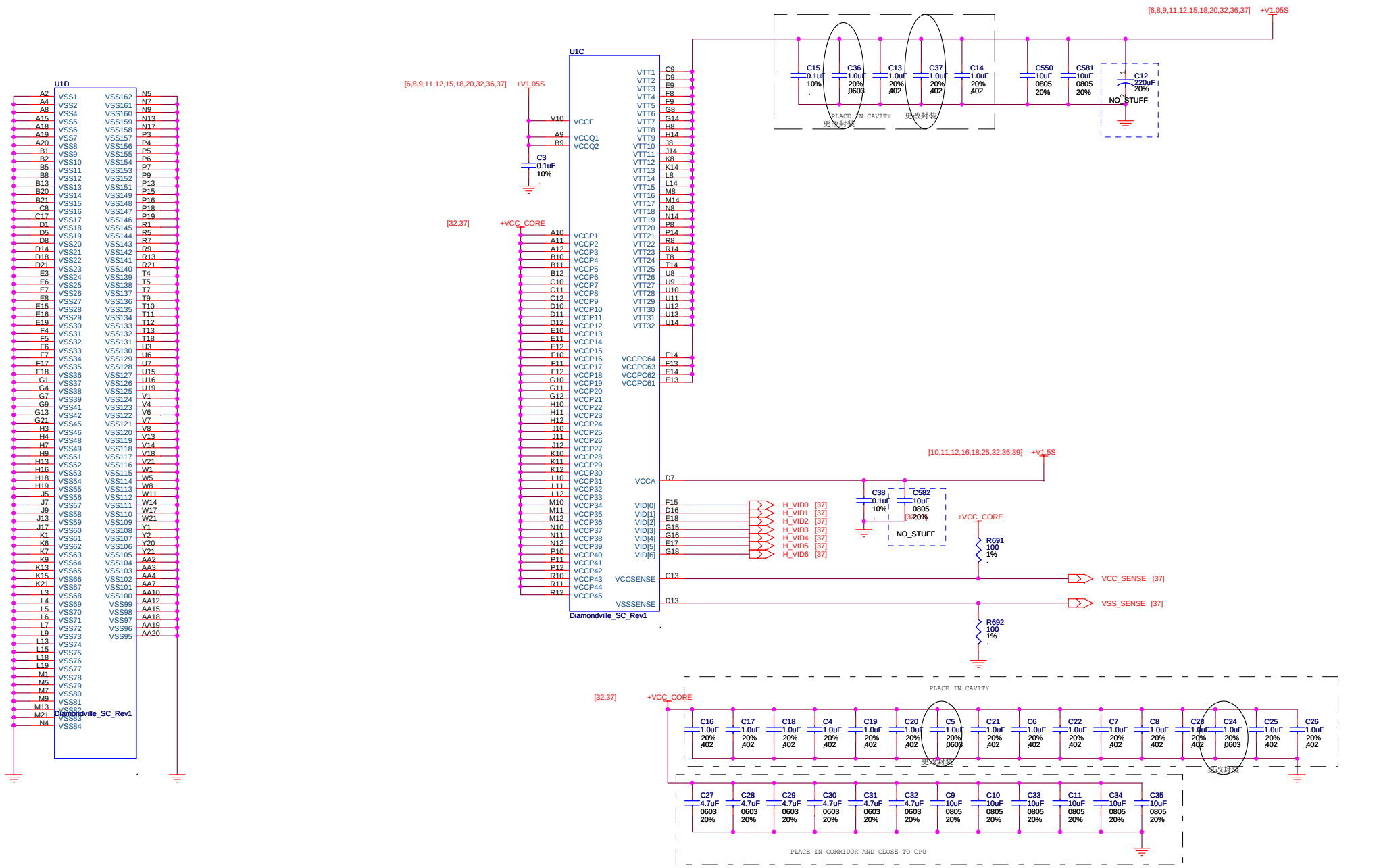

MALATA			
Title: Diamondville(2/2)			
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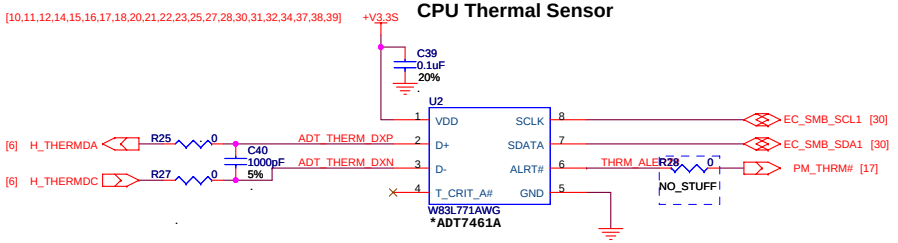
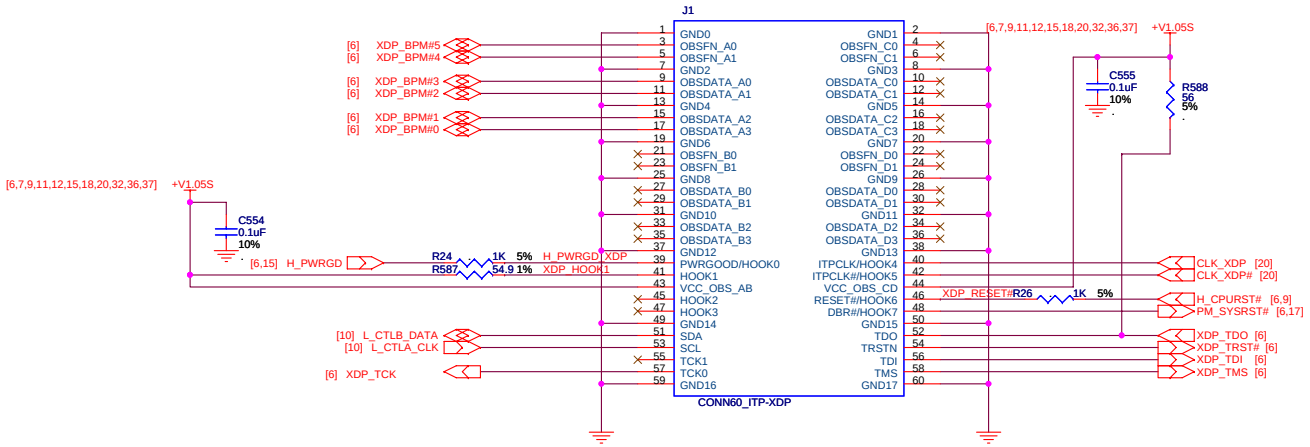
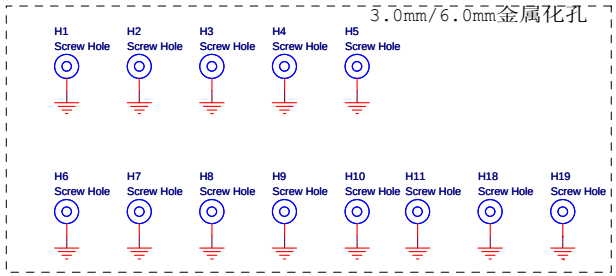
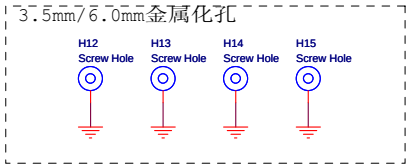
CPU Thermal Sensor

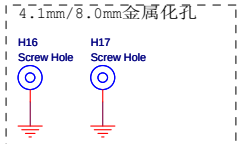


Labels









MALATA		
Title: XDP and THRM		
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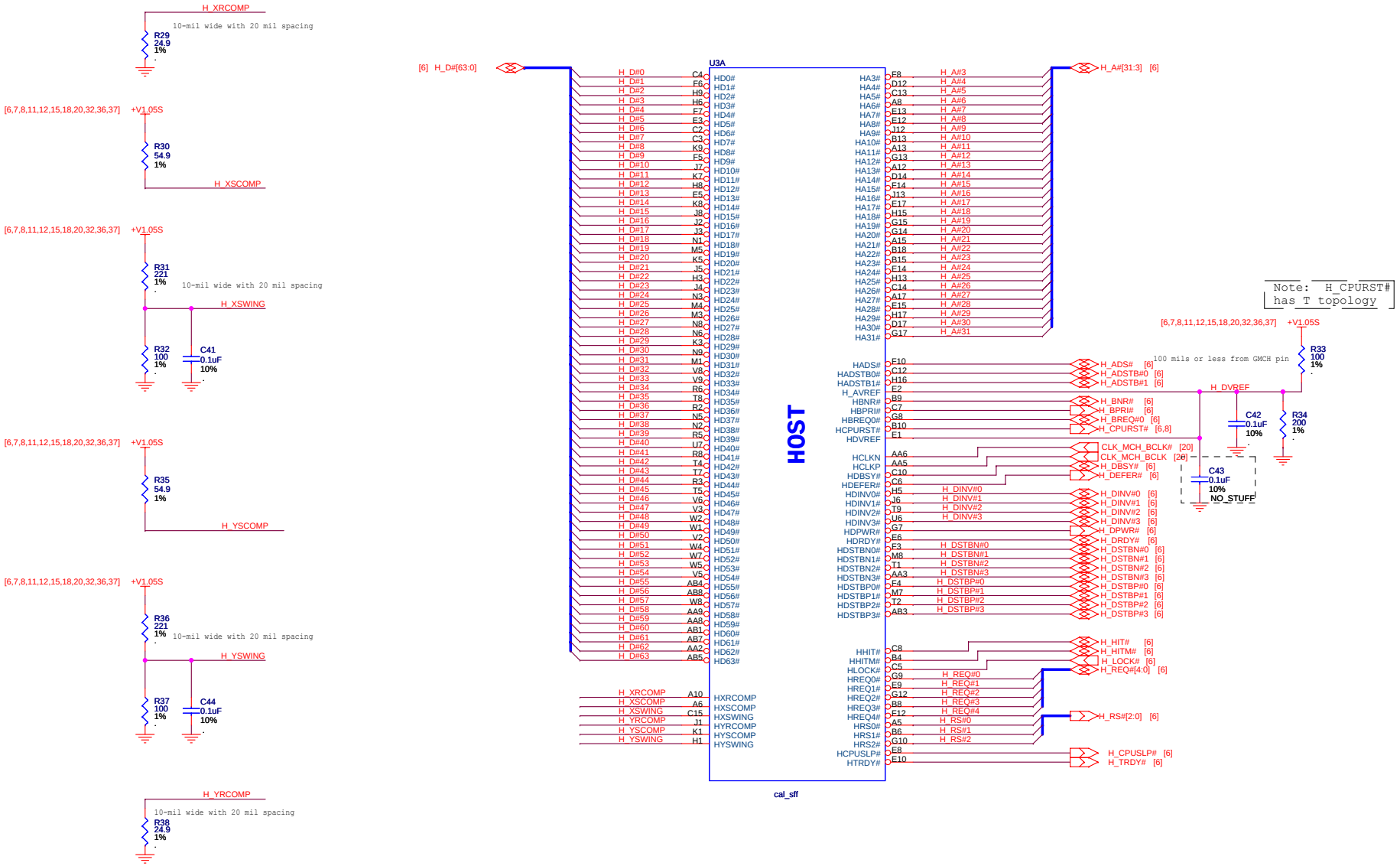

MALATA		
Title	945GMS(1/5)	
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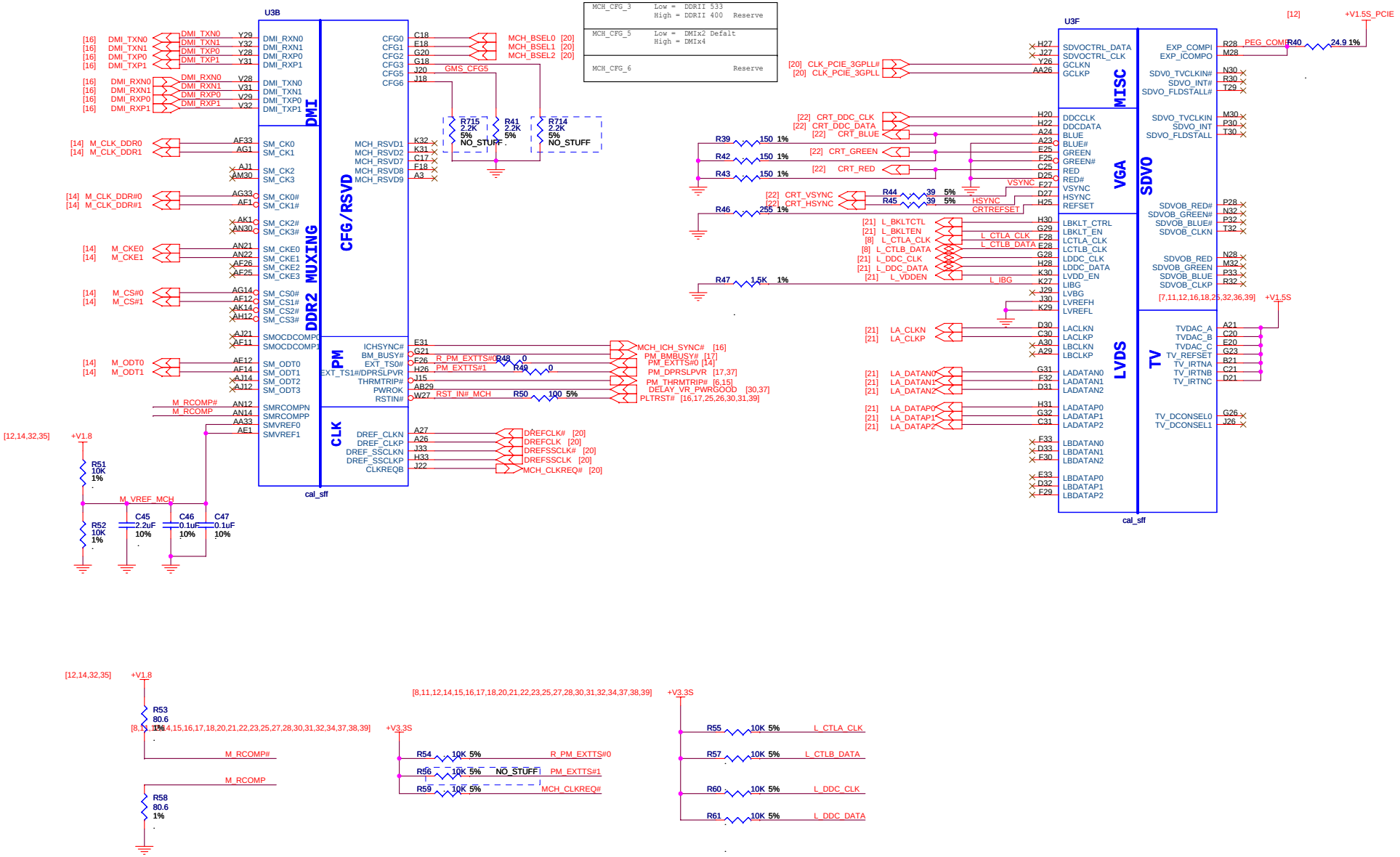
U3B
DMI
DDR2 MUXING
CFG/RSVD
PM
CLK
cal_sff
MCH_CFG_3 Low = DDRII 533 High = DDRII 400 Reserve
MCH_CFG_5 Low = DMIx2 Defalt High = DMIx4
MCH_CFG_6 Reserve
U3F
MISC
VGA
SDVO
LVDS
TV
cal_sff
MALATA
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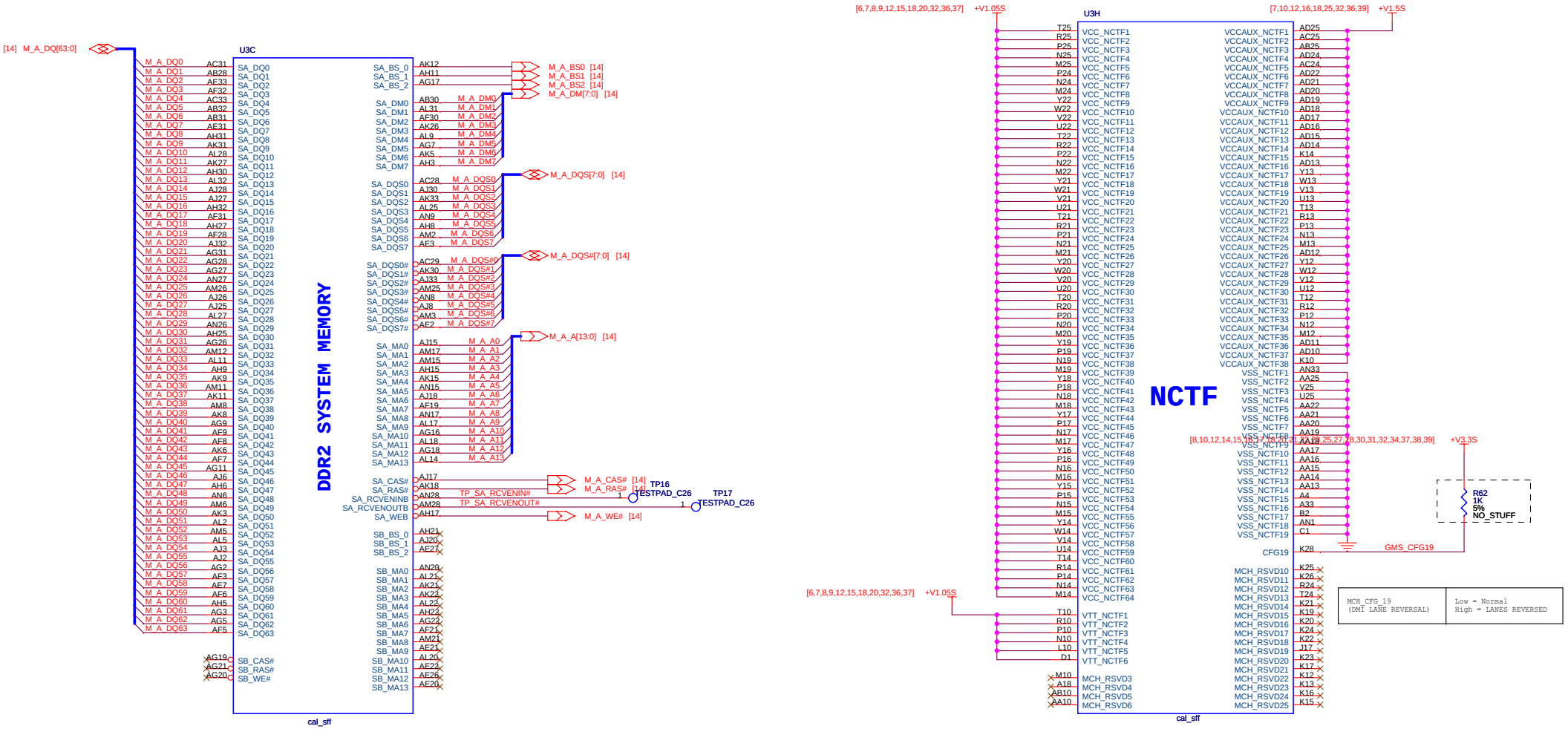

MALATA

Title: 945GMS(3/5)

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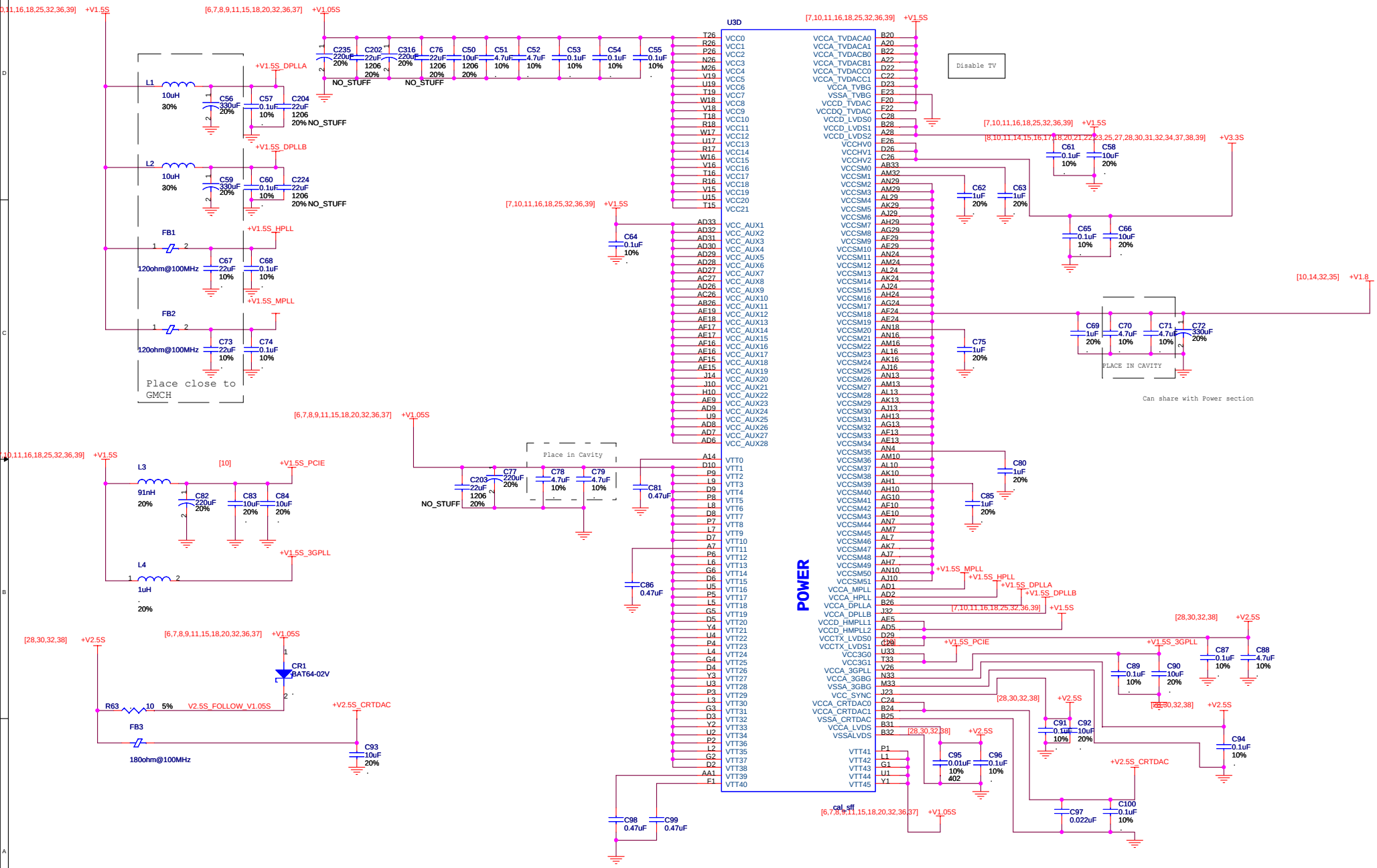

MALATA			
Title	945GMS(4/5)		
Size: Custom	Document Number: 81005		Rev: R1.4
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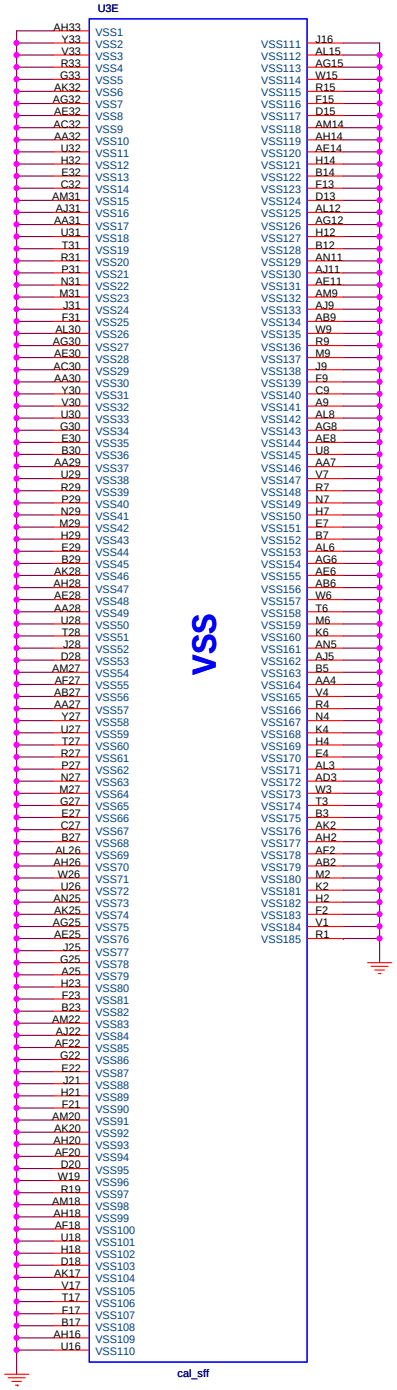

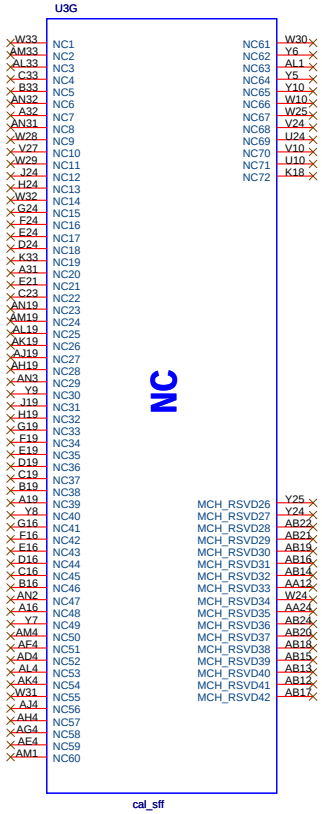

MALATA			
Title: 945GMS(5/5)			
Size: Custom	Document Number: 81005		Rev: R1.4
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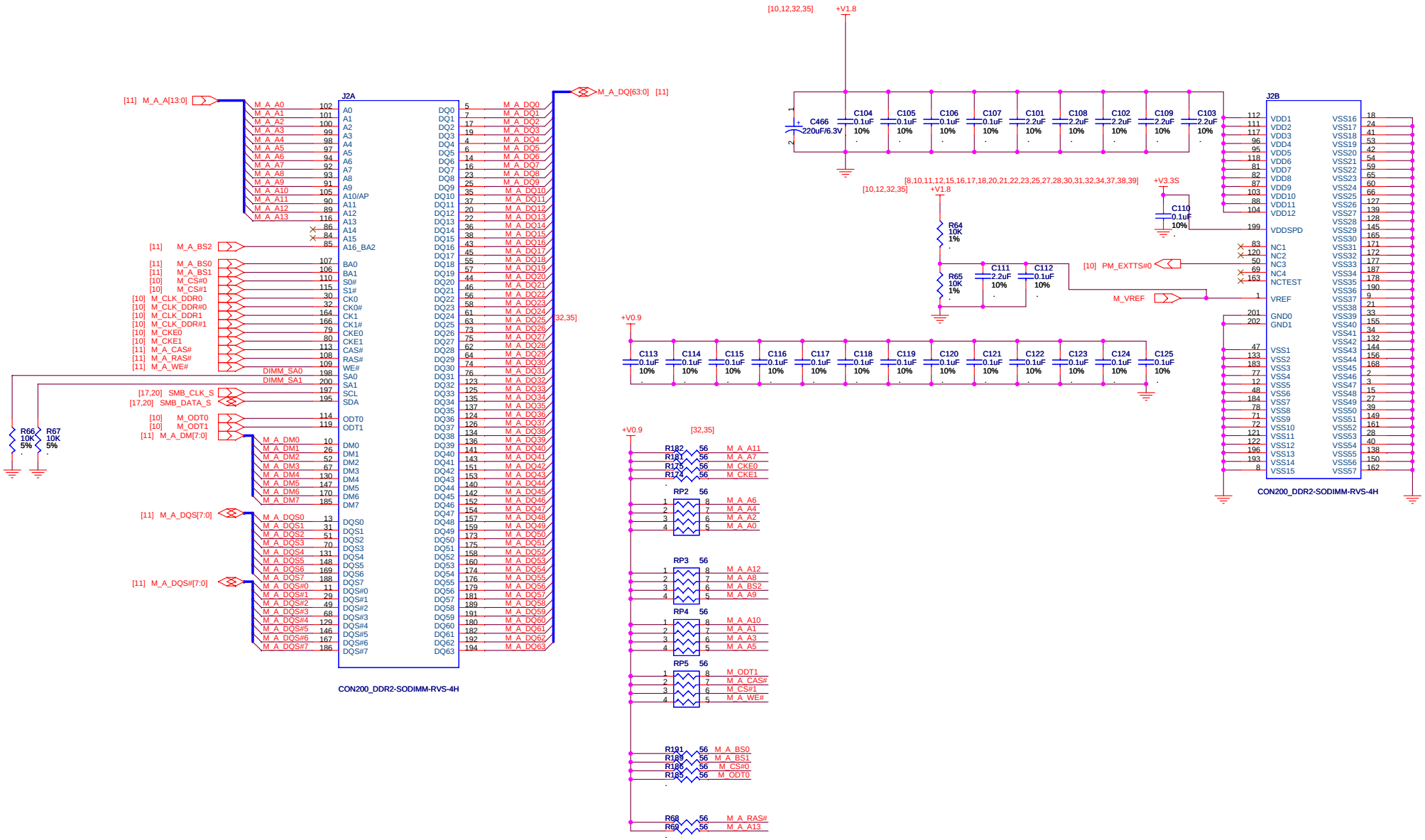

Title	DDR2 SO-DIMM
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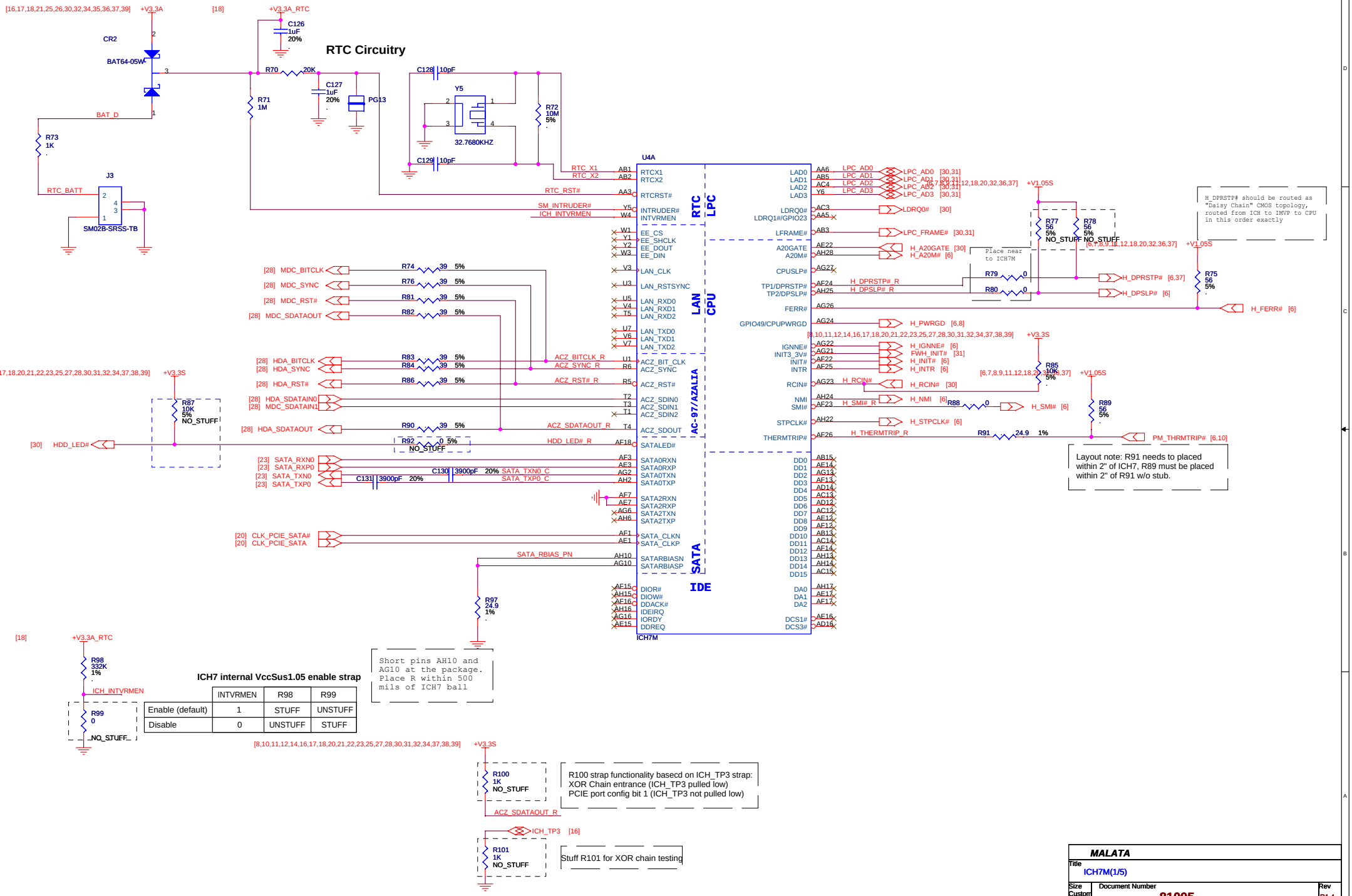
RTC Circuitry
U4A
ICH7M
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
J3
SM02B-SRSS-TB
BAT64-05W
Y5
32.7680KHZ
ICH7 internal VccSus1.05 enable strap
INTVRMEN
R98
R99
Short pins AH10 and AG10 at the package. Place R within 500 mils of ICH7 ball
R100 strap functionality basecd on ICH_TP3 strap:
XOR Chain entrance (ICH_TP3 pulled low)
PCIE port config bit 1 (ICH_TP3 not pulled low)
Stuff R101 for XOR chain testing
H_DPRSTP# should be routed as "Daisy Chain" CMOS topology, routed from ICH to IMVP to CPU in this order exactly
Layout note: R91 needs to placed within 2" of ICH7, R89 must be placed within 2" of R91 w/o stub.
MALATA
ICH7M(1/5)
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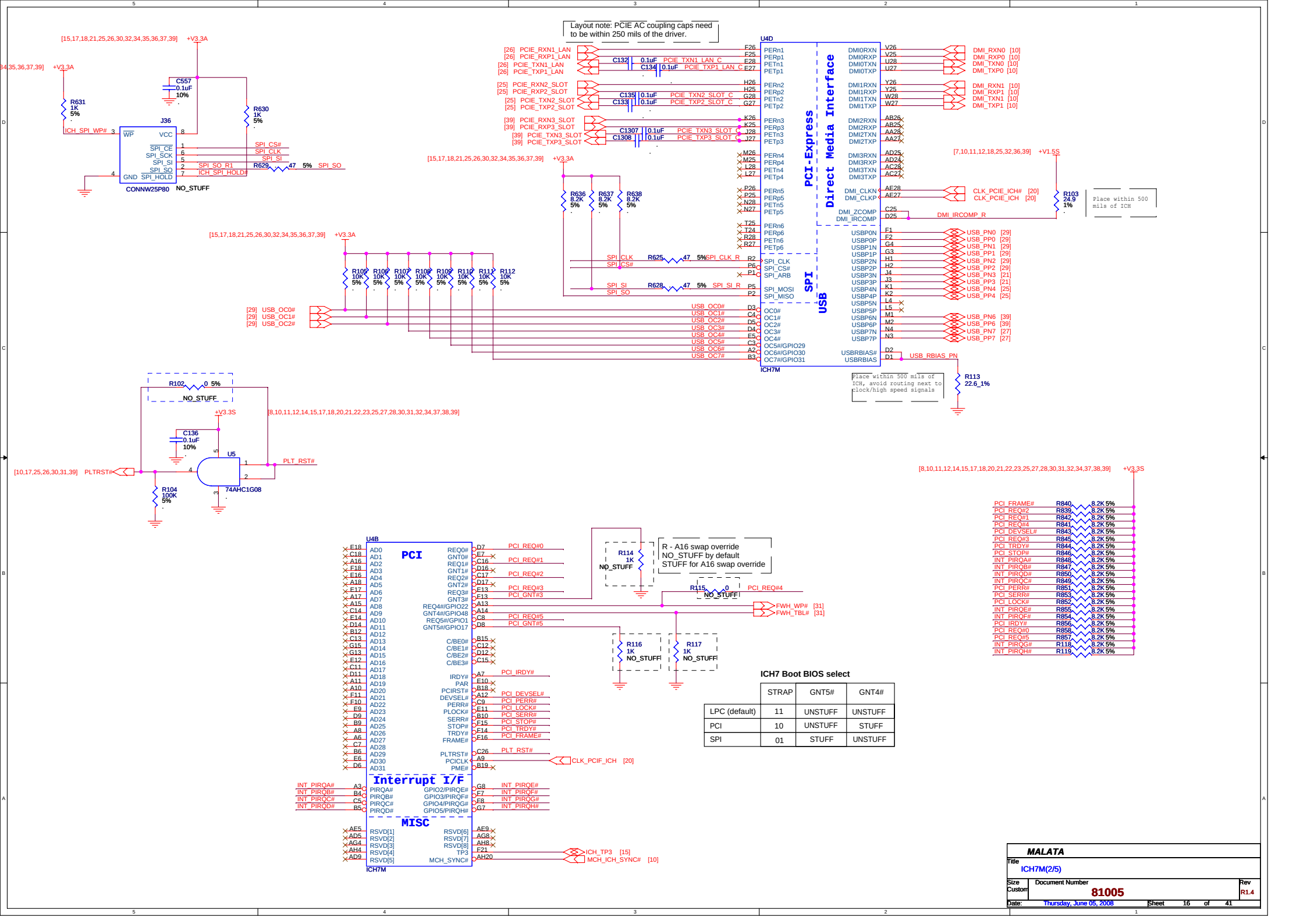
Layout note: PCIE AC coupling caps need to be within 250 mils of the driver.
U4D
PCI-Express
Direct Media Interface
SPI
USB
ICH7M
J36
CONNW25P80
NO_STUFF
U4B
PCI
Interrupt I/F
MISC
ICH7M
R - A16 swap override
NO_STUFF by default
STUFF for A16 swap override
ICH7 Boot BIOS select
STRAP
GNT5#
GNT4#
LPC (default) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
Place within 500 mils of ICH
Place within 500 mils of ICH, avoid routing next to clock/high speed signals
MALATA
Title
ICH7M(2/5)
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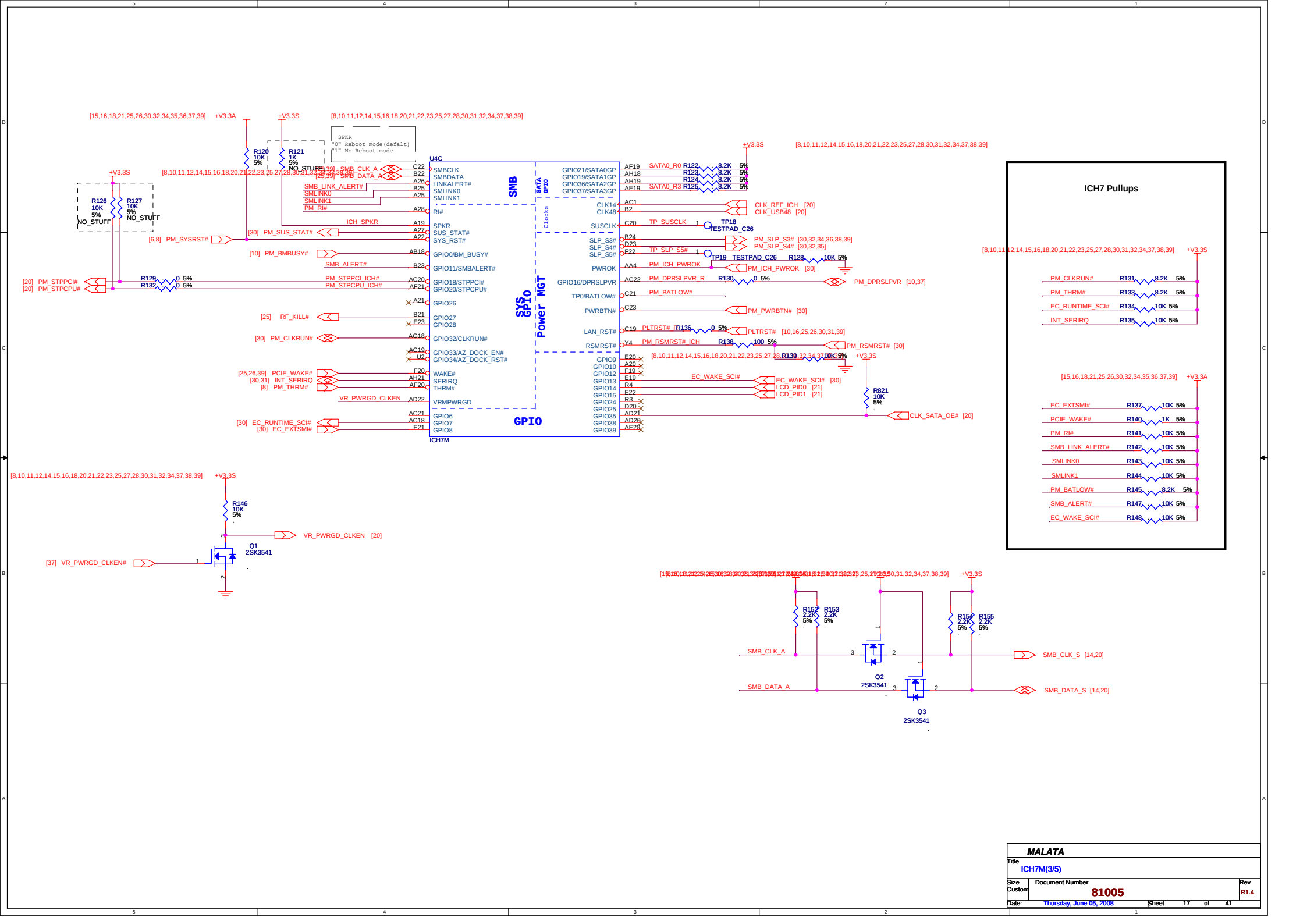

MALATA		
Title: ICH7M(3/5)		
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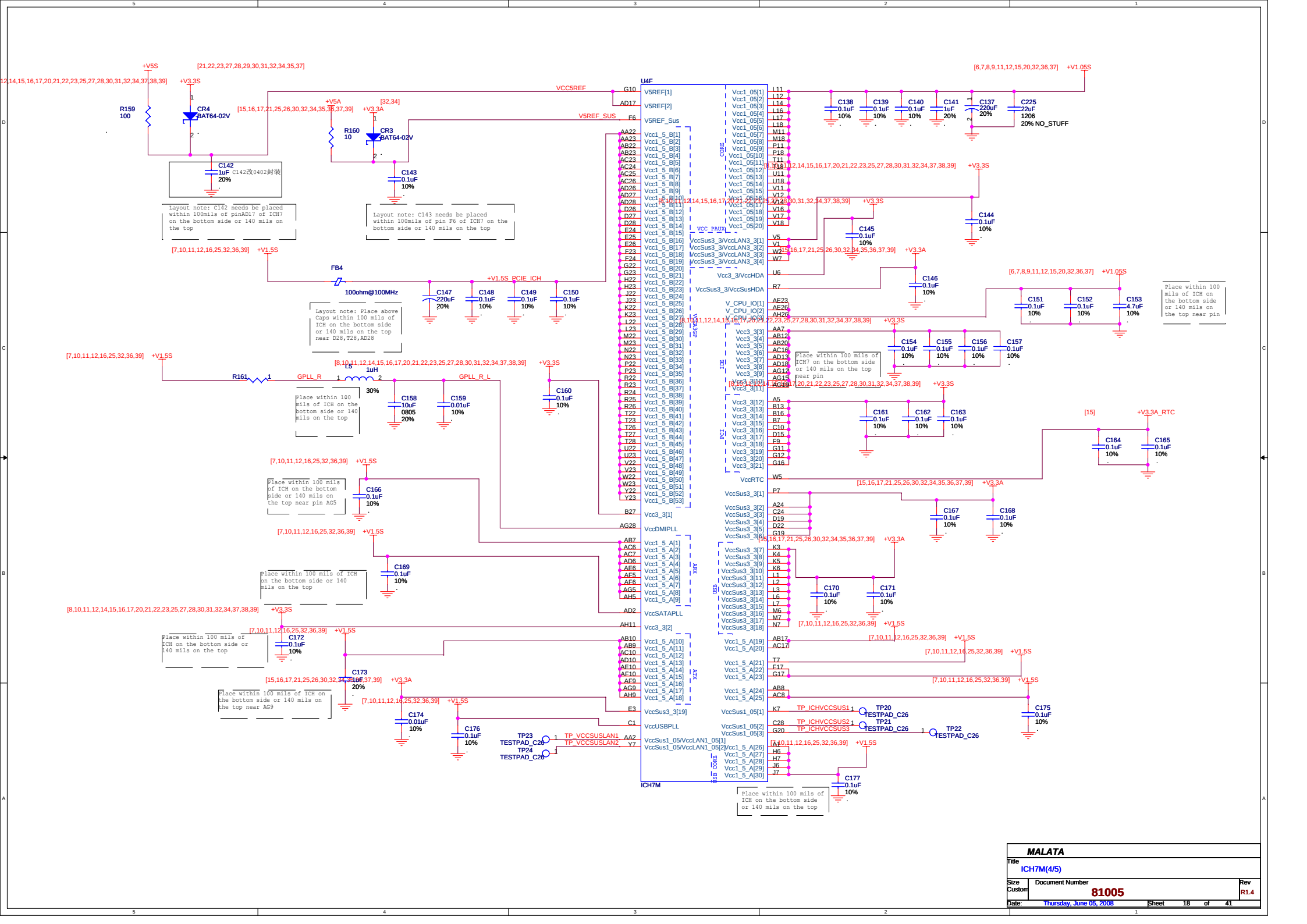
U4F
ICH7M
R159 100
CR4 BAT64-02V
R160 10
CR3 BAT64-02V
R161
L5 1uH
FB4 100ohm@100MHz
C142 1uF 20% C142改0402封装
C143 0.1uF 10%
C147 220uF 20%
C148 0.1uF 10%
C149 0.1uF 10%
C150 0.1uF 10%
C158 10uF 0805 20%
C159 0.01uF 10%
C160 0.1uF 10%
C166 0.1uF 10%
C169 0.1uF 10%
C172 0.1uF 10%
C173 1uF 20%
C174 0.01uF 10%
C176 0.1uF 10%
C138 0.1uF 10%
C139 0.1uF 10%
C140 0.1uF 10%
C141 1uF 20%
C137 220uF 20%
C225 22uF 1206 20% NO_STUFF
C144 0.1uF 10%
C145 0.1uF 10%
C146 0.1uF 10%
C151 0.1uF 10%
C152 0.1uF 10%
C153 4.7uF 10%
C154 0.1uF 10%
C155 0.1uF 10%
C156 0.1uF 10%
C157 0.1uF 10%
C161 0.1uF 10%
C162 0.1uF 10%
C163 0.1uF 10%
C164 0.1uF 10%
C165 0.1uF 10%
C167 0.1uF 10%
C168 0.1uF 10%
C170 0.1uF 10%
C171 0.1uF 10%
C175 0.1uF 10%
C177 0.1uF 10%
TP20 TESTPAD_C26
TP21 TESTPAD_C26
TP22 TESTPAD_C26
TP23 TESTPAD_C26
TP24 TESTPAD_C26
Layout note: C142 needs be placed within 100mils of pinAD17 of ICH7 on the bottom side or 140 mils on the top
Layout note: C143 needs be placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top
Layout note: Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28,T28,AD28
Place within 100 mils of ICH on the bottom side or 140 mils on the top
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin
Place within 100 mils of ICH7 on the bottom side or 140 mils on the top near pin
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG5
Place within 100 mils of ICH on the bottom side or 140 mils on the top
Place within 100 mils of ICH on the bottom side or 140 mils on the top
Place within 100 mils of ICH on the bottom side or 140 mils on the top near AG9
Place within 100 mils of ICH on the bottom side or 140 mils on the top
+V5S
+V3.3S
+V5A
+V3.3A
+V1.5S
+V1.5S_PCIE_ICH
+V1.05S
+V3.3A_RTC
VCC5REF
V5REF_SUS
GPLL_R
GPLL_R_L
TP_ICHVCCSUS1
TP_ICHVCCSUS2
TP_ICHVCCSUS3
TP_VCCSUSLAN1
TP_VCCSUSLAN2
MALATA
Title
ICH7M(4/5)
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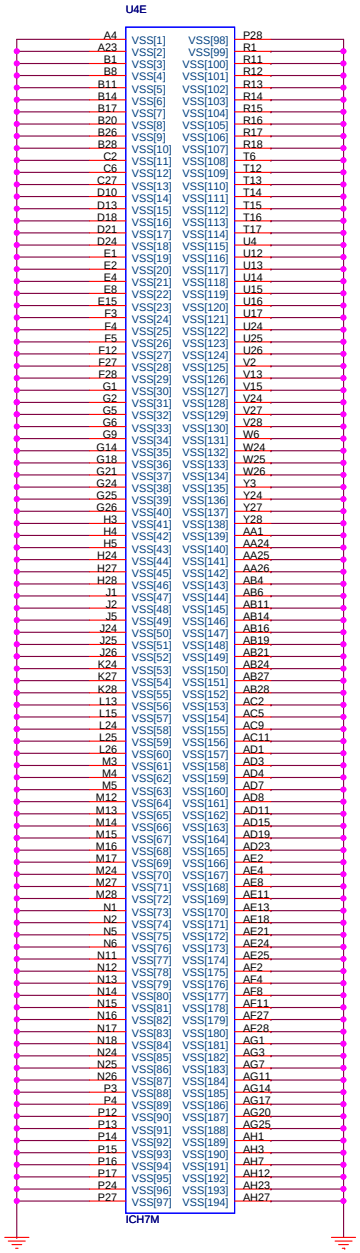

MALATA		
Title: ICH7M(5/5)		
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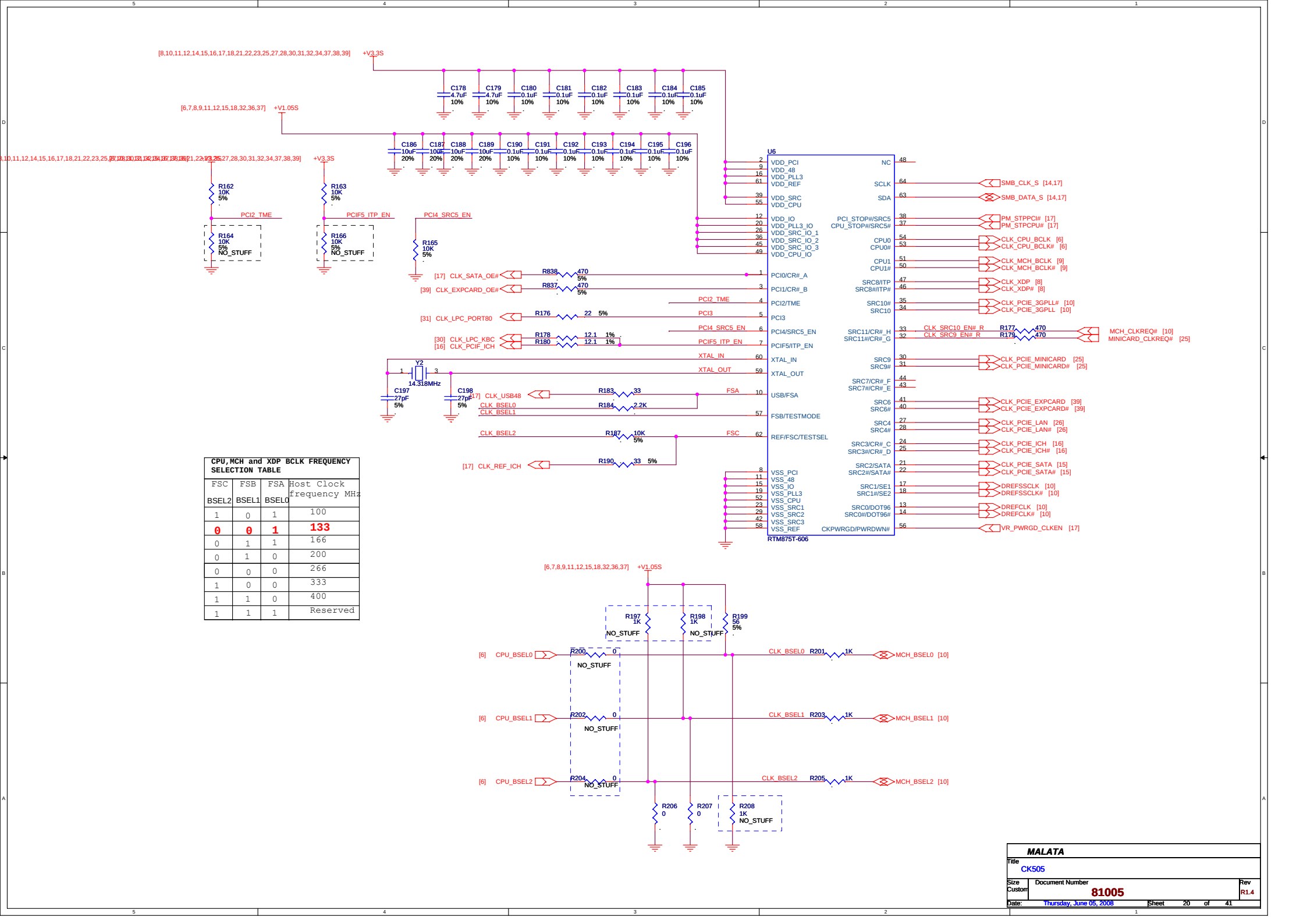

CPU,MCH and XDP BCLK FREQUENCY SELECTION TABLE

FSC BSEL2	FSB BSEL1	FSA BSEL0	Host Clock frequency MHz
1	0	1	100
0	**0**	**1**	**133**
0	1	1	166
0	1	0	200
0	0	0	266
1	0	0	333
1	1	0	400
1	1	1	Reserved

MALATA

Title: CK505

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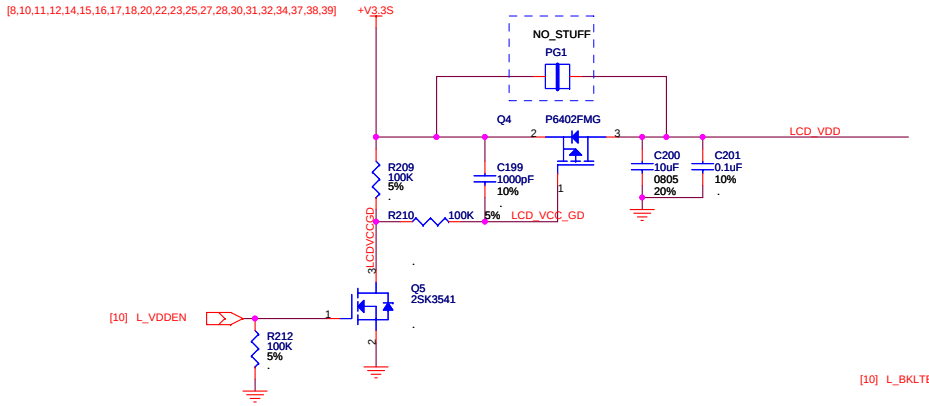
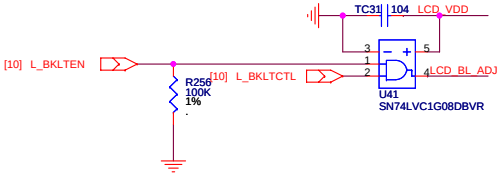
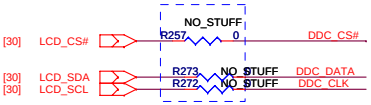
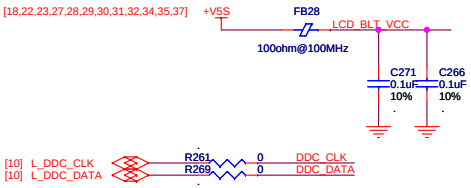
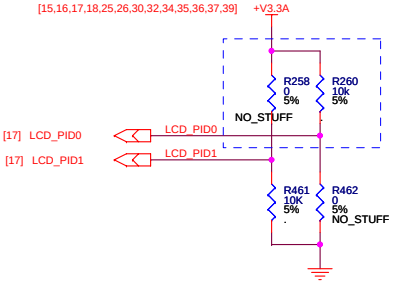






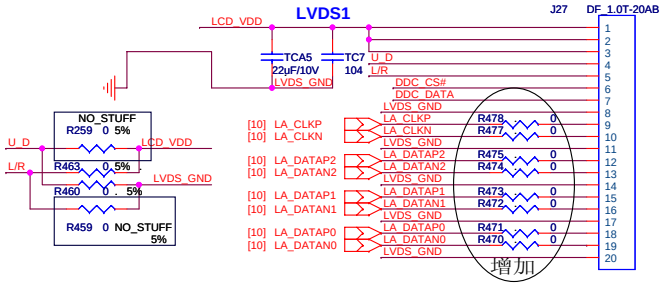
预留

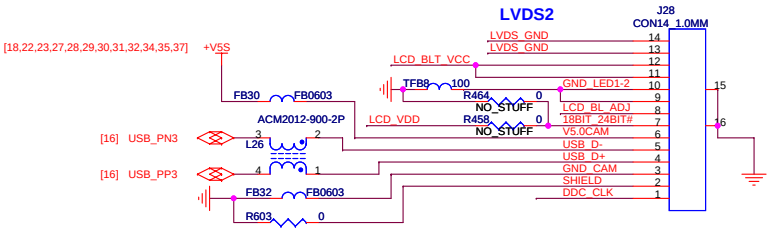




Panel ID Table

PID1	PID0	LCD Panel Type
0	0	8inch w/ LVDS Interface(CMPC used)
0	1	10inch w/ LVDS Interface(CMPC used)
1	0	
1	1	





MALATA			
Title: LVDS			
Size: Custom	Document Number: 81005		Rev: R1.4
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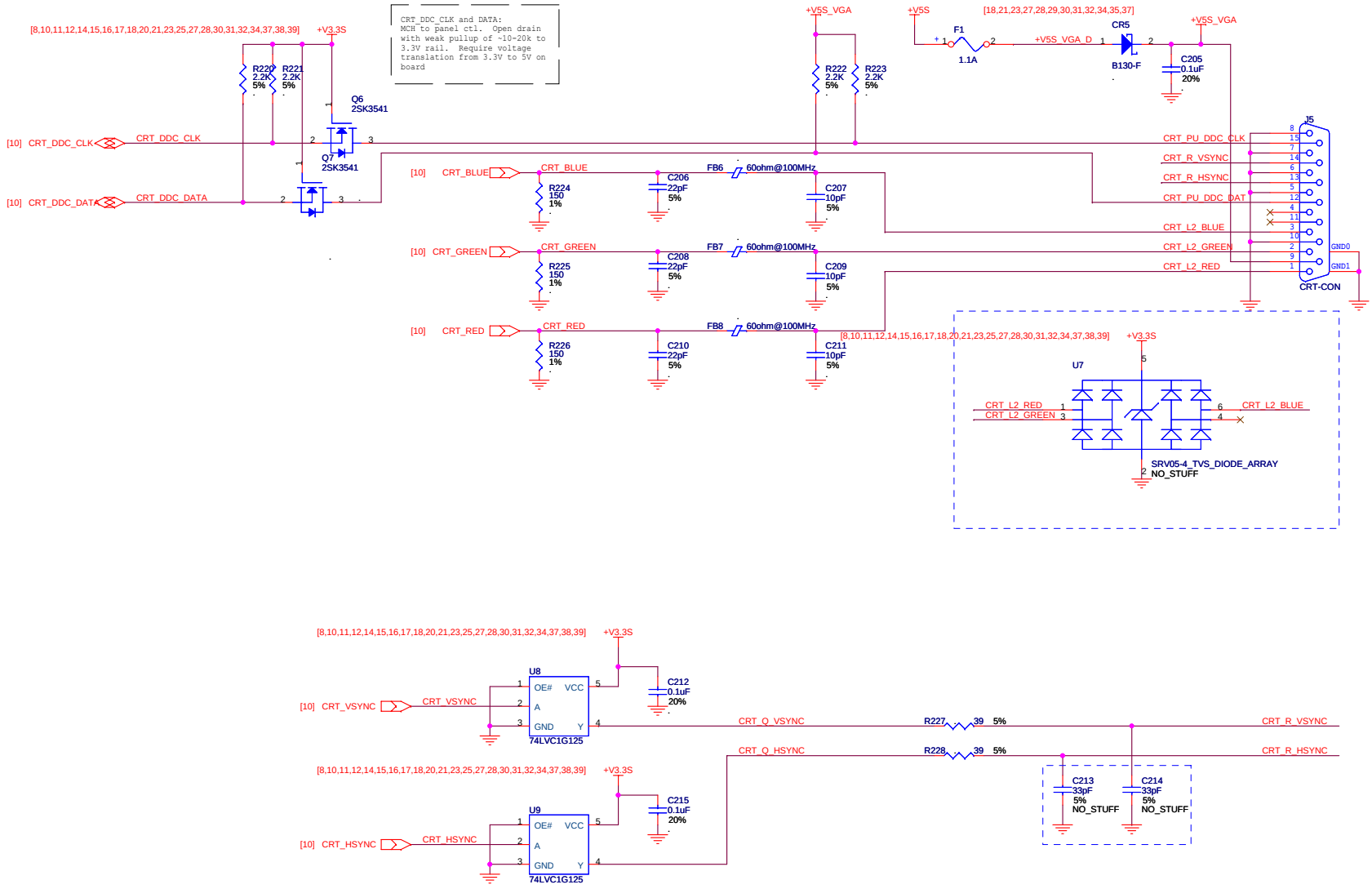
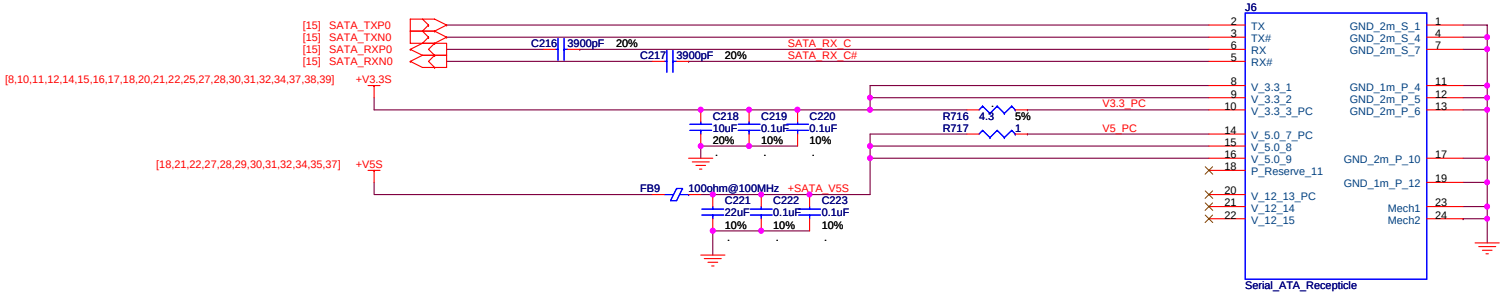
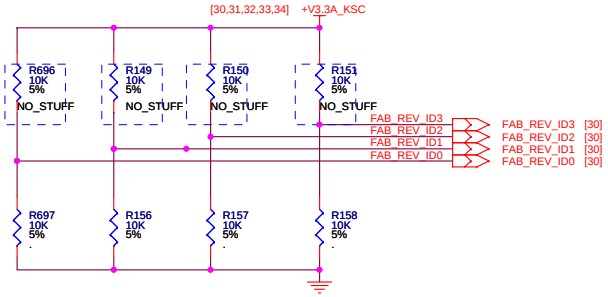


MALATA		
Title: CRT Port		
Size: Custom	Document Number: 81005	Rev: R1.4
Date: Thursday, June 05, 2008	Sheet 22 of 41	





FAB ID Strapping Table

FAB_REV_ID				BOARD FAB
FAB_REV_ID3	FAB_REV_ID2	FAB_REV_ID1	FAB_REV_ID0	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

MALATA		
Title: SATA Connector		
Size: Custom	Document Number: 81005	Rev: R1.4
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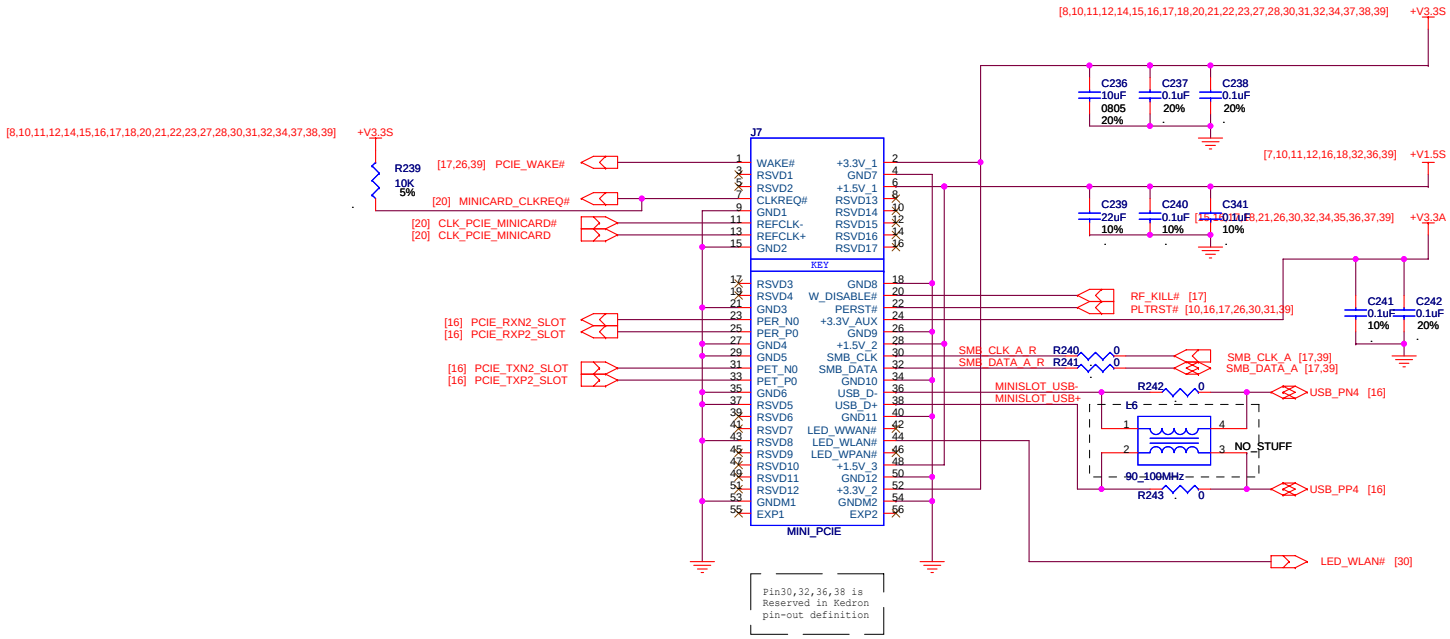

MALATA			
Title: Mini Slot/LPC HDR/Program HDR			
Size: Custom	Document Number: 81005		Rev: R1.4
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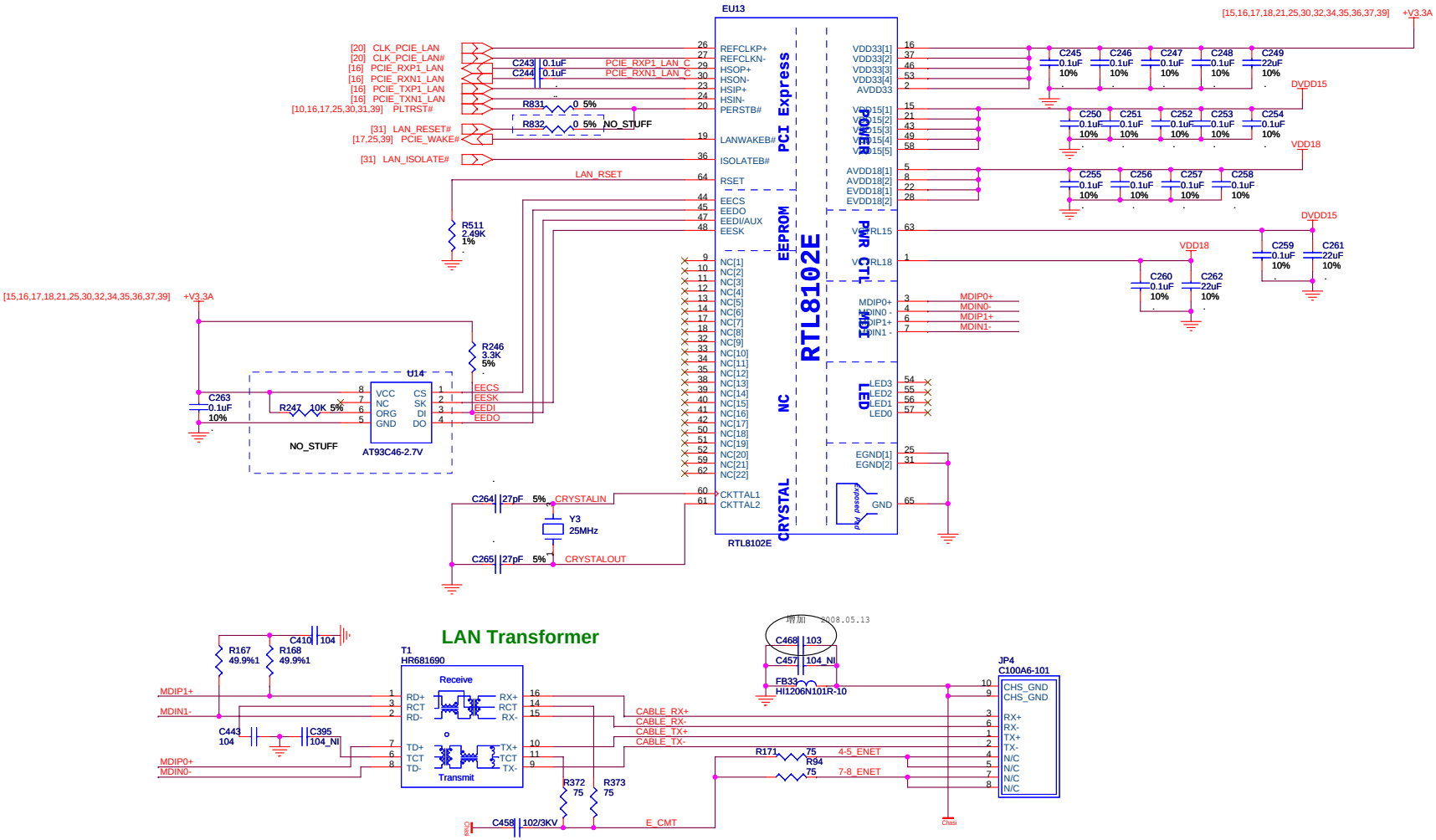
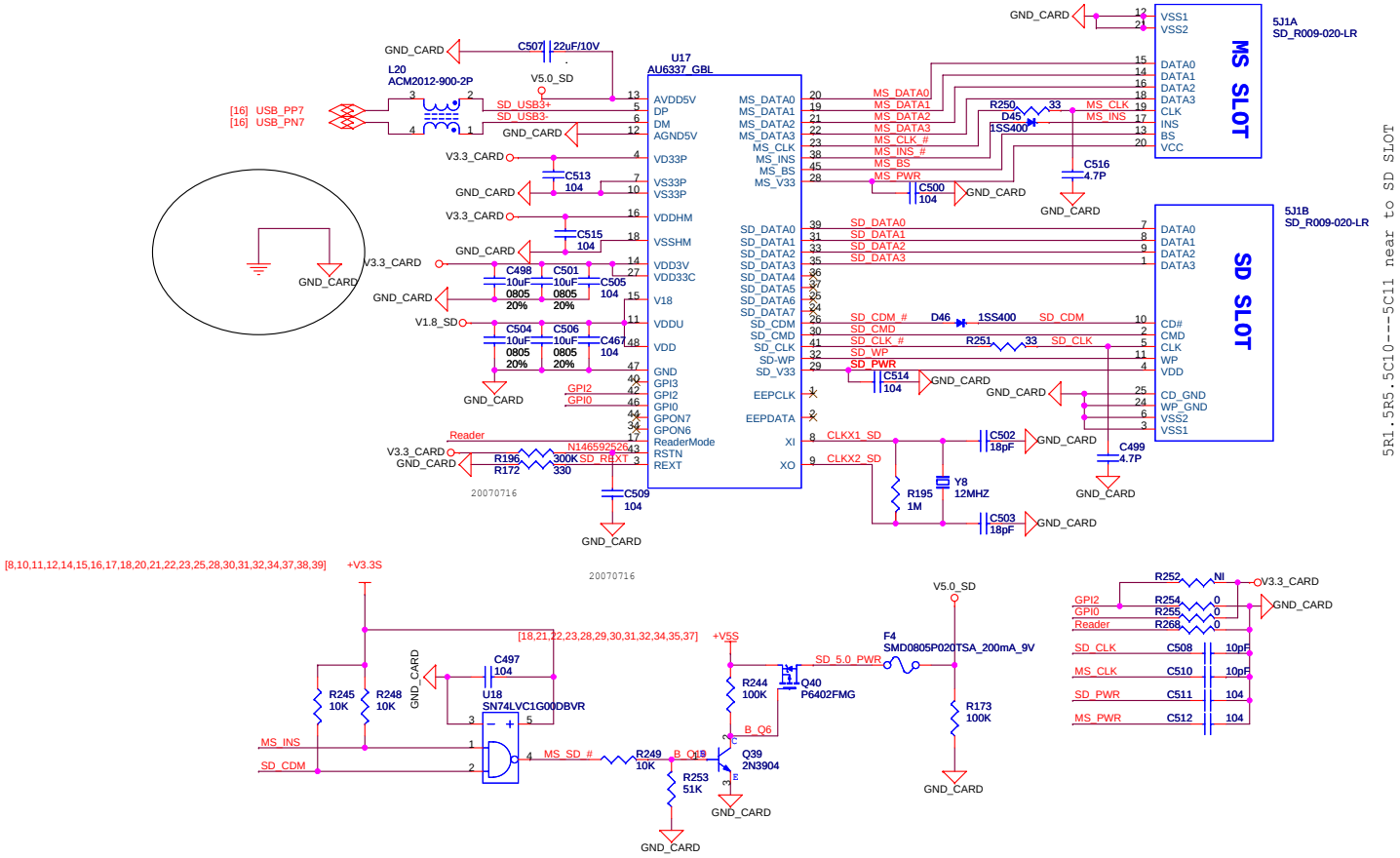


MALATA		
Title: LAN		
Size: Custom	Document Number: 81005	Rev: R1.4
Date: Thursday, June 05, 2008	Sheet 26 of 41	



MALATA		
Title: SD/MMC Card Reader		
Size: Custom	Document Number: 81005	Rev: R1.4
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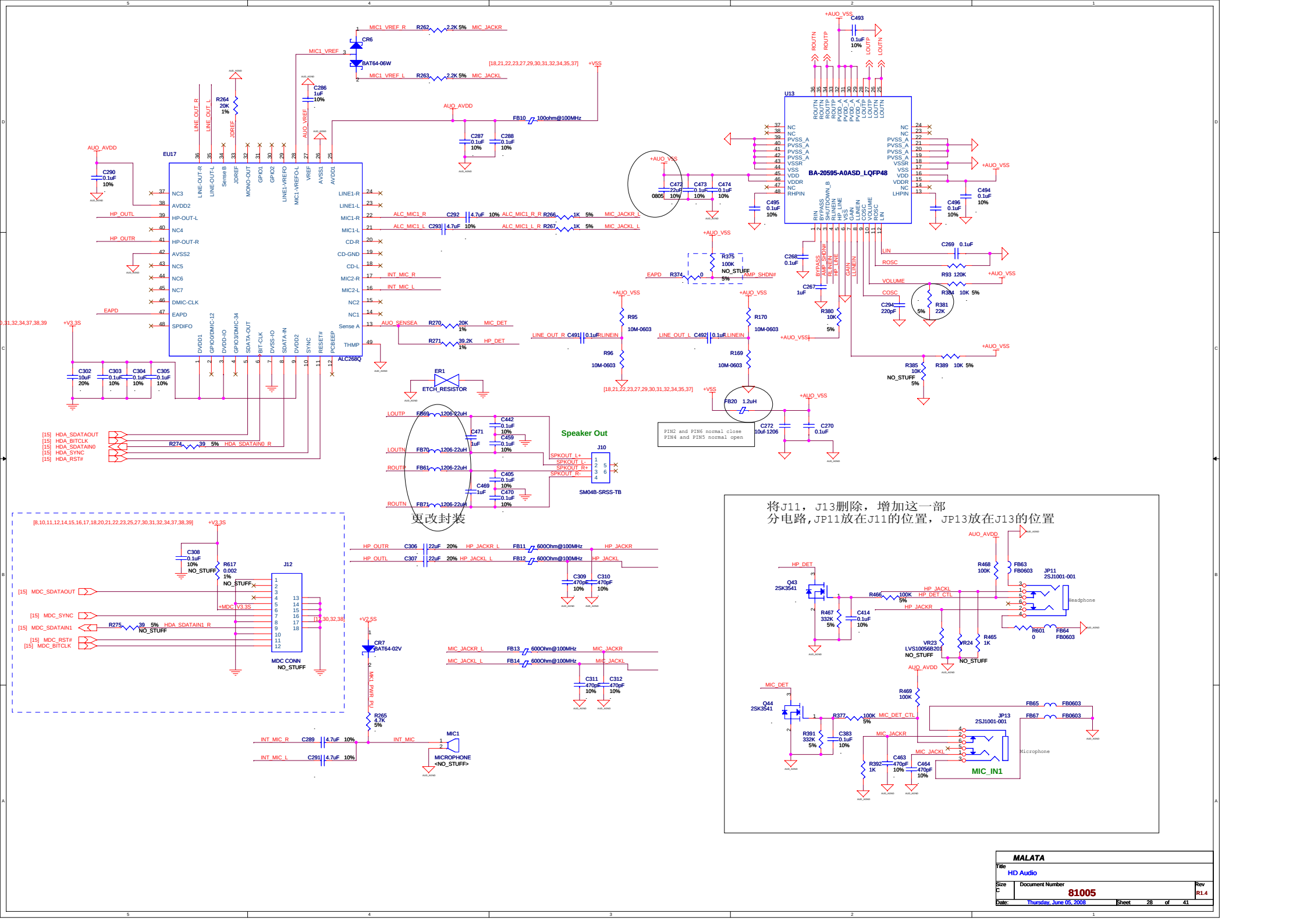
EU17
ALC268Q
BA-20595-A0ASD_LQFP48
U13
ER1
ETCH_RESISTOR
Speaker Out
J10
SM04B-SRSS-TB
更改封装
将J11，J13删除，增加这一部
分电路,JP11放在J11的位置，JP13放在J13的位置
J12
MDC CONN
NO_STUFF
MIC1
MICROPHONE
<NO_STUFF>
Headphone
Microphone
MIC_IN1
MALATA
HD Audio
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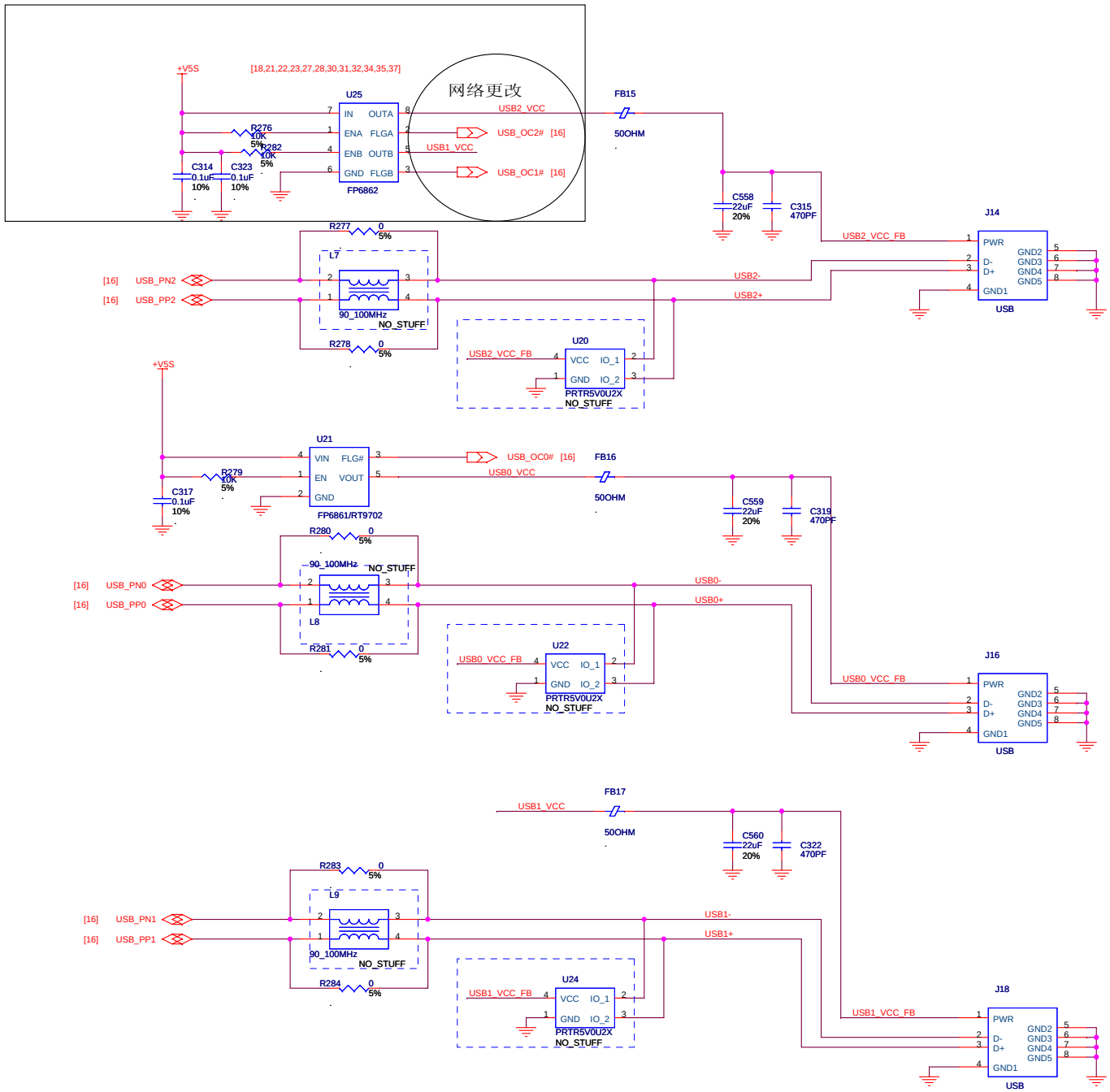

MALATA		
Title: USB Ports		
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EC hardware strap

BADDR1
BADDR0

BADDR 1	BADDR 0	SELECTION
0	0	XOR-Tree Test Mode
0	1	Core Defined
1	0	2Eh - 2Fh
1	1	164Eh - 164Fh

R285 10K 5% NO_STUFF
R286 10K 5% NO_STUFF

KBC_SCANOUT4
KBC_SCANOUT4 [31]
JEN0# JENK#(53PIN,INT PU)
1 0
R288 10K 5% NO_STUFF
JTAG singals and KB scan output share pin

SHBM
R289 10K 5% "0" Enable shared bios

TRIS#
R291 10K 5% NO_STUFF.
"0" forse the device to float all output and I/O port

[8,10,11,12,14,15,16,17,18,20,21,22,23,25,27,28,31,32,34,37,38,39] +V3.3S
[23,31,32,33,34] +V3.3A_KSC

Place one 0.1uF (X7R) capacitor on each VCC-GND pin pair (18/19, 45/46, 76/78, 88/89, 115/116)

C324 0.1uF 10%
C325 10uF 20%
R287 0 5%
C326 10uF 20%
C327 0.1uF 10%
C328 0.1uF 10%
C329 0.1uF 10%
C330 0.1uF 10%
C331 0.1uF 10%
C332 0.1uF 10%
EC_AVCC
C333 1uF 20%
C334 0.1uF 10%
C335 10uF 20%
Place C336 near pin 104 as much as possiable.
+V3.3A_KSC [23,31,32,33,34]
C336 0.1uF 10%

U146A
WPCE775L_LQFP128

VCC0 115, VCC1 88, VCC2 76, VCC3 45, VCC4 19, AVCC 102, VDD 4, VBAT 80
GND0 116, GND1 89, GND2 78, GND3 45, GND4 18, GND5 5, AGND 103

A/D
VREF 104
AD0/GPI90 97
AD1/GPI91 98
AD2/GPI92 99
AD3/GPI93 100
AD4/GPIO05 108
AD5/GPIO04 96

D/A
DA0/GPI94 101
DA1/GPI95 105
GPI96 106
GPI97 107

SP
SWD/GPIO66 81

GPIO
GPIO01 64
GPIO03 95
GPIO06/HGPIO06 93
GPIO07/HGPIO07 94
GPIO23 119
GPIO30 109
GPIO31 120
GPIO32 65
GPIO33 66
GPIO40 16
GPIO42/TCK 17
GPIO43/TMS 20
GPIO44/TDI 21
GPIO45 22
GPIO46/TRST# 23
GPIO47/JEN0# 24
GPIO50/TDO 25
GPIO51 26
GPIO52/RDY# 27
GPIO53 28
GPIO82/HGPIO00/TRIS# 110
VCORF 44

LPC
LPCPD#/GPIO10/HGPIO00 124
LRESET# 2
LCLK 3
LFRAME# 6
LDRQ#/GPIO24/HGPIO01 126
LAD0 127
LAD1 128
LAD2 1
LAD3 125
SERIRQ 8
CLKRUN#/GPIO11/HGPIO02 122
KBRST# 121
GA20 29
ECSCI# 9
SMI# 123
PWUREQ#

SMB
SDA2 68
SCL2 67
SDA1 69
SCL1 70

GPIO
GPIO77 84
GPIO76/SHBM 83
GPIO75 82
GPIO81 91
SOUT_CR/GPIO83/BADDR1 111
SIN_CR/GPIO87 113
GPIO84/HGPIO01/BADDR0 112
GPIO16/HGPIO04 114
GPIO34 14
GPIO36 15
GPIO70 73
GPIO71 74
GPIO72 75

PM_SUS_STAT# [17]
TP34
PLTRST# [10,16,17,25,26,31,39]
TP35
CLK_LPC_KBC [20]
LPC_FRAME# [15,31]
LDRQ0# [15]
LPC_AD0 [15,31]
LPC_AD1 [15,31]
LPC_AD2 [15,31]
LPC_AD3 [15,31]
PM_CLKRUN# [17]
H_RCIN# [15]
H_A20GATE_R
R292 0
CR8 BAT64-02V
H_A20GATE [15]
EC_RUNTIME_SCI# [17]
EC_EXTSMI# [17]
EC_WAKE_SCI# [17]
CR9 BAT64-02V
EC_SMB_SDA2 [33]
EC_SMB_SCL2 [33]
EC_SMB_SDA1 [8]
EC_SMB_SCL1 [8]
EC_EXTSMI#_DEBUG
R725 0 5% NO_STUFF
EC_EXTSMI#
SHBM
FAB_REV_ID3 [23]
FAB_REV_ID2 [23]
BADDR1
BADDR0
ALL_SYS_PWRGD [37]
FAB_REV_ID1 [23]
FAB_REV_ID0 [23]
LCD_SCL [21]
LCD_SDA [21]
LCD_CS# [21]

[23,31,32,33,34] +V3.3A_KSC
EC_SMB_SDA2 R296 10K 5%
EC_SMB_SCL2 R297 10K 5%
[8,10,11,12,14,15,16,17,18,20,21,22,23,25,27,28,31,32,34,37,38,39] +V3.3S
EC_SMB_SDA1 R298 10K 5%
EC_SMB_SCL1 R299 10K 5%
Assume only hot key
[8,10,11,12,14,15,16,17,18,20,21,22,23,25,27,28,31,32,34,37,38,39] +V3.3S
EC_EXTSMI# R302 10K 5% NO_STUFF

EC_RESET# [17]
EC_PWRSW#
R290 0 5% [17,32,34,36,38,39] PM_SLP_S3#
LID_IN
PM_SLP_S3#_R
TP28
TP33
TP32
2.5S_5S_3S_PWRGD
[10,37] DELAY_VR_PWRGOOD
[36] 1.5_1.05_VR_PWRGD

[33] BAT1_IN#
[33] BAT_CHG_I
TP26

[17] PM_PWRBTN#
CR10 BAT64-02V
[33] AC_IN
[37] CPU_VR_ON
[33] BC_SHDN
PWRBTN#
LED_NUM#
LED_BAT_GREEN#
LED_BAT_RED#
LED_PWRSTS#
[34] PM_EN_5VA_3VA#
HOTKEY1
HOTKEY2
HOTKEY3
[32,34] 5V_3V_VR_PWRGD
R300 0 PM_SLP_S4#_R
[17,32,35] PM_SLP_S4#
[35] 1.8V_0.9V_VR_PWRGD
R301 0 PM_RSMRST#_R
[17] PM_RSMRST#
[17] PM_ICH_PWROK
R294 0 PM_ICH_PWROK_R
TRIS#

EC_VCORE
C339 1uF 20%

[15,16,17,18,21,25,26,32,34,35,36,37,39] +V3.3A
R295 47K 5%
LID_IN
Hall Switch
MU3 OCH168
C338 0.1uF 10%
C337 0.1uF 10%
MC2 10uF25v NO_STUFF

[12,28,32,38] +V2.5S
[18,21,22,23,27,28,29,31,32,34,35,37] +V5S
C580 0.1uF 10%
R726 10K 5%
R727 10K 5%
U46 74AHC1G08
2.5S_5S_3S_PWRGD
R303 10K 5%
R728 10K 5%

[8,10,11,12,14,15,16,17,18,20,21,22,23,25,27,28,31,32,34,37,38,39] +V3.3S
[23,31,32,33,34] +V3.3A_KSC
R586 330 5%
R305 330 5%
R306 330 5%
PWRLED_DR
BAT_DR1
BAT_DR2
CR11
CR29 GREEN
RED/GREEN
LED_BAT_RED#
LED_PWRSTS#
LED_BAT_GREEN#

R307 330 5%
R308 330 5%
R309 330 5%
R310 330 5%
CAPLED_DR
NUMLED_DR
HDDLED_DR
WILLED_DR
CR12 GREEN
CR13 GREEN
CR14 GREEN
CR15 GREEN
LED_NUM#
LED_CAPS#
LED_CAPS# [31]
LED_WLAN# [25]
HDD_LED# [15]

Reserve for hotkey optional supported
[15,16,17,18,21,25,26,32,34,35,36,37,39] +V3.3A
C340 0.1uF 10% NO_STUFF
J19
HOTKEY1
HOTKEY2
HOTKEY3
SM05B-SRSS-TB NO_STUFF
Reserve Hot key optional for the different features

[23,31,32,33,34] +V3.3A_KSC
R304 10K 5%
EC_PWRSW#
R311 1K 5% EC_PWRSW#_R
C571 1uF 20%
SW1
Power_Button

MALATA

Title	EC (1/2)	
Size: Custom	Document Number: 81005	Rev: R1.4
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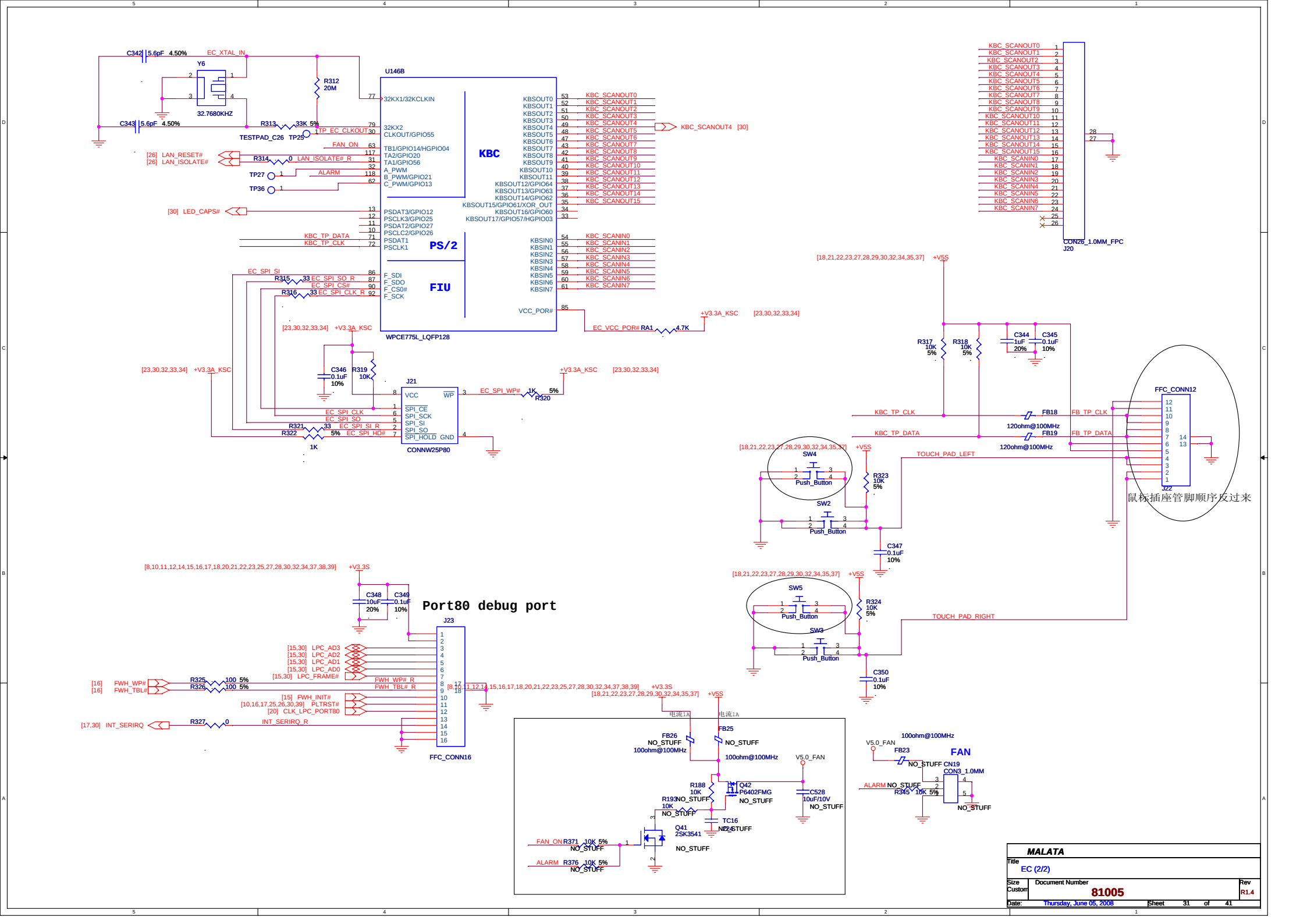
U146B
WPCE775L_LQFP128
KBC
PS/2
FIU
Y6
32.7680KHZ
C342 5.6pF 4.50%
C343 5.6pF 4.50%
EC_XTAL_IN
R312 20M
R313 33K 5%
TESTPAD_C26
TP25
TP_EC_CLKOUT
FAN_ON
[26] LAN_RESET#
[26] LAN_ISOLATE#
R314 0
LAN_ISOLATE#_R
ALARM
TP27
TP36
[30] LED_CAPS#
KBC_TP_DATA
KBC_TP_CLK
EC_SPI_SI
EC_SPI_SO_R
EC_SPI_CS#
EC_SPI_CLK_R
R315 33
R316 33
[23,30,32,33,34] +V3.3A_KSC
C346 0.1uF 10%
R319 10K
J21
CONNW25P80
EC_SPI_WP#
R320 1K 5%
EC_SPI_CLK
EC_SPI_SO
EC_SPI_SI_R
EC_SPI_HD#
R321 33
R322 1K
KBC_SCANOUT4 [30]
EC_VCC_POR#
RA1 4.7K
+V3.3A_KSC [23,30,32,33,34]
CON26_1.0MM_FPC
J20
[18,21,22,23,27,28,29,30,32,34,35,37] +V5S
R317 10K 5%
R318 10K 5%
C344 1uF 20%
C345 0.1uF 10%
FB18 120ohm@100MHz
FB19 120ohm@100MHz
FB_TP_CLK
FB_TP_DATA
FFC_CONN12
J22
鼠标插座管脚顺序反过来
TOUCH_PAD_LEFT
TOUCH_PAD_RIGHT
SW4
SW2
SW5
SW3
Push_Button
R323 10K 5%
R324 10K 5%
C347 0.1uF 10%
C350 0.1uF 10%
[8,10,11,12,14,15,16,17,18,20,21,22,23,25,27,28,30,32,34,37,38,39] +V3.3S
C348 10uF 20%
C349 0.1uF 10%
Port80 debug port
J23
FFC_CONN16
[15,30] LPC_AD3
[15,30] LPC_AD2
[15,30] LPC_AD1
[15,30] LPC_AD0
[15,30] LPC_FRAME#
[16] FWH_WP#
[16] FWH_TBL#
R325 100 5%
R326 100 5%
FWH_WP#_R
FWH_TBL#_R
[15] FWH_INIT#
[10,16,17,25,26,30,39] PLTRST#
[20] CLK_LPC_PORT80
[17,30] INT_SERIRQ
R327 0
INT_SERIRQ_R
[18,21,22,23,27,28,29,30,32,34,35,37] +V5S
电流1A
FB26 NO_STUFF 100ohm@100MHz
FB25 NO_STUFF 100ohm@100MHz
V5.0_FAN
R188 10K
R193 10K NO_STUFF
Q42 P6402FMG NO_STUFF
C528 10uF/10V NO_STUFF
TC16 NO_STUFF
Q41 2SK3541 NO_STUFF
FAN_ON R371 10K 5% NO_STUFF
ALARM R376 10K 5% NO_STUFF
FB23 NO_STUFF
FAN
CN19 CON3_1.0MM
R345 10K 5%
MALATA
EC (2/2)
81005
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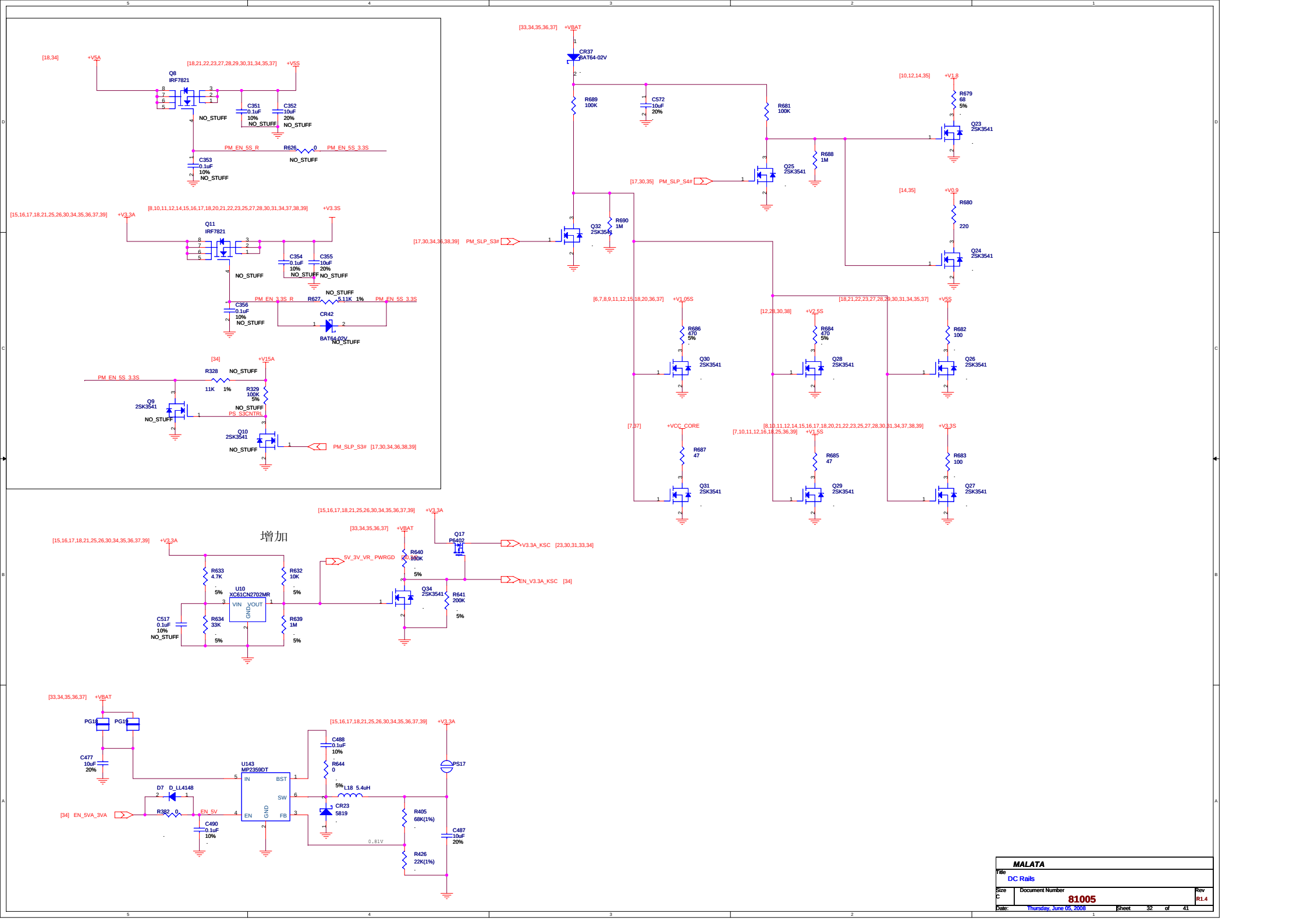
[18,34] +V5A
[18,21,22,23,27,28,29,30,31,34,35,37] +V5S
Q8 IRF7821
C351 0.1uF 10% NO_STUFF
C352 10uF 20% NO_STUFF
NO_STUFF
PM_EN_5S_R
R626 0
PM_EN_5S_3.3S
C353 0.1uF 10% NO_STUFF
[15,16,17,18,21,25,26,30,34,35,36,37,39] +V3.3A
[8,10,11,12,14,15,16,17,18,20,21,22,23,25,27,28,30,31,34,37,38,39] +V3.3S
Q11 IRF7821
C354 0.1uF 10% NO_STUFF
C355 10uF 20% NO_STUFF
PM_EN_3.3S_R
R627 5.11K 1%
C356 0.1uF 10% NO_STUFF
CR42 BAT64-02V NO_STUFF
[34] +V15A
R328 NO_STUFF 11K 1%
R329 100K 5% NO_STUFF
Q9 2SK3541 NO_STUFF
PS_S3CNTRL
Q10 2SK3541 NO_STUFF
PM_SLP_S3# [17,30,34,36,38,39]
[33,34,35,36,37] +VBAT
CR37 BAT64-02V
R689 100K
C572 10uF 20%
R681 100K
R688 1M
Q25 2SK3541
[17,30,35] PM_SLP_S4#
Q32 2SK3541
R690 1M
[17,30,34,36,38,39] PM_SLP_S3#
[10,12,14,35] +V1.8
R679 68 5%
Q23 2SK3541
[14,35] +V0.9
R680 220
Q24 2SK3541
[6,7,8,9,11,12,15,18,20,36,37] +V1.05S
R686 470 5%
Q30 2SK3541
[12,28,30,38] +V2.5S
R684 470 5%
Q28 2SK3541
[18,21,22,23,27,28,29,30,31,34,35,37] +V5S
R682 100
Q26 2SK3541
[7,37] +VCC_CORE
R687 47
Q31 2SK3541
[7,10,11,12,16,18,25,36,39] +V1.5S
R685 47
Q29 2SK3541
[8,10,11,12,14,15,16,17,18,20,21,22,23,25,27,28,30,31,34,37,38,39] +V3.3S
R683 100
Q27 2SK3541
增加
[15,16,17,18,21,25,26,30,34,35,36,37,39] +V3.3A
[33,34,35,36,37] +VBAT
Q17 P6402
+V3.3A_KSC [23,30,31,33,34]
5V_3V_VR_PWRGD
R640 100K 5%
EN_V3.3A_KSC [34]
R633 4.7K 5%
R632 10K 5%
U10 XC61CN2702MR VIN VOUT GND
Q34 2SK3541
R641 200K 5%
C517 0.1uF 10% NO_STUFF
R634 33K 5%
R639 1M 5%
[33,34,35,36,37] +VBAT
PG15 PG16
C477 10uF 20%
U143 MP2359DT IN BST SW EN GND FB
C488 0.1uF 10%
R644 0 5%
L18 5.4uH
PS17
D7 D_LL4148
[34] EN_5VA_3VA
R382 0
EN_5V
C490 0.1uF 10%
CR23 5819
0.81V
R405 68K(1%)
C487 10uF 20%
R426 22K(1%)
MALATA
Title DC Rails
Size C
Document Number 81005
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Date: Thursday, June 05, 2008
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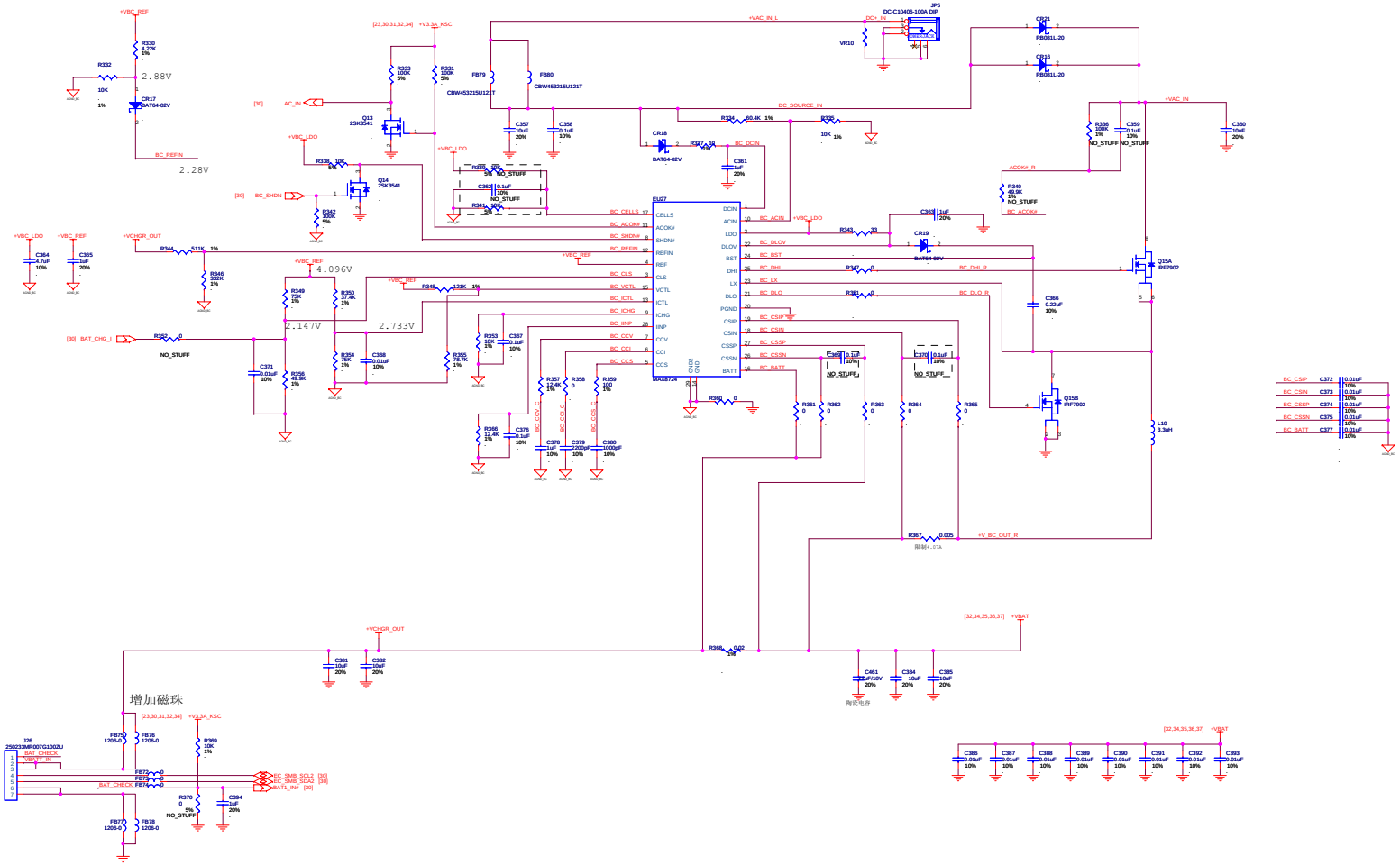

热敏电阻阻值与温度对应关系：

-10℃：R=56.14kΩ；	V_BAT1_IN#=2.8V
0℃：R=32.96kΩ；	V_BAT1_IN#=2.53V
25℃：R=10kΩ；	V_BAT1_IN#=1.65V
65℃：R=2.065kΩ；	V_BAT1_IN#=0.56V

MALATA			
Title: Charger			
Size: B	Document Number: 81005		Rev: R1.4
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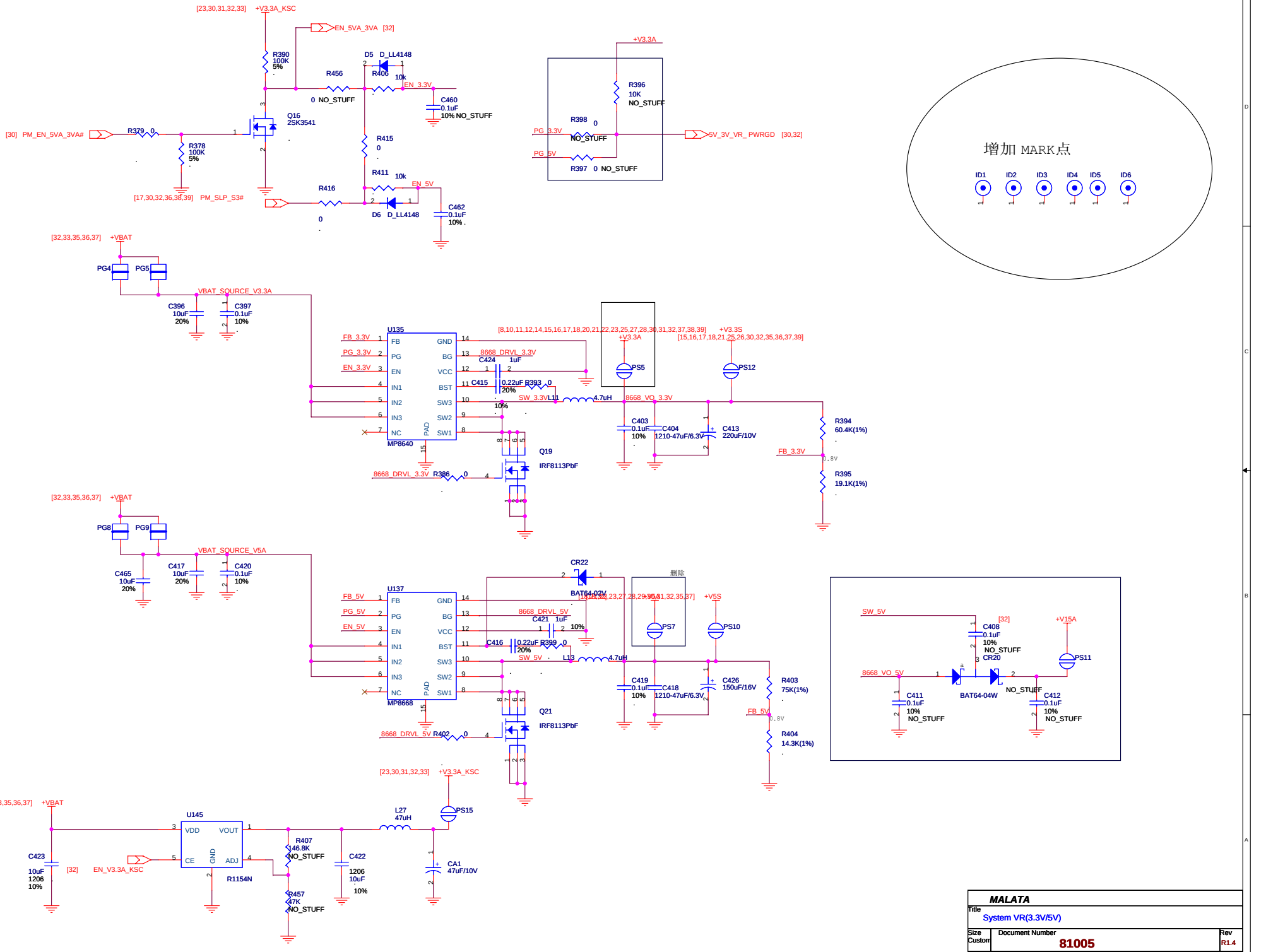
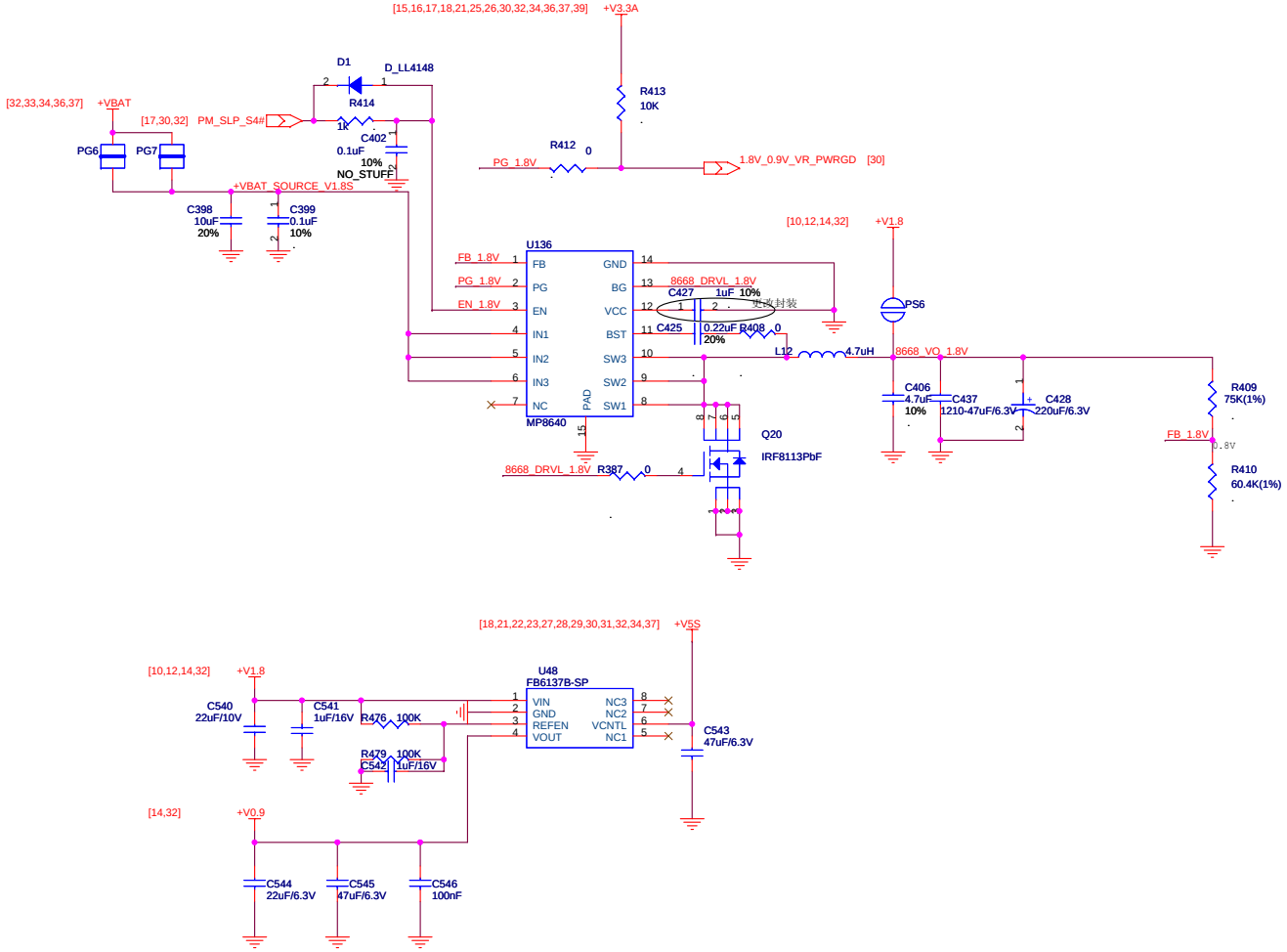
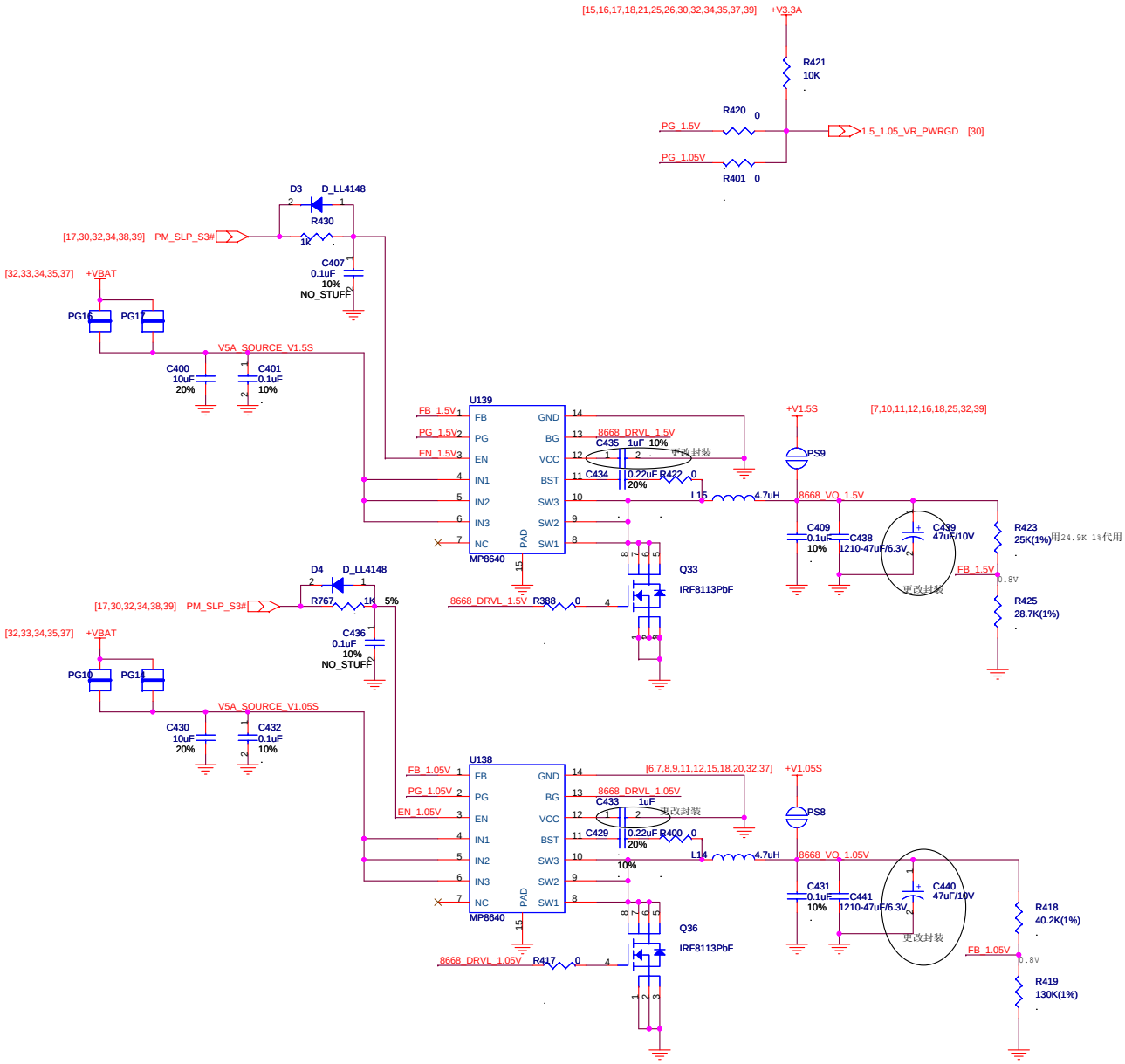


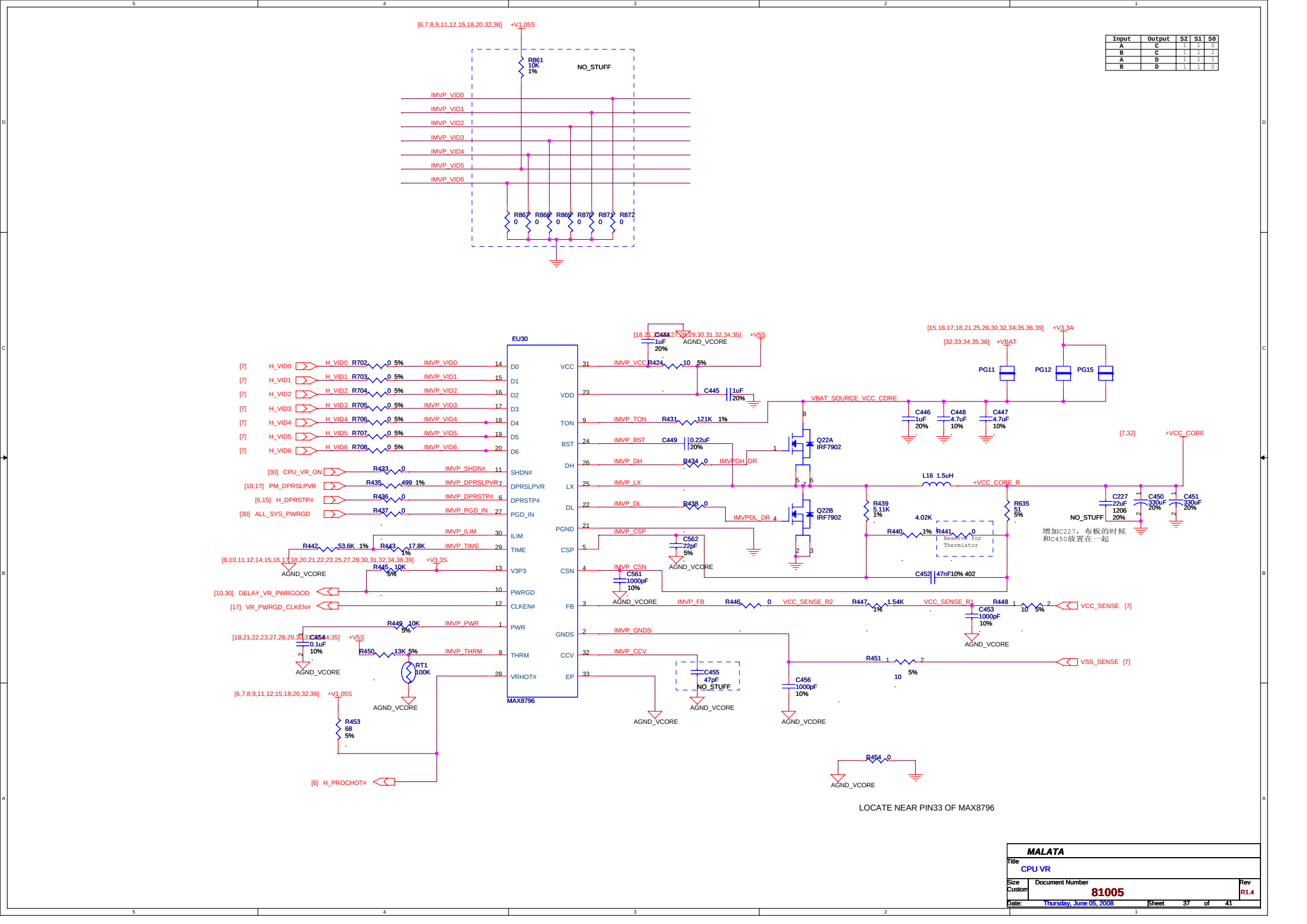
MALATA		
Title: System VR(3.3V/5V)		
Size: Custom	Document Number: 81005	Rev: R1.4
Date: Thursday, June 05, 2008	Sheet 34 of 41	



MALATA		
Title: DDR VR		
Size: Custom	Document Number: 81005	Rev: R1.4
Date: Thursday, June 05, 2008	Sheet 35 of 41	



MALATA		
Title: Chipset VR		
Size: Custom	Document Number: 81005	Rev: R1.4
Date: Thursday, June 05, 2008	Sheet 36 of 41	


[6,7,8,9,11,12,15,18,20,32,36] +V1.05S
R861 10K 1% NO_STUFF
IMVP_VID0
IMVP_VID1
IMVP_VID2
IMVP_VID3
IMVP_VID4
IMVP_VID5
IMVP_VID6
R867 0
R868 0
R869 0
R870 0
R871 0
R872 0
Input Output S2 S1 S0
A C 1 1 0
B C 1 1 1
A D 1 1 1
B D 1 1 0
EU30
MAX8796
D0 D1 D2 D3 D4 D5 D6
SHDN# DPRSLPVR DPRSTP# PGD_IN
ILIM TIME V3P3 PWRGD CLKEN# PWR THRM VRHOT#
VCC VDD TON BST DH LX DL PGND CSP CSN FB GNDS CCV EP
H_VID0 R702 0 5% IMVP_VID0
H_VID1 R703 0 5% IMVP_VID1
H_VID2 R704 0 5% IMVP_VID2
H_VID3 R705 0 5% IMVP_VID3
H_VID4 R706 0 5% IMVP_VID4
H_VID5 R707 0 5% IMVP_VID5
H_VID6 R708 0 5% IMVP_VID6
[30] CPU_VR_ON R433 0 IMVP_SHDN#
[10,17] PM_DPRSLPVR R435 499 1% IMVP_DPRSLPVR
[6,15] H_DPRSTP# R436 0 IMVP_DPRSTP#
[30] ALL_SYS_PWRGD R437 0 IMVP_PGD_IN
IMVP_ILIM
R442 53.6K 1% R443 17.8K 1% IMVP_TIME
[8,10,11,12,14,15,16,17,18,20,21,22,23,25,27,28,30,31,32,34,38,39] +V3.3S
R445 10K 5%
[10,30] DELAY_VR_PWRGOOD
[17] VR_PWRGD_CLKEN#
R449 10K 5% IMVP_PWR
[18,21,22,23,27,28,29,30,31,32,34,35] +V5S
C454 0.1uF 10%
R450 13K 5% IMVP_THRM
RT1 100K
[6,7,8,9,11,12,15,18,20,32,36] +V1.05S
R453 68 5%
[6] H_PROCHOT#
AGND_VCORE
[18,21,22,23,27,28,29,30,31,32,34,35] +V5S
C444 1uF 20%
IMVP_VCC R424 10 5%
C445 1uF 20%
IMVP_TON R431 121K 1%
IMVP_BST C449 0.22uF 20%
IMVP_DH R434 0 IMVPDH_DR
IMVP_LX
IMVP_DL R438 0 IMVPDL_DR
IMVP_CSP
C562 22pF 5%
IMVP_CSN
C561 1000pF 10%
IMVP_FB R446 0 VCC_SENSE_R2 R447 1.54K 1% VCC_SENSE_R1 R448 10 5% VCC_SENSE [7]
C453 1000pF 10%
IMVP_GNDS
IMVP_CCV
C455 47pF NO_STUFF
C456 1000pF 10%
R451 10 5% VSS_SENSE [7]
R454 0
VBAT_SOURCE_VCC_CORE
Q22A IRF7902
Q22B IRF7902
[15,16,17,18,21,25,26,30,32,34,35,36,39] +V3.3A
[32,33,34,35,36] +VBAT
PG11 PG12 PG15
C446 1uF 20%
C448 4.7uF 10%
C447 4.7uF 10%
L16 1.5uH
+VCC_CORE_R
R439 5.11K 1%
4.02K
R440 1% R441 0
Reserve for Thermistor
R635 51 5%
C452 47nF 10% 402
[7,32] +VCC_CORE
C227 22uF 1206 20% NO_STUFF
C450 330uF 20%
C451 330uF 20%
增加C227，布板的时候和C450放置在一起
LOCATE NEAR PIN33 OF MAX8796
MALATA
Title CPU VR
Size Custom
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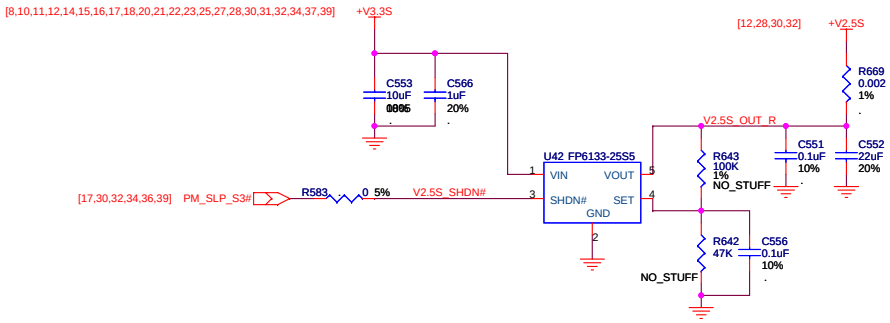

MALATA		
Title: 2.5V VR		
Size: Custom	Document Number: 81005	Rev: R1.4
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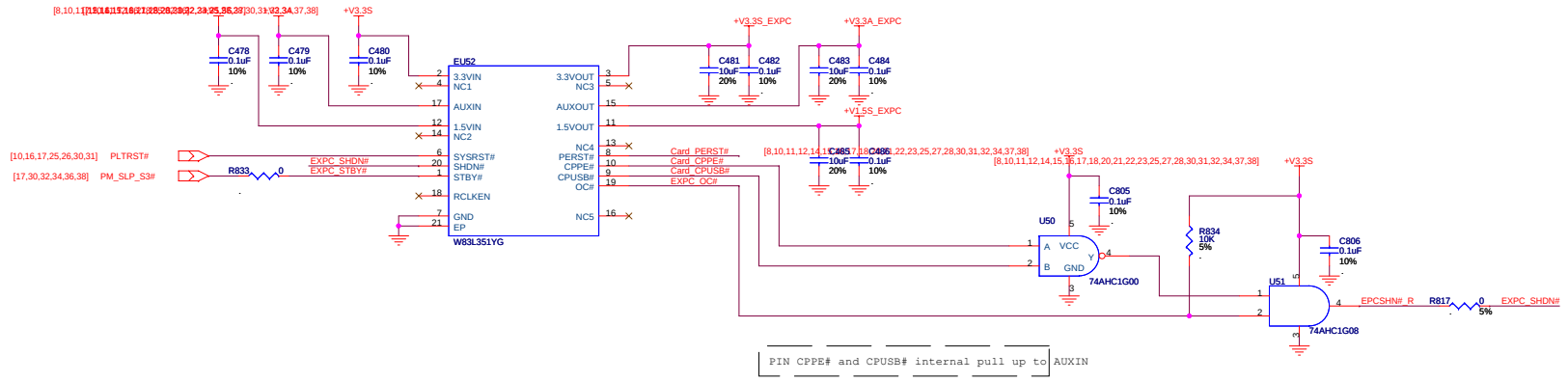
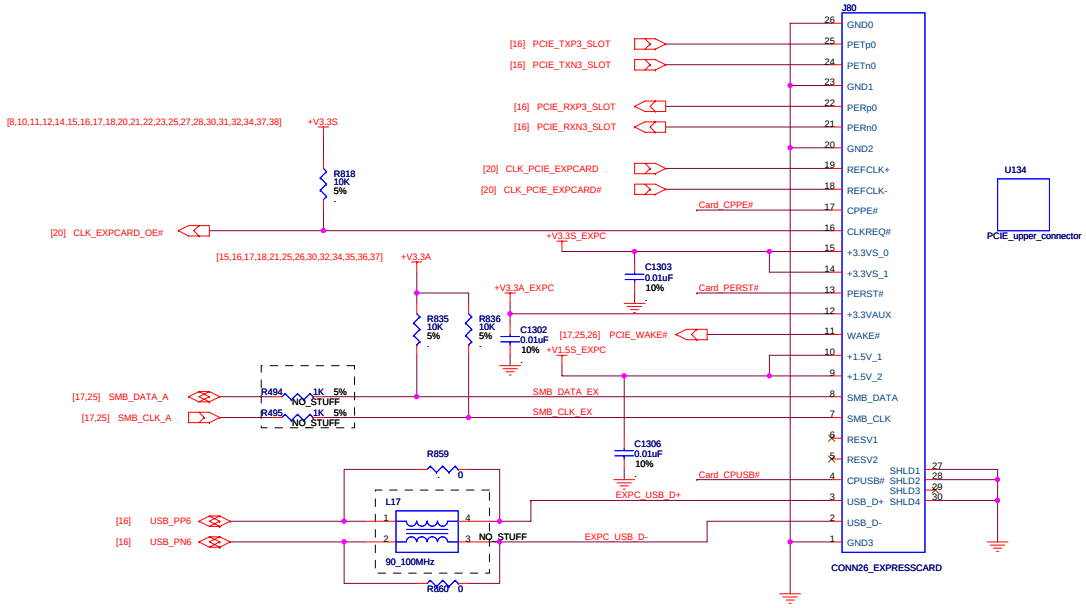
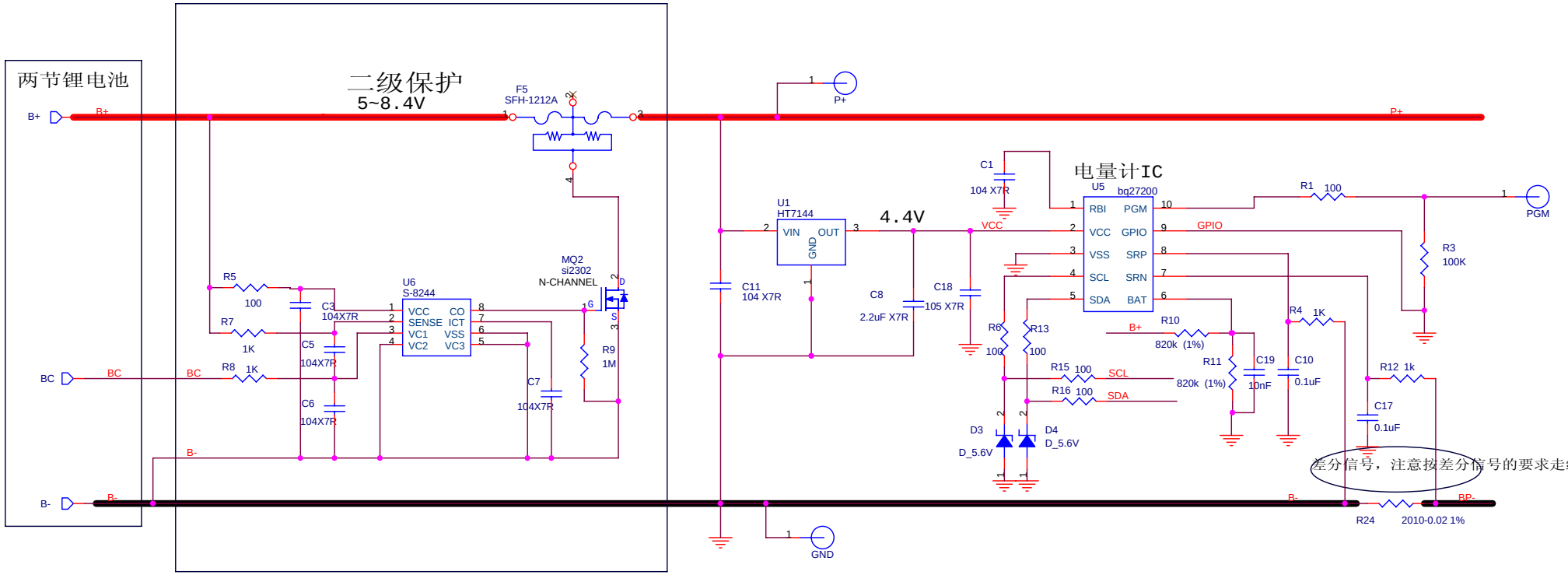




MALATA		
Title: Express Card		
Size: C	Document Number: 81005	Rev: R1.4
Date: Thursday, June 05, 2008	Sheet 39 of 41	



布板要求：

1. 五个测试点 P+ B- PGM SCL SDA 都放在同一层，
2. 加粗的线为大电流走线（1.6A）
3. 差分信号走线要注意.
4. 拼版按8拼1

Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Friday, May 23, 2008	Sheet 1 of 1	