

Operational Description

1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore4-ROM to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, an ADC is used to digitise the IF received signal.

2 RF Transmitter

2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore4-ROM to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter.

4 Power Control and Regulation

BlueCore4-ROM contains a 1.8V linear regulator which can be used to power the complete chip.

5 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8 and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.