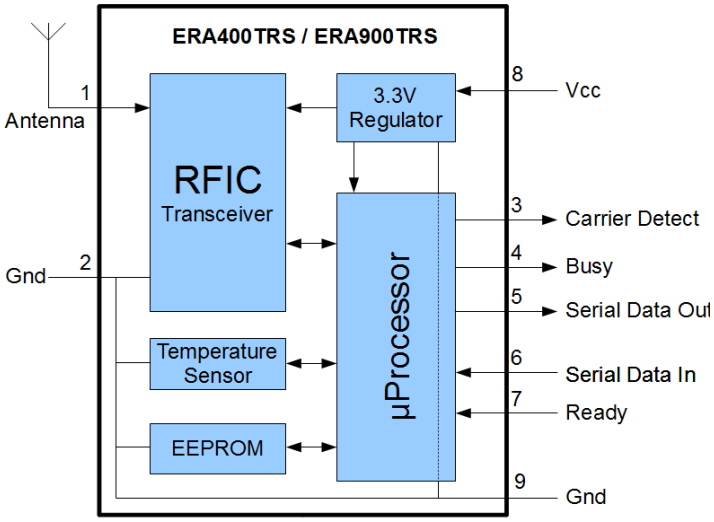

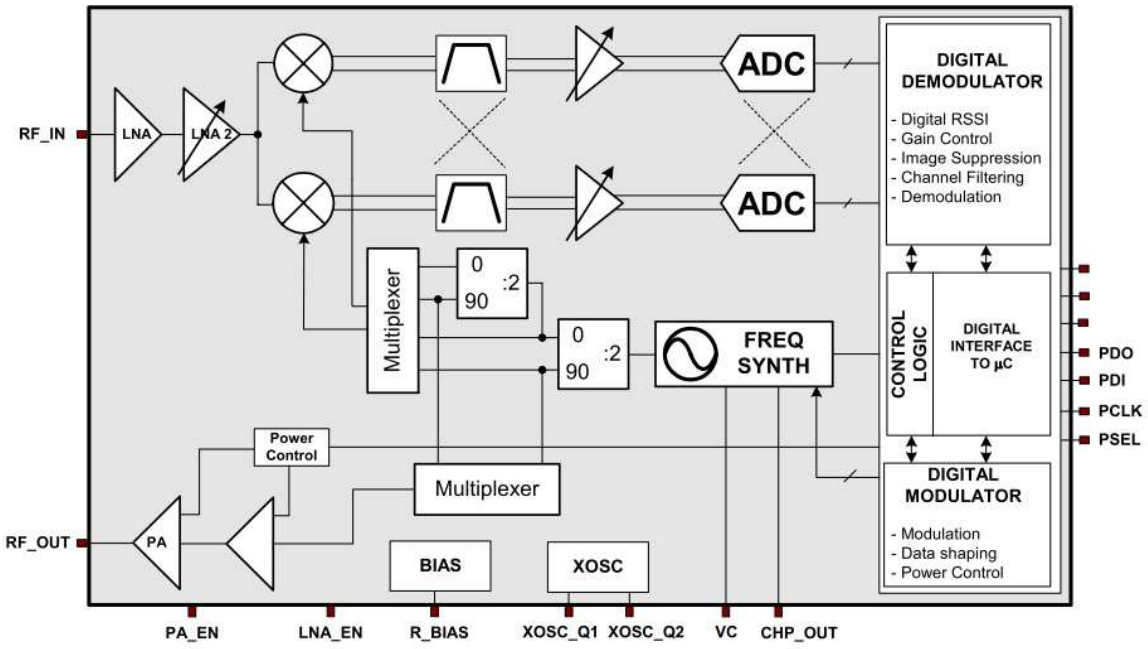

CC1020 simplified block diagram

A simplified block diagram of CC1020 is shown in Figure 2. Only signal pins are shown. CC1020 features a low-IF receiver. The received RF signal is amplified by the low noise amplifier (LNA and LNA2) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signal is complex filtered and amplified, and then digitized by the ADCs.

Automatic gain control, fine channel filtering, demodulation and bit synchronization is performed digitally.

CC1020 outputs the digital demodulated data on the DIO pin. A synchronized data clock is available at the DCLK pin. RSSI is available in digital format and can be read via the serial interface. The RSSI also features a programmable carrier sense indicator.

In transmit mode, the synthesized RF frequency is fed directly to the power amplifier (PA). The RF output is frequency shift keyed (FSK) by the digital bit stream that is fed to the DIO pin. Optionally, a Gaussian filter can be used to obtain Gaussian FSK (GFSK).

The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase splitter for generating the LO_I and LO_Q signals to the down conversion mixers in receive mode. The VCO operates in the frequency range 1.608-1.880 GHz. The CHP_OUT pin is the charge pump output and VC is the control node of the on-chip VCO. The external loop filter is placed between these pins. A crystal is to be connected between XOSC_Q1 and XOSC_Q2. A lock signal is available from the PLL.

The 4-wire SPI serial interface is used for configuration.