Elliott
An NTS company
Elliott Laboratories LLC
www.elliottlabs.com
41039 Boyce Road
Fremont, CA 94538
510-578-3500 Phone
510-440-9525 Fax

FCC

August 2, 2012

RE: FCC ID: SK6XI-N450
Correspondence Number: EA18873, dated 7/25/12

Attention: Jyun-Cheng Chen

Please find our responses to your comments on this application below:

Comment:
Thank you for your reply to my inquiry. However, your answer raised an issue. Previously we have been under the impression that the DFS radar detection is performed by each module independently as well as tasks associated with stop transmission, and that the host processor only coordinates frequency relocation (since it maintains the master channel and power plan) plus other tasks.

If, as mentioned in your reply, in fact "the host processor performs the radar detection algorithm, and that if the system believes radar is present the host processor initiates instructions to the module to close transmission," then the module should be classified as a limited split-modular transmitter.

A general purpose CPU is usually not equipped to process real-time physical layer signal, in this case up to 4 receive signals from 4 modules. Radar signal (which is not modulated) detection is typically done with correlation thus the raw physical data will need to be passed from the module through the PCIe interface to the CPU for radar detection.

Please clarify the host's exact role in DFS so that we can review the module in the correct context as well as understanding the impact of the host to DFS detection.

Response:

The Atheros chipset, at the lowest physical level, is the one performing the identification and filtering of all potential radar signature and encapsulate all pertinent information into a packet format which would be received by the host processor just like receiving a packet from a station. So technically speaking it is not the host processor doing the radar detection, the host processor do have to sort out the real radar signature among all the potential radar packets being presented.

Our host processor is capable of processing close to 1Gbps worth of UDP traffic. Most of the radar packet is very small, about 64 bytes including the header like UDP. This translate to our host processor can process roughly 3 million packets per second. Depending on the environment, a single Atheros chip probably would send from 0 to 10 radar packets to the host processor per second, our host processor can certainly be able to handle such amount of radar packets even for 8 radios. Also, in our XR4830 module, there are 4 cores with 8 radios, that means each host processor only handle 2 Atheros chip.

Furthermore, the Channel Closing Time stated by FCC ruling is 260ms maximum, it is quite a long period of computer time for the more advance host processor such as Cavium.

For any modular radio, the host system will provide some control over the radio. At the minimum, the host system will determine if the radio is enabled or disabled. Commonly (applicable in this case), a host will also determine the operating channel. The rules for a split-modular transmitter (from KDB 996369) do not provide any guidance on what constitutes the "transmitter control element". It seems that every module would fall into the definition of split-modular.

We believe that the limited modular approval, with the modules limited to the host devices described in the filing is appropriate.

Regards,

Mark Hill