OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
HD0	memory data bus	H4	I/O	VDDE3	HD0			
HD1		H3	I/O	VDDE3	HD1			
HD2		H2	I/O	VDDE3	HD2			
HD3		J3	I/O	VDDE3	HD3			
HD4		E5	I/O	VDDE3	HD4			
HD5		H1	I/O	VDDE3	HD5			
HD6		B1	I/O	VDDE3	HD6			
HD7		E4	I/O	VDDE3	HD7			
HD8		F3	I/O	VDDE3	HD8			
HD9		F2	I/O	VDDE3	HD9			
HD10		F1	I/O	VDDE3	HD10			
HD11		E1	I/O	VDDE3	HD11			
HD12		D1	I/O	VDDE3	HD12			
HD13		E3	I/O	VDDE3	HD13			
HD14		E2	I/O	VDDE3	HD14			
HD15		B2	I/O	VDDE3	HD15			
HWR_N	memory control signals	L5	O	VDDE3	HWR_N			
HRD_N		H5	O	VDDE3	HRD_N			
CS_N0		N4	O	VDDE3	CS0_N			
CS_N1		G5	O	VDDE3	CS1_N			
CS_N2		M5	O	VDDE3	CS2_N			
CS_N3		G3	O	VDDE3	CS3_N			
Keyboard scanner								
KBIO7	keyboard matrix	L14	I/O	VDDE1	KBIO7			
KBIO6		L12	I/O	VDDE1	KBIO6			
KBIO5		L13	I/O	VDDE1	KBIO5			
KBIO4		L11	I/O	VDDE1	KBIO4			
KBIO3		J11	I/O	VDDE1	KBIO3			
KBIO2		K12	I/O	VDDE1	KBIO2			
KBIO1		J10	I/O	VDDE1	KBIO1			
KBIO0		K10	O	VDDE1	KBIO0			
UART0								
CTS0_N	clear to send	B5	I	VDDE2	CTS0_N			
RTS0_N	request to send	A5	O	VDDE2	RTS0_N			
TXD0	transmit data	C5	O	VDDE2	TXD0			
RXD0	receive data	C4	I/O	VDDE2	RXD0			

OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
UART1								
TXD1	transmit data	A4	O	VDDE2	TXD1			
RXD1	receive data	D4	I/O	VDDE2	RXD1			
SIM Interface								
SIMCLK	interface clock	M13	O	VDDE1	SIMCLK			
SIMIO	data transfer	M12	I/O	VDDE1	SIMIO			
SIMERR	error removal	M11	I	VDDE1	SIMERR			
General Purpose I/O Port								
GPIO10	general purpose signal	K8	I/O	VDDE2	GPIO10			
GPIO9		N8	I/O	VDDE2	GPIO9			
GPIO8		P6	I/O	VDDE2	GPIO8			
GPIO7		N7	I/O	VDDE2	GPIO7			
GPIO6		L9	I/O	VDDE2	GPIO6			
GPIO5		L7	I/O	VDDE2	GPIO5			
GPIO4		P7	I/O	VDDE2	GPIO4			
GPIO3		N6	I/O	VDDE2	GPIO3			
GPIO2		L8	I/O	VDDE2	GPIO2			
GPIO1		L6	I/O	VDDE2	GPIO1			
GPIO0		P5	I/O	VDDE2	GPIO0			
Pulse Width Modulator								
PWM1	pulse width modulator signal	E6	O	VDDE2	PWM1			
PWM0		F4	O	VDDE2	PWM0			
JTAG and Test Access Port								
TCK	interface clock	A3	I	VDDE2	TCK			
TMS	test mode select	A2	I	VDDE2	TMS			
TDI	test data input	D2	I	VDDE2	TDI			
TDO	test data output	D3	O	VDDE2	TDO			
TRST_N	reset	A1	I	VDDE2	TRST_N			
J_SEL	controller select BBP DSP or BBP SC	B4	I	VDDE2	J_SEL			
Power-Down Control								
GPON2	general purpose power down signal	N9	O	VDDE2	GPON2			
GPON1		L10	O	VDDE2	GPON1			
AUXST		G10	O	VDDE1	GPON0	I	VDDD	AUXST
PCF50732 General Purpose Output								
AMPCTRL		H10				O	VDDD	AMPCTRL

OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
IF Signals								
IP	baseband differential I signal	J13				I/O	VDDA1	IP
IN		J14				I/O	VDDA1	IN
QP	baseband differential Q signal	H13				I/O	VDDA1	QP
QN		H14				I/O	VDDA1	QN
Auxiliary Functions								
AUXADC1	auxiliary ADC input	F14				I	VDDD	AUXADC1
AUXADC2		G14				I	VDDD	AUXADC2
AUXADC3		E14				I	VDDD	AUXADC3
AUXADC4		F13				I	VDDD	AUXADC4
AUXDAC1	auxiliary DAC outputs	E12				O	VDDA1	AUXDAC1
AUXDAC2		D13				O	VDDA1	AUXDAC2
AUXDAC3		D12				O	VDDA1	AUXDAC3
Voiceband Codec								
MICP	microphone differential input	A13				I	VDDA3	MICP
MICN		B13				I	VDDA3	MICN
AUXMICP	auxiliary microphone differential input	B14				I	VDDA3	AUXMICP
AUXMICN		A14				I	VDDA3	AUXMICN
EARN	earphone differential output	A11				O	VDDA4	EARN
EARP		B10				O	VDDA4	EARP
AUXSP	auxiliary earphone differential output	A10				O	VDDA4	AUXSP
BUZ		B11				O	VDDA4	BUZ

Notes: TYPE I Input signal

O: Output signal

I/O: Duplexer signal

P: Power

G: Ground

Table 7 Power supply domains for LFBGA180 package

TYPE	NUMBER	DESCRIPTION	PIN
VDDC	4	core power supply pins	F5, N13, M8, K6
VDDE1	4	IO power supply pins	C8, H11, N12, P9
VDDE2	2	IO power supply pins with level shifter	P8, C1
VDDE3	4	IO power supply pins with level shifter	G2, L3, P4, M6
VSS, VSS_VB, VSS_VBOUT, VSS_REF, VSSD, VSS_BB, AVSS	19	ground pins	A12, C3, C11, C13, D11, E8, E13, G1, G13, J1, K1, K7, M7, N5, N10, N11, N14, P1, P10
VDD_D	1	Digital Supply of PCF50732	C9
VDD_VB, VDD_VBOUT, VDD_REF, VDD_BB	4	Analog supplies of PCF50732	F12, D14, B12, C12
AVDD	1	PLL supply pin	P12

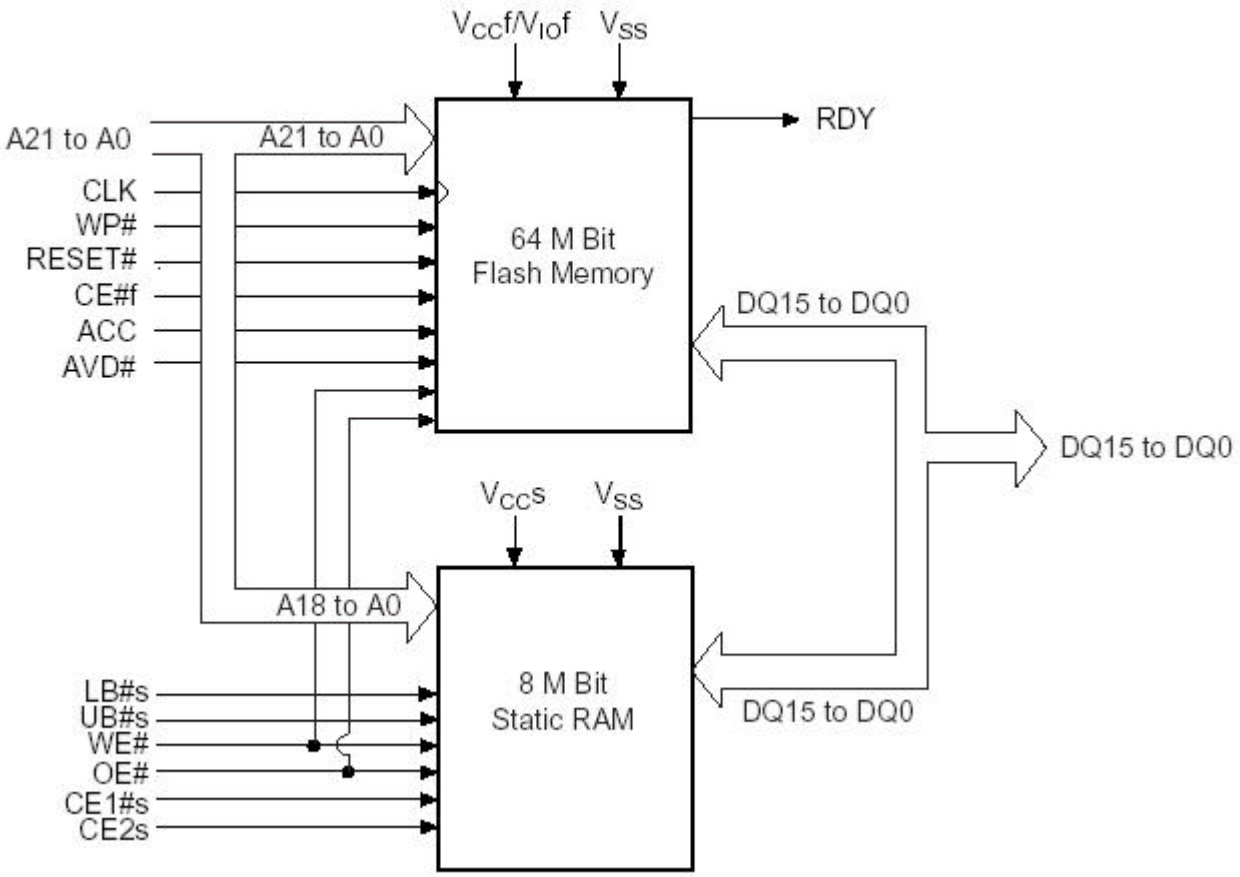
9 Limiting Values

In accordance with the Absolute Maximum Rating System (IEC 134).

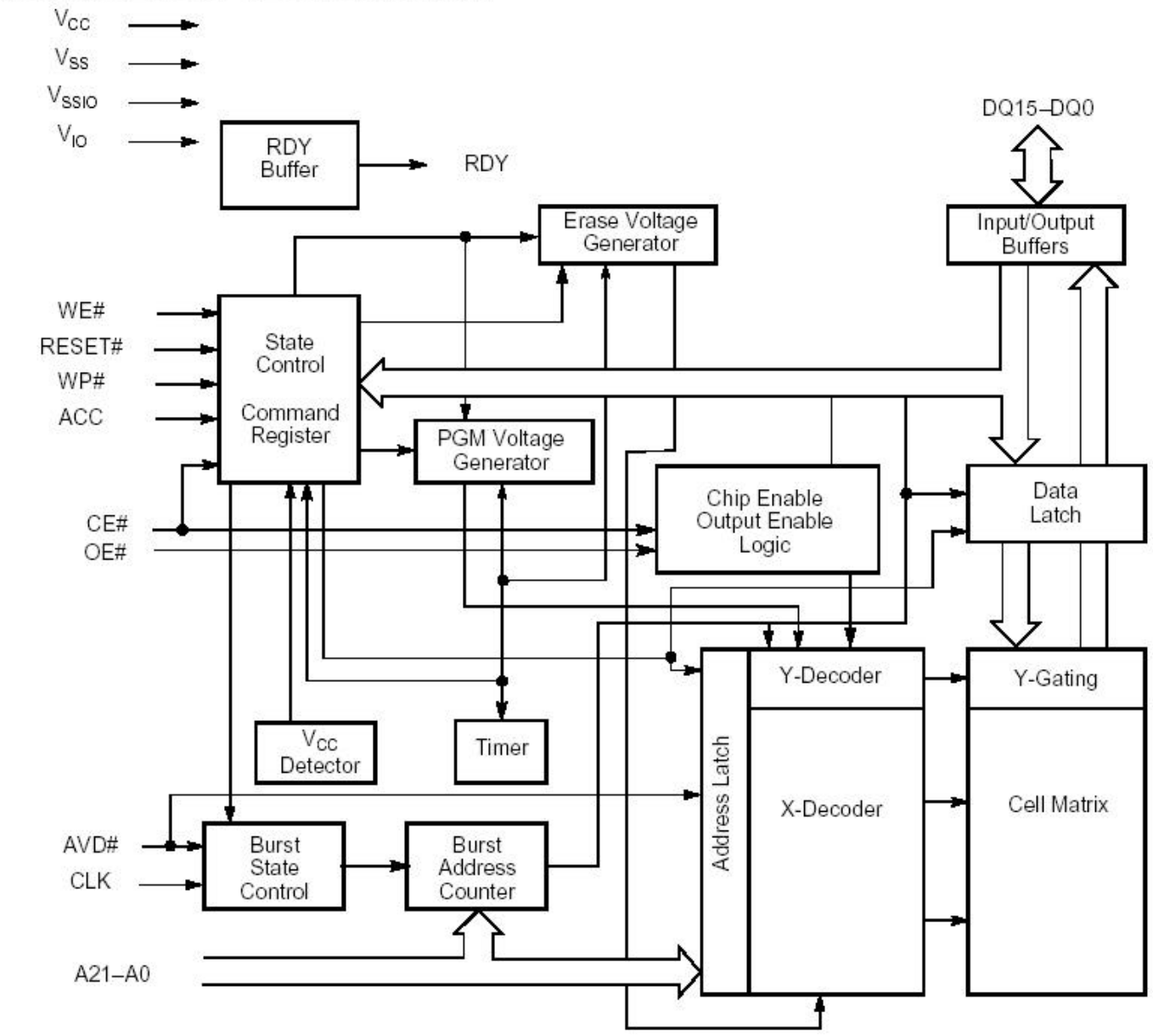
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD}C$	PCF50874 Core supply voltage	–0.5	+3.3	V
VDDD VDD_BB VDD_VB VDD_VBOUT VDD_REF	PCF50732 Digital and Analog supplies	-0.5	+3.3	V
VDDE1	PCF50874 IOs supply voltage VDDE1	-0.5	+3.3	V
VDDE2	PCF50874 IOs supply voltage VDDE2	-0.5	+3.6	V
VDDE3	PCF50874 IOs supply voltage VDDE3	-0.5	+3.6	V
V_I	Input voltage on any pin with respect to ground (VSS)	–0.5	VDDx+0.5	V
IIBBI1	PCF50732 DC current into any pin (except EARP/EARN,AUX,BUZ)	-10	+10	mA
IIBBI2	PCF50732 DC current into EARP/EARN, AUX, BUZ	-100	+100	mA
I_I, I_O	DC current into any input or output	–10	+10	mA
P_{tot}	total power dissipation	–	1.36	W
T_{stg}	storage temperature range	–65	+150	°C
T_{amb}	operating ambient temperature range	–40	+85	°C
T_j	operating junction temperature range	–	+125	°C

U500: Memory chip adopts AM42BDS6408GT89I. It integrates with 64M Bit Flash Memory and 8M Bit SRAM?

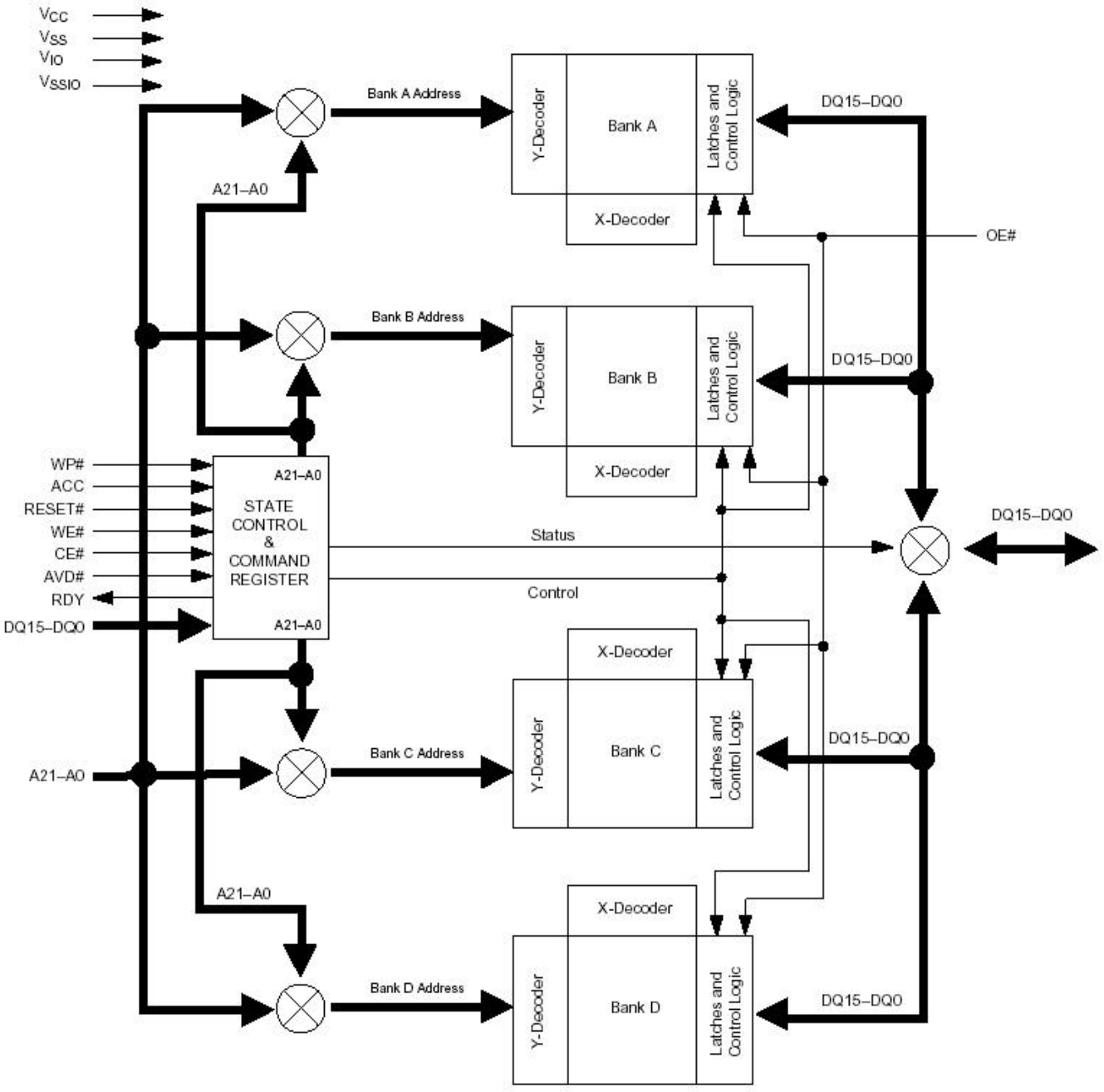
BLOCK DIAGRAM



FLASH MEMORY BLOCK DIAGRAM



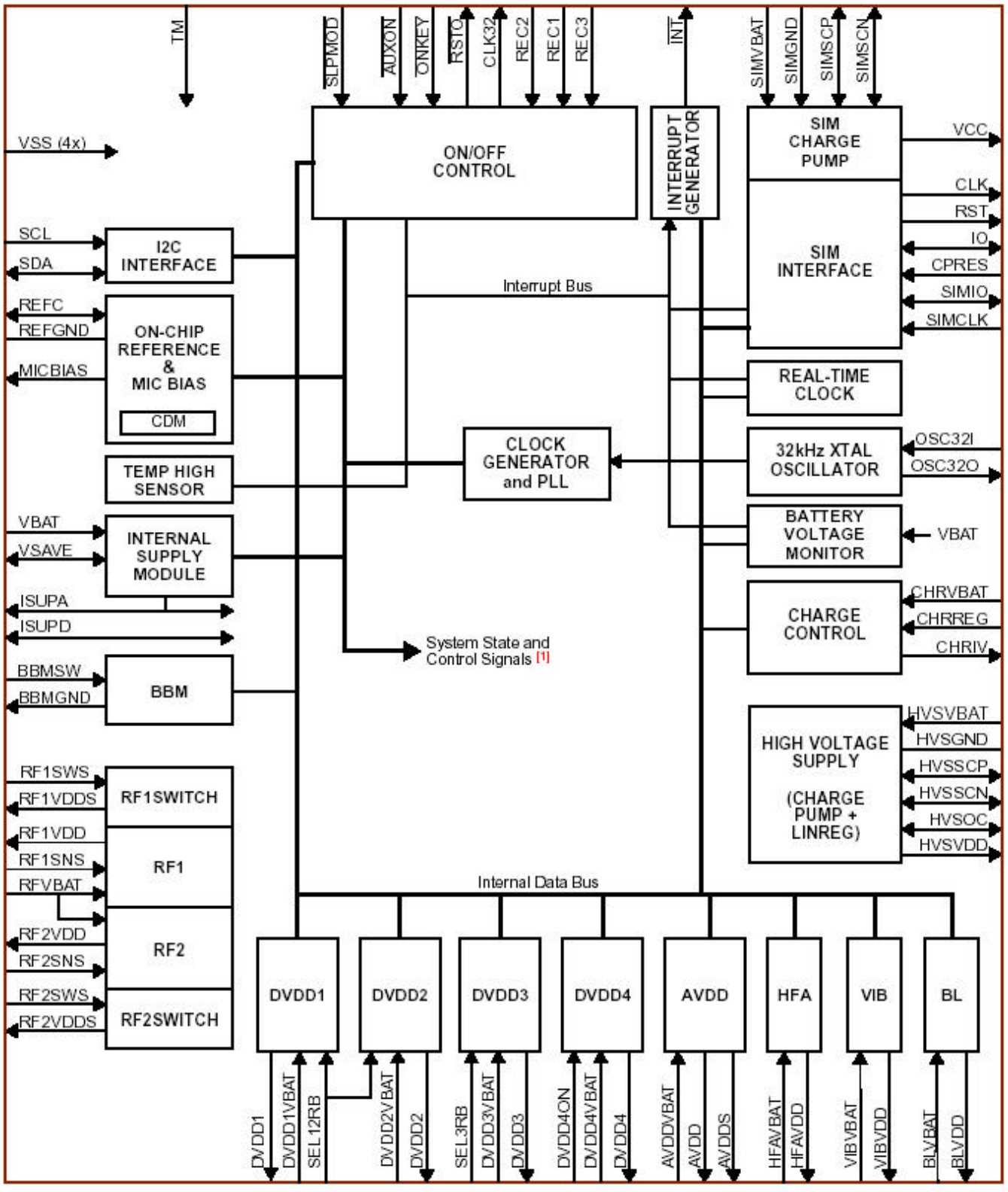
FLASH MEMORY SIMULTANEOUS OPERATION DIAGRAM



Pins description is as below:

A18–A0	19 Address Inputs (Common)
A21–A19	3 Address Inputs (Flash)
DQ15–DQ0	16 Data Inputs/Outputs (Common)
CE#f	Chip Enable (Flash)
CE1#s	Chip Enable 1 (SRAM)
CE2s	Chip Enable 2 (SRAM)
OE#	Output Enable (Common)
WE#	Write Enable (Common)
UB#s	Upper Byte Control (SRAM)
LB#s	Lower Byte Control (SRAM)
RESET#	Hardware Reset Pin, Active Low
VCCf	Flash 1.8 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
VIOf	Input & Output Buffer Power Supply must be tied to VCC.
VCCs	SRAM Power Supply
VSSIOf	Output Buffer Ground
VSS	Device Ground (Common)
NC	Pin Not Connected Internally
RDY	Ready output; indicates the status of the Burst read.
	Low = data not valid at expected time.
	High = data valid.
CLK	CLK is not required in asynchronous mode. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter.
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs (A21–A0).
	Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched.
	High = device ignores address inputs
WP#	Hardware write protect input. At VIL, disables program and erase functions in the two outermost sectors. Should be at VIH for all other conditions.
ACC	At VID, accelerates programming; automatically places device in unlock bypass mode. At VIL, locks all sectors. Should be at VIH for all other conditions.

U401: POWE-SIM-MANAGEMENT adopts PCF50601ET-C2?It mainly provides Baseband power supply, RF power supply, SIM interface and so on. Diagram and pin description are shown below:



Symbol[1]	Ball	Supply	Description/Remarks
Linear regulators			
RFVBAT	G8	-	Input for RF1 and RF2 linear regulators
RF1SNS	F8	-	Voltage sense input for RF1; shall be connected to RF1VDD
RF2SNS	H8	-	Voltage sense input for RF2; shall be connected to RF2VDD
RF1SWS	E6	DVDD1	Output switch enable input for RF1; switches the RF1VDDS on.
RF2SWS	F6	DVDD2	Output switch enable input for RF2; switches the RF2VDDS on.
RF1VDD	F9	-	RF1 linear regulator 1 output voltage
RF1VDDS	E9	-	RF1 linear regulator switched output voltage
RF2VDD	G9	-	RF2 linear regulator 2 output voltage
RF2VDDS	H9	-	RF2 linear regulator switched output voltage
SEL12RB	E7	DVDD2	Select register B for DVDD1&2; note that this signal shall be stable at start-up.
DVDD1VBAT	F2	-	Input for DVDD1 linear regulator
DVDD1	F1	-	DVDD1 linear regulator output voltage
DVVD2VBAT	G2	-	Input for DVDD2 linear regulator
DVDD2	G1	-	DVDD2 linear regulator output voltage
SEL3RB	E5	ISUPD	Select Control Register B for DVDD3; note that this signal shall be stable at start-up.
DVDD3VBAT	H2	-	Input for DVDD3 linear regulator
DVDD3	H1	-	DVDD3 linear regulator output voltage
DVDD4VBAT	B4	-	Input for DVDD4 linear regulator
DVDD4	A4	-	DVDD4 linear regulator output voltage
DVDD4ON	F7	DVDD2	Switches DVDD4 linear regulator on; pin has pull-down resistor to VSS.
AVDDVBAT	H7	-	Input for AVDD linear regulator
AVDD	J7	-	AVDD linear regulator output voltage
AVDDS	G7	-	AVDD linear regulator switched output voltage
HFAVBAT	B5	-	Input for hands-free audio linear regulator
HFAVDD	A5	-	Hands-free audio linear regulator output voltage
VIBVBAT	B3	-	Input for vibrator linear regulator
VIBVDD	A3	-	Vibrator linear regulator output voltage

Backlight supply and control			
BLVBAT	B6	-	Input for backlight linear regulator
BLVDD	A6	-	Backlight linear regulator output voltage
BBMGND	B7	-	Backlight brightness modulator ground
BBMSW	A7	BLVDD	Backlight brightness modulator switch
Control interfaces			
$\overline{\text{SLPMOD}}$	D5	DVDD1	Signal switches the system to SLEEP state. At start up this signal is ignored until enabled by the system controller (see OOCC2 register).
TM	F5	ISUPD	Test mode selection; shall be connected to ground for normal operation.
$\overline{\text{RSTO}}$	D6	DVDD1	Active-low reset for logic supplied by DVDD1
$\overline{\text{ONKEY}}$	F4	ISUPD	Active Low On-key input with debouncing. Input implemented as Schmitt trigger input with internal pull-up resistor to ISUPD. Edge sensitive input.
$\overline{\text{AUXON}}$	G4	ISUPD	Active Low Auxiliary On-Key input with 62 msec debouncing. Input implemented as Schmitt trigger input with internal pull-up resistor to ISUPD. Level sensitive input.
CLK32	B8	DVDD1	32.768 kHz digital clock output; note that this output is only available when system is in ACTIVE or SLEEP state and DVDD1 is on.
$\overline{\text{INT}}$	D7	DVDD1	Interrupt to system controller; this active low signal is realized as an open drain output. Requires external pull-up resistor.
REC1	J2	DVDD2	Accessory recognition with interrupt; these inputs have selectable debounce filters (0, 14 or 62 ms) to prevent multiple interrupt generation
REC2	H3	DVDD2	
REC3	G3	DVDD2	
32.768 kHz oscillator			
OSC32I	J8	ISUPA	32.768 kHz oscillator input
OSC32O	J9	ISUPA	32.768 kHz oscillator output
Internal supply			
ISUPA	H5	-	Internal supply voltage output
ISUPD	G5	-	Internal supply voltage for digital logic. This pin shall be connected to ISUPA.
VSAVE	J4	-	Backup (auxiliary) battery
VBAT	J3	-	Main battery connection for general internal usage