CONTENT

1.0 Objective

This document is intended for FCC testing; it mainly includes Tuning Up Procedure and Operational Manual.
It describes the key principles of C570&K570; their tuning up, their operation among the interfaces and their different antenna features.

2.0 Abbreviation and glossary

3WBUS Three-Wired BUS (Signalname)
AUXADC AUXilary Analog Digital Converter (Signalname)
AUXDAC AUXilary Digital Analog Converter (Signalname)
BB Baseband
BAI Baseband Audio Interface
COMBO Multi chip package consisting FLASH and SRAM
CPU Central Processing Unit
CSx Chip Select (Signalname)
DAI Digital Audio Interface
DCS Digital Cellular System
EEPROM Electrically Erasable Programmable Read-Only Memory
EVITA Evaluation, Verification, Integration, Test and Application platform
FLASH special kind of programmable memory devices
GPIO General Purpose Input/Output (Signalname)
GPON General Power ON (Signalname)
GPRS General Packet Radio Service
GSM Global System for Mobil Communication
IrDA Infra-red Data Adapter
IIC Inter-IC (Signalname)
JTAG IEEE standardized test interface for ICs (Signalname),
abb. from Join Test Action Groupe
KBIO KeyBoard Input/Output (Signalname)
LCD Liquid Crystal Display
LED Light Emitting Diode
MMI Man Machine Interface
PA Power Amplifier
PCB Printed Circuit Board
PCS Personal Communications System
PROM Programmable Read Only Memory
PMU Power Management Unit

RFSIG Signal lines to control the function of the RF parts (Signalname)
SIM Subscriber Identity Module
SIOX Serial Input/Output interface for baseband (Signalname)
SIOY Serial Input/Output interface for audio (Signalname)
SRAM Static Random Access Memory
TC Transceiver
UART Universal Asynchronous Receiver / Transmitte

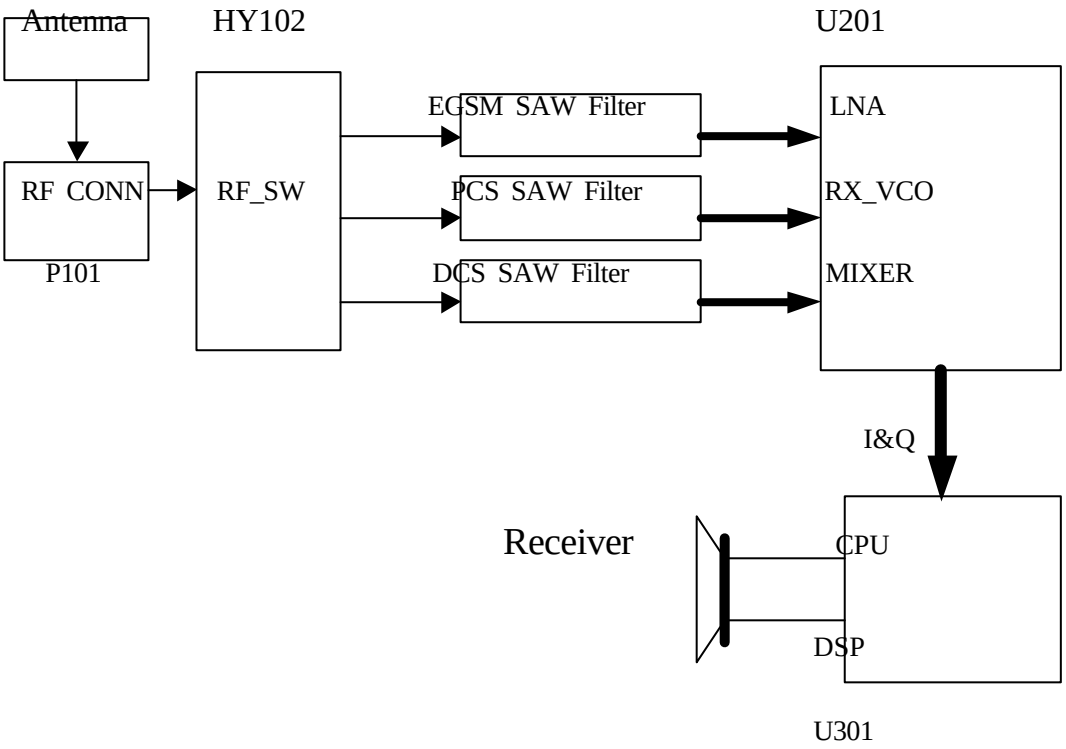
3.1 Principle of Rx Circuit

3.1.1 C570 supports three bands: EGSM 900/DCS 1800/PCS 1900.

PCS:

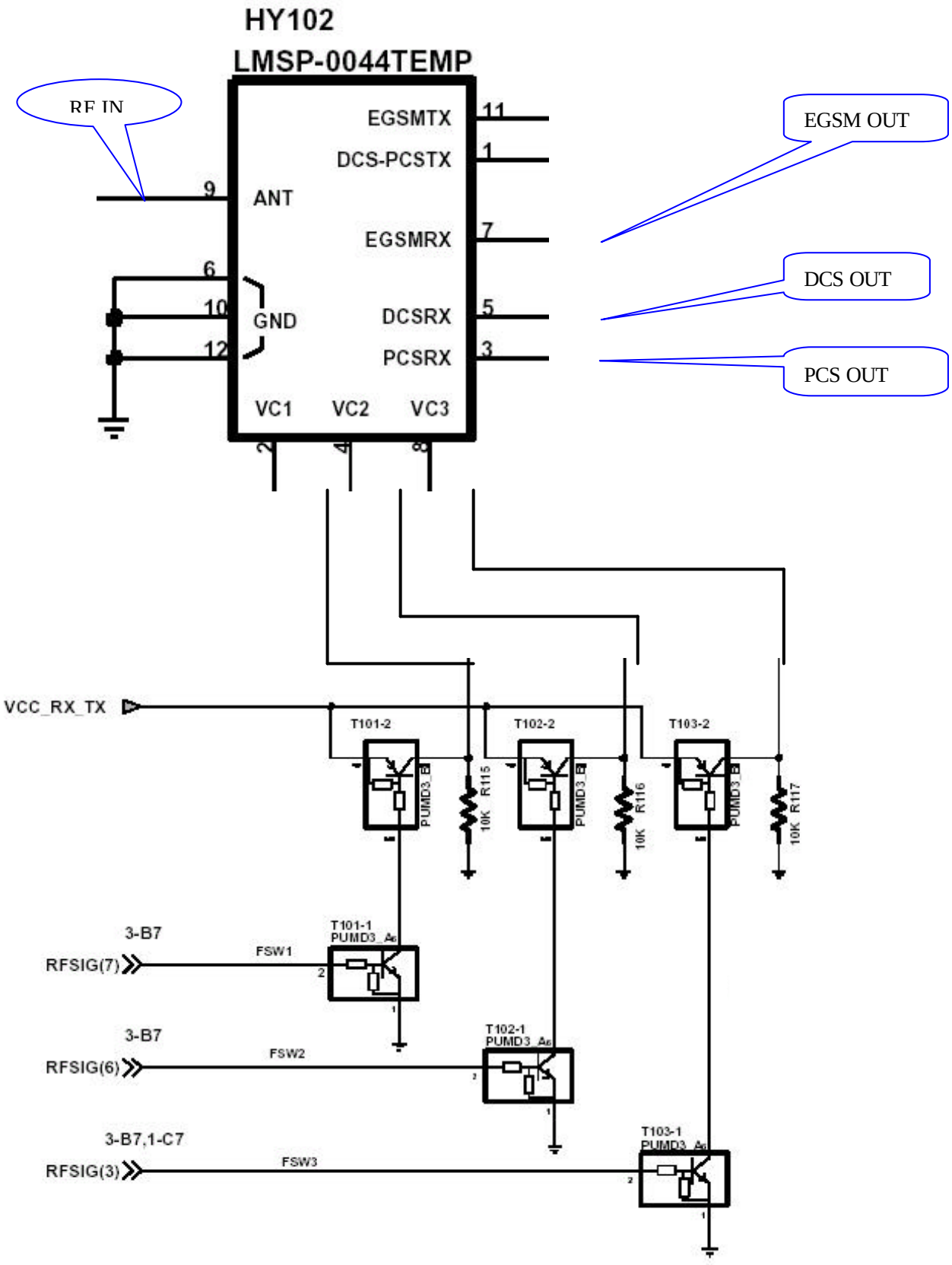
Channel Range：512-810
Downlink: 1930MHZ-1990MHZ
Uplink: 1850MHZ-1910MHZ
Duplexer: 80 MHZ
Bandwidth: 200 KHZ
Power Level Range: 0-15

3.1.2 C570 Block Diagram for Receive Path:

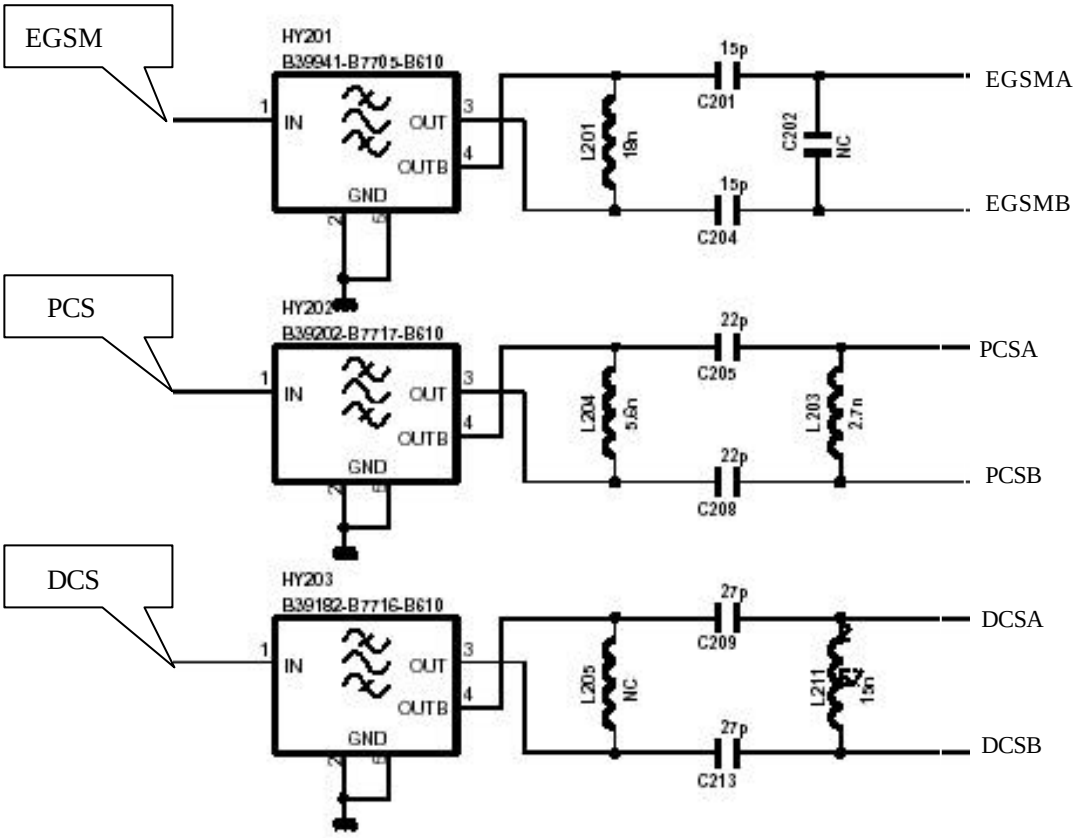


Block Diagram of Rx

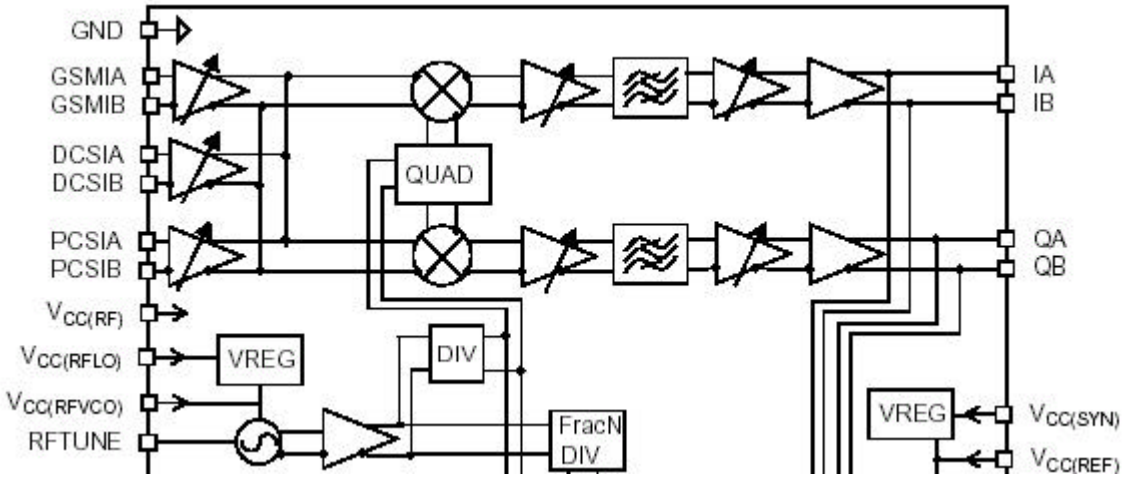
3.1.3 Signal is coming from the RF Connector. RF Connector is designed for testing; with the RF cable and equipment our test engineers can analyze the Rx/Tx signal through the RF Connector. The Signal goes into RF_Switch from the RF Connector to control the working status.



After the signal comes out from RF_Switch, it goes into the related Saw Filter, and the signal turns into two signals.



U201 is the transceiver, a very important chip set. For the receive part, it mainly completes: LNA(Low Noise Amplifier)? Mixer? baseband filter and so on. For example: signal from EGSM path comes out GSMA and GSMB. After LNA, they go into the mixer and are being demodulated perpendicularly with RX-VCO. The output baseband signals (IA?IB?QA?QB) after amplifier?filter come out of Pin6? Pin7? Pin8? Pin9 and input to the J13? J14? H13? H14 of CPU.



The baseband signals inside the CPU will be proceeded with analog to digital conversion?decoding?digital processor?digital to analog conversion, and the audio signal will be available to drive receiver.

3.1.4 Receive path circuit tuning up

Testing of the receive path includes RX LEVEL? RX QUALITY? BER, and so on. There are mainly five possible reasons make the receive path works abnormallyt: small amplitude of the LNA ? MIXER without outputs? no RX-VCO signal? I&Q signal of U301 and CPU incorrect decoding.

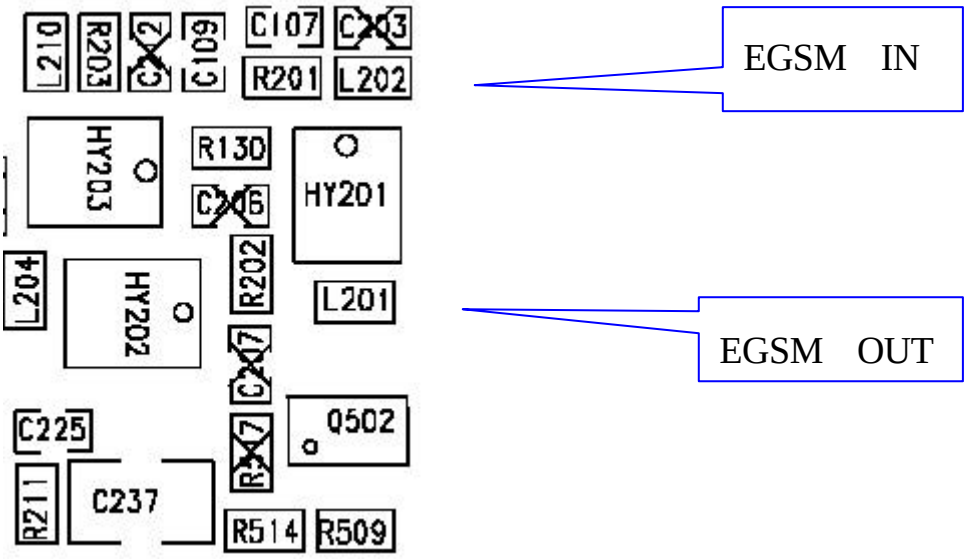
Here are the equipment we need to analyzer the problems(Such as. EGSM):

a. Set Agilent8960 to the specific channel and set the basestation out put transmit signal to -30dbm?

b. Power on the mobile, the mobile is connected with Agilent8960 by the RF cable, and let the mobile be in the receive & testing mode.

c. Power meter and oscilloscope

Step 1: According to the signal block diagram test step by step, first get rid of HY201(Saw Filter) , in this way we can avoid the interference from the backwards and test the input signal to the HY201. If the signal is kind of small, we should check the input to HY102(RF-SW) . It might be the problem with P101, C106; otherwise it might be the problem with RF-SW CS? SS? CD or other control circuit.



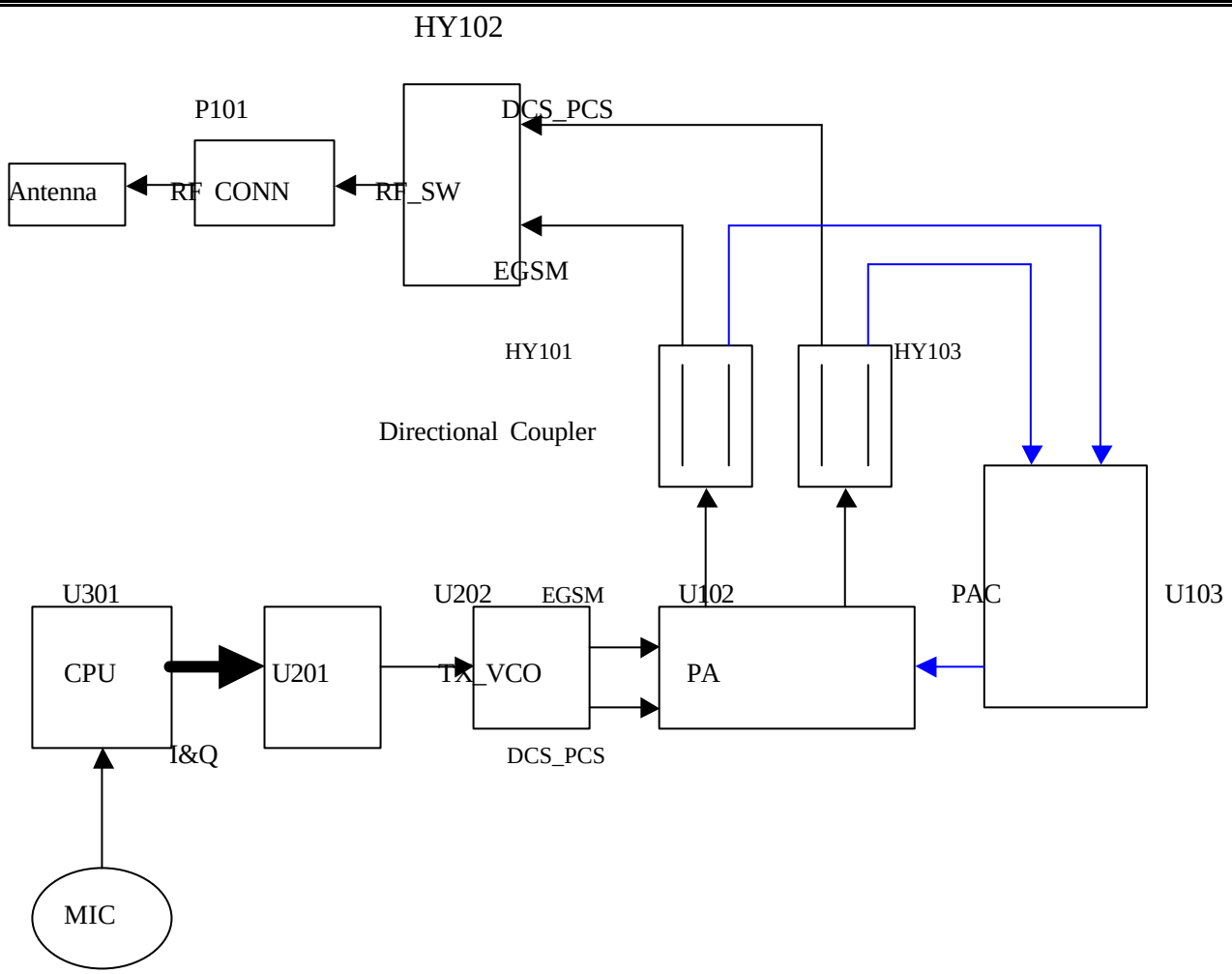
Step 2: Solder the HY201 on, test if its output signal attenuation is big, if it is big, it might have something to do with HY201-CD? SS? CS etc, or its load L201, C204, C201, U201.

Step 3: Test if RX-VCO,I&Q signals are normal or not, usually it might be the problem with C227, C230 or U201, U301—CS? CD? SS.

Step 4: If we cannot find the problem, we should changeU301, U201 or the problem with PCB.

3.2 Principle of TX Circuit

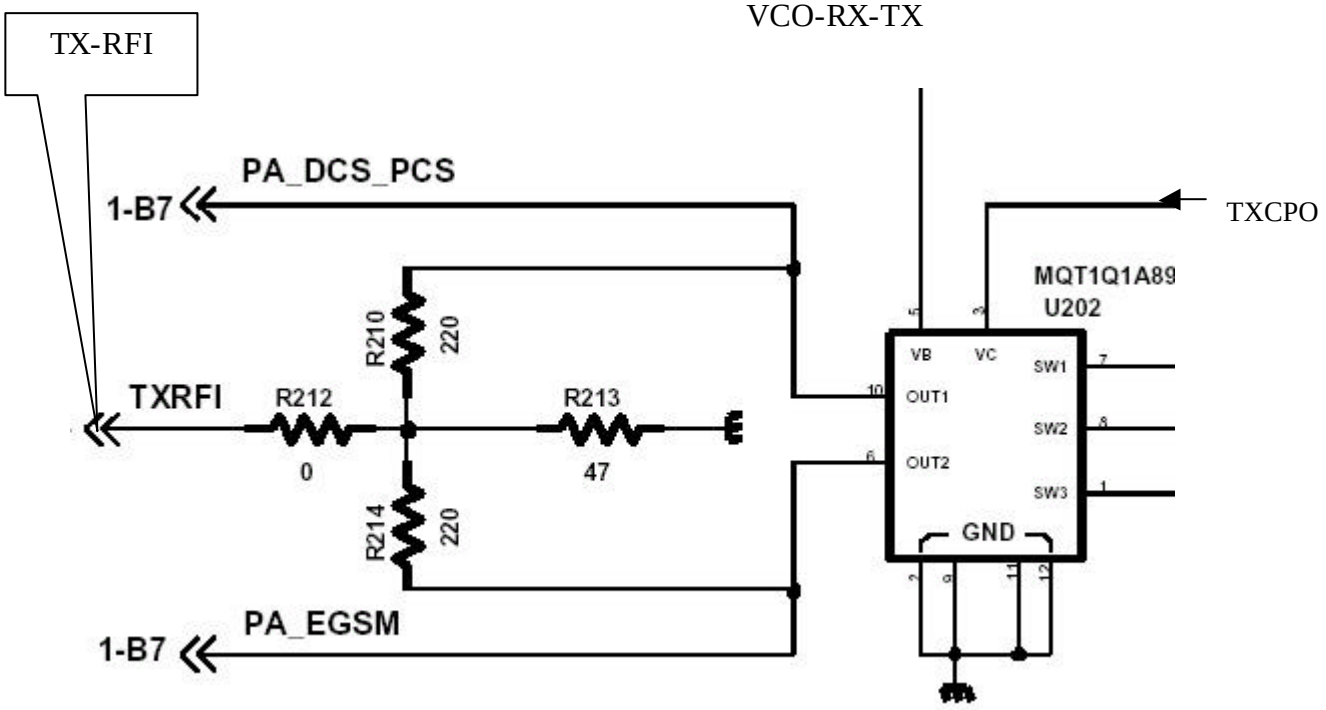
3.2.1 Transmit path circuit block diagram



Transmit signal block diagram

3.2.2 Audio signal turns into electrical signal by MIC, changes into baseband signals by A\D conversion?encoding?D\A conversion inside the CPU, output from J13?J14?H13?H14 and input into Pin6 ? Pin7 ? Pin8 ? Pin9 of U201. Baseband signals inside the U201 precede perpendicular demodulation, phase comparison etc. The output TXCPO signal, drive TX-VCO to work around the specific frequency. The TX-VCO signal from TX-RFI feeds back to U201?

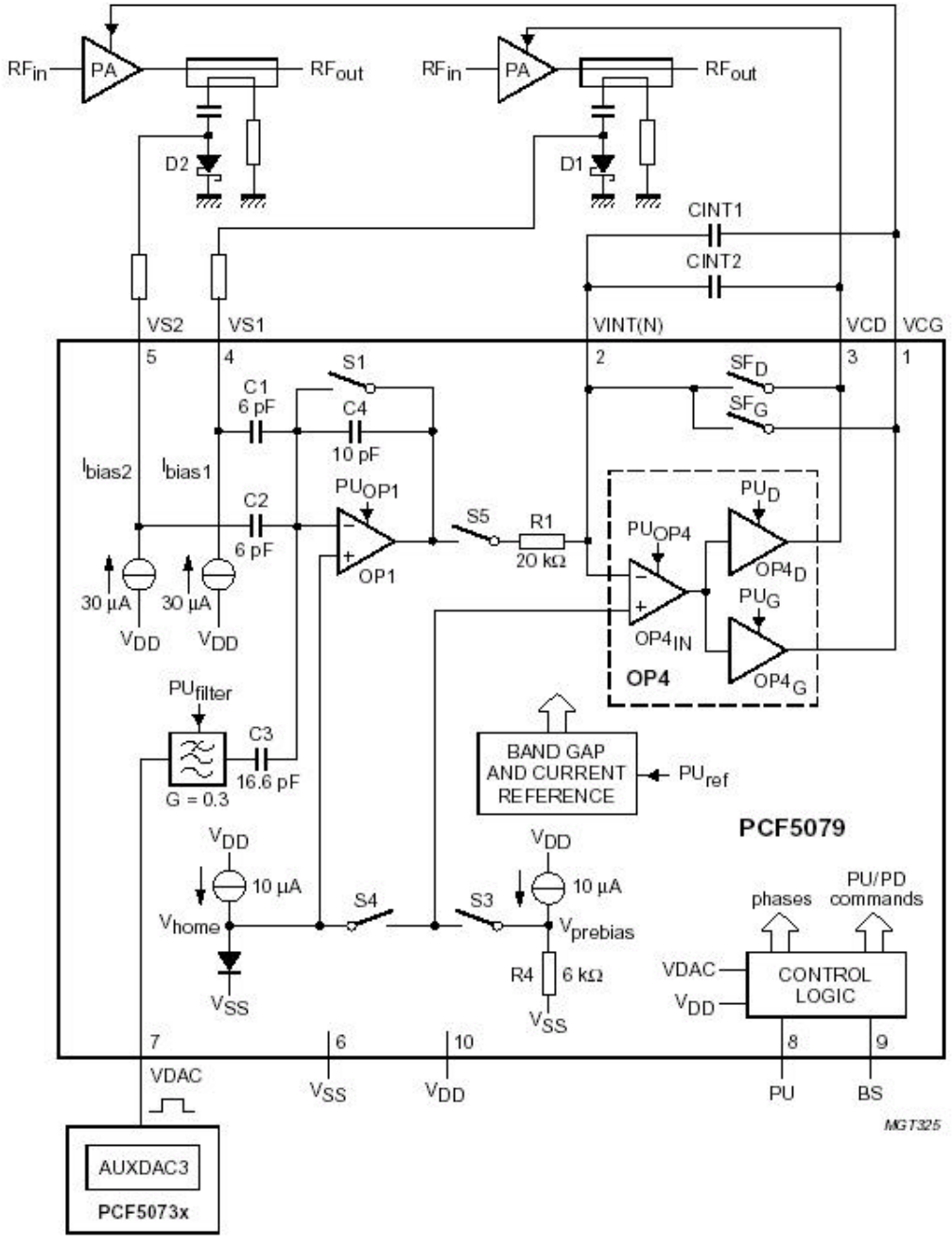
VCO-RX-TX



TX-VCO has two outputs, one is PA-EGSM and the other is PA-DCS-PCS. They all go into PA(U102)?PA is a three-band amplifying module, the maximum gain for EGSM is 35dB; the maximum gain for DCS/PCS is 32dB. PAC controls its magnifying amplitude. PA output is connected with directional coupler, which transmits RF signal and feeds back PAC. PAC will control PA's gain by the RF signal. PAC's pin description and its Black diagram are shown as below:

SYMBOL	PIN	TYPE	DESCRIPTION
VCG	1	O and A	PA control voltage output (GSM)
VINT(N)	2	I and A	negative integrator input
VCD	3	O and A	PA control voltage (DCS)
VS1	4	I/O and A	sensor signal input 1
VS2	5	I/O and A	sensor signal input 2
VSS	6	G	reference ground

VDAC	**7**	**I and A**	**DAC input voltage**
PU	**8**	**I and D**	**power-up input**
BS	**9**	**I and D**	**band selection input**
VDD	**10**	**P**	**positive supply voltage**



RF signal comes out of RF-SW from directional coupler, and transmits from the antenna by the RF-Connector.

3.2.3 Transmit circuit tuning up

The testing of transmit path includes MAX POWER? TX-CURRENT? etc.

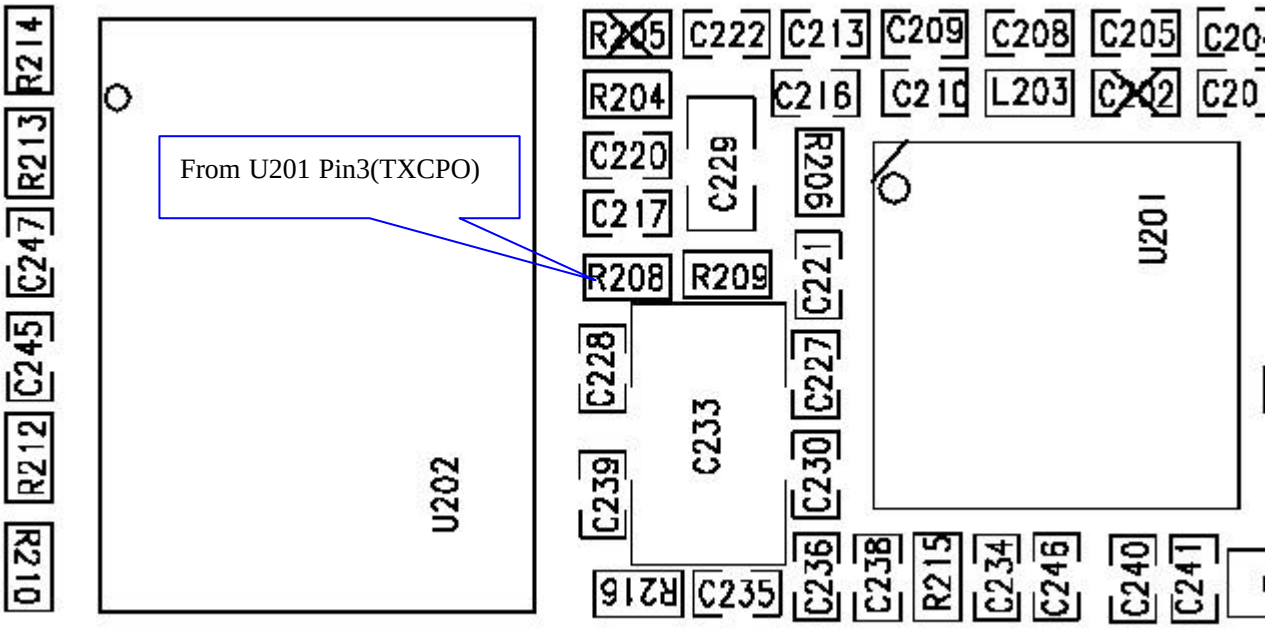
First prepare the equipment we need to analyze the mobiles with problems:(For example: EGSM)

a. Power on the mobile, enter the key and let the mobile be in the transmit/testing mode, like EGSM: Channel 1? Power Level 15;
b. Set the spectrum analyzer to the correct center frequency 890.2MHZ? bandwidth 10MHZ? and suitable scan time;
c. Power meter and oscilloscope.

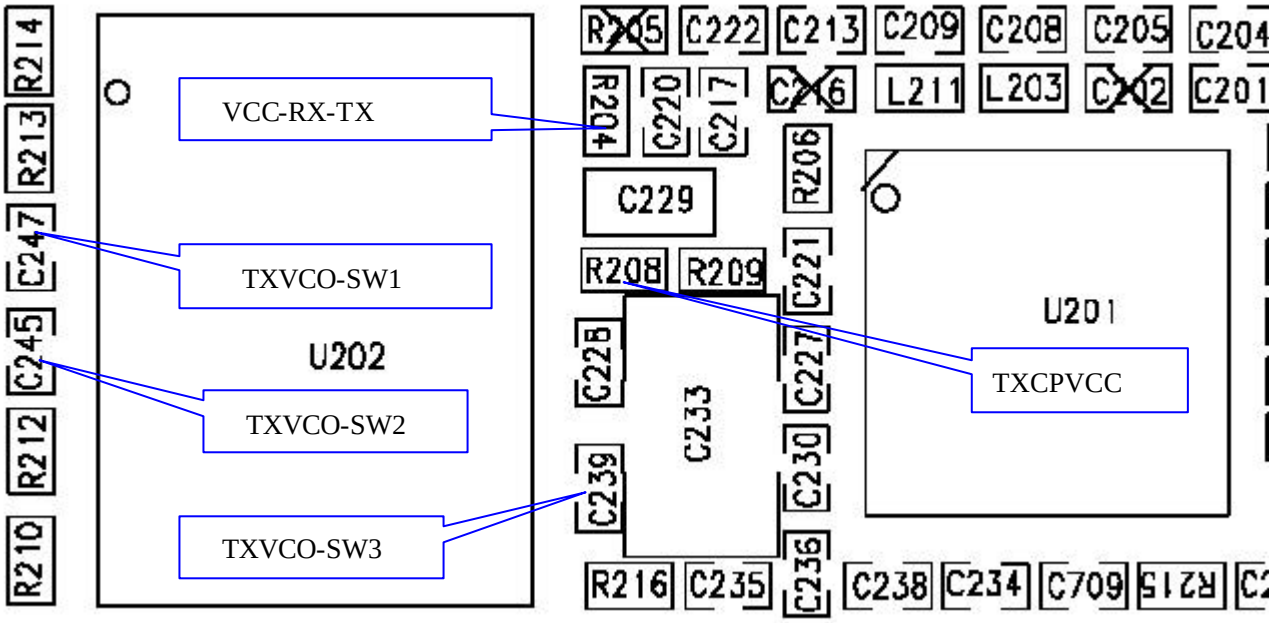
Here are the steps to check with the transmit circuit, if we are not sure about the spectrum, power or other parameter of the transmit signal, we can compare with a passed one:

Step 1: Test waveform of the IQ signal from CPU to U201 modulation/demodulation chip set. If the IQ signal is not good, we check with CPU and see if it is soldered well or not.

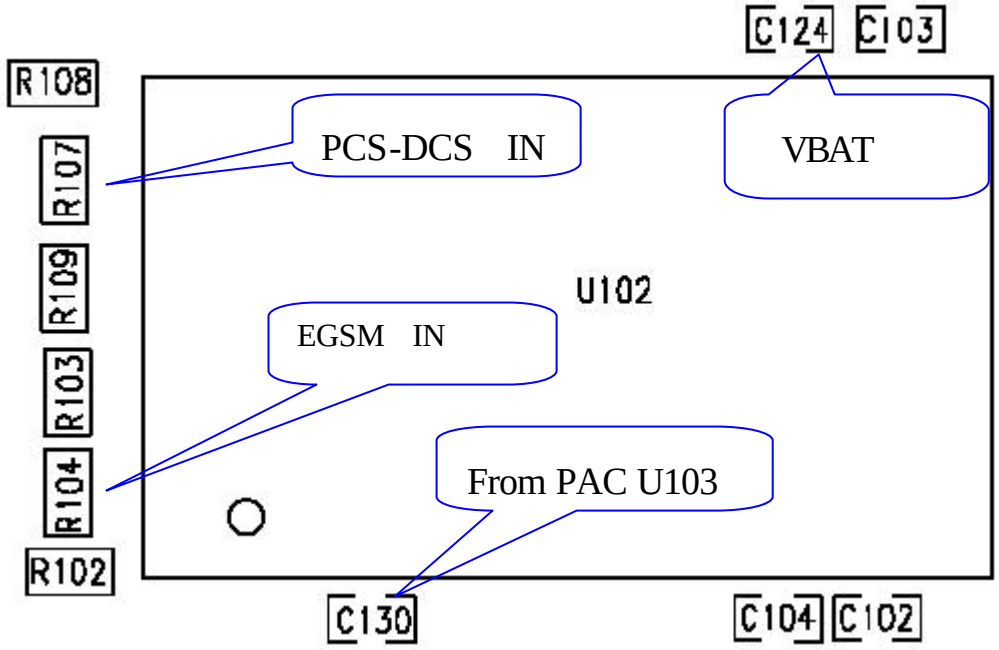
Step 2: If the IQ signal is not good, we test the TXCPO signal from U201 then. If the transmit signal is not good, check with U201; the circuit around it; and power supply voltage. If they all work well, we could think about change another U201.



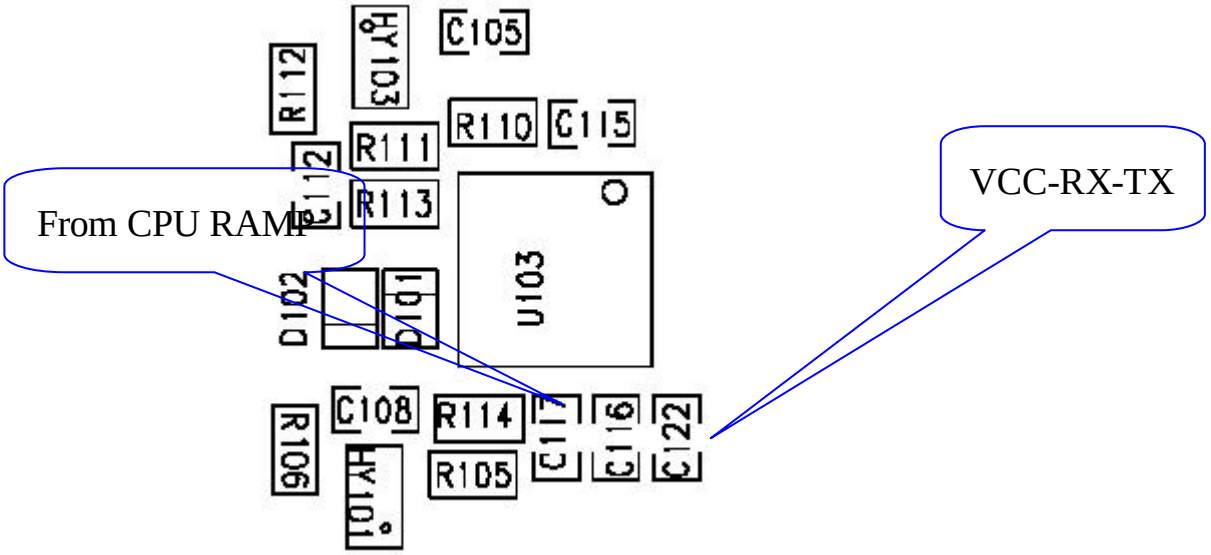
Step 3, If the output signal TXCPO from IC104 is fine, test the output of the U202: EGSM—pin 10, DCS-PCS pin6. And if the output signal is not good, test the supply voltage VCC-RX-TX of the U202 and EGSM?DCS ?PCS signal from CPU. If supply voltage signal is not good, check with U401 or change a good one; If EGSM ?DCS?PCS switching signals not nice, check with U301 or change another one. If those signals work fine, and resistance/ coil/ capacitor are all fine, then we change U202, and U201 in the end.



Step 4, If the output signal of U202 is fine, check the output signal from PA U102: for EGSM test U102 pin 5, for DCS-PCS test U102 pin 7. If the output signal from PA U102 is not good, then see if the PA is soldered well and the small stuff around it. Test VBAT of the PA and control signal RFSIG(3)?

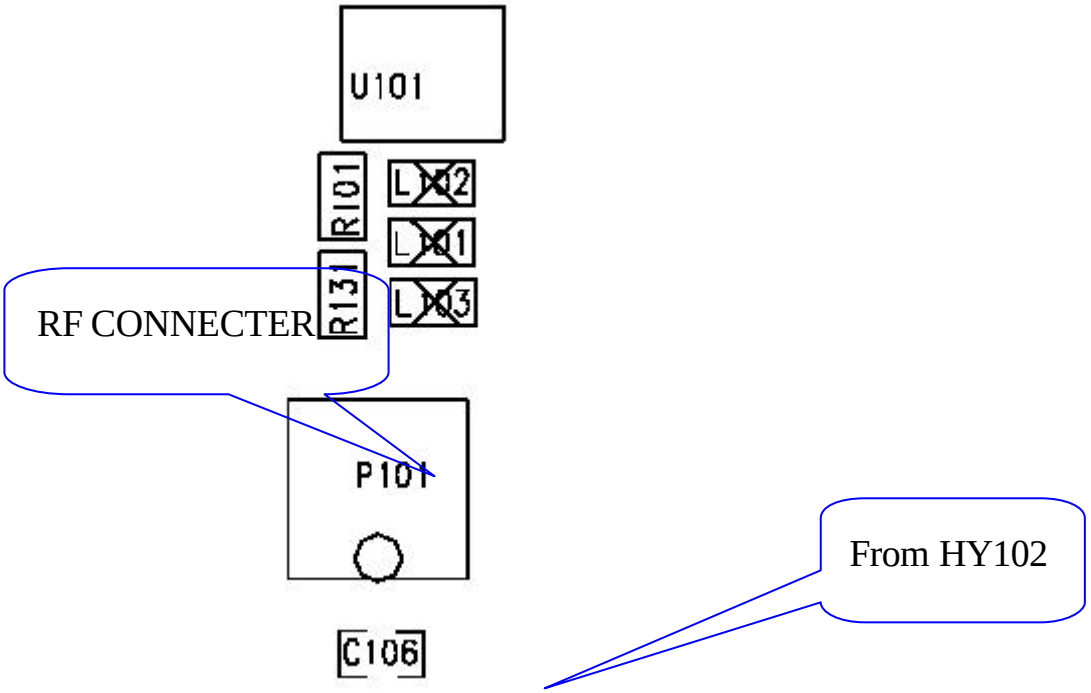


Step 5, Check PAC, U103, test VCC-RX-TX of U103 (we can test C116 instead), and see if U103 is soldered well. Check PAC and pieces around it. If they are all fine, we should change U102, U103, U201 in order.



Step 6, Test RF-SWITCH HY102 input/ output signals. Test C120 when the input signal is EGSM; test C105 when the input signal is DCS-PCS. For the output signal we could test C106. And test the supply voltage of the HY102 and its control signals.

At last, we could test the antenna, if the signal is not good from the antenna check P101, R131, R101



3.3 RF Circuit Reference

3.3.1 **UAA3536HN** Low power GSM/DCS/PCS multi-band transceiver

Features:

- Multiple band application for GSM, DCS and PCS cellular phone systems
- Compliant to GPRS class 12 operation
- Compliant to EDGE RX operation
- Low noise and wide dynamic range low IF receiver
- More than 35 dB on chip image rejection in receive
- More than 84 dB gain control range in receive
- Integrated channel filter
- Integrated TX filters
- High precision IQ modulator
- Multi-Band Tx modulation loop architecture including offset mixer and phase-frequency detector
- Fully integrated fractional N RF synthesizer with AFC control possibility
- Fully integrated RF VCO with integrated supply regulator
- Semi integrated reference oscillator with integrated coarse AFC possibility and with integrated supply regulator
- Two outputs to control RF front end switches (pin diodes)

- Fully differential design minimizing cross-talk and spurs
- Functional down to 2.4 V and up to 3.3 V
- 3-wire serial bus interface
- HVQFN40 package

Pins description:

SYMBOL	PIN	DESCRIPTION
TXRFI	1	Input from RF transmit VCOs
EXTRES	2	reference resistor for transmit modulation loop
TXCPO	3	transmit modulation loop charge-pump output
VCC(TXCP)	4	transmit modulation loop charge-pump supply
TXON	5	TX mode control pin
IA	6	baseband input-output; I path
IB	7	baseband input-output; I path
QA	8	baseband input-output; Q path
QB	9	baseband input-output; Q path
VCC(IF)	10	IF supply
CLKOUT	11	reference oscillator output
CAFCSUP	12	coarse AFC memory supply
CLKFDBX	13	reference oscillator feedback
REFGND	14	Ground for reference oscillator
REFIN	15	reference oscillator input
VCC(REF) r	16	eference oscillator supply
DATA	17	3-wire bus; DATA input
CLK	18	3-wire bus; CLOCK input
EN	19	3-wire bus; ENABLE control pin
VCC(RFCP)	20	RF charge-pump supply
RFCPO	21	RF charge-pump output
VCC(SYN)	22	synthesizer supply
RXON	23	RX mode control pin
SYNON	24	SYN mode control pin
VCC(RFVCO)	25	RF VCO supply
RFTUNE	26	tuning input of RF VCO
GNDTUNE	27	Ground for RF VCO tuning
VCC(RFLO)	28	RF LO supply
FESW1	29	frontend switch control output
FESW2	30	frontend switch control output
VCC(RF)	31	RF front-end and transmit modulation loop supply
GSMIA	32	receiver GSM RF input
GSMIB	33	receiver GSM RF input
RFGND1	34	Ground for RF frontend

PCSIA	35	receiver PCS RF input
PCSIB	36	receiver PCS RF input
RFGND2	37	Ground for RF frontend
DCSIA	38	receiver DCS RF input
DCSIB	39	receiver DCS RF input
FESWON	40	frontend switch control input

BLOCK DIAGRAM:

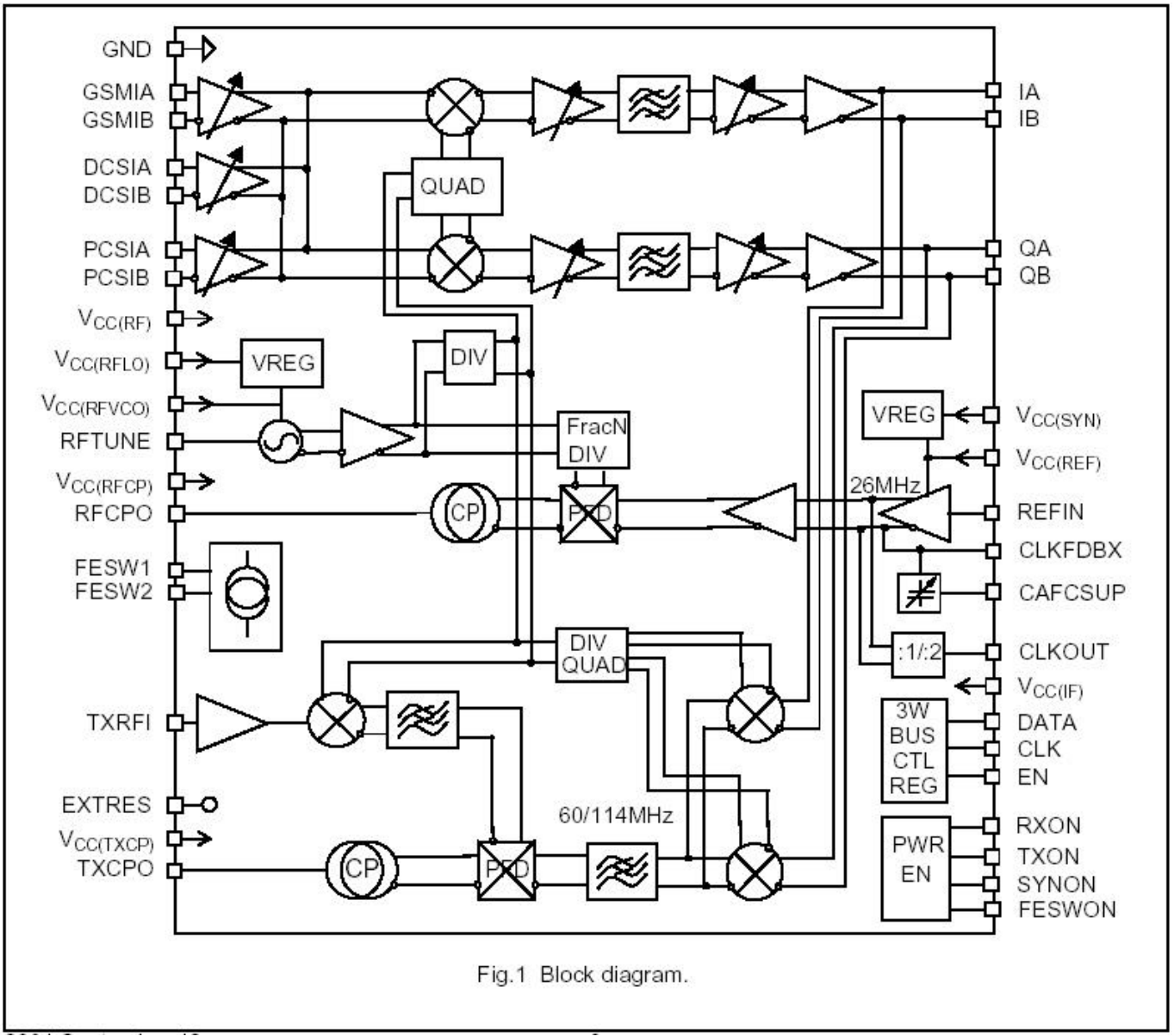


Fig.1 Block diagram.

3.4 Principle of Logic Circuit and tuning up

3.4.1 Principle of the logic circuit:

U301: OM6357EL/3C3/5 is adopted, there are two complete circuits inside the chipset, provide baseband processor？charge control？EMS memory management, etc. It includes：1？**PCF50874**：an individual System Controller with ARM, Digital Signal Processor & clock, keypad control, etc. 2？**PCF50732**：an analog baseband & audio interface，with audio processor, baseband & ancillary multi-media digital signal encoder, A/D？D/A conversers, etc. Diagram & pin description are as below:

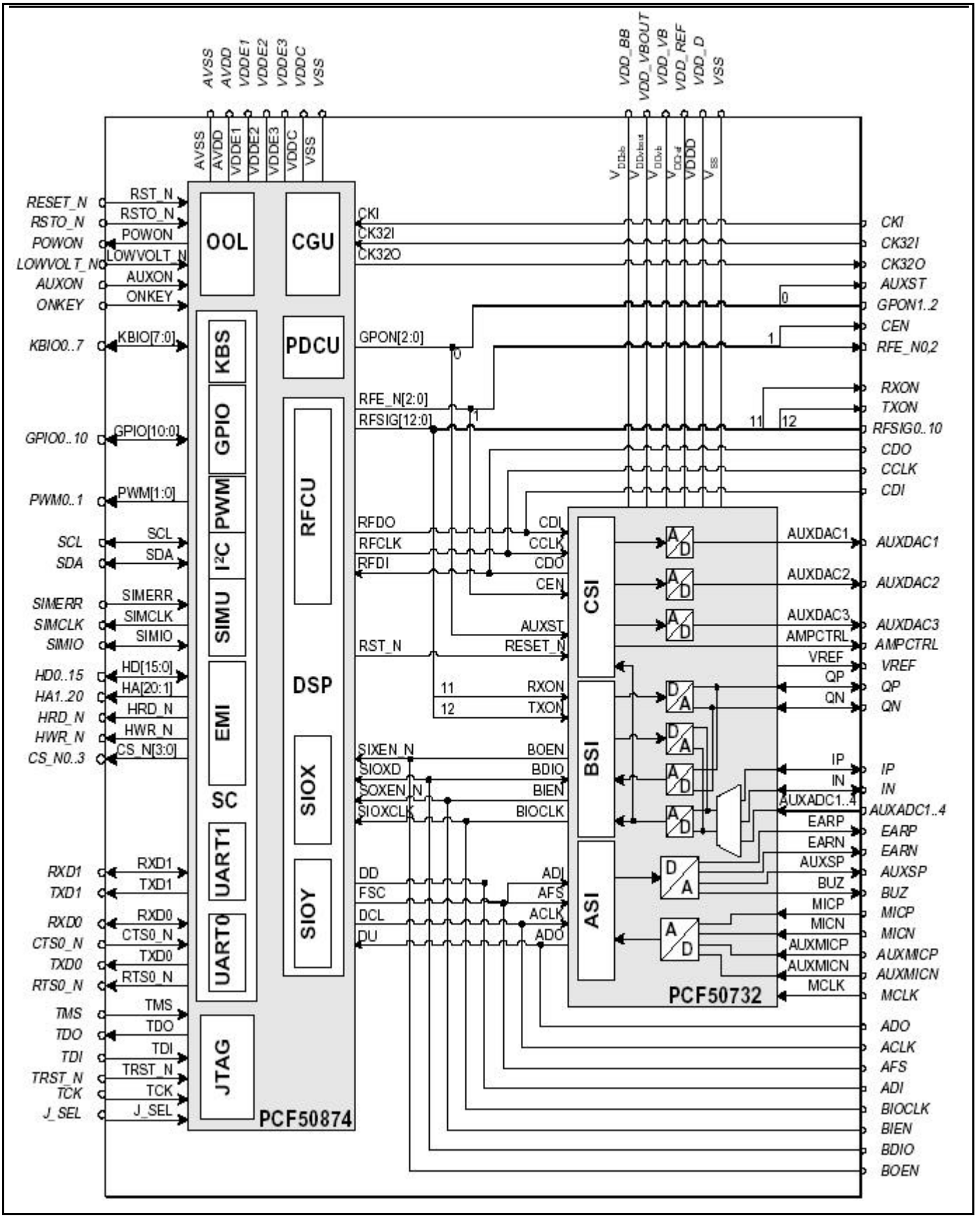


Table 6 Pin Description

OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
Power and Ground								
VSS	Ground connections PCF50874	C3, E8, G1, G13, J1, K1, K7, M7, N5, N10, N11, N14, P1, P10	G		VSS			
AVSS	Analog ground PCF50874	P10	G		AVSS			
VSS_BB	Baseband analog ground	E13				G		V_{SS}
VSS_REF	Bandgap Reference ground	C13				G		V_{SS}
VSS_VB	Voiceband ground	A12				G		V_{SS}
VSS_VBOUT	Voiceband output drivers ground	C11				G		V_{SS}
VSSD	Digital ground	D11				G		V_{SS}
VDD_BB	Analog supplies PCF50732	F12				P		VDDbb
VDD_REF		D14				P		VDDref
VDD_VB		B12				P		VDDvb
VDD_VBOUT		C12				P		VDDvbout
VDD_D	Digital supply PCF50732	C9	P			P		VDDD
AVDD	Analog supply PCF50874	P12	P		AVDD			
VDDE1	Digital supplies for PCF50874	C8, H11, N12, P9	P		VDDE1			
VDDE2		P8, C1	P		VDDE2			
VDDE3		P4, M6, G2, L3	P		VDDE3			
VDDC	Digital supply for core of PCF50874	F5, N13, M8, K6	P		VDDC			
Reference Voltage								
VREF	bandgap reference for external noise decoupling	C14				I/O	VDDref	VREF
On/Off Logic								
RESET_N	chip set reset output	C10	I/O	VDDE1	RST_N	I	VDDD	RESET_N
RSTON	PCF50874 reset input	M10	I	VDDE1	RSTO_N			
LOWVOLT_N	low voltage alarm	M9	I	VDDE1	LOWVOLT_N			
POWON	power-on	K14	O	VDDE1	POWON			

OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
AUXON	auxiliary power-on signal	K13	I	VDDE1	AUXON			
ONKEY	on/off key	M14	I	VDDE1	ONKEY			
Clocks								
CKI	13MHz clock input	P11	I	AVDD	CKI			
CKI32I	32kHz clock input	P13	I	VDDE1	CLK32I			
CK32O	32kHz clock output	P14	O	VDDE1	CLK32O			
MCLK	13MHz clock input	D10				I	VDDbb	MCLK
RF Control Interface								
CCLK	RF interface clock	E10	O	VDDE1	RFCLK	I	VDDD	CCLK
CDO	control serial data	E9	I	VDDE1	RFDI	O	VDDD	CDO
CDI	control serial data	D8	O	VDDE1	RFDO	I	VDDD	CDI
CEN	enable ctrl. serial	D9	O	VDDE1	RFE_N1	I	VDDD	CEN
RFE_N2	additional RF interface enables	K11	O	VDDE1	RFE_N2			
RFE_N0		J12	O	VDDE1	RFE_N0			
TXON	baseband transmit active	G12	O	VDDE1	RFSIG12	I	VDDD	TXON
RXON	baseband receive active	H12	O	VDDE1	RFSIG11	I	VDDD	RXON
RFSIG10	signal generator output	D7	O	VDDE1	RFSIG10			
RFSIG9		K9	O	VDDE1	RFSIG9			
RFSIG8		E7	O	VDDE1	RFSIG8			
RFSIG7		C6	O	VDDE2	RFSIG7			
RFSIG6		B7	O	VDDE2	RFSIG6			
RFSIG5		C7	O	VDDE2	RFSIG5			
RFSIG4		A7	O	VDDE2	RFSIG4			
RFSIG3		B6	O	VDDE2	RFSIG3			
RFSIG2		D6	O	VDDE2	RFSIG2			
RFSIG1		A6	O	VDDE2	RFSIG1			
RFSIG0		D5	O	VDDE2	RFSIG0			
Baseband Interface								
BIOCLK	interface clock	F11	I	VDDE1	SIOXCLK	O	VDDD	BIOCLK
BOEN	baseband serial data enable RX	G11	I	VDDE1	SIXEN_N	O	VDDD	BOEN
BDIO	baseband serial data	E11	I/O	VDDE1	SIOXD	I/O	VDDD	BDIO
BIEN	baseband serial data enable TX	F10	I	VDDE1	SOXEN_N	O	VDDD	BIEN

OM6354			CONNECTED TO DEVICE SIGNALS					
NAME	DESCRIPTION	BALL	PCF50874			PCF50732		
			TYPE	SUPPLY	NAME	TYPE	SUPPLY	NAME
Audio Interface								
ACLK	audio serial interface clock	B8	I/O	VDDE1	DCL	I	VDDD	ACLK
AFS	audio serial frame	B9	I/O	VDDE1	FSC	I	VDDD	AFS
ADO	TX audio serial	A9	I	VDDE1	DU	O	VDDD	ADO
ADI	RX audio serial	A8	O	VDDE1	DD	I	VDDD	ADI
I²C Bus								
SCL	interface clock	C2	I/O	VDDE2	SCL			
SDA	data transfer	B3	I/O	VDDE2	SDA			
Memory Interface								
HA1	memory address bus	M4	O	VDDE3	HA1			
HA2		P3	O	VDDE3	HA2			
HA3		L4	O	VDDE3	HA3			
HA4		N3	O	VDDE3	HA4			
HA5		K5	O	VDDE3	HA5			
HA6		M3	O	VDDE3	HA6			
HA7		P2	O	VDDE3	HA7			
HA8		N2	O	VDDE3	HA8			
HA9		M1	O	VDDE3	HA9			
HA10		N1	O	VDDE3	HA10			
HA11		L2	O	VDDE3	HA11			
HA12		L1	O	VDDE3	HA12			
HA13		M2	O	VDDE3	HA13			
HA14		J2	O	VDDE3	HA14			
HA15		J5	O	VDDE3	HA15			
HA16		K3	O	VDDE3	HA16			
HA17		J4	O	VDDE3	HA17			
HA18		K4	O	VDDE3	HA18			
HA19		K2	O	VDDE3	HA19			
HA20		G4	O	VDDE3	HA20			