
# PUCCINI Operation Theory

T-000-0000

V 1.0

2004-08-10

# History

| | |
|---|---|
| 2004/8/10 | Created by PUC Team |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |

# Table of Contents

**1 GENERAL DESCRIPTION OF PUCCINI GSM RADIO CIRCUITS..... 4**

1.1 BASEBAND CIRCUITS ..... 5

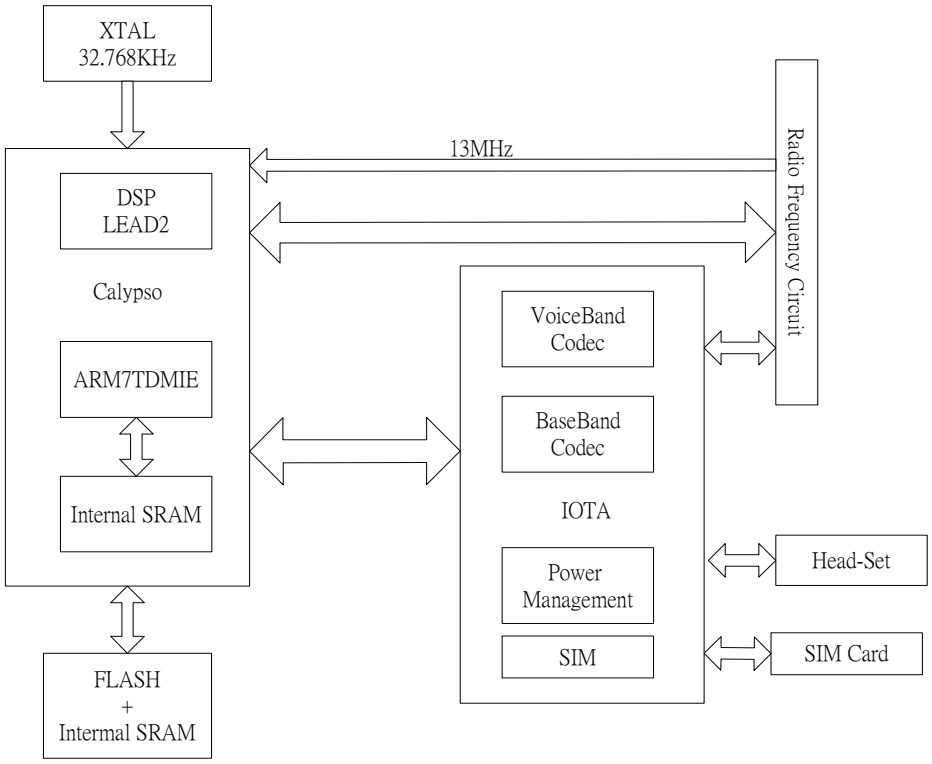
1.2 RADIO FREQUENCY CIRCUITS ..... 7

**2 FUNCTIONAL DESCRIPTION..... 8**

# 1 General Description of PUCCINI GSM Radio Circuits

Generally, the PUCCINI GSM Radio circuits are divided into 2 parts: Baseband(BB) circuits and Radio Frequency (RF) circuits.

## 1.1 Baseband circuits




Block Diagram of Base-band Circuit

The Base-band circuits mainly consist of 3 chips: CALYPSO, IOTA, Flash memory.

CALYPSO (U201) is a chip implementing the digital Base-band processes of a GSM/GPRS mobile phone. This chip combines a DSP sub-chip (LEAD2 CPU) with its program and data memories, a Micro-Controller core with emulation facilities (ARM7TDMIE), internal 8Kb of Boot ROM memory, 4M bit SRAM memory, a clock squarer cell, several compiled single-port or 2-ports RAM and CMOS gates.

The application of CALYPSO is the management of the GSM/GPRS Base-band processes through the GSM layer 1, 2 and 3 protocols as described in the ETSI standard with a specific attention to the power consumption in both GSM dedicated and idle modes, and GPRS (class 12) capability.

The IOTA-TWL3014 (U203), includes a complete set of Base-band functions that perform the interface and processing of the following voice signals, the Base-band in-phase (I) signal and quadrature (Q) signals, which support single-slot and multi-slot modes. The IOTA also includes associated auxiliary RF control features, supply voltage regulation, battery charging controls, and switch ON/OFF system analysis.

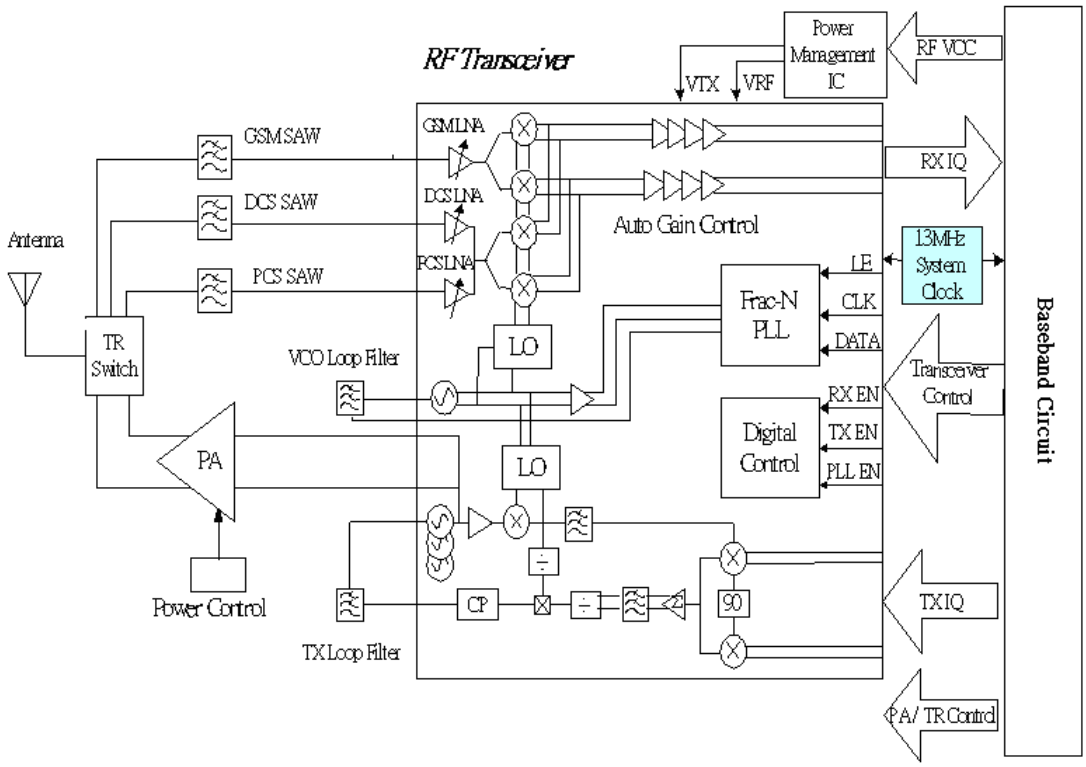
The IOTA interfaces with the digital Base-band device, Calypso, through a digital Base-band serial port (BSP) and a voice-band serial port (VSP). The signal ports communicate with a DSP core (LEAD). A micro-controller serial port (USP) communicates with the micro-controller core and a time serial port (TSP) communicates with the time processing unit (TPU) for real time control.

A specific module is dedicated to support the 3V SIM card interface. The module includes the generation of the SIM card supply voltage as well as level shifters to adapt the SIM card signal levels to the micro-controller I/O signal levels.

The IOTA also includes an on-chip voltage reference; under-voltage detection and power-on reset circuits.

The Flash memory (U301) is used to store code and other parameters. It contains 32M-bit Flash memory

## 1.2 Radio frequency circuits




The RF circuits consist of the Skyworks transceiver (CX74063), Power amplifier (CX77315), T/R switch, RF SAW Filter, voltage regulator, TCXO, and some other circuits.

The TCXO is used to generate 26MHz signal. It's the fundamental frequency source of the PUC GSM Radio circuits.

The voltage regulator is used to offer the stable, low-noise 2.8V. This 2.8V supplies all RF circuits except PA.

The T/R switch is used to switch the signal path to the directions of Transmit / Receive of GSM900 / DCS1800 / PCS1900 so that the signal goes to the correct path.

The RF SAW Filters are used to filter out-of channel noise.

The PA CX77315 is used to amplify uplink signal to the required signal strength.

# 2 Functional Description

The Skyworks Chipset provides a low cost, highly integrated RF solution that supports GSM/GPRS applications in up to triple bands (EGSM, DCS, and PCS). The chipset also supports EDGE receive mode1.

Extremely high levels of integration and optimum system architecture combine to reduce component count and cost as compared to traditional GSM approaches and “new” direct conversion architectures currently available.

The GSM/EDGE solution consists of the transceiver CX74063, and the CX77315 Tri-BAND Power Amplifier Module.

When combined with a future integrated tri-band T/R “switchplexer” module, and minimal external discrete resistors, capacitors, and inductors, the chipset forms a complete state-of-the-art antenna-to-baseband Tri-BAND RF solution.

The receiver is consist of the DCR (Direct Conversion Receiver) architecture was chosen to obtain the benefits of direct conversion.

The transmit section is OPLL (Offset Phase Lock Loop) structure and reduce external SAW filter and excellent phase error performance.

The synthesizer is Fractional-N PLL structure, its benefit is fast locking time and can meet GPRS multi-slot requirement.

The Tri-BAND Power Amplifier module allows for an extremely simple PA lineup. The fully self-contained module includes all input and output matching, as well as fully integrated power control circuitry which varies the PA output power according to a ramp control voltage, while keeping the devices operating in saturation, for maximum efficiency throughout the gain range. The integrated power control circuitry eliminates the need for directional couplers, detector diodes, and power control ASIC’s, reducing complexity and improving PA efficiency.