1. HW Feature

Table1.1 HW Feature

Item	Description	Remark
Modem	Qualcomm MSM6025 Packet data rates of 153 kbps on the forward and reverse links	
RF chip	RFT6122+RFR6122+RF PAM+19.2MHz TCXO	
PMU	PM6610	
LCD	1. 128*128pixels CSTN, Transflective type 2. 65K colors 3. Solomon SSD1779Z Driver 4. 1.41inch	
Antenna	Internal type	
Memory	Silicon7 SV6C2832UTA 1. 128Mbits Nor-Flash 2. 32Mbits SRAM	
Camera	1. Sensor 300K -. HV7131RP-FB-SD74 2. Camera backend chip -. MV3018SOK	
External I/F	1. UART for DM 2. USB for Data service 3. Hands-Free (analog mode) 4. Travel Adapter 5. JTAG for Development	
Travel adapter	1. Input AC 100 ~ 240V, 50 ~ 60Hz 2. Output DC 5V, 500mA	
Other	Shield CAN Usage	

2. System block diagram

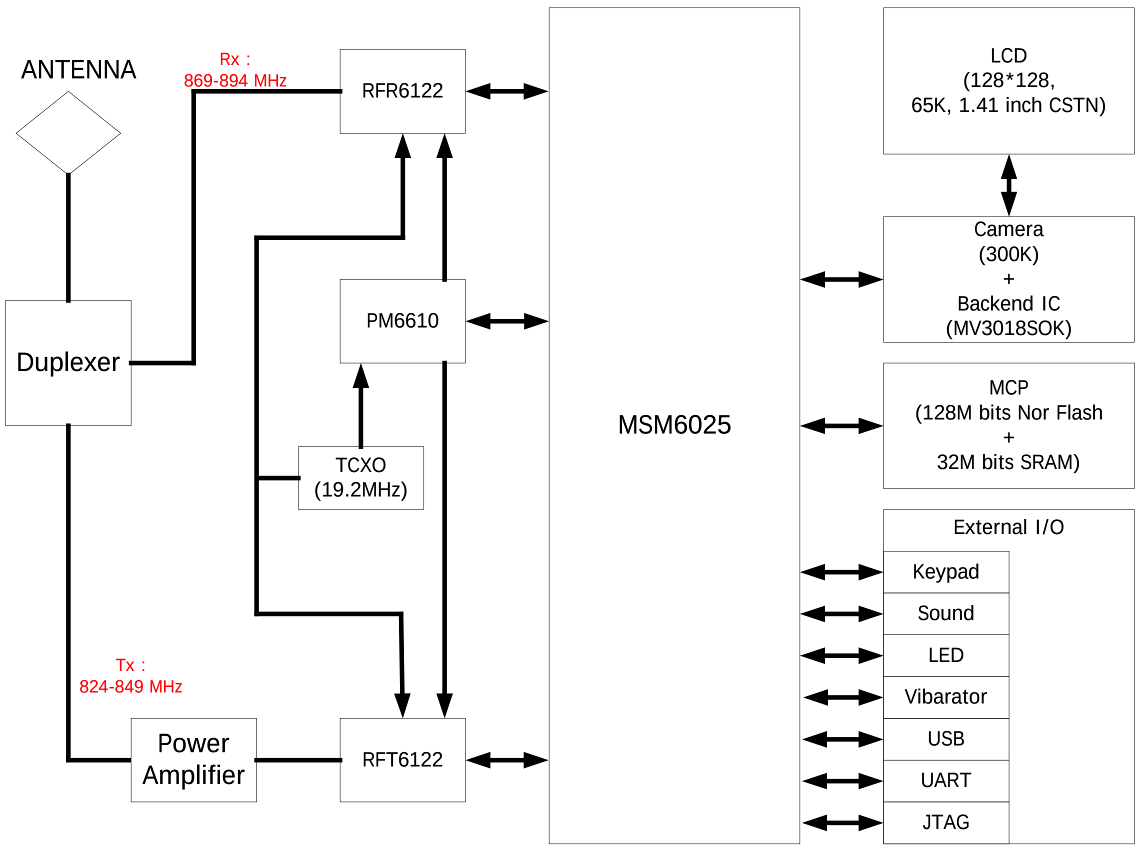

FIG.2-1 SYSTEM BLOCK DIAGRAM

3. SYSTEM OVERVIEW

3.1 Description of HW Circuitry

3.1.1 MSM6025

1. radioOne architecture
2. CDMA2000 1X support, offering data rates up to 153kbps on the forward and reverse links
3. Vocoder support (EVRC)
4. Integrated wideband mono voice CODEC
5. Voice recognition (VR)
6. Acoustic echo cancellation
7. External stereo DAC support
8. CMX (text, picture, and MIDI streaming)

3.1.2 PM6610

1. Power management, housekeeping, and user interface functions
2. Input power management
   A. Valid external supply attachment and removal detection
   B. Supports unregulated external charger supplies
   C. Supports lithium-ion main batteries
   D. Constant current, constant voltage, and pulse charging
   E. Battery voltage detectors with programmable thresholds
   F. Charger current regulation and real-time monitoring
   G. Charger transistor protection by power limit control
   H. Control driver for an external pass transistor
   I. Voltage, current, and power control loops

3. Output voltage regulation
   A. Seven low dropout regulator circuits with programmable output voltages, implemented using two different current ratings: 150 mA (six) and 50 mA (one). These can be used to power MSMP, MSMC, MSMA, RUIM, RFRX, RFTX, and TCXO circuits.
   B. Supports dynamic voltage scaling (DVS) for MSMC
   C. All regulators can be individually enabled/disabled for power savings

D. All regulated outputs are derived from a common bandgap reference – close tracking

4. Integrated handset-level user interface
5. IC-level interfaces
   A. MSM-compatible 3-line serial bus interface for efficient initialization, status, and control
   B. Supports the MSM interrupt processing with an internal interrupt manager
   C. Many functions monitored and reported through real-time and interrupt status signals
   D. Dedicated circuits for controlled power-on sequencing, including the MSM reset signal
   E. Several events continuously monitored for triggering power-on/power-off sequences
   F. Supports and orchestrates soft resets

3.1.3 RFR6122

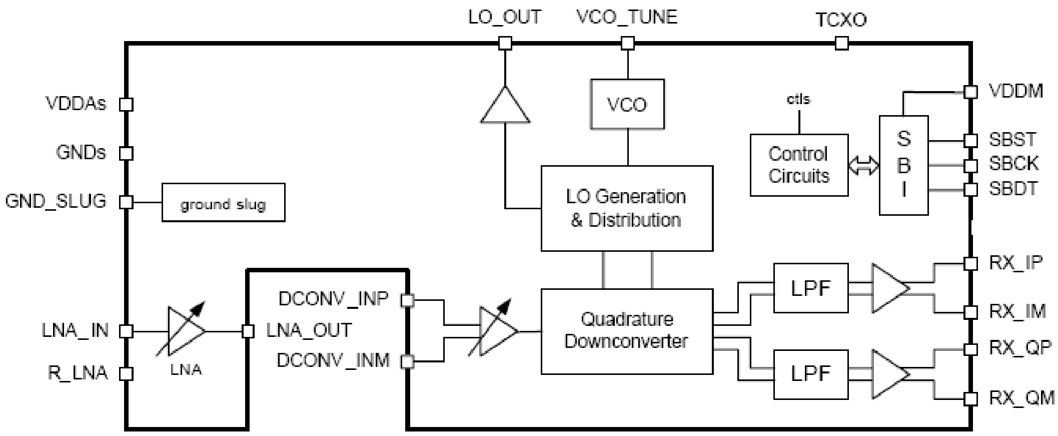

FIG.3-1 RFR6122 IC FUCTIONAL BLOCK DIAGRAM

1. This model use ***QUALCOMM's radioOne CMOS RF chipset*** that eliminates receive and transmit intermediate frequencies.(zero IF Support)
2. This chip is optimized for single-band, single-mode operation: Cellular-CDMA
3. Supports CDMA2000 1X and CDMA2000 1X EV-DO modes
4. Suitable for receive diversity applications that requires two RFRs and antennas.
5. Full downconversion from RF to analog baseband.
6. RF amplifiers (LNA) with Stepped gain control function are implemented.
7. RF-to-baseband quadrature downconverters

8. Lowpass filters, baseband amplifiers
9. Rx LO generation (UHF VCO) except receiver PLL
10. Receiver VCO is locked by other IC's PLL (included in RFT6122 in this model)
11. Power reduction features control extends handset standby time
12. Low power supply voltage (2.5 to 2.8 V), low power dissipation

3.1.4.RFT6122

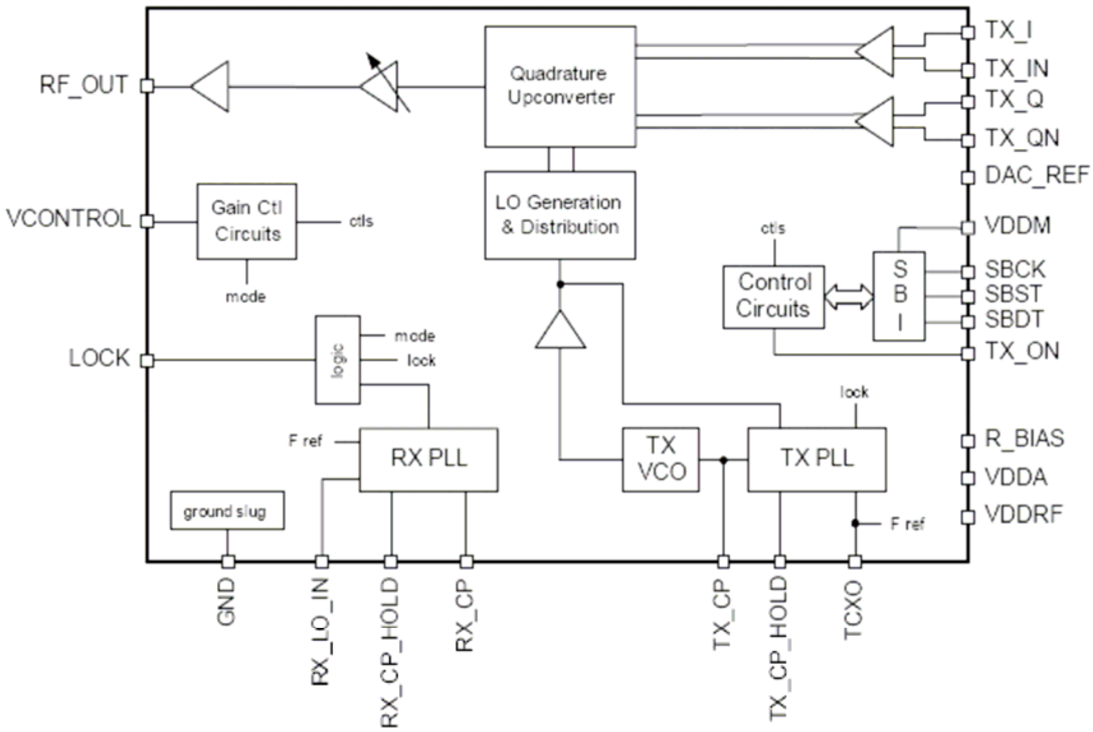

FIG.3-2 RFT6122 IC FUCTIONAL BLOCK DIAGRAM

1. This model use QUALCOMM's radioOne CMOS RF chipset that eliminates receive and transmit intermediate frequencies.
2. This chip is designed to support for single-band, single-mode operation: Cellular-CDMA
3. Supports CDMA2000 1X and CDMA2000 1X EV-DO modes
4. Full upconversion from analog baseband to RF
5. Transmit signal path circuits
    A. Baseband amplifiers
    B. Baseband-to-RF quadrature upconverters
    C. RF AGC amplifiers and driver amplifiers

6. Supports all handset LO sources
    A. Tx synthesizer (on-chip VCO and PLL circuits)
    B. Rx PLL circuit
7. RF AGC Amplifier have greater than 85-dB transmit power control range.
8. Power reduction features via MSM control extends handset talk-time
    A. Optimized for low DC power consumption versus RF output power level
    B. Transmit puncturing
    C. Selective circuit power-down
    D. Gain control
9. Low power supply voltage (2.5 to 2.8 V), low power dissipation

3.2 MSM6025's Memory Interface

In the MSM6025 device, the external memory interface is upgraded to support page mode memories and NAND flash memories, and allows access to external memories by the ADSP QDSP4 processor. The ADSP uses the direct memory exchange (DME) interface for that purpose.

1. Interface support for generic (asynchronous interface) NOR FLASH and SRAM devices
2. Interface support for byte addressable 16-bit devices (ub_n and lb_n signals)
3. Interface support for 8-bit devices on SRAM0, SRAM1, GP0 and GP1 chip selects
4. Interface support for page mode memories on all chip selects (with the exception of LCD)
5. Programmable first access wait state for page mode memories
6. Interface support for some Pseudo-Static types of RAM by means of a programmable address to cs_n setup time
7. Programmable recovery/turnover wait states for each cs_n
8. Programmable and separate write access and read access wait states for each cs_n

3.2.1 Access Types

In the MSM6025 AHB system, three different transfer sizes can be attempted: WORD(32bits), HWORD(16bits), and BYTE transfers.

Table 3.2.1 Access Type by chip select

Chip Select	32x16	16	8ubx16	8lbx16	32x8	16x8	8
ROM_CS0_N	Y	Y	Y	Y	N	N	N
ROM_CS1_N	Y	Y	Y	Y	N	N	N
RAM_CS0_N	Y	Y	Y	Y	Y	Y	Y

RAM_CS1_N	Y	Y	Y	Y	Y	Y	Y
GP_CS0_N	Y	Y	Y	Y	Y	Y	Y
GP_CS1_N	Y	Y	Y	Y	Y	Y	Y
LCD_CS_N	Y	Y	N	N	Y	Y	Y

3.2.2 Memory Map

Table 3.2.2 Memory Map

ADDRESS RANGE	SIZE	USE	DATABUS
0X10000000~0X11FFFFFF	32Mbytes	ROM_CS0_N	16Bit Silicon7 : 128Mbits
0X12000000~0X13FFFFFF	32Mbytes	Reserved	
0X14000000~0X15FFFFFF	32Mbytes	RAM_CS0_N	16Bit Silicon7 : 32Mbits
0X1C000000~0X1DFFFFFF	32Mbytes	LCD_CS_N(MV3018SOK)	LCD (LCD_CS_N): 8Bit (128x128 dots) 65K color

3.3 System connector

Table 3.3 System connector

Pin num.	Pin name	Description	I/O
1	UART_TX	Transmit data of UART interface	O
2	TDO	JTAG Data Output	O
3	TCK	JTAG Clock	I
4	TMS	JTAG Mode Selection	I
5	TDI	JTAG Data Input	I
6	TRST	JTAG Reset	I
7	GND	General Ground	G
8	HF_RIGHT	Hands Free speaker right line. There is decoupling capacitor of 47uF inside the phone.	O
9	HF_RECO1	Hands Free Recognition. This pin must be connected to GND inside Hands Free accessory.	I
10	HF_MIC	Hands Free MIC line. Internal DC Supply is applied to Hands Free Device.	I

11	HF_LEFT	Hands Free speaker left line. There is decoupling capacitor of 47uF inside the phone.	O
12	RST_IN	System Reset	I
13	USB_VBUS	Power supply from USB interface	I
14	USB_DN	Negative data line from USB interface.	O
15	USB_DP	Positive data line from USB interface	O
16	GND	General Ground	G
17	VCHARGE	Charger voltage	P
18	UART_RX	Receive data of UART interface	I

I: INPUT O: OUTPUT P: POWER G: GROUND

3.4 GPIO Map

Table 3.4 GPIO Mapping

GPIO Num.	Function (RESET STATUS)	Description	I/O
0	RESERVED		
1	TX_ON	ALTERNATE FUNCTION	
2	RESERVED (PU)		
3	RESERVED	-	I
4	HF_RECO (PD)	Recognize an existence of Hands Free Set . Hands Free set must have GND	I
5	RESERVED (PD)		
6	RESERVED (PD)		
7	KEY_LED_EN (PD)	LED enable	O
8	RESERVED (PD)		
9	RESERVED		
10	RESERVED		
11	USB_DATA		
12	USB_OE_N		
13	USB_VMO		
14	USB_VPO		
15	EXT_MIC_SW_N (PU)	If [GPIO_4 = High] External MIC Switch in Hands Free (ACTIVE High).	I
16	PS_HOLD (PU)	Power enable holding signal (ACTIVE HIGH). After power on, this pin must be high quickly	O

17	RESERVED (PU)		
18	EAR_PATH (PD)	EAR PATH SWITCHING. 0: ear sound enable 1: car ear sound enable	O
19	-	-	I
20	RESERVED (PD)		
21	RESERVED (PD)		
22	RESERVED (PU)		
23	RESERVED (PD)		
24	RESERVED (PU)		
25	RESERVED (PD)		
26	RESERVED (PD)		
27	RESERVED (PD)		
28	RESERVED (PD)		
29	RESERVED (PD)		
30	RESERVED (PD)		
31	RESERVED (PD)		
32	RESERVED (PU)		
33	RESERVED (PU)		
34	RESERVED (PU)		
35	RESERVED (PU)		
36	RESERVED (PD)		
37	MLCD_CS_N		
38	A21		
39	A22		
40	RESERVED (PD)		
41	RESERVED (PD)		
42	AUDIO_AMP_EN (PD)	Audio amplifier shutdown control 0: Shutdown status 1: On status	O
43	PM_INT_N (PU)	PM IC interrupt signal (ACTIVE LOW)	I
44	-	-	O
45	CAM_INIT (PD)		I
46	RESERVED (PD)		O
47	RESERVED (PD)		
48	MEMORY READY (PU)	Flash Memory ready/busy	I

		1: Memory ready 0: Memory busy	
49	LCD_LIGHT_EN (PD)	Control LCD Back light. LCD Backlight Charge pump IC need trigger signal to control output voltage of IC. 32 individual current level setting. Code 32 is full scale.	O
50	RST_MV (PU)	Camera backend chip reset signal (ACTIVE LOW)	O
51	RESERVED (PU)		
52	RESERVED (PU)		
53	RESERVED (PD)		
54	USB_SUSPND (PD)	USB transceiver suspend (ACTIVE HIGH).	O
55	TCXO_EN (PU)	Enable main clock (ACTIVE HIGH).	O
56	-	-	I
57	SCAN1 (PD)	Pulse for Key matrix	O
58	SCAN2 (PD)	Pulse for Key matrix	O
59	SCAN3 (PD)	Pulse for Key matrix	O
60	SCAN4 (PD)	Pulse for Key matrix	O
61	SCAN5 (PD)	Pulse for Key matrix	O
62	KYPD0	ALTERNATE FUNCTION	
63	KYPD1	ALTERNATE FUNCTION	
64	KYPD2	ALTERNATE FUNCTION	
65	KYPD3	ALTERNATE FUNCTION	
66	PWR_ON_SENSE_N	ALTERNATE FUNCTION	

3.5 HKADC

Table 3.5 Housing Keeping ADC

HK ADC Num.	Function	Description
0	PMIC_AMUX	PMIC
1	THM_ADC	POWER AMP Temperature
2	-	-
3	PWR_DET	Transmitter RF Power Level
4	BATT_ID	Check the Battery exist or not

3.6 Powers and Reset

3.6.1 Powers

Table 3.6.1 PM6610 LDO Output Voltage Init. Value (default status)

Output Name	**Description**	**Output Voltage**	**Limit Current**
VREG_MSMP	MSM peripheral function.	2.8V (on, 2.85V)	150mA
VREG_MSMC	MSM core function.	1.8V (on, 1.9V)	150mA
VREG_MSMA	MSM analog function.	2.6V (on, 2.6V)	150mA
VREG_RX	Receiver circuits.	2.6V (off, 2.6V)	150mA
VREG_TX	Transmitter circuits.	2.6V (off, 2.6V)	150mA
VREG_TCXO	VCTCXO circuits.	2.8V (on, 2.85V)	50mA
VREG_RUIM	Camera Module.	2.8V (off, 2.85V)	150mA

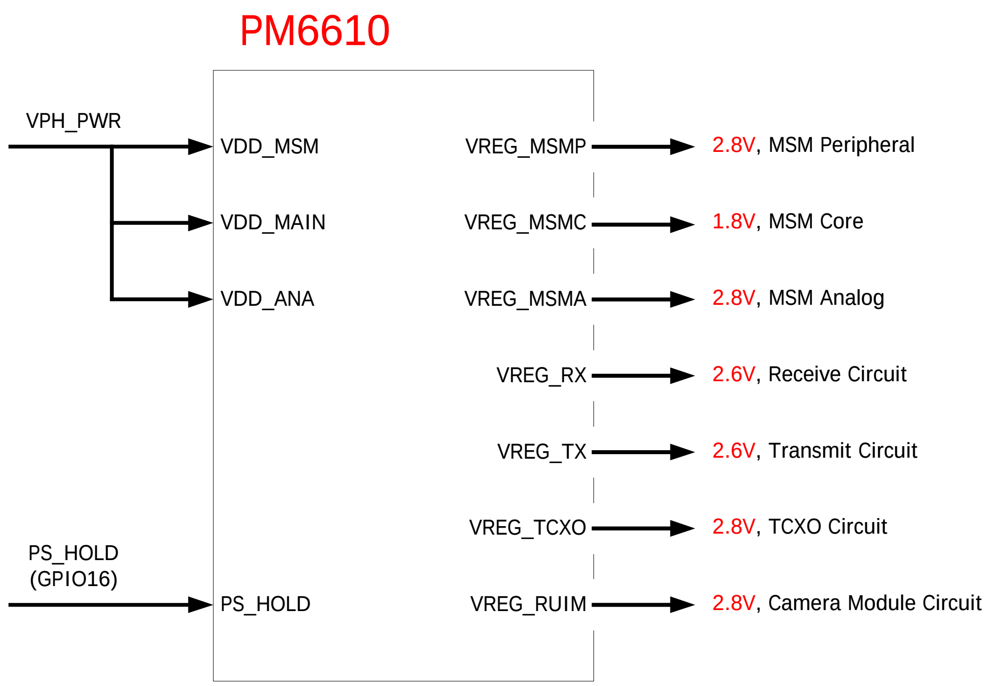

FIG.3-3 PM6610 OUTPUT VOLTAGE

3.6.2 POWER Sequence

1. Power on

A. Power Keypad pressed pulls KPDPWR_N low

B. Default ON regulators turned on sequentially and PON_RESET_N(Out in PMIC) is low

C. PON_RESET_N goes high, releasing MSM reset

D. MSM drives PS_HOLD high in PMIC to keep phone on

2. Power off

A. Keypad pressed pulls KPDPWR_N low and MSM recognize Power Keypad in low state, and then maybe start to count in low state. When MSM meet thread

B. MSM drives PS_HOLD low (MSM requests power-down to PMIC in status type)

C. PM drives PON_RESET_N low – resets MSM, others

D. In case of Power off, Regulators turned off sequentially

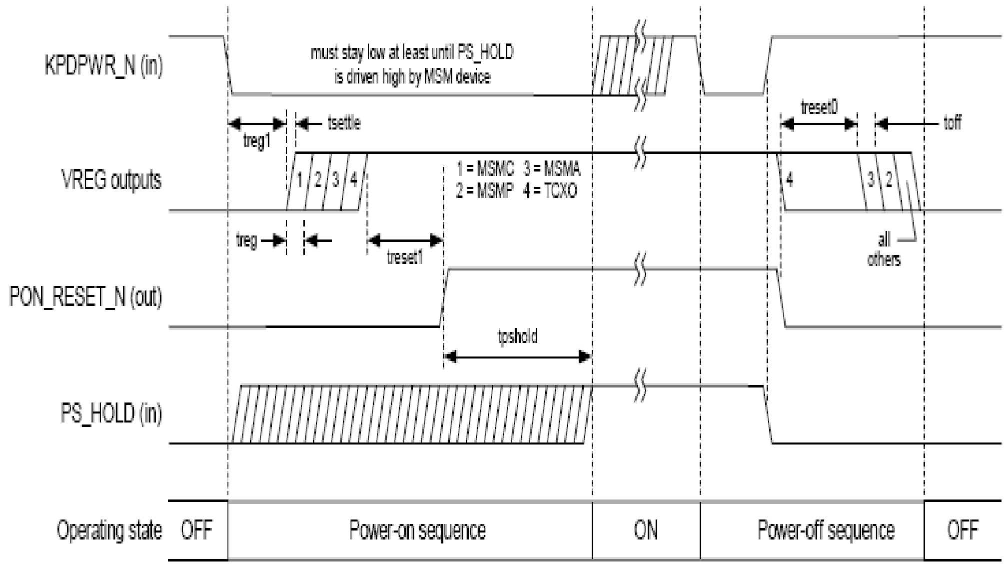

FIG.3-4 POWER ON-OFF SEQUENCES

3.6.3 Reset

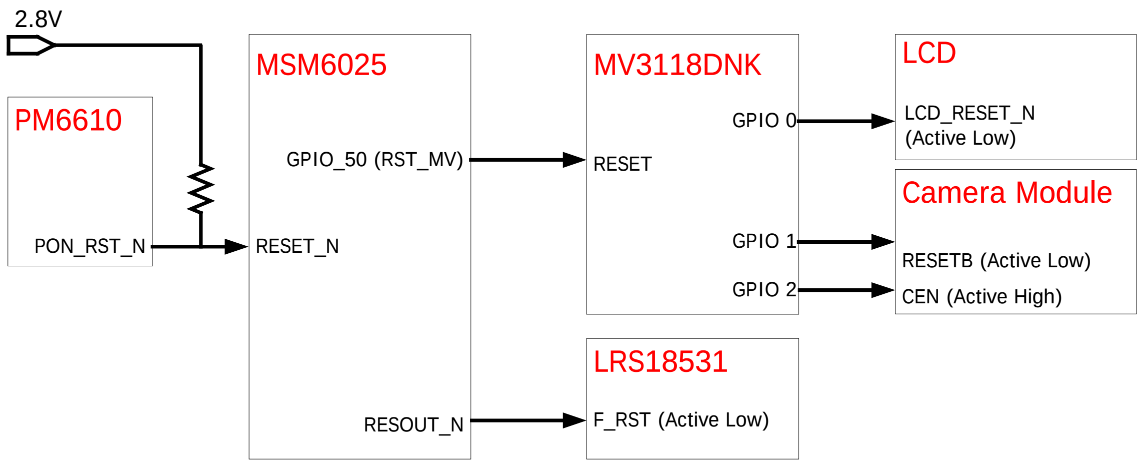

FIG.3-5 RESET BLOCK DIAGRAM

4. INTERAFCE DESCRPTION

4.1 Memory

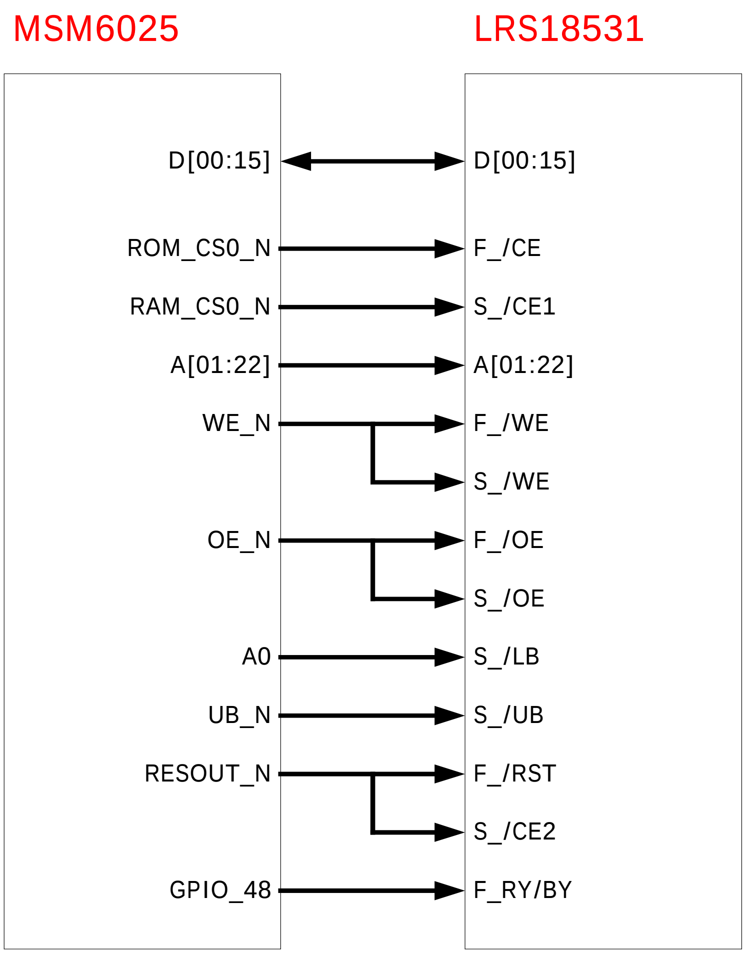

FIG.4-1 MSM TO MEMORY PIN MAP BLOCK DIAGRAM

4.1.1 Memory Block

1. Silicon 7 SV6C2832UTA
2. 128Mbits Flash + 32Mbits SRAM

4.1.2 ROM_CS0

1. Size : 16Mbyte, 1chip, 6banks
2. ROM_CS0_N (16Mbyte)

4.1.3 RAM_CS0

1. Size : 4Mbyte
2. RAM_CS0_N (4Mbyte)

4.2 LCD Module

1. LCD: 128X128 dot (CSTN, 65K, 8bits data bus)
2. Driver: SSD1779
3. MWEN, MREN, MCS are ACTIVE LOW signals.
4. MINT is the interrupt request signal from MV3018SOK to MSM6025.
5. AAT3113 is the CLOCK for GPIO49 which controls the brightness.[32 steps]

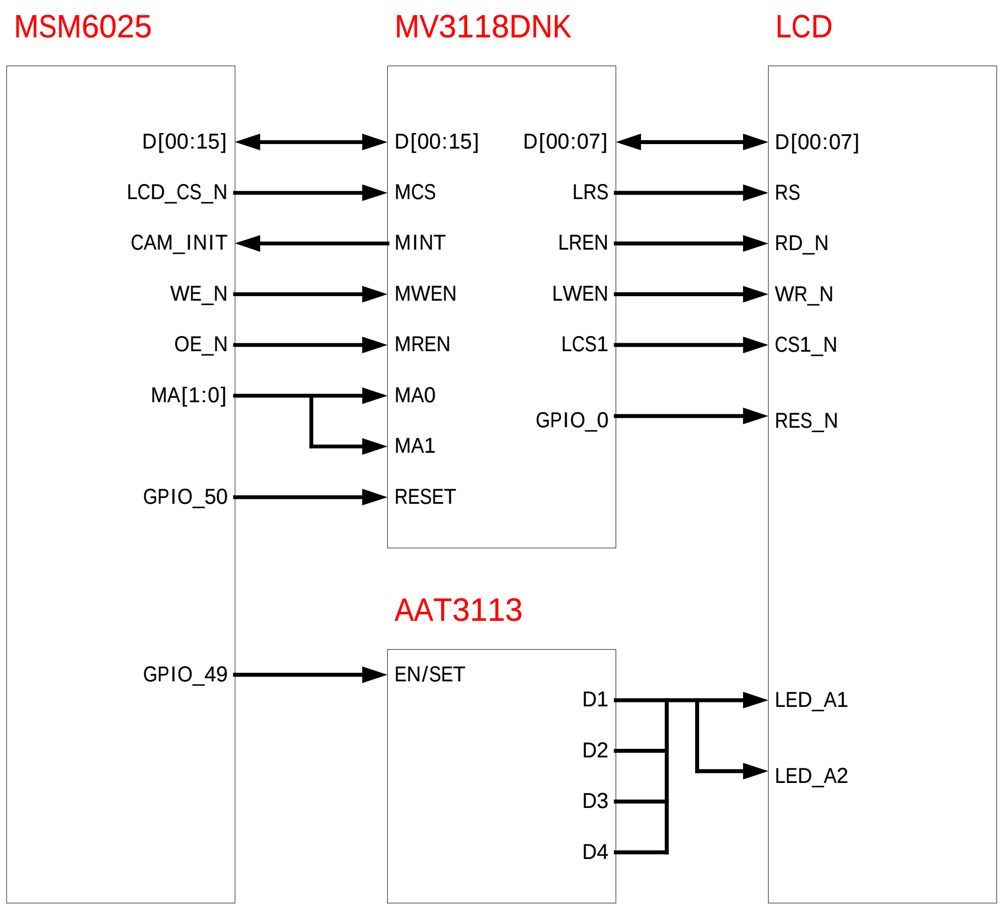

FIG.4-3 LCD BLOCK DIAGRAM

4.3 CAMERA

1. Camera Sensor 300K : HV7131RP-FB-SD74
2. VSYNC is the synchronous signal to differentiate the Frame and HREF is the synchronous signal to differentiate the Line. These signals are synchronous with Pixel Clock.
3. SDA and SCL signals are used as Data and Clock for I2C communication.

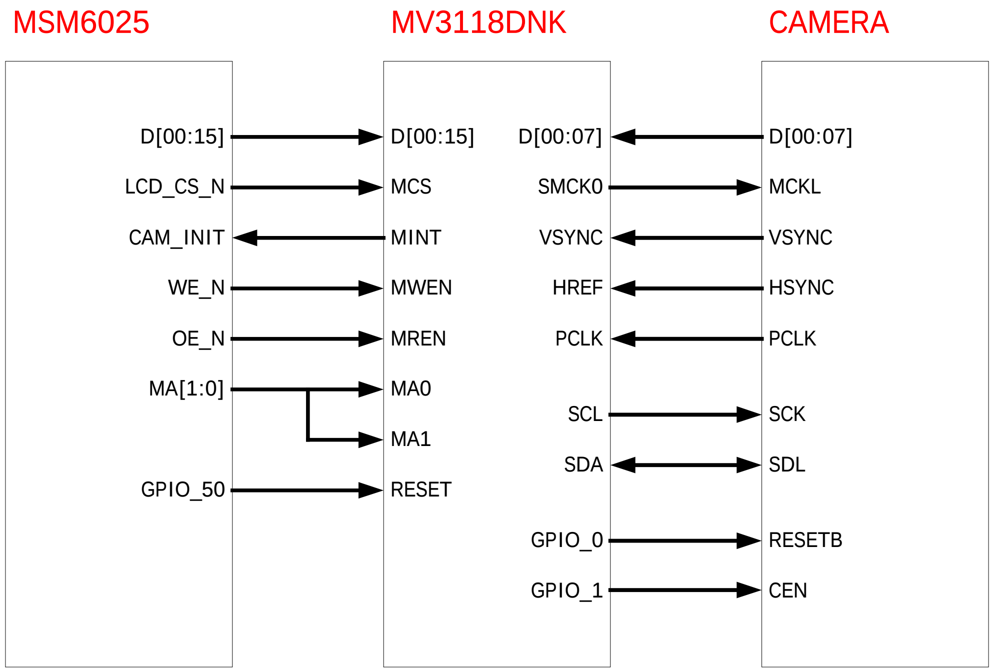

FIG.4-4 CAMERA BLOCK DIAGRAM

4.4 USB

1. S1M8720X USB Transceiver converts single-ended or different logic signals into USB signals, and converts USB signals into single-ended or different logic signals.
2. S1M8720X operates in Low speed(1.5Mbps) and Full speed(12Mbps).
   [Circuit is set to Full speed]
3. SUS is used to save power. If SUS=L then the Differential Receiver is enabled and if SUS=H then the Differential Receiver is turned off and reduces power usage.

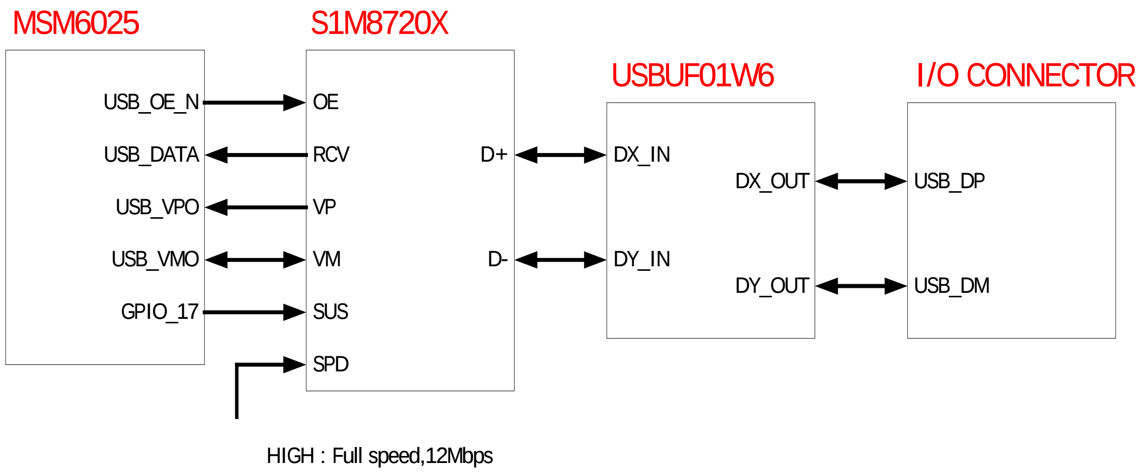

FIG.4-5 USB BLOCK DIAGRAM

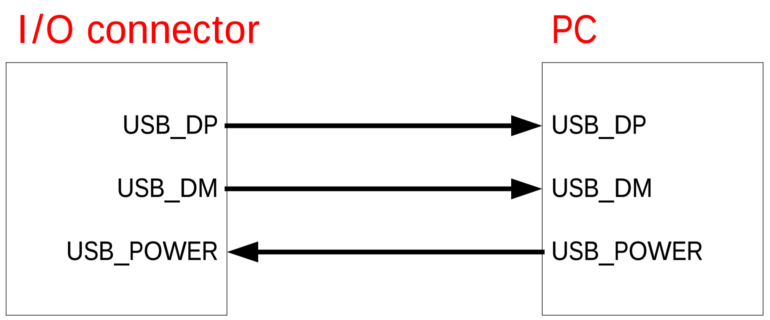

FIG.4-6 USB DATA CABLE PIN MAP

4.5 UART

MSM6025 includes UART1, UART2, UART3 but only UART1 is used currently for DM. UART is a port to communicate between a PC and a Phone via Serial.

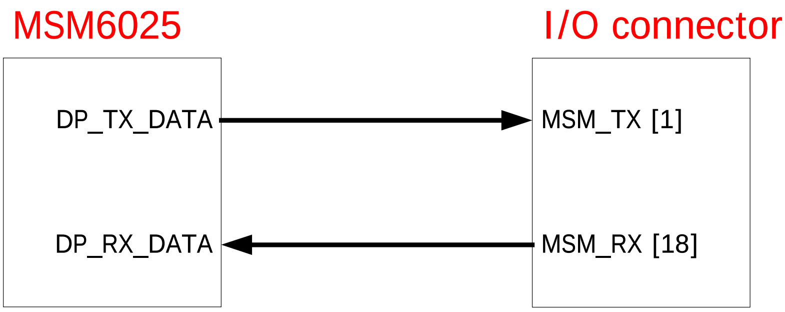

FIG.4-7 UART BLOCK DIAGRAM

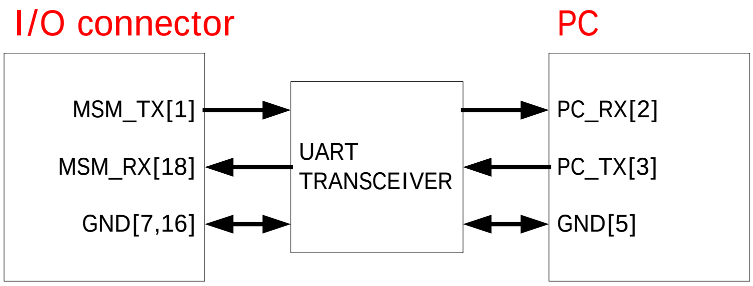

FIG.4-8 UART DATA CABLE PIN MAP

4.6 JTAG

Used for testing and debugging.

The 470pF capacitor is removed form JTAG signal line because of delay time.

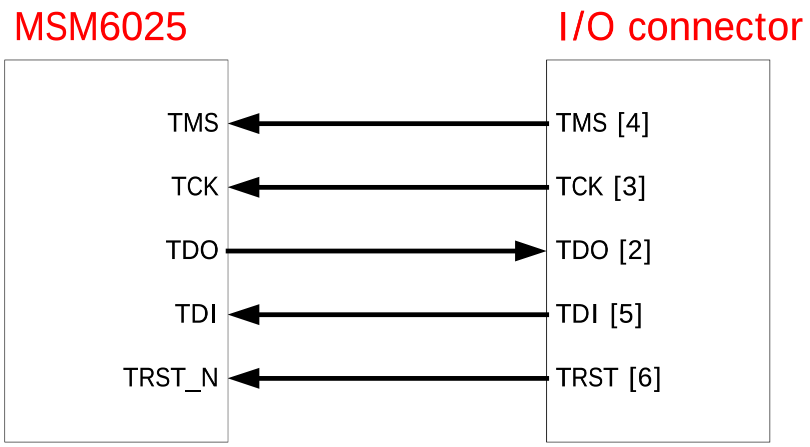

FIG.4-9 JTAG BLOCK DIAGRAM

4.7 SOUND

A. DG3535(Analog Switch); When EAR_PATH(GPIO_18) signal is active low, voice signal comes out through EAR_SOUND else if it's active high then voice signal comes out through CAR_EAR_SOUND.

B. LM4898(Audio Amp) is used to amplify the CMX(Bell). GPIO_42 pin is used to control Shutdown control.

C. EAR_SOUND needs to support CMX and Voice. Because of this, MSM audio Codec (EAR_AMP_SEL Register) divides the sound and does the output.

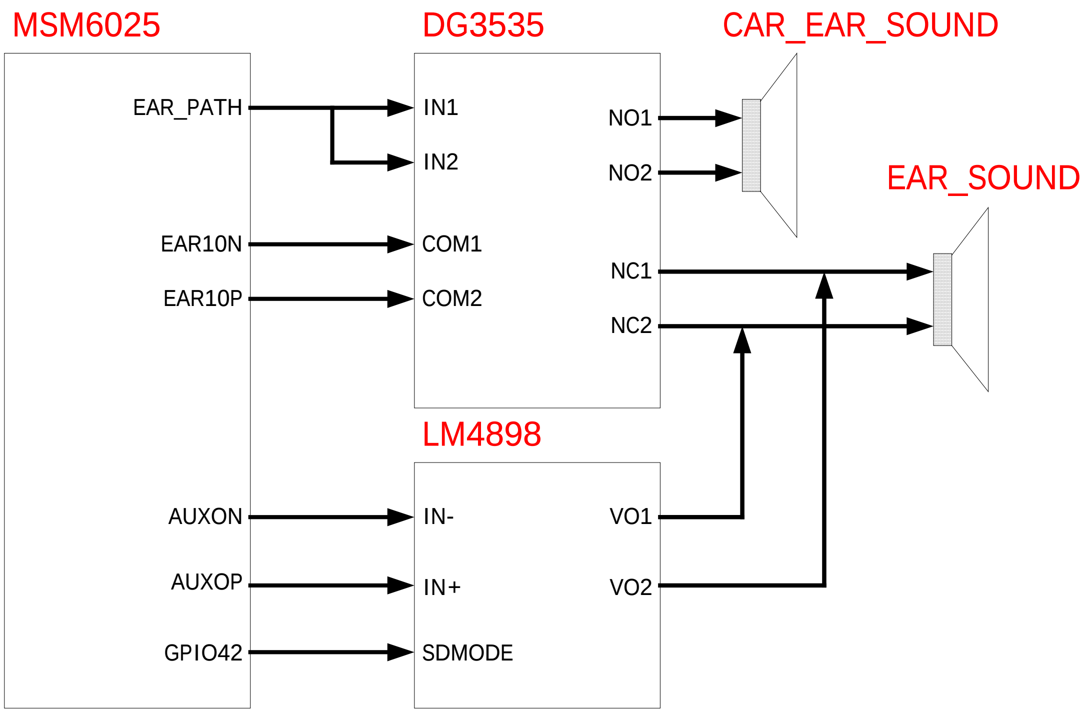

FIG.4-10 SOUND PATH BLOCK DIAGRAM

4.8 USER INTERFACE

4.8.1 Keypad Interface

A. KEYSEN_N is internally Pulled up.

B. SCAN 1, 2, 3, 4, 5 drops to LOW and then raises back to HIGH every 25 msec.

When KEY is pressed KEYSEN_N is changed to LOW and location of the KEY is available.

Result => Eliminate Keypad Varistor or change the value

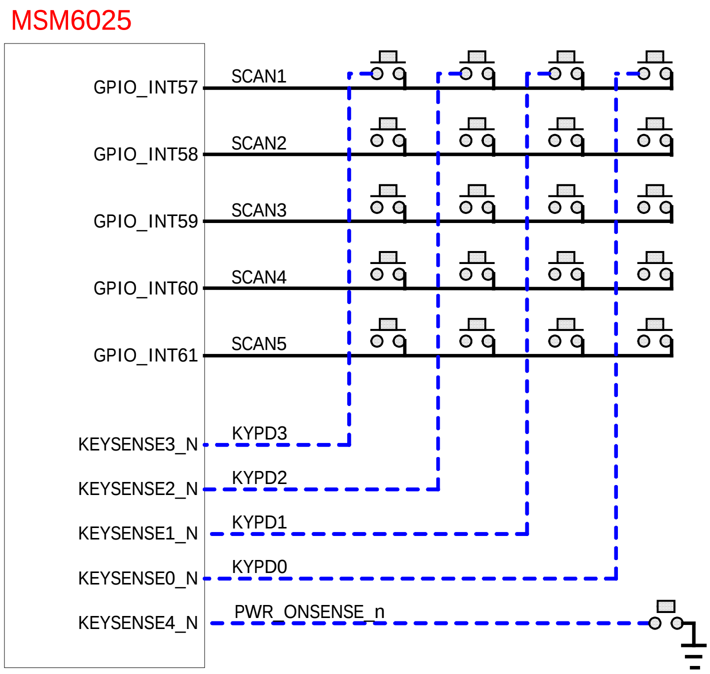

FIG.4-11 KEYPAD BLOCK DIAGRAM

*	0	#	CLR
7	8	9	MENU
4	5	6	SEND
1	2	3	OK
UP	DOWN	LEFT	RIGHT

FIG.4-12 KEYPAD MAP

4.8.3 Motor

Circuit 1: If PM6610 KPD_DRV_N is HIGH then the motor activates.

Circuit 2: By using MSM6025 GPIO_44 LDO is ON and activates motor.

This will be settled after testing circuit 1 and 2.

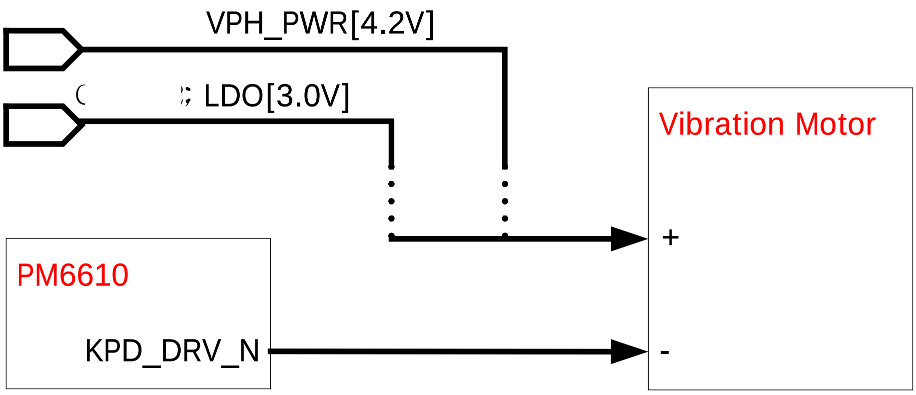

FIG.4-13 VIBRATION MOTOR BLOCK DIAGRAM

4.8.3 LED

If MSM6025 GPIO_7 is HIGH then the LED turns on.

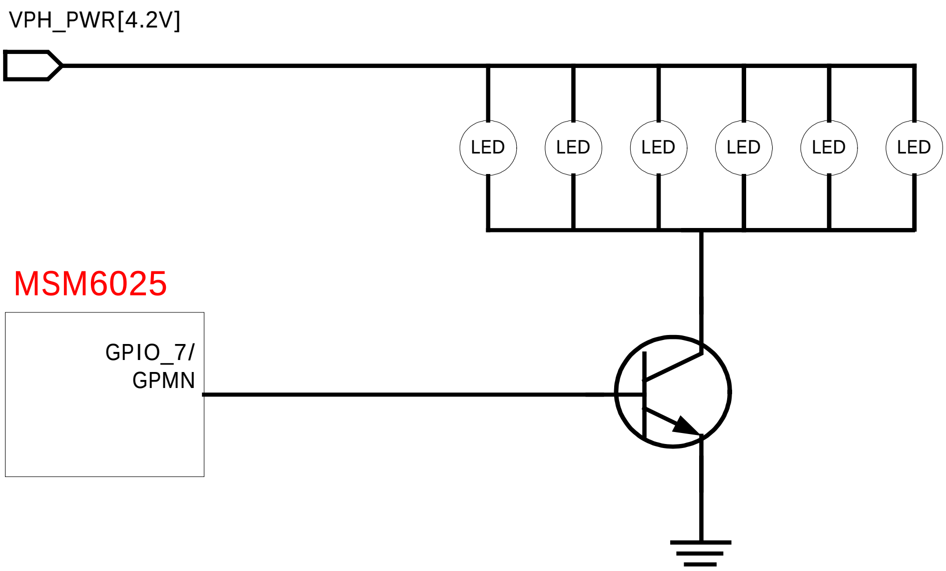

FIG.4-14 LED BLOCK DIAGRAM