

532 SCHEMATICS

REV.: B.0

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DATE	9/27/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27

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DATE	9/27	9/27	9/27	9/27	9/27	9/27	9/27	9/27

P/N : 15-F56-010020

PCB M/B.532.V.B.318*173.8*1.6mm.6L YELLO



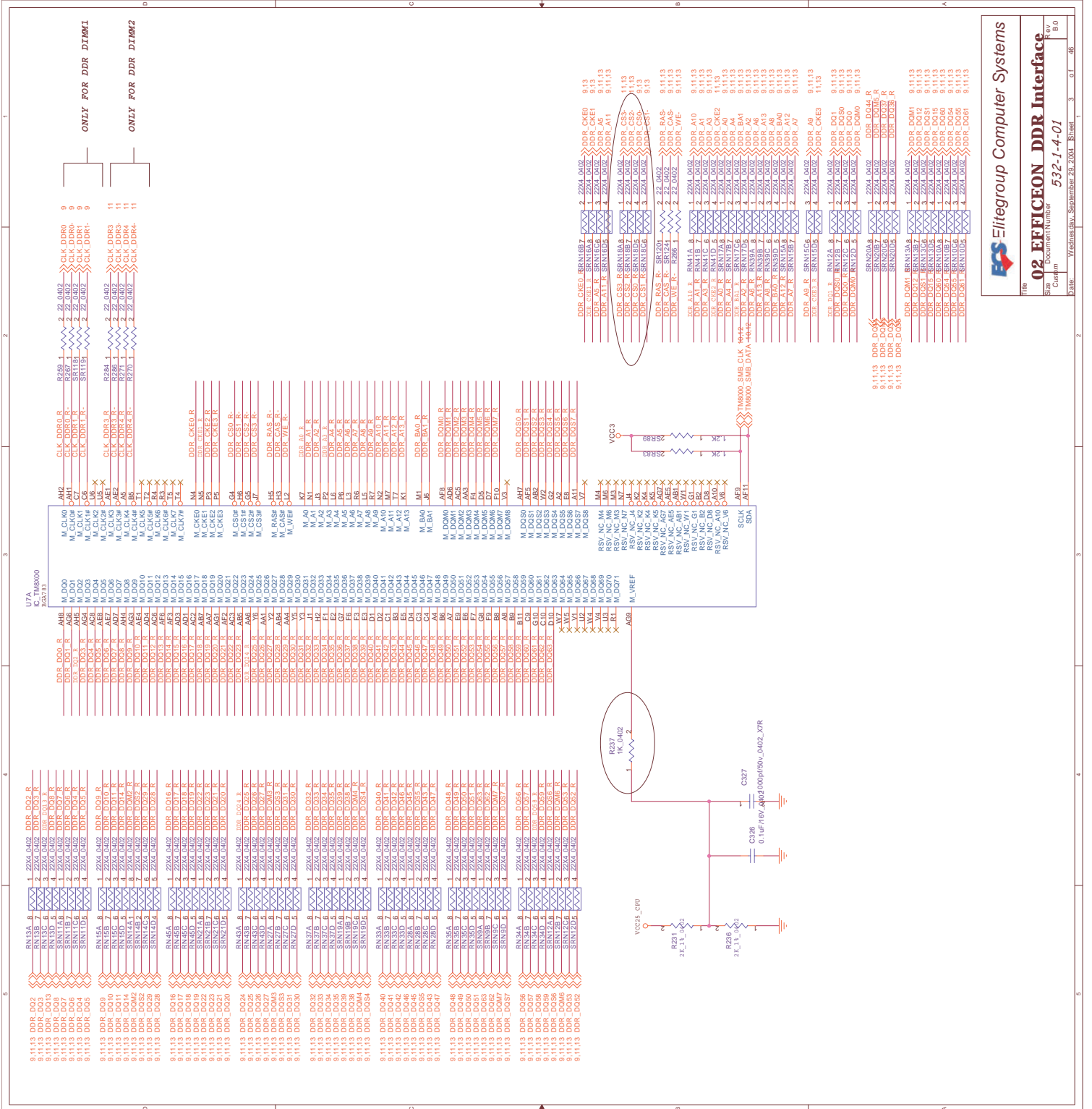
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REVISION HISTORY

A.0 INITIAL RELEASE



REVISION HISTORY			
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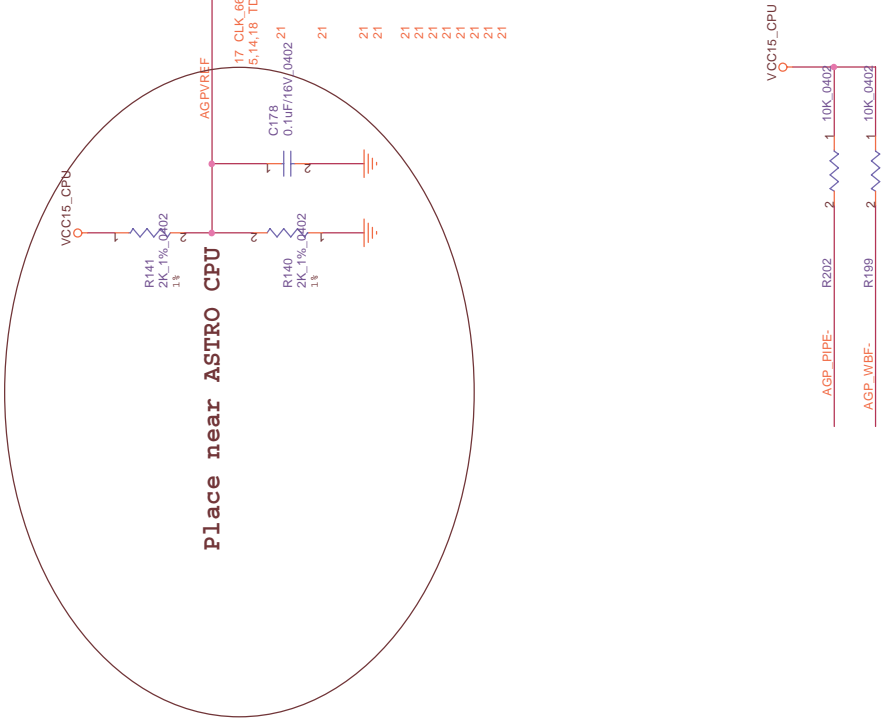


ONLY FOR DDR DTMM1

ONLY FOR DDR DTMM2

02 EFFICEON DDR Interface

 Document Number: 532-I-4-01



U7B
IC: TM6X00
862A793

A_A2B	A_VREF	A_PIPE#	A_PIPE#	A_FRAME#	AB18	AGP_FRAME- 21
AB14	A_CLK	AGP_PIPE-	AG17	A_IRDY#	AG25	AGP_IRDY- 21
AD16	A_RST#	AGP_WBF-	AE17	A_TRDY#	AH26	AGP_TRDY- 21
AE15	A_REQ#	AGP_PIPE-	AG17	A_STOP#	AG26	AGP_STOP- 21
AG17	A_REQ#	AGP_WBF-	AH17	A_DEVSEL#	AE24	AGP_DEVSEL- 21
AG17	A_PIPE#	AGP_PIPE-	AG17	A_GNT#	AG16	AGP_GNT- 21
AG17	A_PIPE#	AGP_WBF-	AH17	A_S10	AE16	AGP_S10 21
AH17	A_RBF#	AGP_WBF-	AH17	A_S11	AH17	AGP_S11 21
AH17	A_WBF#	AGP_WBF-	AE18	A_S12	AE18	AGP_S12 21
AH17	A_WBF#	AGP_WBF-	AE18	A_ADSTB0	AB23	AGP_ADSTB0 21
AH17	A_WBF#	AGP_WBF-	AB24	A_ADSTB0#	AB24	AGP_ADSTB0- 21
AH17	A_WBF#	AGP_WBF-	AE21	A_ADSTB1	AE21	AGP_ADSTB1 21
AH17	A_WBF#	AGP_WBF-	AE21	A_ADSTB1#	AE21	AGP_ADSTB1- 21
AH17	A_WBF#	AGP_WBF-	AC24	A_CBE0#	AC24	AGP_CBE0- 21
AH17	A_WBF#	AGP_WBF-	AE25	A_CBE1#	AE25	AGP_CBE1- 21
AH17	A_WBF#	AGP_WBF-	AE25	A_CBE2#	AE25	AGP_CBE2- 21
AH17	A_WBF#	AGP_WBF-	AG22	A_CBE3#	AG22	AGP_CBE3- 21
AH17	A_WBF#	AGP_WBF-	AC28	A_AD0	AC28	AGP_AD0 21
AH17	A_WBF#	AGP_WBF-	AD27	A_AD1	AD27	AGP_AD1 21
AH17	A_WBF#	AGP_WBF-	AD28	A_AD2	AD28	AGP_AD2 21
AH17	A_WBF#	AGP_WBF-	AD28	A_AD3	AD28	AGP_AD3 21
AH17	A_WBF#	AGP_WBF-	AD28	A_AD4	AD28	AGP_AD4 21
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AH17	A_WBF#	AGP_WBF-	AD28	A_AD30	AD28	AGP_AD30 21
AH17	A_WBF#	AGP_WBF-	AD28	A_AD31	AD28	AGP_AD31 21
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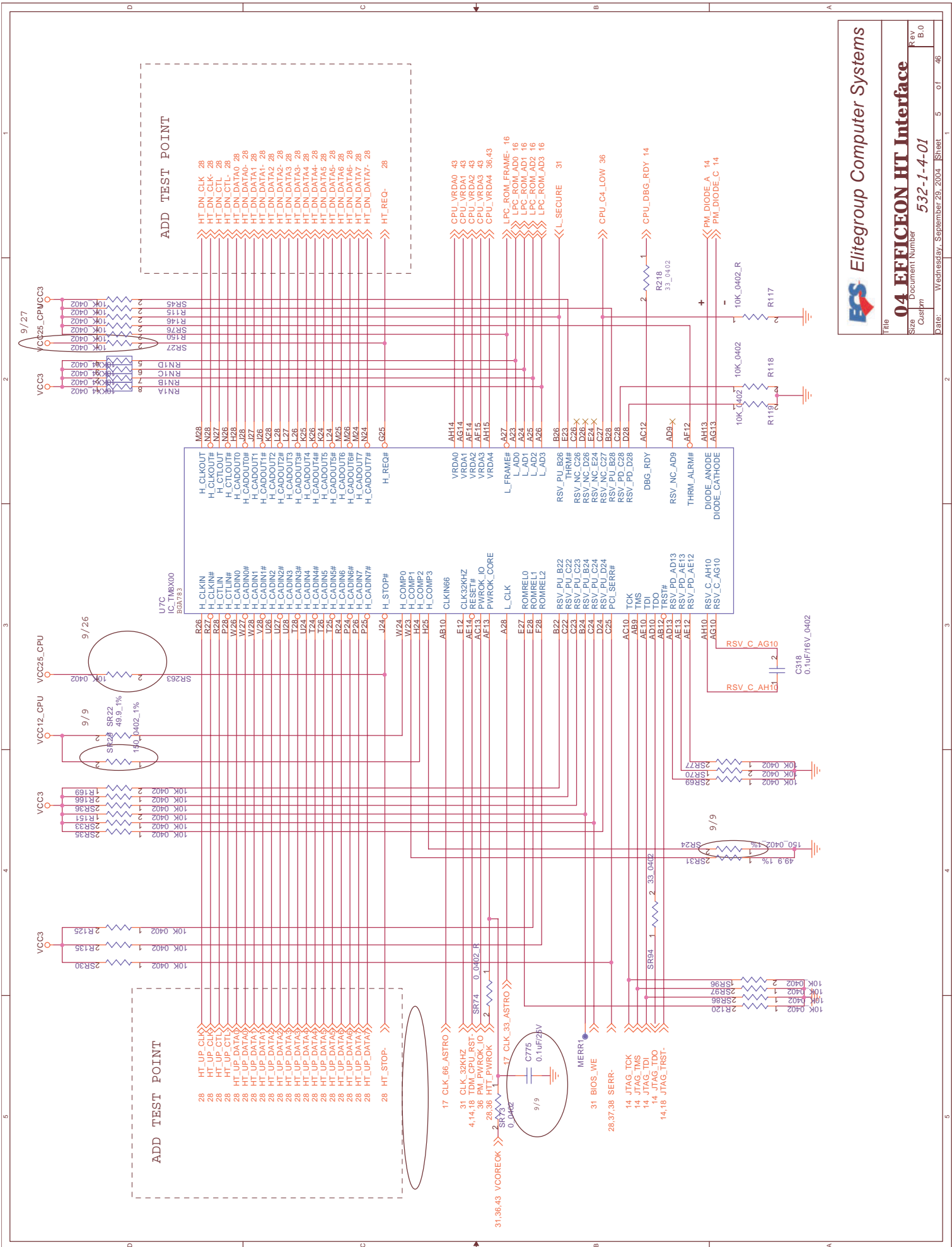
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Size: **532-1-4-01**

Rev: B.0

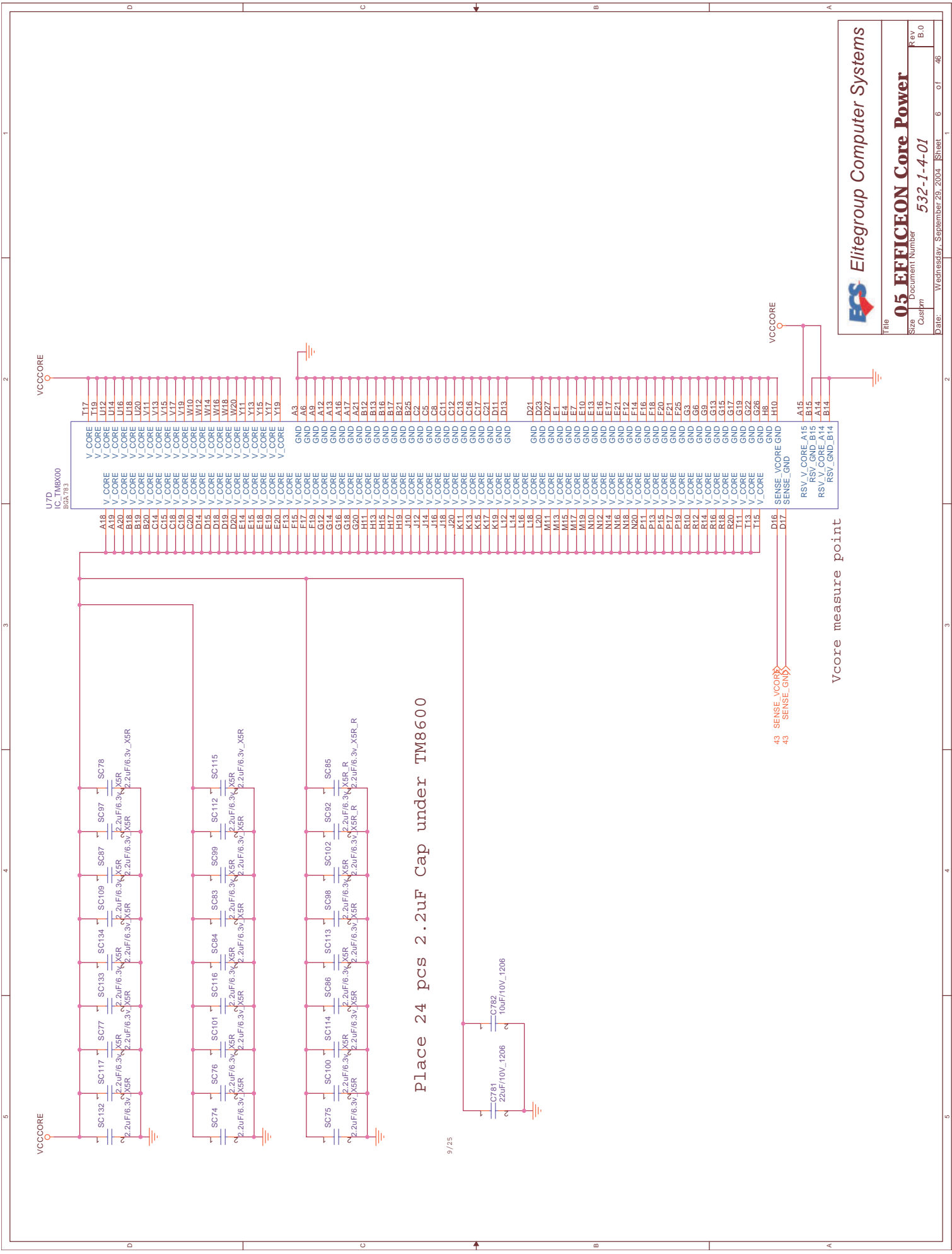
Customer: _____

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ADD TEST POINT

ADD TEST POINT



Place 24 pcs 2.2uF Cap under TM8600

9/25

43 SENSE_VCCORE
43 SENSE_GND

Vccore measure point

U7D
C: TM8600
Rev: 1.0

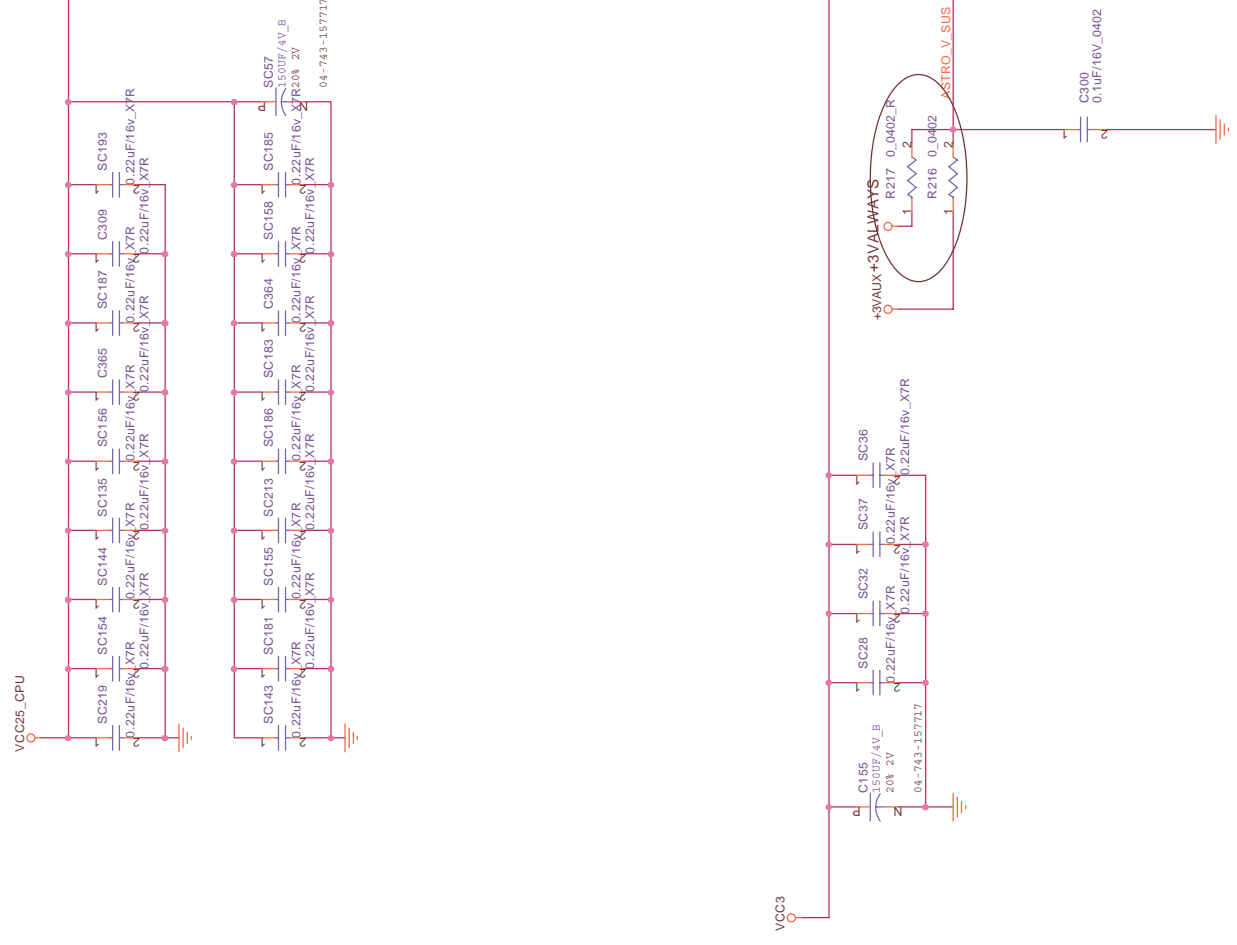
A18	V_CORE	T17	V_CORE
A19	V_CORE	U12	V_CORE
A20	V_CORE	U14	V_CORE
B18	V_CORE	U16	V_CORE
B19	V_CORE	U20	V_CORE
B20	V_CORE	U14	V_CORE
C14	V_CORE	V13	V_CORE
C15	V_CORE	V15	V_CORE
C18	V_CORE	V17	V_CORE
C19	V_CORE	V19	V_CORE
C20	V_CORE	W10	V_CORE
D14	V_CORE	W12	V_CORE
D15	V_CORE	W14	V_CORE
D18	V_CORE	W18	V_CORE
D20	V_CORE	W20	V_CORE
E14	V_CORE	Y11	V_CORE
E15	V_CORE	Y13	V_CORE
E18	V_CORE	Y15	V_CORE
E19	V_CORE	Y17	V_CORE
E20	V_CORE	Y19	V_CORE
F15	V_CORE	A3	GND
F17	V_CORE	A8	GND
F19	V_CORE	A9	GND
G12	V_CORE	A12	GND
G14	V_CORE	A13	GND
G18	V_CORE	A16	GND
G20	V_CORE	A27	GND
H11	V_CORE	B12	GND
H13	V_CORE	B13	GND
H15	V_CORE	B16	GND
H17	V_CORE	B17	GND
H19	V_CORE	B21	GND
J10	V_CORE	B25	GND
J14	V_CORE	C5	GND
J16	V_CORE	C8	GND
J18	V_CORE	C11	GND
J20	V_CORE	C12	GND
K11	V_CORE	C13	GND
K13	V_CORE	C16	GND
K15	V_CORE	C17	GND
K19	V_CORE	D11	GND
L12	V_CORE	D13	GND
L14	V_CORE	D21	GND
L16	V_CORE	D23	GND
L18	V_CORE	D27	GND
L20	V_CORE	E4	GND
M11	V_CORE	E7	GND
M13	V_CORE	E10	GND
M17	V_CORE	E13	GND
M19	V_CORE	E16	GND
N12	V_CORE	E17	GND
N14	V_CORE	E20	GND
N16	V_CORE	E25	GND
N18	V_CORE	F8	GND
N20	V_CORE	F18	GND
P11	V_CORE	F19	GND
P13	V_CORE	F25	GND
P15	V_CORE	G8	GND
P19	V_CORE	G9	GND
R10	V_CORE	G13	GND
R14	V_CORE	G15	GND
R16	V_CORE	G17	GND
R18	V_CORE	G19	GND
R20	V_CORE	G22	GND
T11	V_CORE	H8	GND
T13	V_CORE	H10	GND
T18	V_CORE	H11	GND
D16	SENSE_VCCORE	A15	RSV_V_CORE_A15
D17	SENSE_GND	B15	RSV_GND_B15
		A14	RSV_V_CORE_A14
		B14	RSV_GND_B14

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Title: **05 EFFICEON Core Power**
 Size: **532-1-4-01**
 Cust: **532-1-4-01**
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U7E
IC: TM6X00
BGA1781

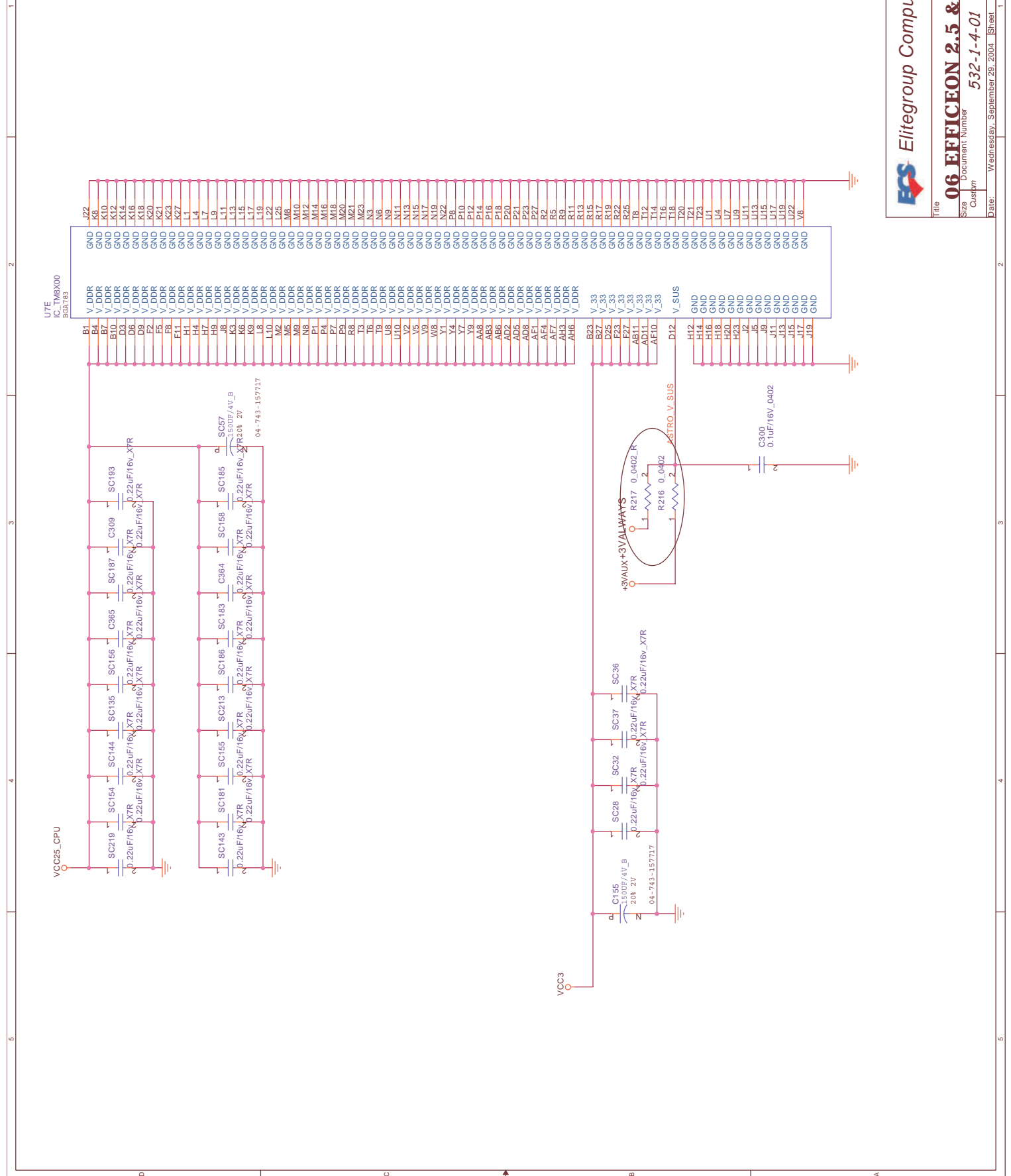


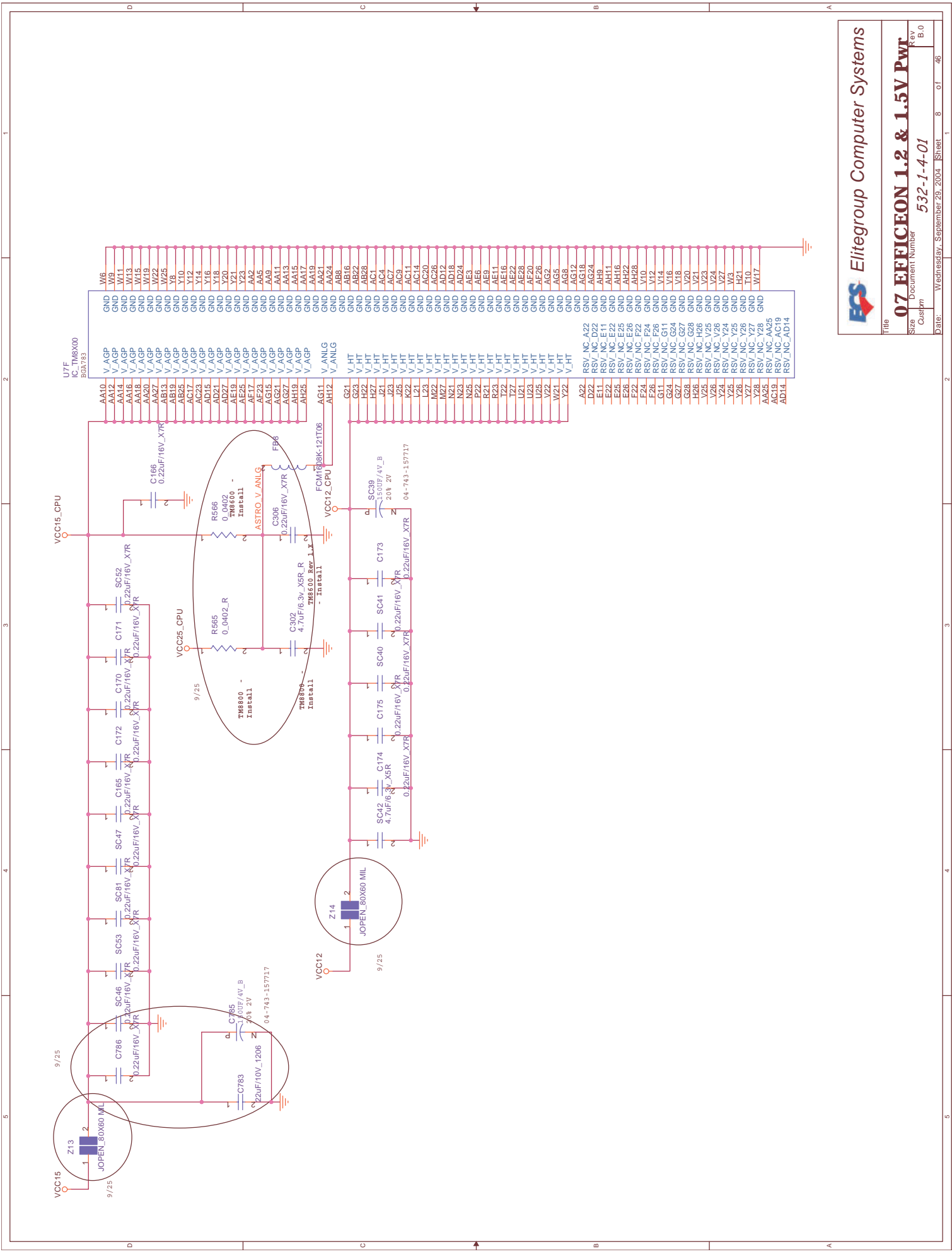
B2	V_DDR
K9	GND
K10	GND
K12	V_DDR
K14	V_DDR
K16	V_DDR
K18	V_DDR
K20	V_DDR
K22	V_DDR
K23	V_DDR
K27	GND
L1	GND
L4	GND
L7	GND
L9	V_DDR
L11	V_DDR
L13	V_DDR
L15	V_DDR
L17	V_DDR
L19	V_DDR
L22	GND
L25	GND
M8	V_DDR
M10	V_DDR
M12	V_DDR
M14	GND
M16	V_DDR
M18	V_DDR
M20	GND
M21	GND
M23	V_DDR
M6	V_DDR
N8	V_DDR
N9	V_DDR
N11	GND
N13	GND
N15	V_DDR
N17	V_DDR
N19	V_DDR
P22	GND
P8	V_DDR
P10	GND
P12	GND
P14	V_DDR
P16	V_DDR
P18	GND
P20	V_DDR
P22	V_DDR
P23	GND
P27	GND
R2	GND
R5	GND
R9	V_DDR
R11	GND
R13	V_DDR
R17	V_DDR
R19	V_33
R22	V_33
R25	GND
T8	GND
T12	GND
T14	V_33
T18	GND
T20	GND
T21	GND
T23	GND
U1	GND
U4	GND
U9	GND
U11	GND
U13	GND
U15	GND
U17	GND
U19	GND
U22	GND
V8	GND

Elitegroup Computer Systems

Title
06 EFFICEON 2.5 & 3.3V Pwr
Document Number
532-1-4-01
Rev
B.0

Size
CustPm
Date:
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VCC_DIMM

CM114A
200_SODIMM_DDR
GSI_CA0115-200N01_DDR52_S

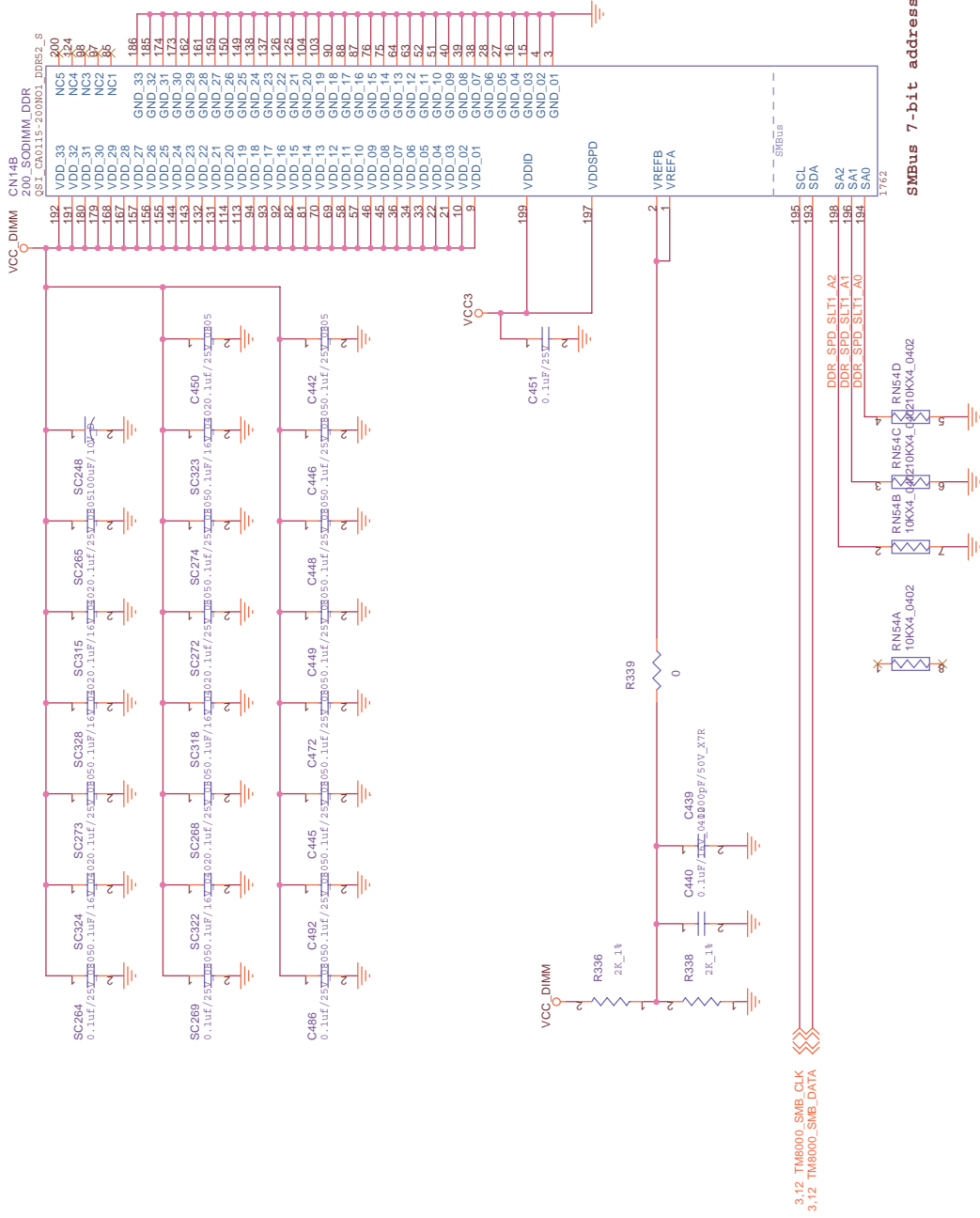
3	3,11,13	3	CLK_DDR0	180	CK1	DQ_58	187	DDR_D058	3,11,13
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3	3,11,13	3	CLK_DDR2	35	CK0	DQ_56	176	DDR_D056	3,11,13
3,13	3,11,13	3,13	DDR_CKE0	95	CKE0#	DQ_53	166	DDR_D053	3,11,13
3,13	3,11,13	3,13	DDR_CKE1	96	CKE1	DQ_52	164	DDR_D052	3,11,13
3,11,13	3,11,13	3,11,13	DDR_A10	123	A_13	DQ_50	171	DDR_D050	3,11,13
3,11,13	3,11,13	3,11,13	DDR_A11	99	A_12	DQ_49	164	DDR_D049	3,11,13
3,11,13	3,11,13	3,11,13	DDR_A12	100	A_11	DQ_48	163	DDR_D048	3,11,13
3,11,13	3,11,13	3,11,13	DDR_A13	115	A_10	DQ_47	154	DDR_D047	3,11,13
3,11,13	3,11,13	3,11,13	DDR_A14	101	A_09	DQ_46	152	DDR_D046	3,11,13
3,11,13	3,11,13	3,11,13	DDR_A15	102	A_08	DQ_45	146	DDR_D045	3,11,13
3,11,13	3,11,13	3,11,13	DDR_A16	105	A_07	DQ_44	142	DDR_D044	3,11,13
3,11,13	3,11,13	3,11,13	DDR_A17	106	A_06	DQ_43	153	DDR_D043	3,11,13
3,11,13	3,11,13	3,11,13	DDR_A18	109	A_05	DQ_42	145	DDR_D042	3,11,13
3,11,13	3,11,13	3,11,13	DDR_A19	108	A_04	DQ_41	141	DDR_D041	3,11,13
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3,11,13	3,11,13	3,11,13	DDR_A21	111	A_02	DQ_38	136	DDR_D038	3,11,13
3,11,13	3,11,13	3,11,13	DDR_A22	112	A_01	DQ_37	130	DDR_D037	3,11,13
3,11,13	3,11,13	3,11,13	DDR_BA0	116	BA1	DQ_36	128	DDR_D036	3,11,13
3,11,13	3,11,13	3,11,13	DDR_BA1	117	BA0	DQ_35	138	DDR_D035	3,11,13
3,13	3,13	3,13	DDR_CS0	122	S#	DQ_34	129	DDR_D034	3,11,13
3,13	3,13	3,13	DDR_CS1	121	S#	DQ_33	127	DDR_D033	3,11,13
3,11,13	3,11,13	3,11,13	DDR_RAS#	118	RAS#	DQ_31	68	DDR_D031	3,11,13
3,11,13	3,11,13	3,11,13	DDR_CAS#	119	CAS#	DQ_30	66	DDR_D030	3,11,13
3,11,13	3,11,13	3,11,13	DDR_WE#	120	WE#	DQ_29	60	DDR_D029	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DM0	184	DM_7	DQ_28	67	DDR_D028	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DM1	170	DM_6	DQ_27	65	DDR_D027	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DM2	148	DM_5	DQ_26	59	DDR_D026	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DM3	134	DM_4	DQ_24	54	DDR_D024	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DM4	62	DM_3	DQ_23	50	DDR_D023	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DM5	28	DM_2	DQ_22	44	DDR_D022	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DM6	26	DM_1	DQ_21	44	DDR_D021	3,11,13
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3,11,13	3,11,13	3,11,13	DDR_DQ0	183	DQS_7	DQ_19	49	DDR_D019	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DQ1	169	DQS_6	DQ_18	43	DDR_D018	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DQ2	147	DQS_5	DQ_16	41	DDR_D016	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DQ3	83	DQS_4	DQ_15	32	DDR_D015	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DQ4	63	DQS_3	DQ_14	30	DDR_D014	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DQ5	47	DQS_2	DQ_13	20	DDR_D013	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DQ6	25	DQS_1	DQ_12	31	DDR_D012	3,11,13
3,11,13	3,11,13	3,11,13	DDR_DQ7	11	DQS_0	DQ_11	29	DDR_D011	3,11,13
						DQ_09	23	DDR_D09	3,11,13
						DQ_08	19	DDR_D08	3,11,13
						DQ_07	18	DDR_D07	3,11,13
						DQ_06	14	DDR_D06	3,11,13
						DQ_05	6	DDR_D05	3,11,13
						DQ_04	17	DDR_D04	3,11,13
						DQ_03	13	DDR_D03	3,11,13
						DQ_02	7	DDR_D02	3,11,13
						DQ_01	7	DDR_D01	3,11,13
						DQ_00	5	DDR_D00	3,11,13

84	CBQ7	
80	CBQ6	
74	CBQ5	
72	CBQ4	
63	CBQ3	
59	CBQ2	
57	CBQ1	
56	CBQ0	



08 DDR SO-DIMM 1 (1/2)
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SMBus 7-bit address 1010 000

3,12 TM8000_SMB_CLK
3,12 TM8000_SMB_DATA

Title
09 DDR SO-DIMM 1 (2/2)
 Size Document Number
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VCC_DIMM

SCNEA
200_SODIMM_DDR
GSI_CA0115-200N01_DDR52_R

86	RESET#	DO_E3	190	DDR_D063	3,9,13
87	CK2	DO_E4	188	DDR_D062	3,9,13
88	CK2#	DO_E5	187	DDR_D061	3,9,13
89	CK1	DO_E6	186	DDR_D060	3,9,13
90	CK1#	DO_E7	185	DDR_D059	3,9,13
91	CK0	DO_E8	184	DDR_D058	3,9,13
92	CK0#	DO_E9	183	DDR_D057	3,9,13
93	CKE0	DO_EA	182	DDR_D056	3,9,13
94	CKE1	DO_EB	181	DDR_D055	3,9,13
95	CKE2	DO_EC	180	DDR_D054	3,9,13
96	CKE3	DO_ED	179	DDR_D053	3,9,13
97	CKE4	DO_EE	178	DDR_D052	3,9,13
98	CKE5	DO_EF	177	DDR_D051	3,9,13
99	A_13	DO_F0	176	DDR_D050	3,9,13
100	A_12	DO_F1	175	DDR_D049	3,9,13
101	A_11	DO_F2	174	DDR_D048	3,9,13
102	A_10	DO_F3	173	DDR_D047	3,9,13
103	A_09	DO_F4	172	DDR_D046	3,9,13
104	A_08	DO_F5	171	DDR_D045	3,9,13
105	A_07	DO_F6	170	DDR_D044	3,9,13
106	A_06	DO_F7	169	DDR_D043	3,9,13
107	A_05	DO_F8	168	DDR_D042	3,9,13
108	A_04	DO_F9	167	DDR_D041	3,9,13
109	A_03	DO_FA	166	DDR_D040	3,9,13
110	A_02	DO_FB	165	DDR_D039	3,9,13
111	A_01	DO_FC	164	DDR_D038	3,9,13
112	A_00	DO_FD	163	DDR_D037	3,9,13
116	BA1	DO_FE	162	DDR_D036	3,9,13
117	BA0	DO_FF	161	DDR_D035	3,9,13
122	S1#	DO_00	160	DDR_D034	3,9,13
121	S0#	DO_01	159	DDR_D033	3,9,13
118	RAS#	DO_02	158	DDR_D032	3,9,13
119	CAS#	DO_03	157	DDR_D031	3,9,13
120	WE#	DO_04	156	DDR_D030	3,9,13
184	DM_7	DO_05	155	DDR_D029	3,9,13
170	DM_6	DO_06	154	DDR_D028	3,9,13
148	DM_5	DO_07	153	DDR_D027	3,9,13
134	DM_4	DO_08	152	DDR_D026	3,9,13
62	DM_3	DO_09	151	DDR_D025	3,9,13
26	DM_2	DO_10	150	DDR_D024	3,9,13
12	DM_1	DO_11	149	DDR_D023	3,9,13
12	DM_0	DO_12	148	DDR_D022	3,9,13
183	DQS_7	DO_13	147	DDR_D021	3,9,13
169	DQS_6	DO_14	146	DDR_D020	3,9,13
147	DQS_5	DO_15	145	DDR_D019	3,9,13
83	DQS_4	DO_16	144	DDR_D018	3,9,13
67	DQS_3	DO_17	143	DDR_D017	3,9,13
47	DQS_2	DO_18	142	DDR_D016	3,9,13
25	DQS_1	DO_19	141	DDR_D015	3,9,13
11	DQS_0	DO_20	140	DDR_D014	3,9,13
84	CBDM	DO_21	139	DDR_D013	3,9,13
80	CBOS	DO_22	138	DDR_D012	3,9,13
74	CBOS	DO_23	137	DDR_D011	3,9,13
72	CBOS	DO_24	136	DDR_D010	3,9,13
63	CBOS	DO_25	135	DDR_D009	3,9,13
59	CBOS	DO_26	134	DDR_D008	3,9,13
55	CBOS	DO_27	133	DDR_D007	3,9,13
51	CBOS	DO_28	132	DDR_D006	3,9,13
47	CBOS	DO_29	131	DDR_D005	3,9,13
43	CBOS	DO_30	130	DDR_D004	3,9,13
39	CBOS	DO_31	129	DDR_D003	3,9,13
35	CBOS	DO_32	128	DDR_D002	3,9,13
31	CBOS	DO_33	127	DDR_D001	3,9,13
27	CBOS	DO_34	126	DDR_D000	3,9,13
23	CBOS	DO_35	125	DDR_D000	3,9,13
19	CBOS	DO_36	124	DDR_D000	3,9,13
15	CBOS	DO_37	123	DDR_D000	3,9,13
11	CBOS	DO_38	122	DDR_D000	3,9,13
7	CBOS	DO_39	121	DDR_D000	3,9,13
3	CBOS	DO_40	120	DDR_D000	3,9,13

84	CBDM
80	CBOS
74	CBOS
72	CBOS
63	CBOS
59	CBOS
55	CBOS
51	CBOS
47	CBOS
43	CBOS
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35	CBOS
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27	CBOS
23	CBOS
19	CBOS
15	CBOS
11	CBOS



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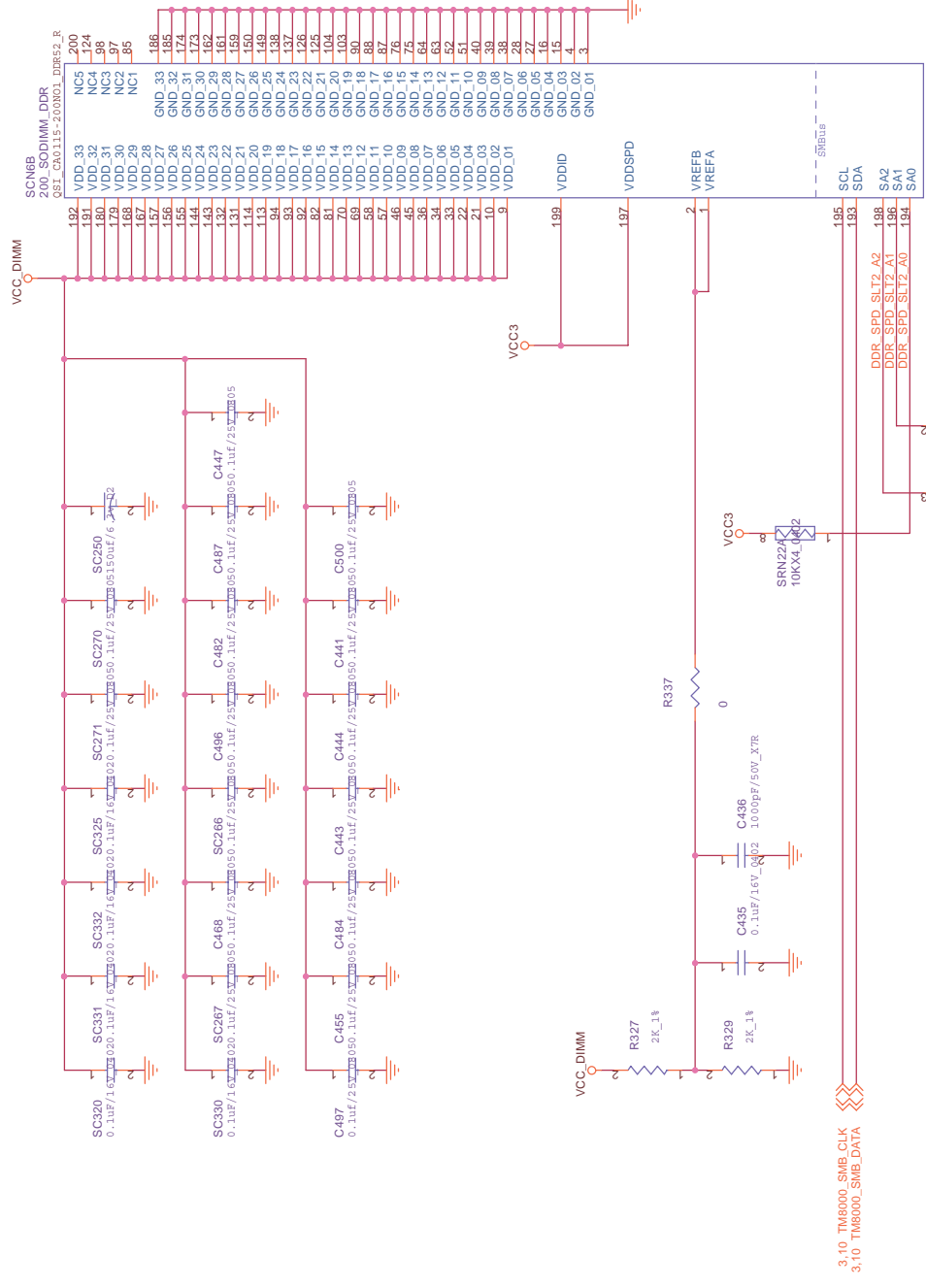
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Size: Document Number **532-1-4-01**

Customer: **532-1-4-01**

Date: Wednesday, September 29, 2004 Sheet 11 of 46

Rev: B.0



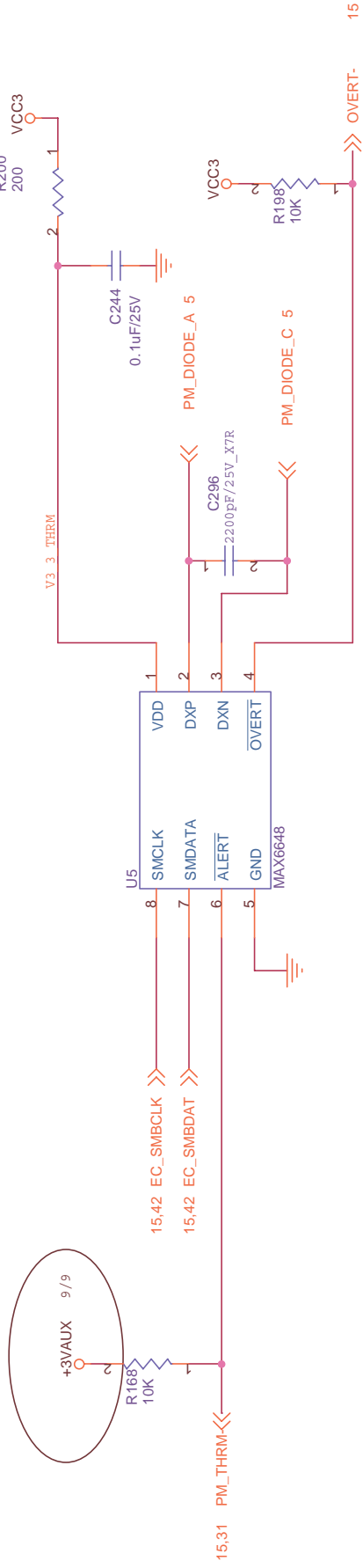
SMBus 7-bit address 1010 001

3.10 TM6000 SMB_CLK
3.10 TM6000 SMB_DATA

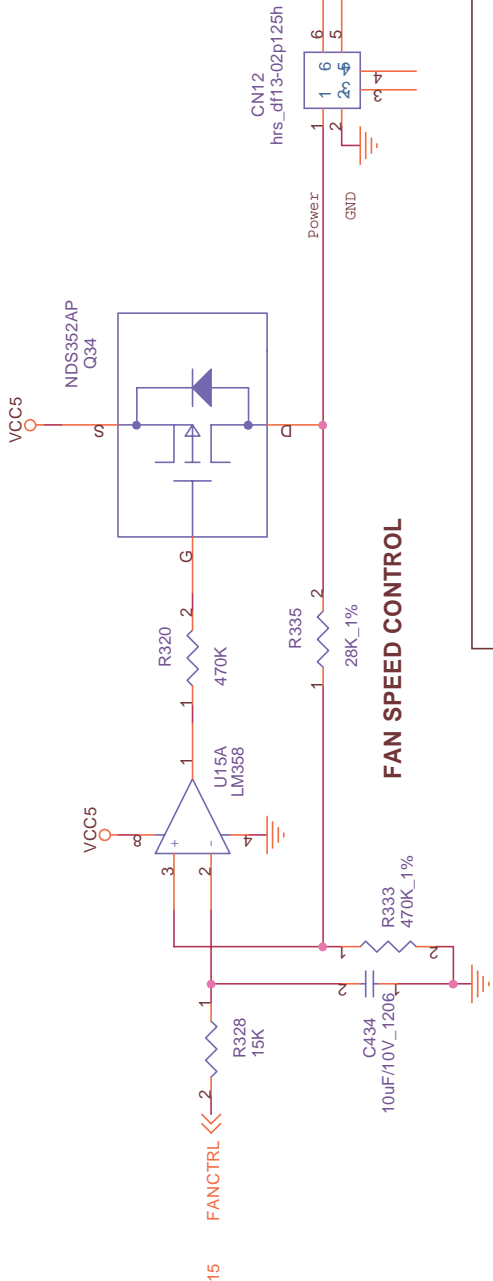
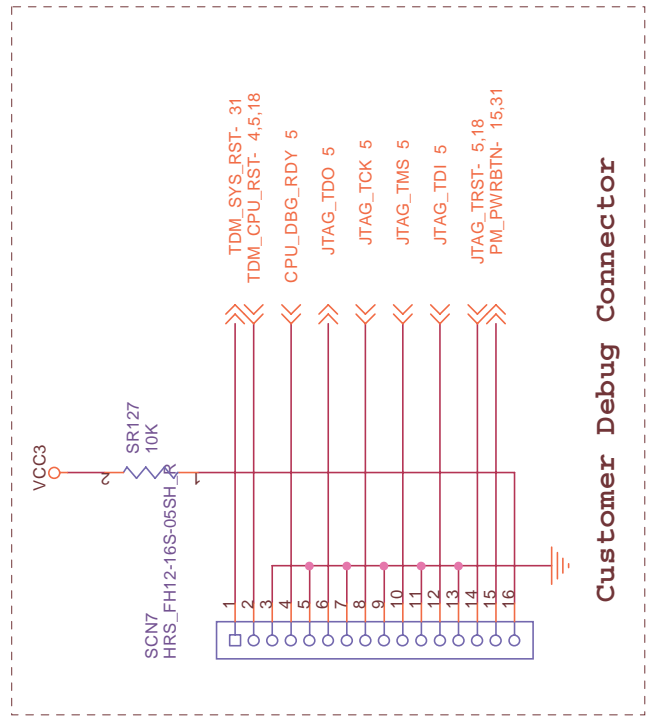
1762



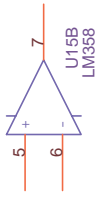
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Size	Document Number	532-1-4-01	
Customer	Rev	B.0	
Date:	Wednesday, September 29, 2004	Sheet	12 of 46



Place close to TM8600



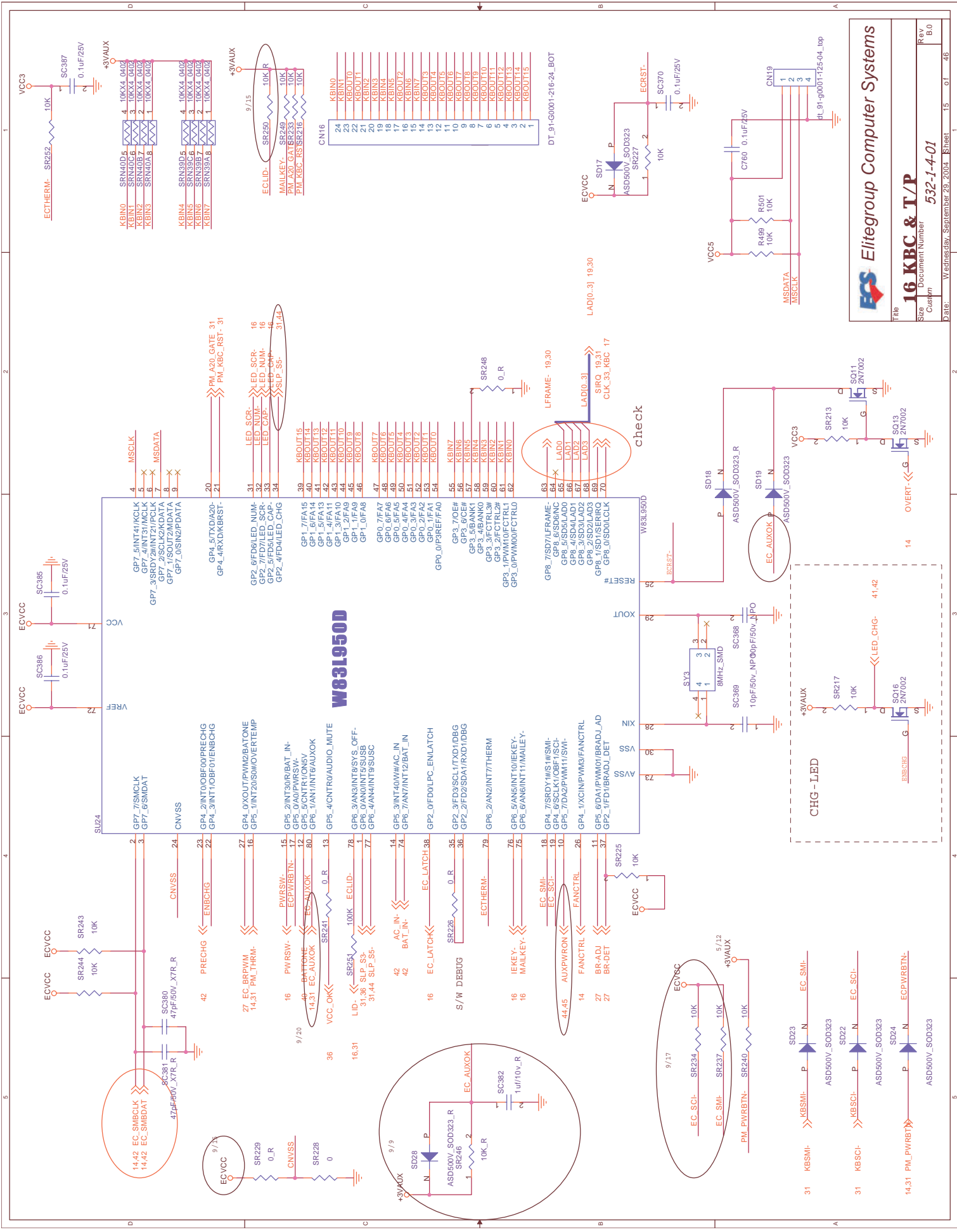
FAN SPEED CONTROL



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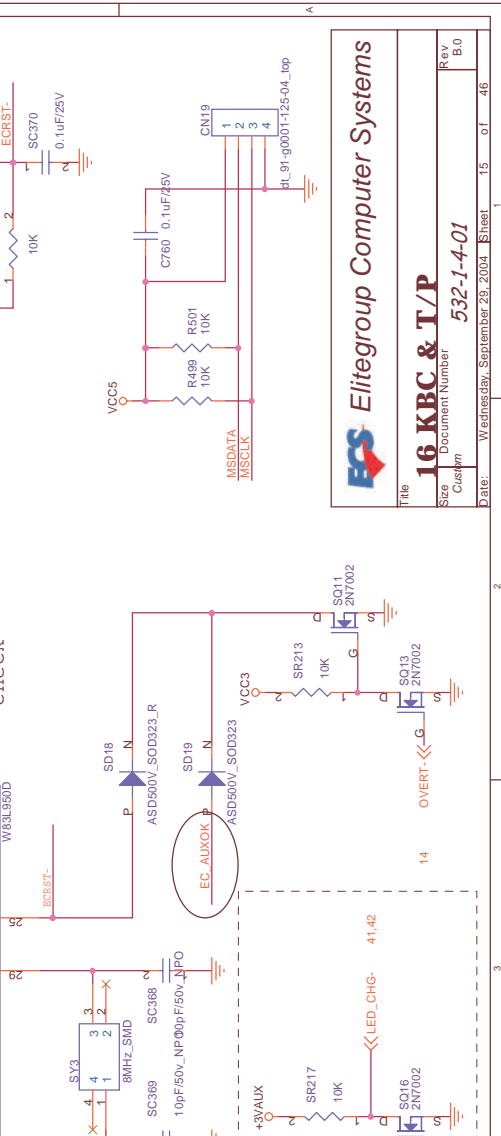
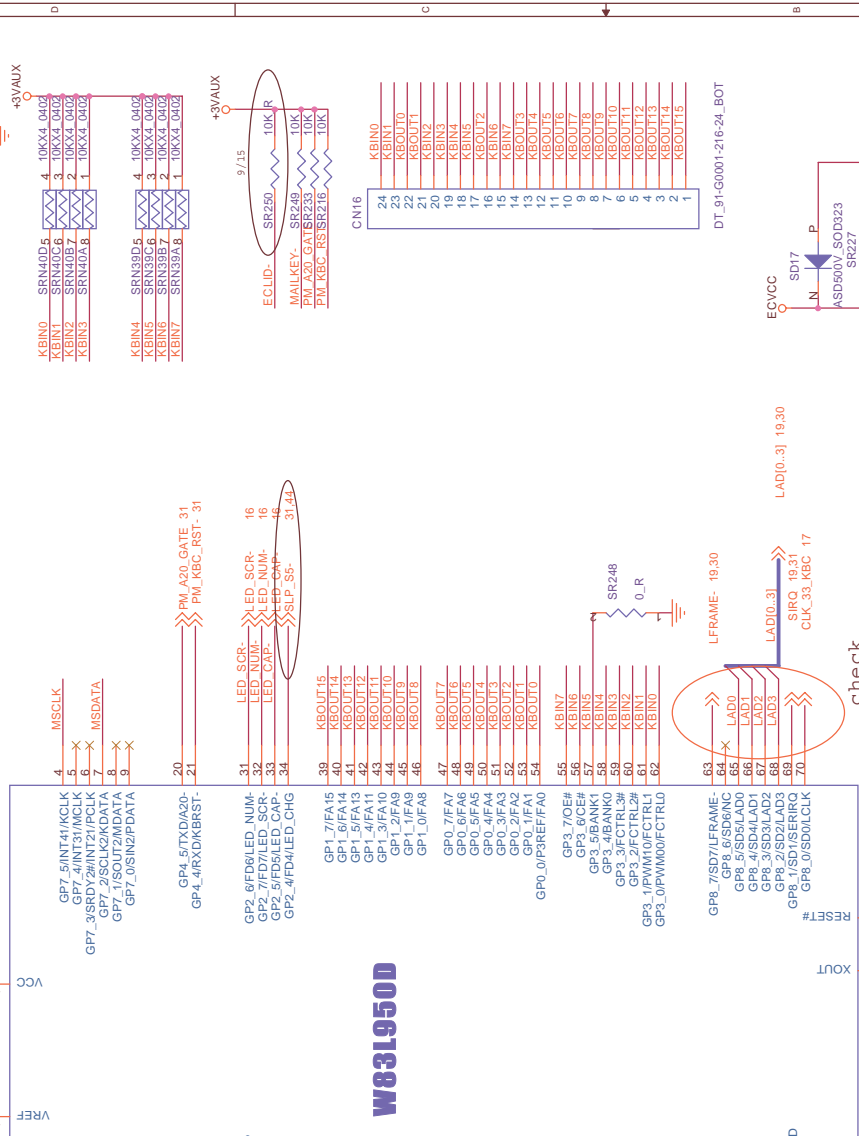
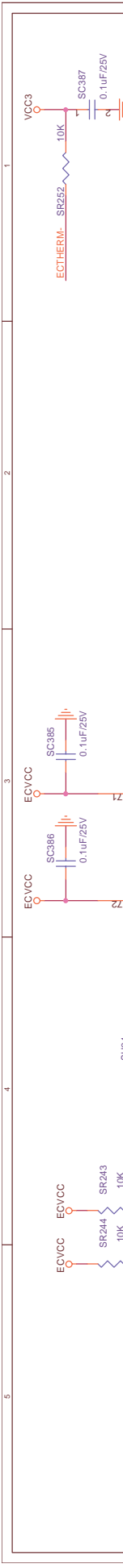
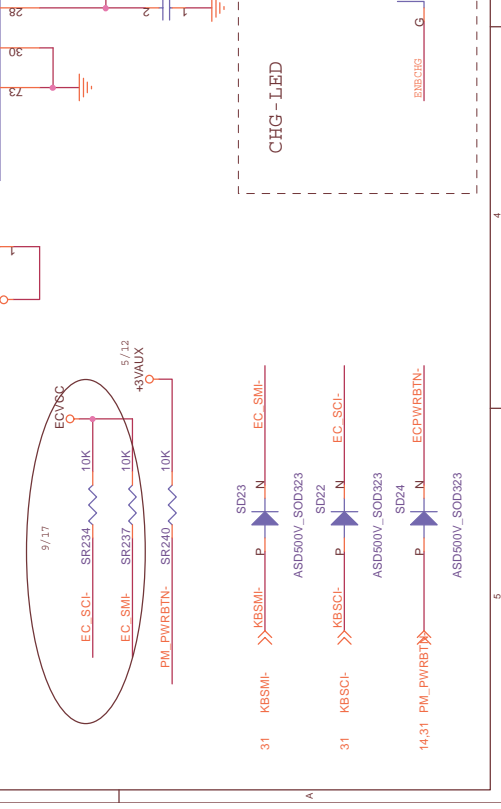
File 14 TDM-2 Conn & Thermal Sensor

Size	Document Number	Rev	B.0
Custom	532-1-4-01		
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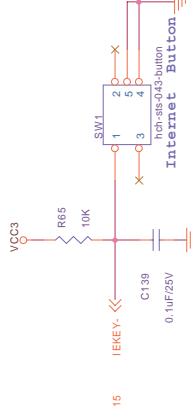
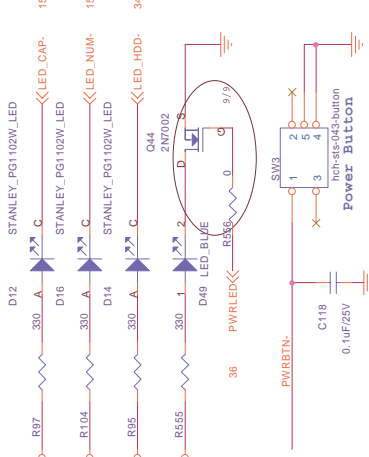
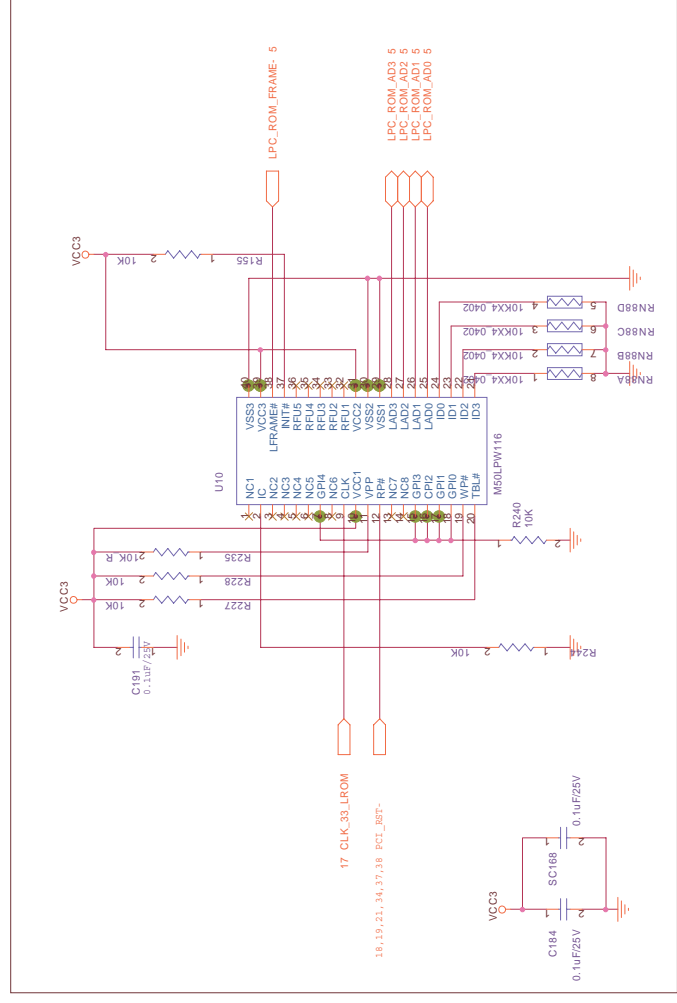
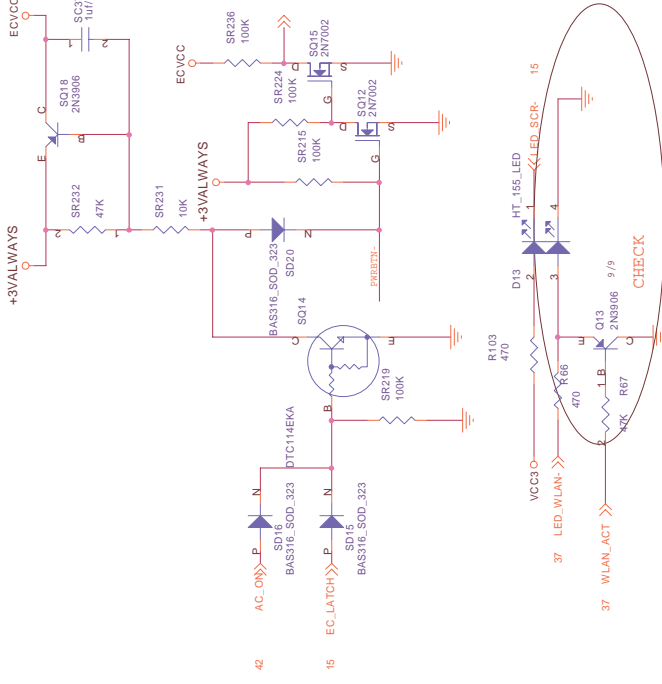


W63L950D

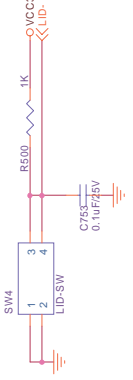
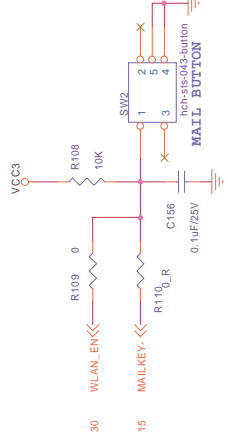
14,42	EC_SMBCLK	10K	EC_SMBDAT	10K
14,42	EC_SMBDAT	10K	EC_SMBCLK	10K
42	PRECHG	ENBCHG		
27	EC_BRPWM	14,31	PM_THRM	
16	PWRSW	15	EC_PWRBTRN	
16	BATTONE	12	EC_AUXOK	
14,31	EC_AUXOK	14,31	EC_AUXOK	
36	VCC_OK	0		
16,31	LID	SR254	100K	ECLID
31,36	SLP_S3	31,44	SLP_S5	
42	BAT_IN	42	BAT_IN	
16	EC_LATCH	16	EC_LATCH	
S/W	DEBUG	SR226	0	
16	IEKEY	16	MAILKEY	
44,45	AUXPWRON	10		
17	FANCTRL	26		
14	BRADJ	11		
27	BRDET	37		
31	KBSMI	SD23		
31	KBSCI	SD22		
14,31	PM_PWRBTRN	SD24		



EC LATCH CIRCUIT

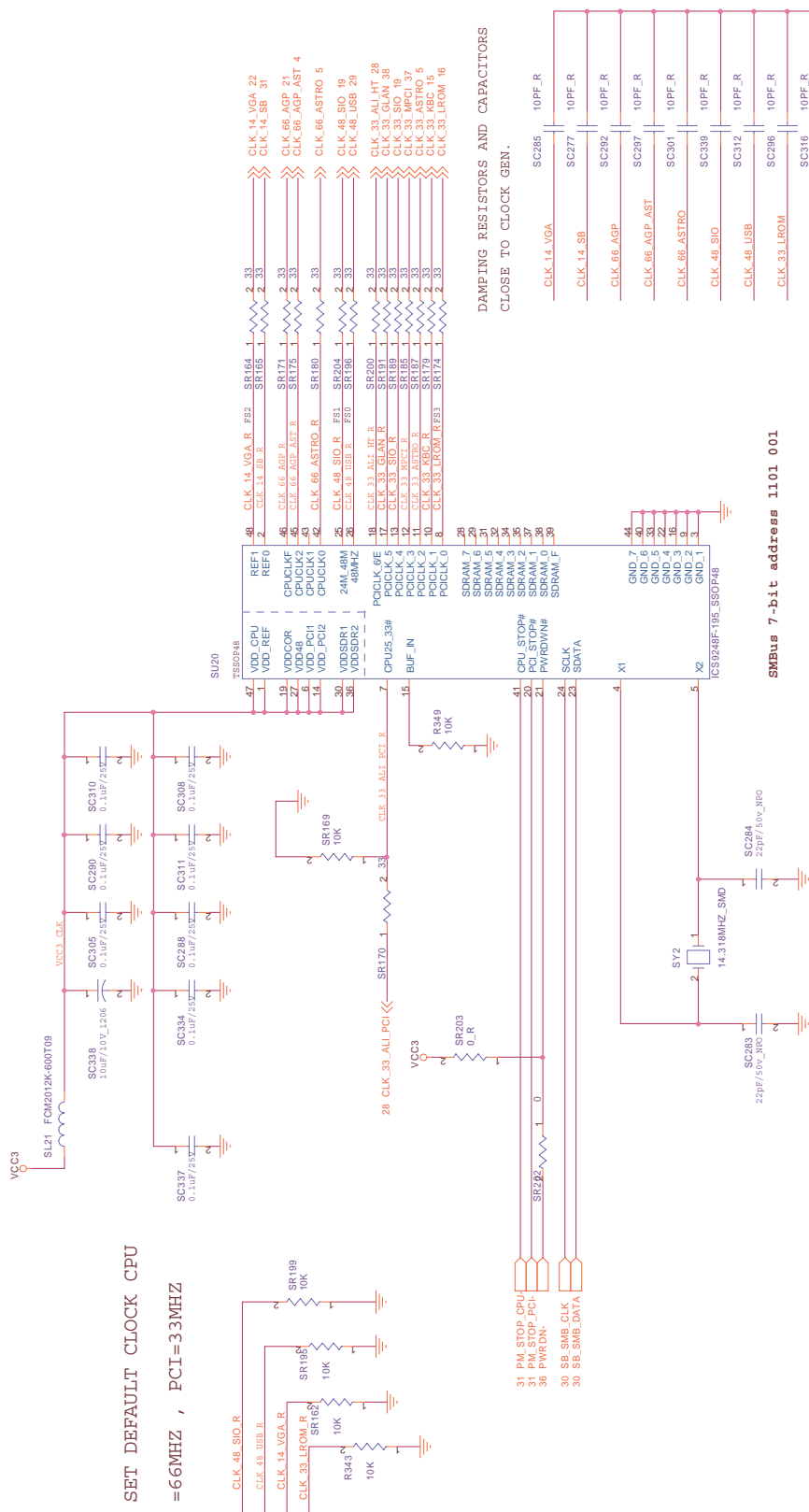


pin 1 & 4 to press



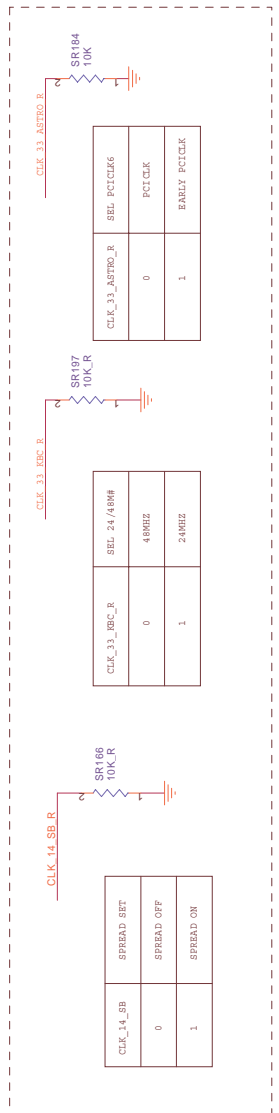
SET DEFAULT CLOCK CPU

=66MHZ , PCI=33MHZ

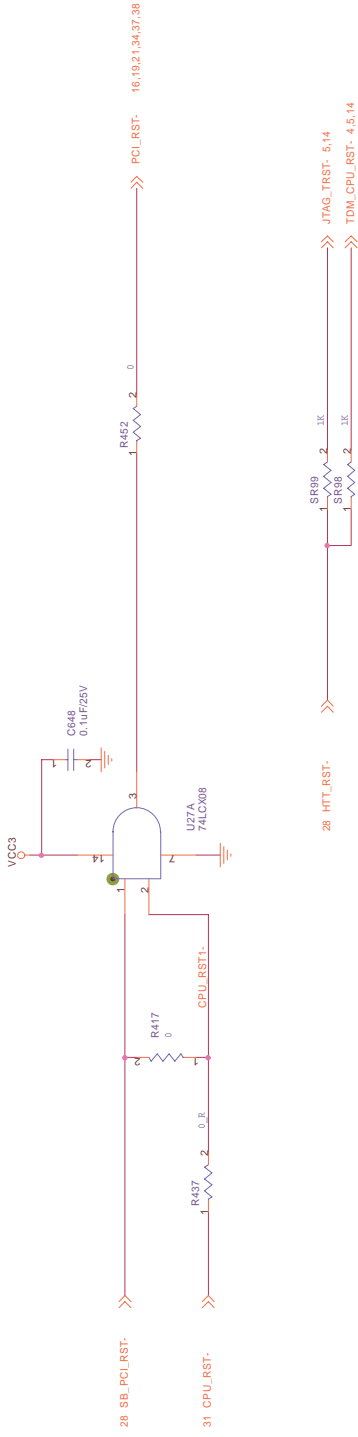


SMBus 7-bit address 1101 001

STRAP SETTING

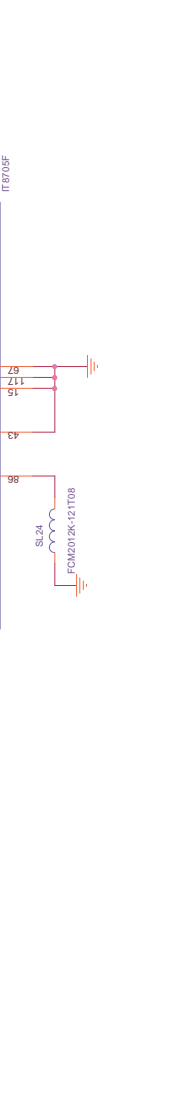
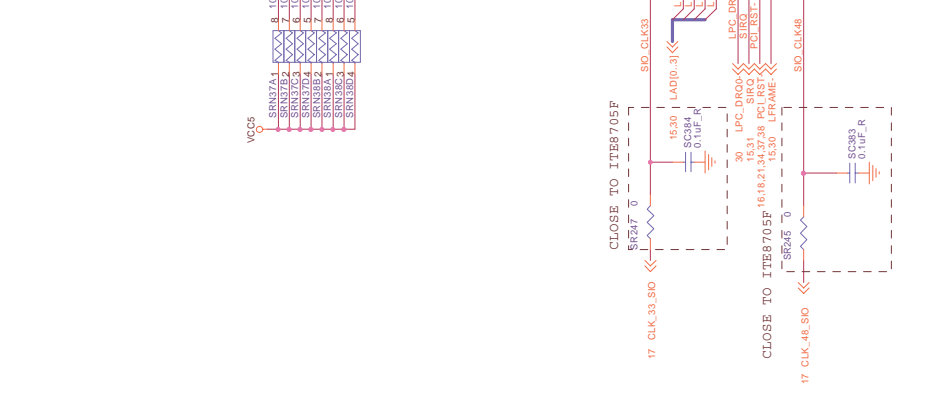
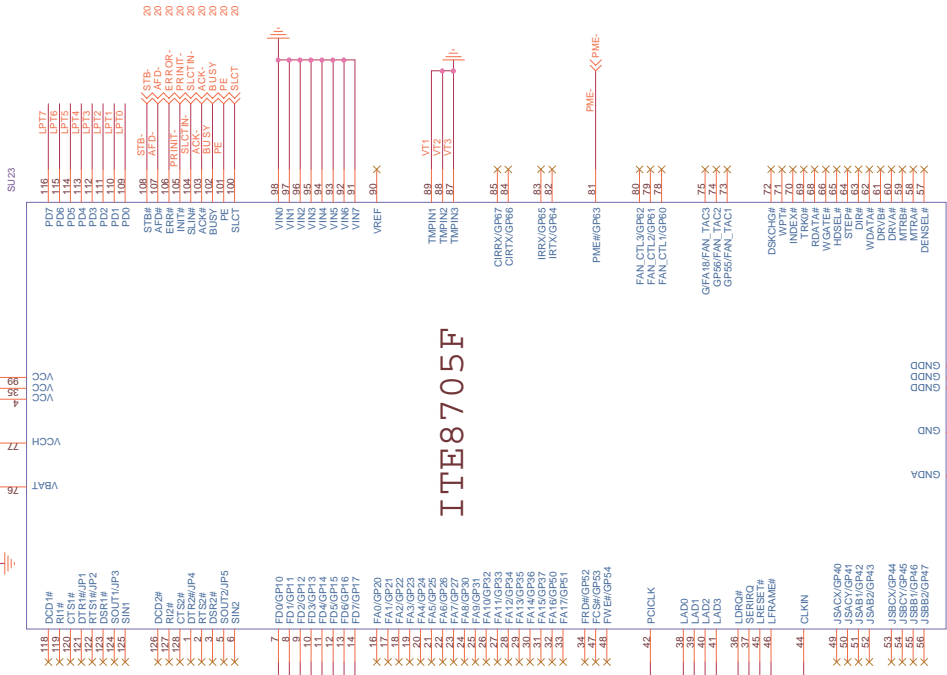
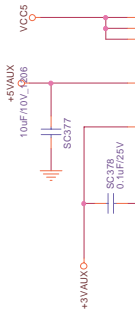
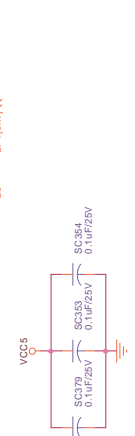


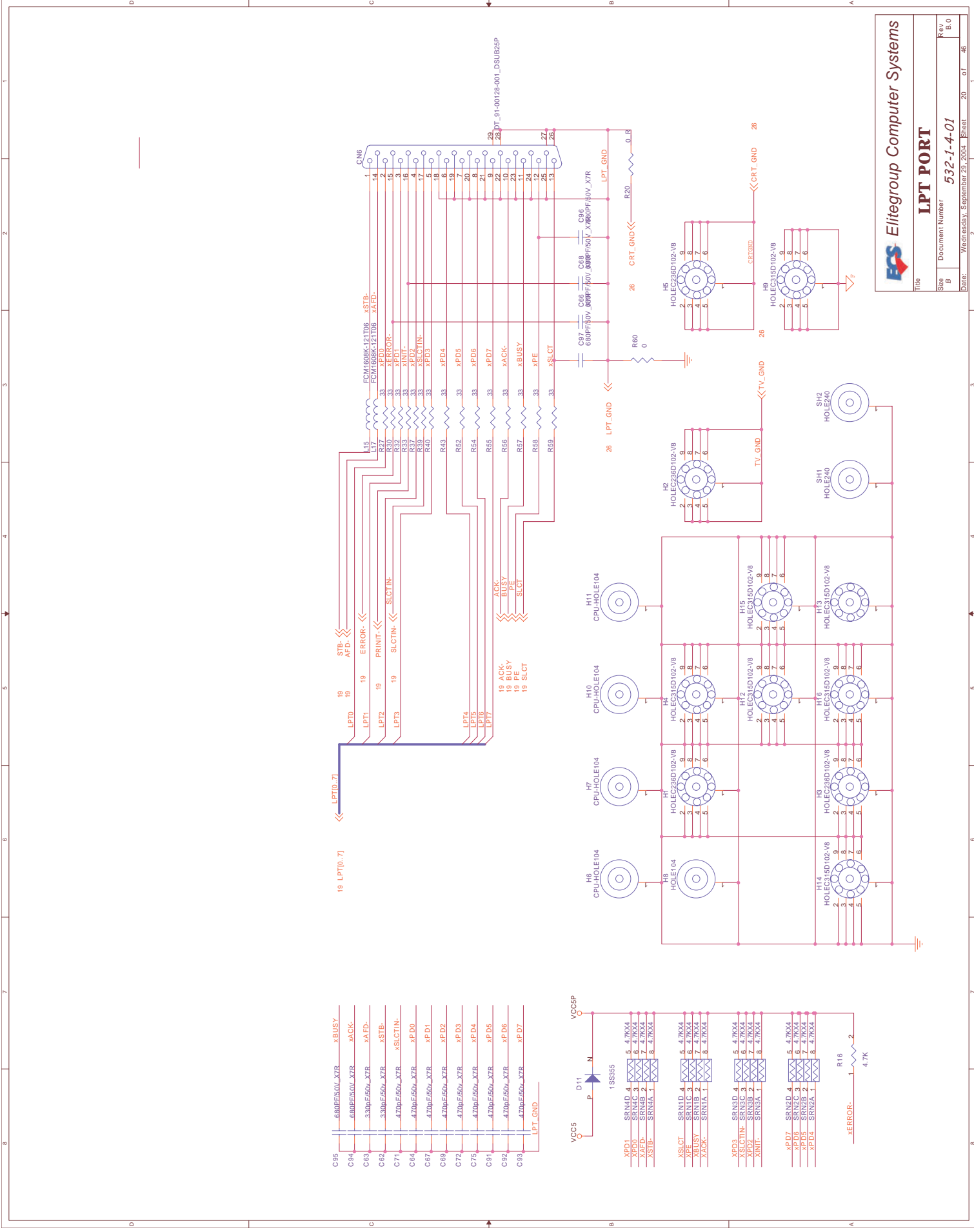
DAMPING RESISTORS AND CAPACITORS
CLOSE TO CLOCK GEN.

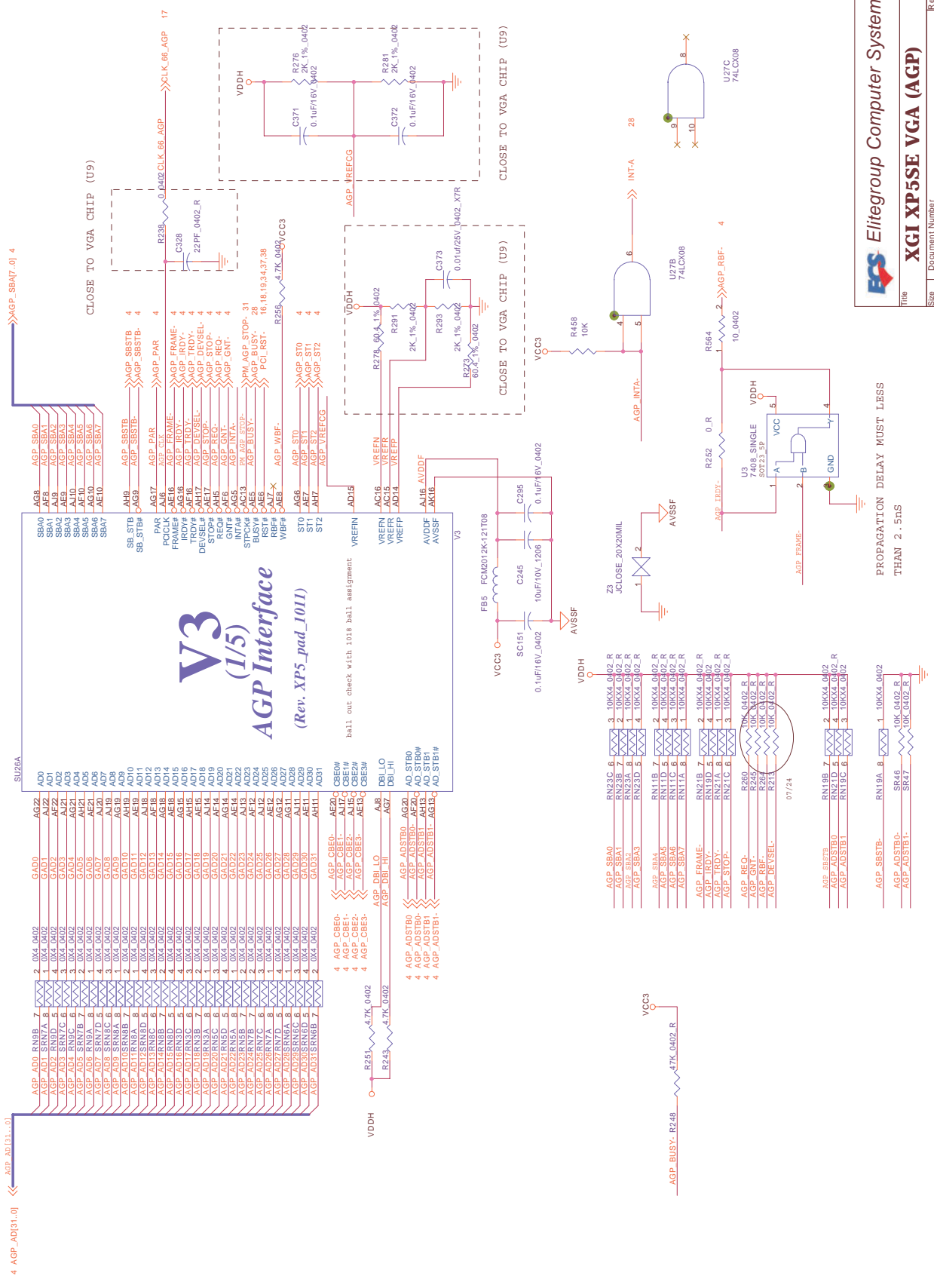


Title		RESET	
Size	Document Number	532-1-4-01	
B	Date:	Wednesday, September 29, 2004	Sheet 18 of 46

20 LPT10-71 LPT10-71







V3 (1/5) AGP Interface

(Rev. XP5_pad_1011)

ball out check with 1018 ball assignment

PROPAGATION DELAY MUST BE LESS THAN 2.5ns

Based on Volari V3 Dip Switch and Config. Ver.2.0 Oct 03.

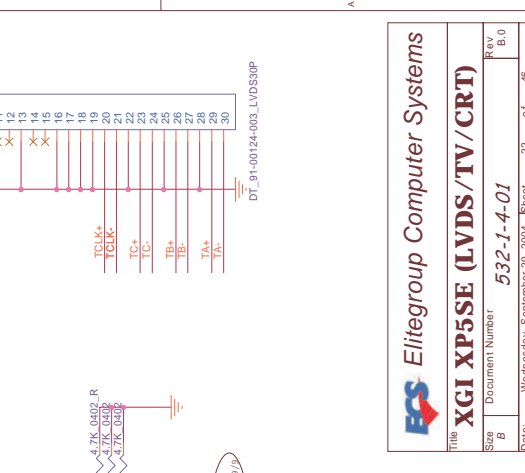
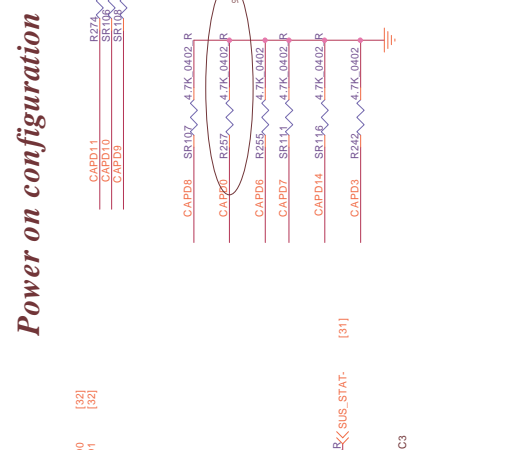
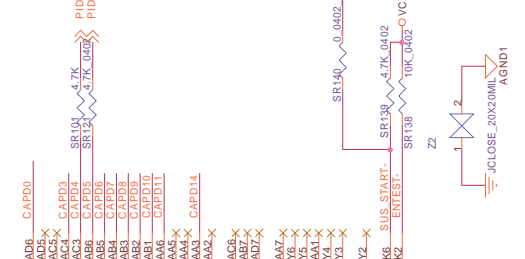
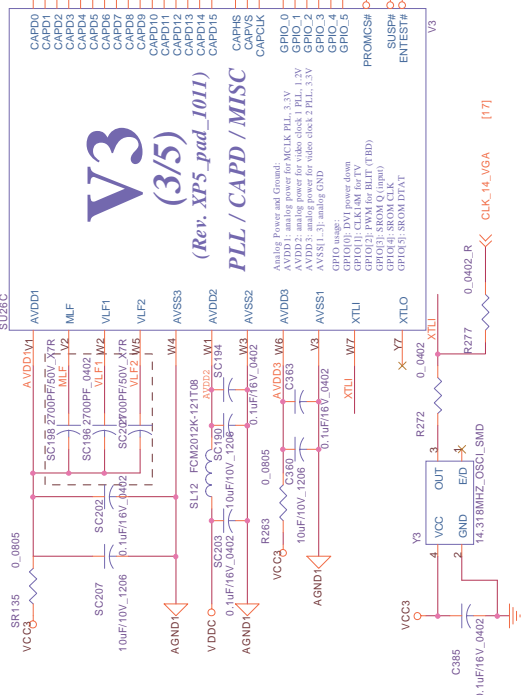
CAPD [11..1.9]	SYNC
000	230MHz
001	125MHz
010	166MHz
011	215MHz
100	200MHz
101	250MHz
110	275MHz
111	300MHz

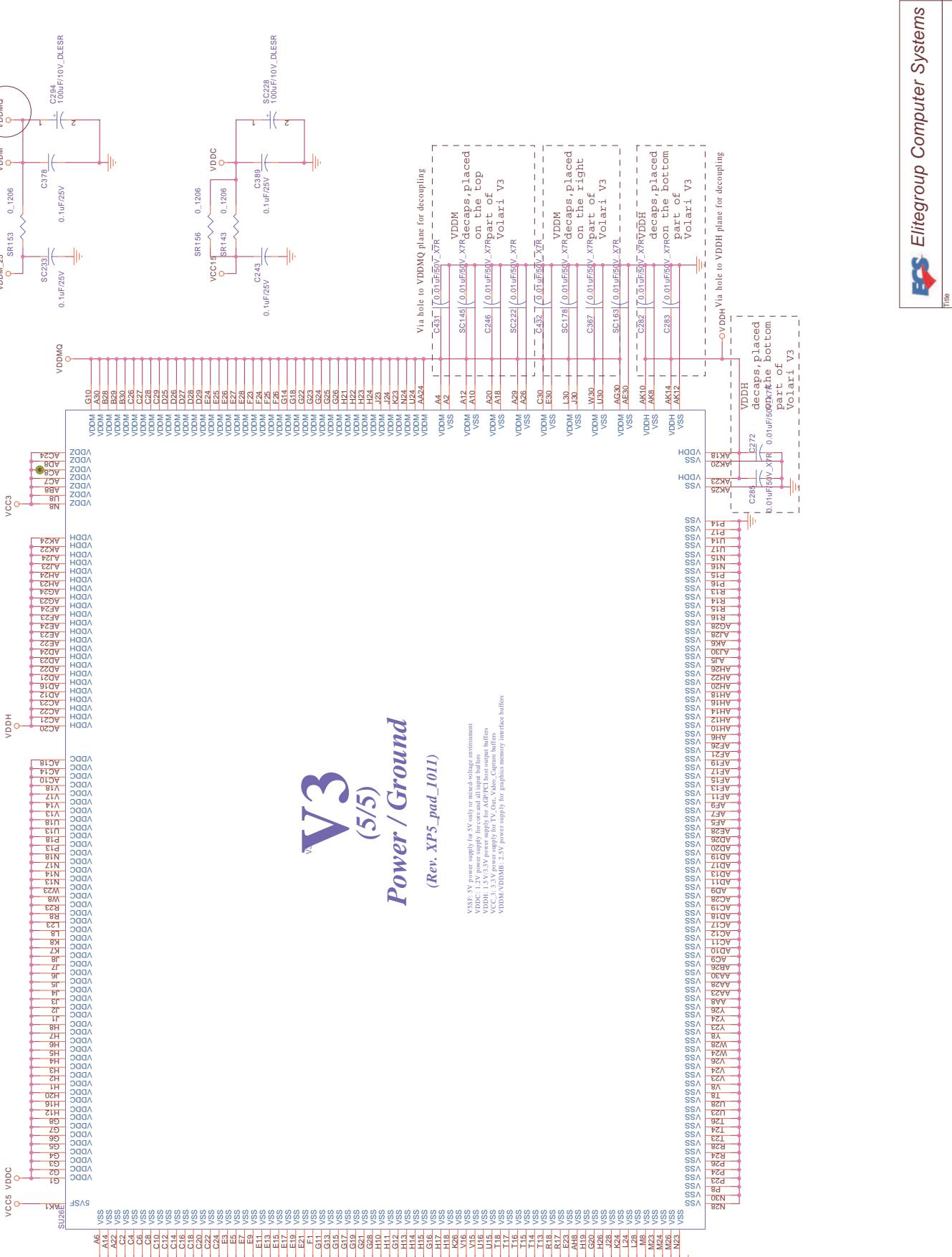
PANEL ID

PANID [1..01] : (CAPD [5..4])	PANEL TYPE
00	RESERVED
01	TFT 1024x768 - 18 0DI
10	TFT 1024x768 - 18
11	RESERVED

Configuration Table:

CAPD	FUNCTION	Config(Stuff R4.7K=0)	Default
0	CLOCK MODE	0: External, 1: Internal	1: Internal
1	BUS TYPE	0: RESERVED, 1: AGP	1: AGP
2	ID SELECT	0: AD17, 1: AD16	1: AD16
3	BIOS	0: Disable, 1: Enable	0: Disable
5,4	PANEL ID TYPE	See Panel Type Table	
6	RESERVED		
8	LCD ON/OFF	0: OFF, 1: ON	1: LCD ON
11..9	MEMORY CLOCK	See Table	100: 200MHz
12	VDDQ VOLTAGE	0: 3.3V, 1: 1.5V	1: 1.5V
13	DDR/SDR SELECT	0: SDR, 1: DDR	1: DDR
7	VIDEO RAM TYPE	0: 2MX32, 1: 4MX32	1: 4MX32
15	AGP Version	0: AGP 3.0, 1: AGP 2.0	1: AGP 2.0





V3 (5/5) Power / Ground

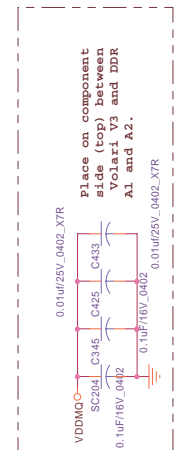
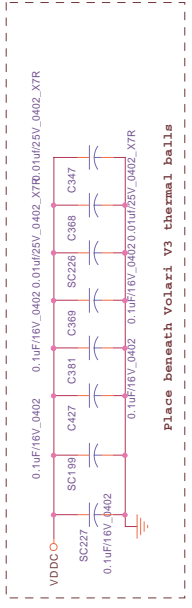
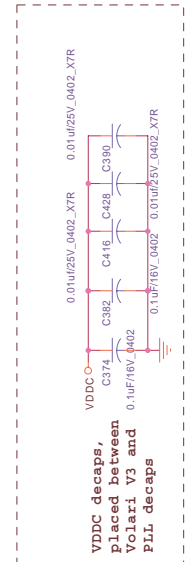
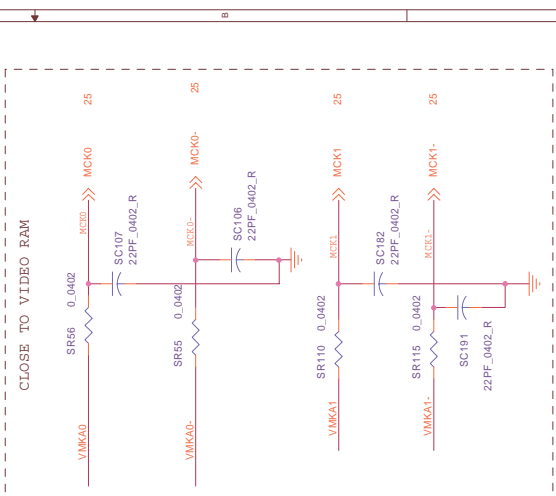
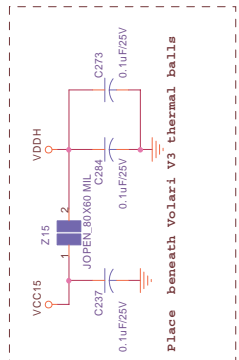
(Rev. XP5_pad_1011)

VDDH: 5V power supply for 5V logic and bridge environment
 VDDC: 1.2V power supply for core and all logic buffers
 VDDH: 1.2V/3.3V power supply for ACP/PCI host output buffers
 VDDM: VDDM0: 2.5V power supply for graphics memory interface buffers

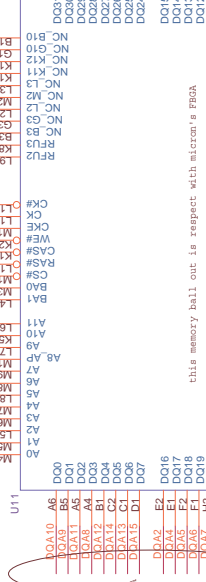
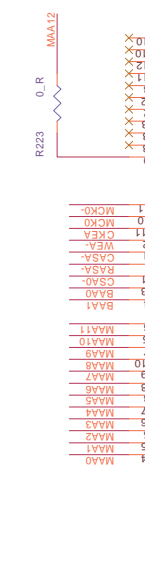
V3 (2/5)

Memory Interface

(Rev. XP5_pad_1011)



Port A 2M/4M x 32 DDRs



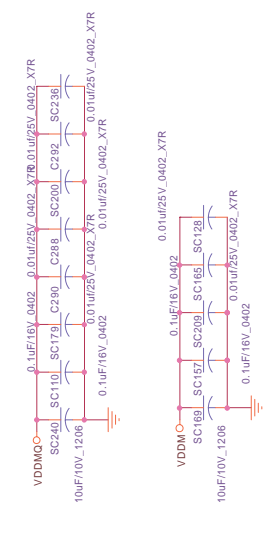
4M x 32 DDR

FBGA 144

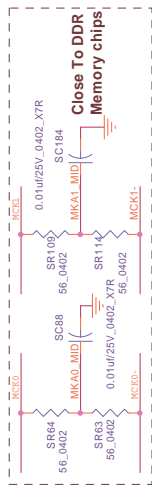
this memory ball out is respect with micron's FBGA



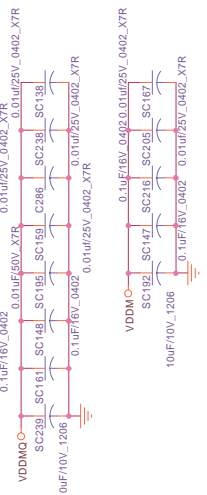
DDR VDDMIO / VDDM de-caps



DDR Port A Decoupling Capacitors

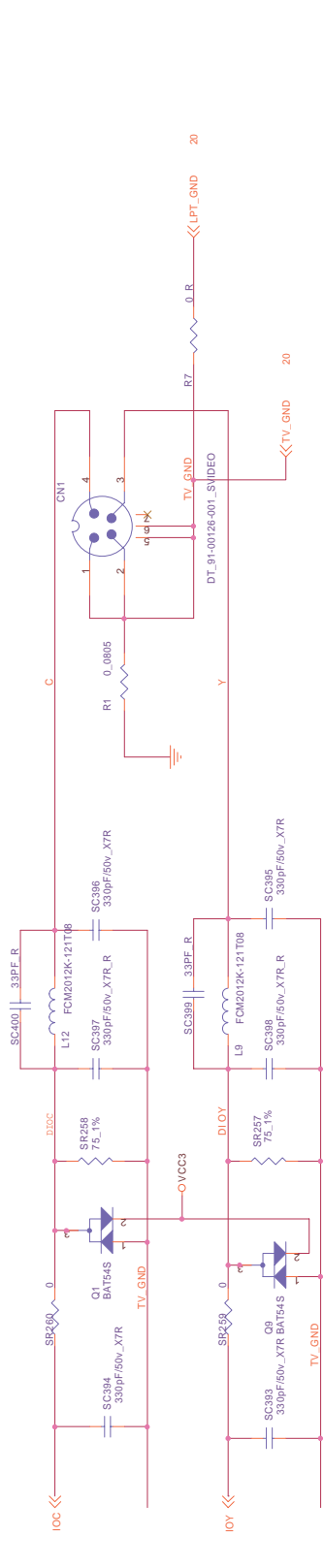
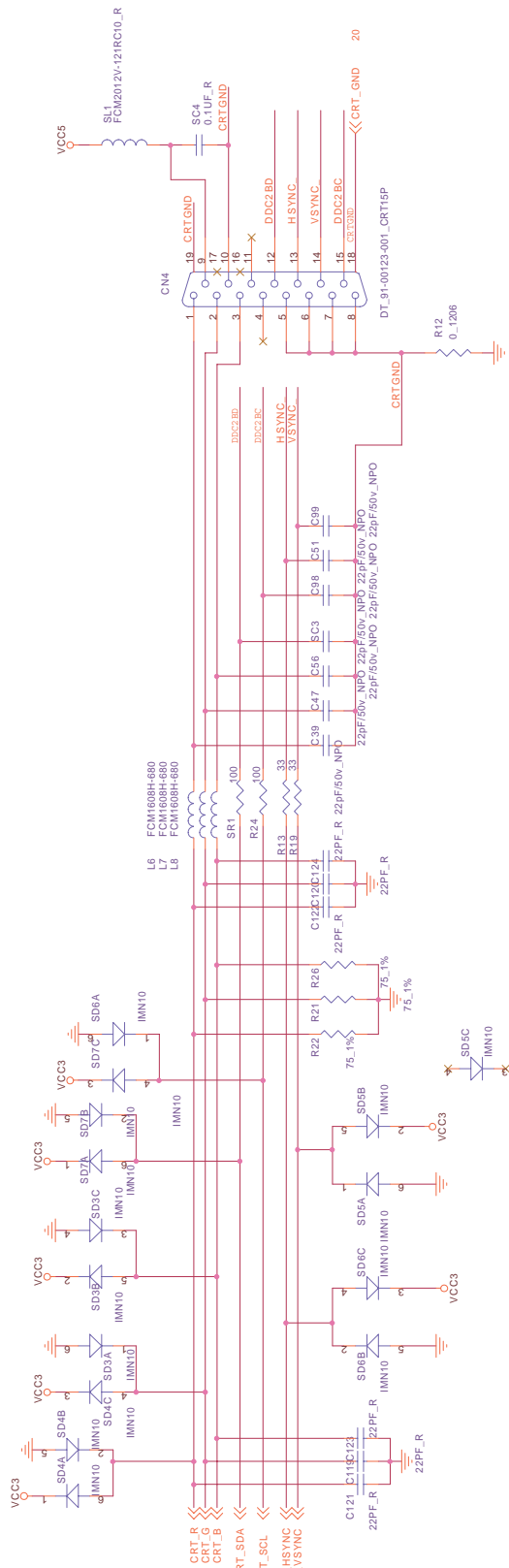


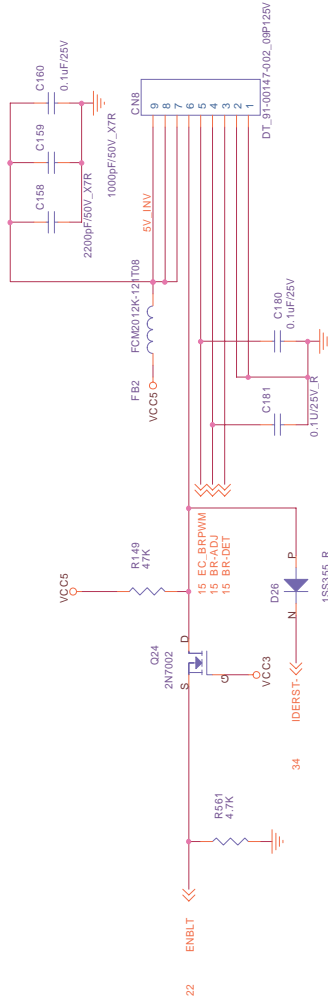
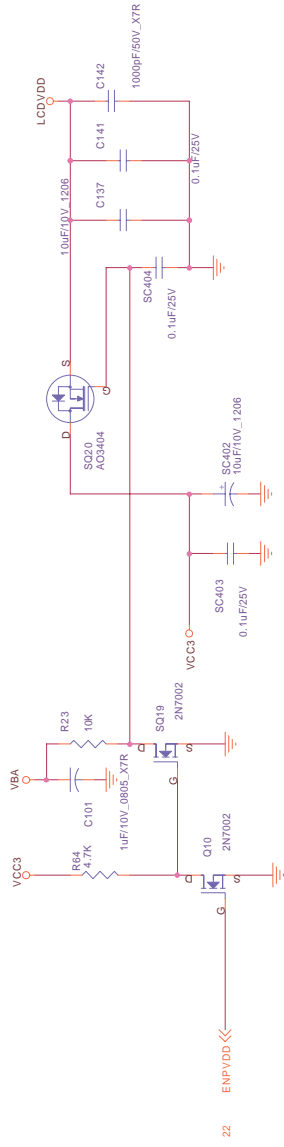
DDR VDDMQ / VDDM de-caps

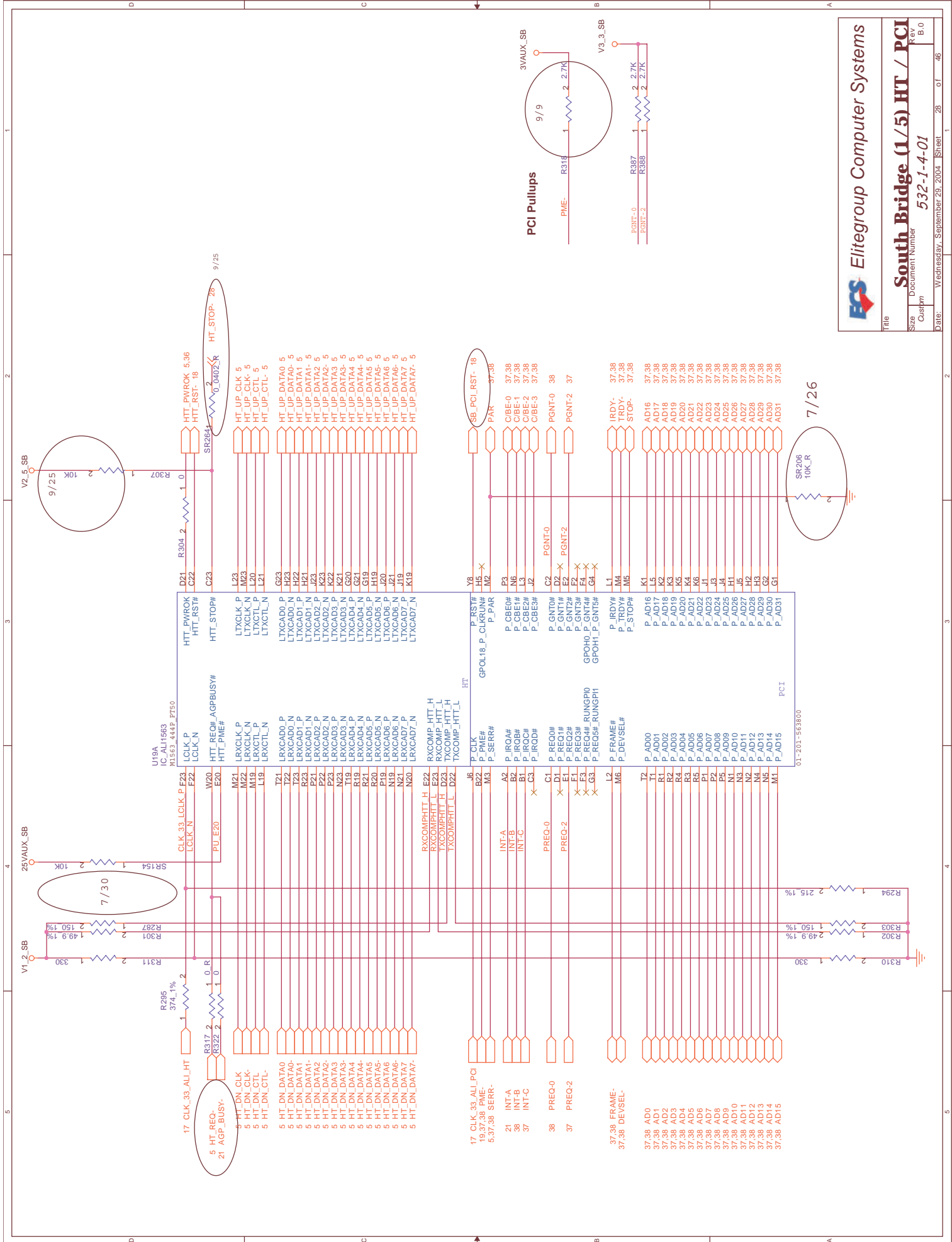


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File
 Size B
 Document Number 532-1-4-01
 Rev B.0
 Date: Wednesday, September 29, 2004 8:02 AM 25 of 46

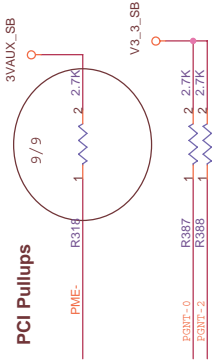






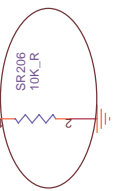
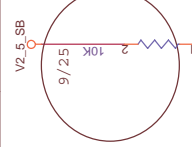
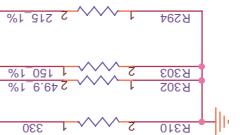
7/26

9/25

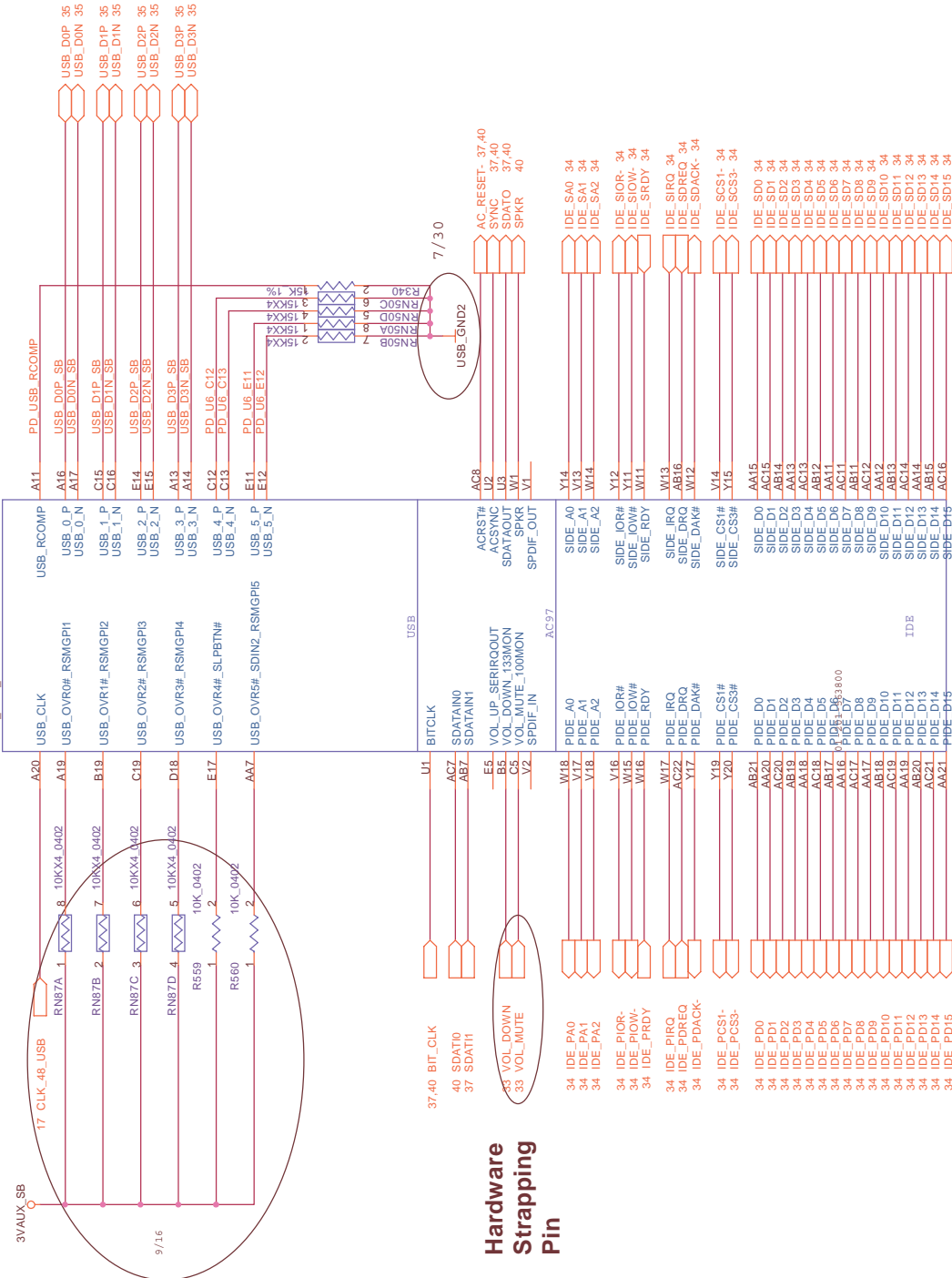


PCI Pullups

01-201-563800



U19B
IC_ALH1563
M1563_444P_P750



Hardware Strapping Pin

Elitegroup Computer Systems

Title: **South Bridge (2/5) USB / IDE / AUDIO**

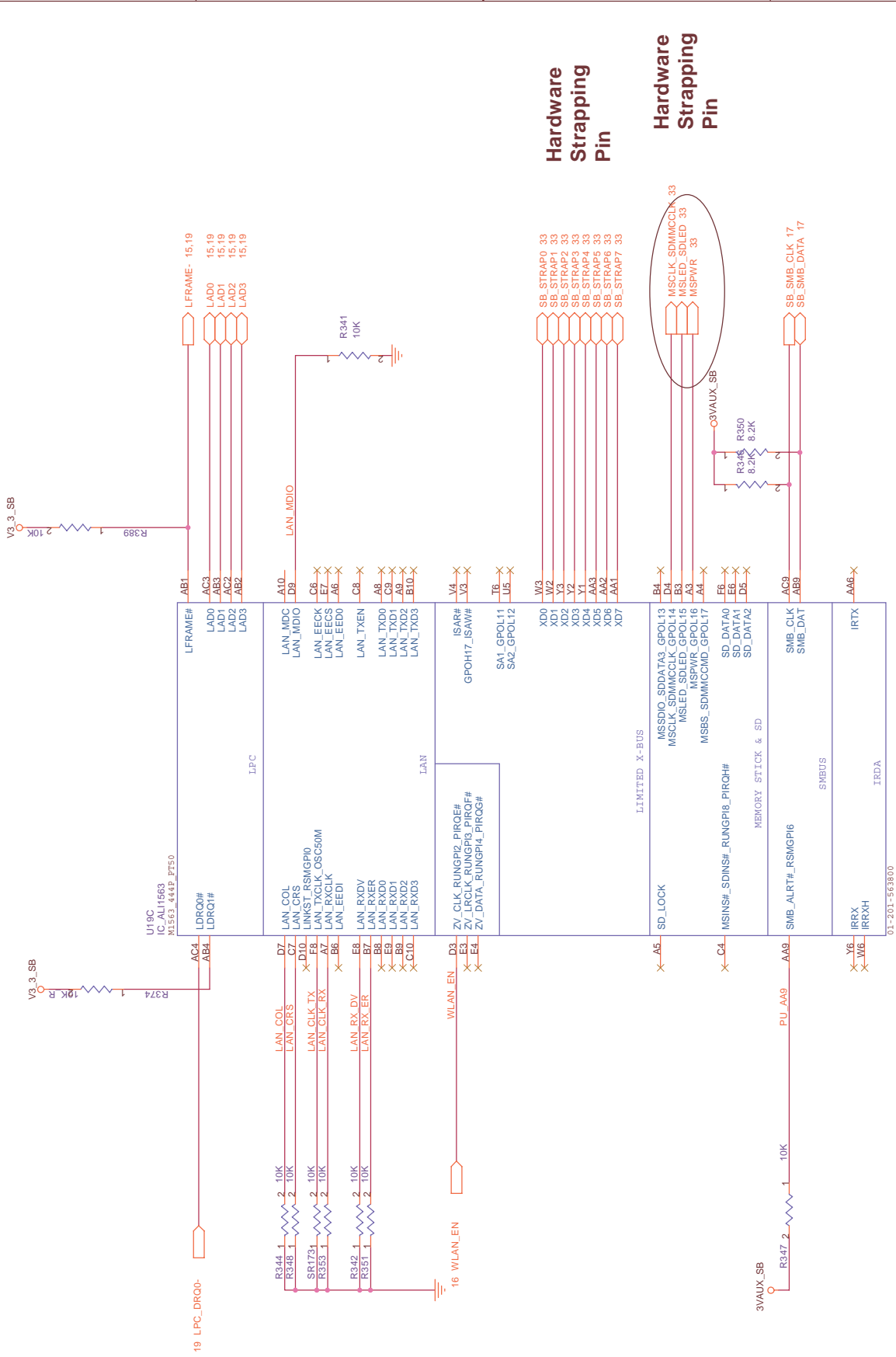
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Date: **Wednesday, September 29, 2004**

Sheet: **29** of **46**

Rev: **B.0**

Cust#m



Hardware Strapping Pin

Hardware Strapping Pin

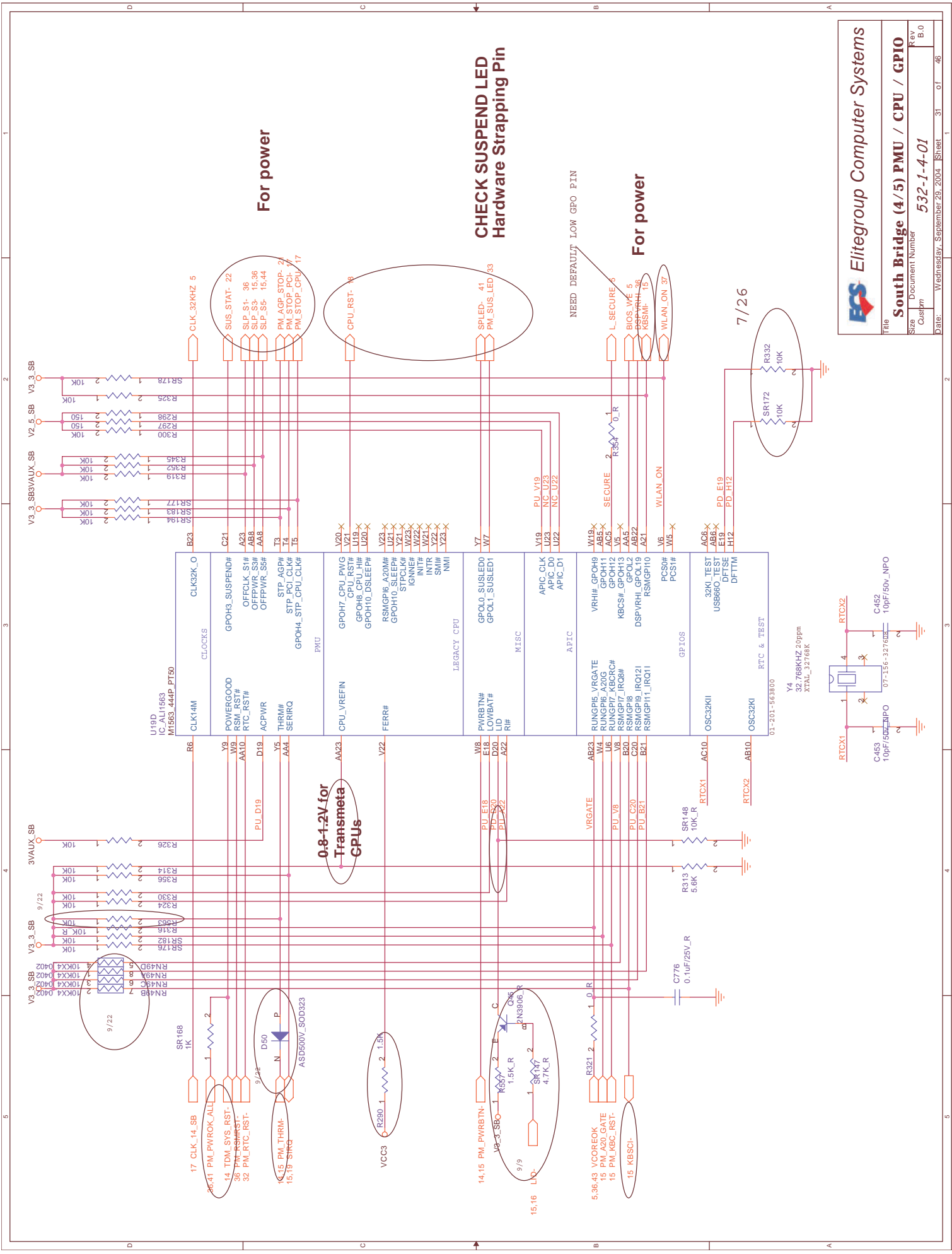
Elitegroup Computer Systems

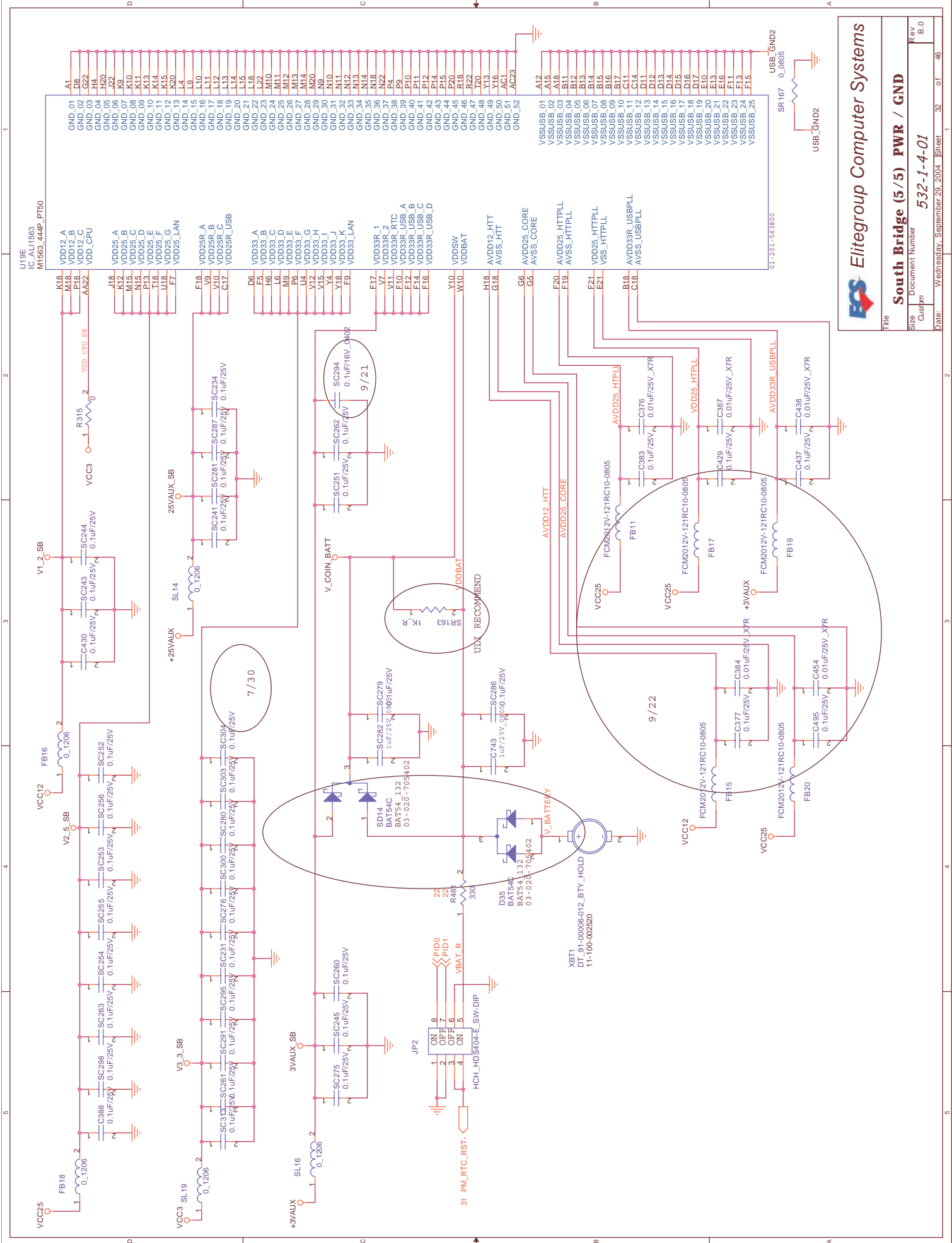
Title: **South Bridge (3/5) LPC / SMBUS**

Size: **532-1-4-01**

Rev: **B.0**

Date: **Wednesday, September 29, 2004**





U19E
IC_ALI1563
MT563_444P_PTF50

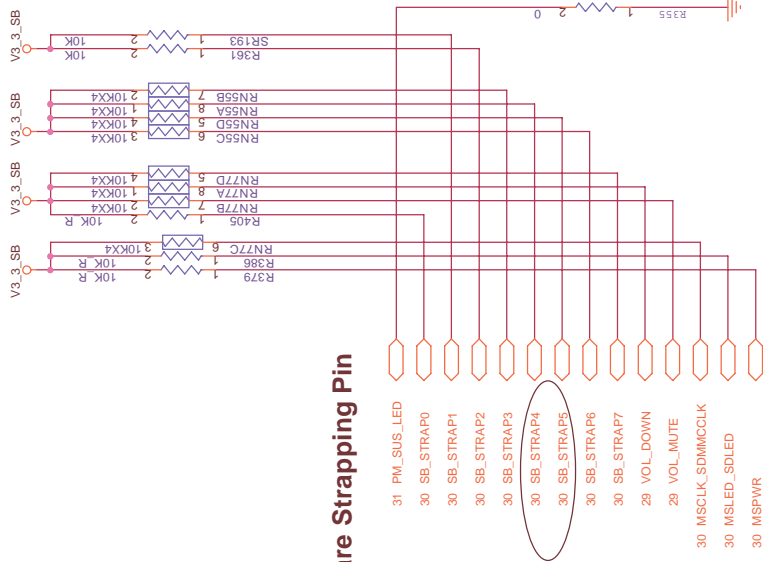
DT_91-00006-012.BTY_HOLD
11-100-002520

Elitegroup Computer Systems		
Title	South Bridge (5/5) PWR / GND	
Size	Document Number	532-1-4-01
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Pin Name	External Pull-low/High Settings	Function Description	Corresponding Status Register and Value
PM_SUS_LED	L	Normal Operation Mode Full chip 32K clock test mode enabled (32K Input Test mode from 32K Clock Test Input pin)	Default
XD[0]	L	Full chip debug mode enabled to bypass internal bus to PCI slot	Default
XD[1]	L	UART/KBC test mode enabled if SUSLED is pulled high for chip test mode.	Default
XD[2]	H	Normal Operation Mode	Default
XD[3]	L	Full chip simulation mode enabled to shorten reset time for simulation.	Default
XD[4]	H	Normal Operation Mode	Default
XD[5:4]	L	Jumper-less Mode Enabled. The AZDN#, IGNNS#, INTR, and MNT will be used as the CPU frequency strap during the reset sequence	Default
XD[6]	H	Jumper-less Mode Disabled. The AZDN#, IGNNS#, INTR, and MNT will not be used as the CPU frequency strap during the reset sequence. These signals will work as the original function (inactive) during the reset period.	Default
XD[7]	L	Full chip copes PFI internal bus clock setting ALI Reserved (66MHz)	Default
	LH	33MHz	
	HL	66MHz	
	HH	100MHz	
XD[8]	L	Full chip pattern testing mode enabled.	Default
XD[9]	H	Normal Operation Mode	Default
XD[10]	L	External PCI bus type select to BIOS0	Default
XD[11]	H	External PCI bus type select to BIOS1	Default
VOLUME_DOWN	L	Parallel ROM multiplexed feature supported. (This is reserved for ALI internal use only)	Default
VOLUME_MUTE	H	Normal Operation. (No parallel ROM multiplexed feature supported)	Default
	L	Non-x86 Boot ROM Address Load Mechanism supported. (This is reserved for ALI internal use only)	
	H	Normal Operation	
MSCK	HTT PLL test register setting		
MSLED	L/H	T[7]	
MSPWR	L/H	T[0]	
	L/H	T[1]	

HTT PLL test register setting

Hardware Strapping Pin

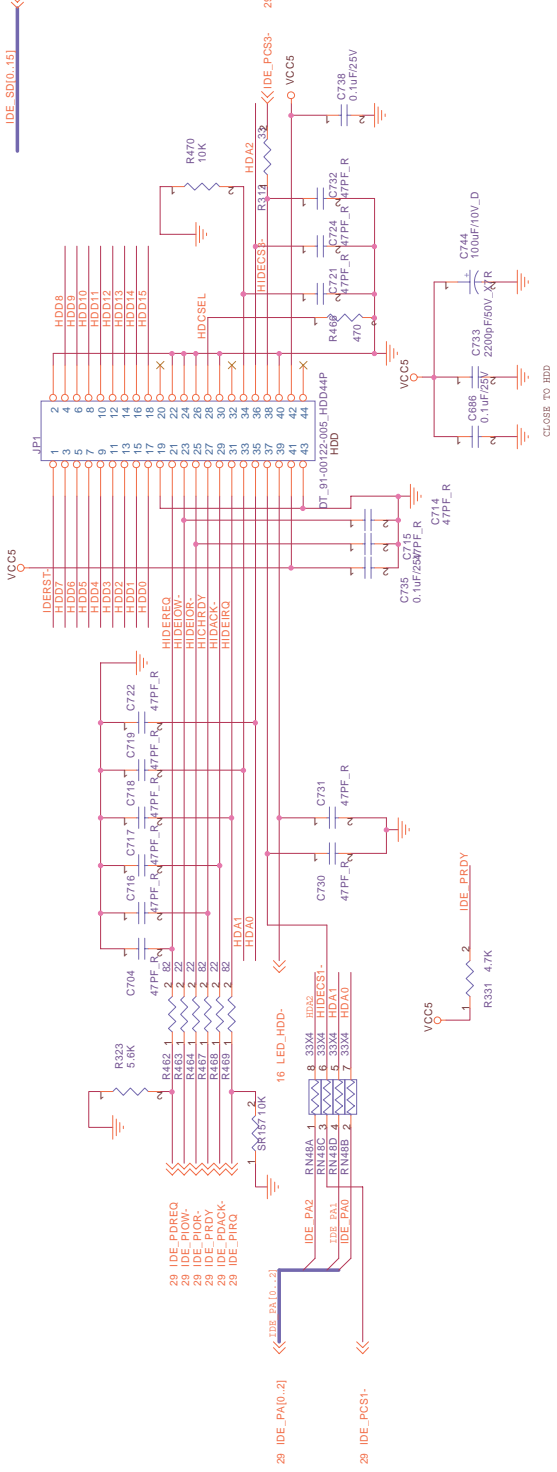


FROM SECTION 2.4 OF THE 1563 DATA SHEET

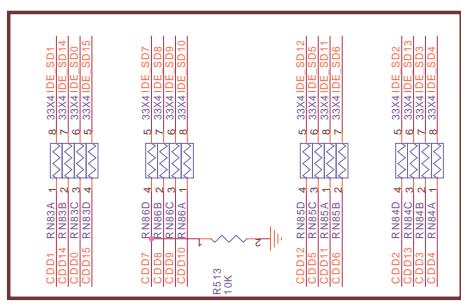
Elitegroup Computer Systems

Title		SB STRAP SETTING	
Size	Document Number	Rev	B.0
Custpm	532-1-4-01	Date	Wednesday, September 29, 2004
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IDE_PD[0..15] << IDE_PD[0..15] 29
 IDE_SDI[0..15] << IDE_SDI[0..15] 29

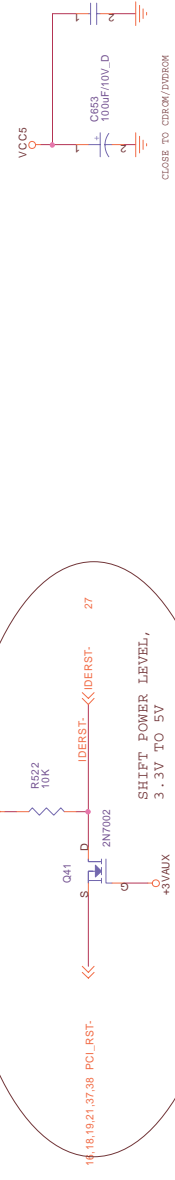


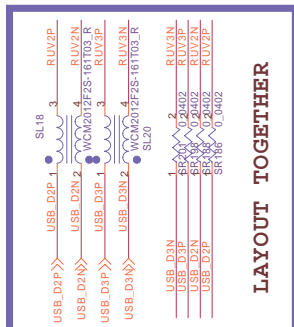
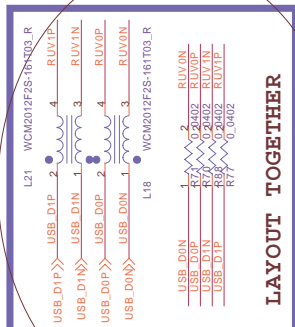
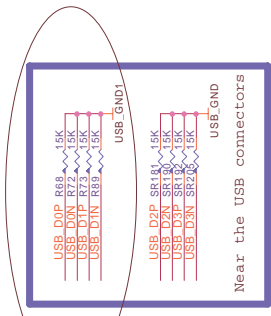
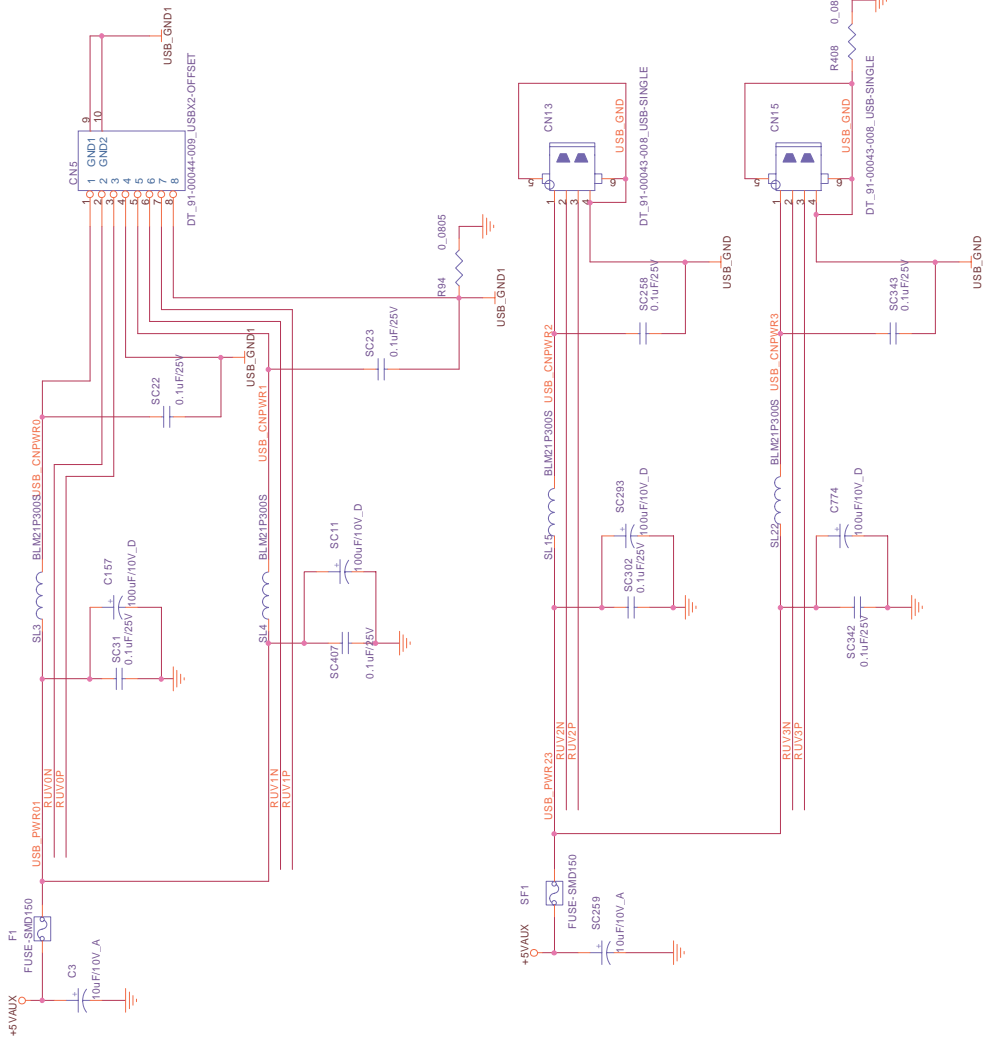
CLOSE TO HDD CONN.

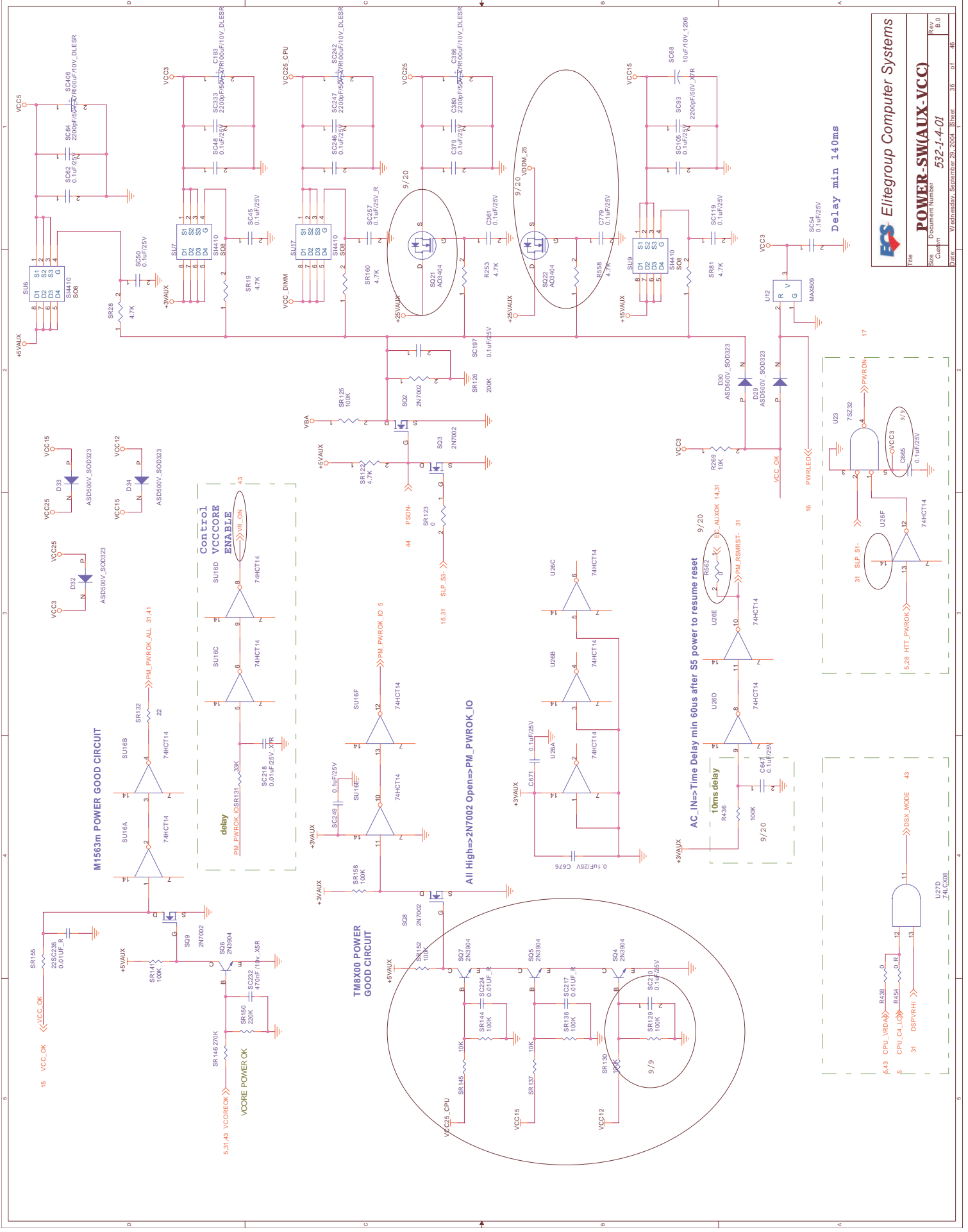


CLOSE TO CDROM CONN.

CSEL : "NC" ; "Hi" --> Master (CDROM) / Slave (DVDROM)
CSEL : "Low" --> Slave (CDROM) / Master (DVDROM)







M1563m POWER GOOD CIRCUIT

Control VCCORE ENABLE

TM8X00 POWER GOOD CIRCUIT

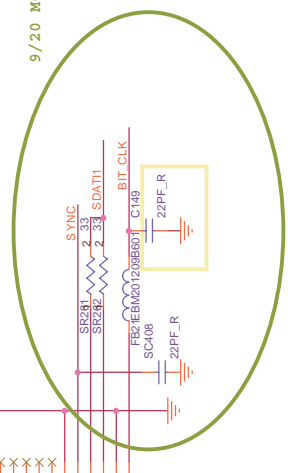
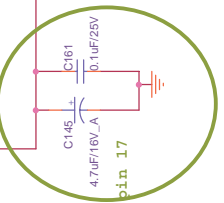
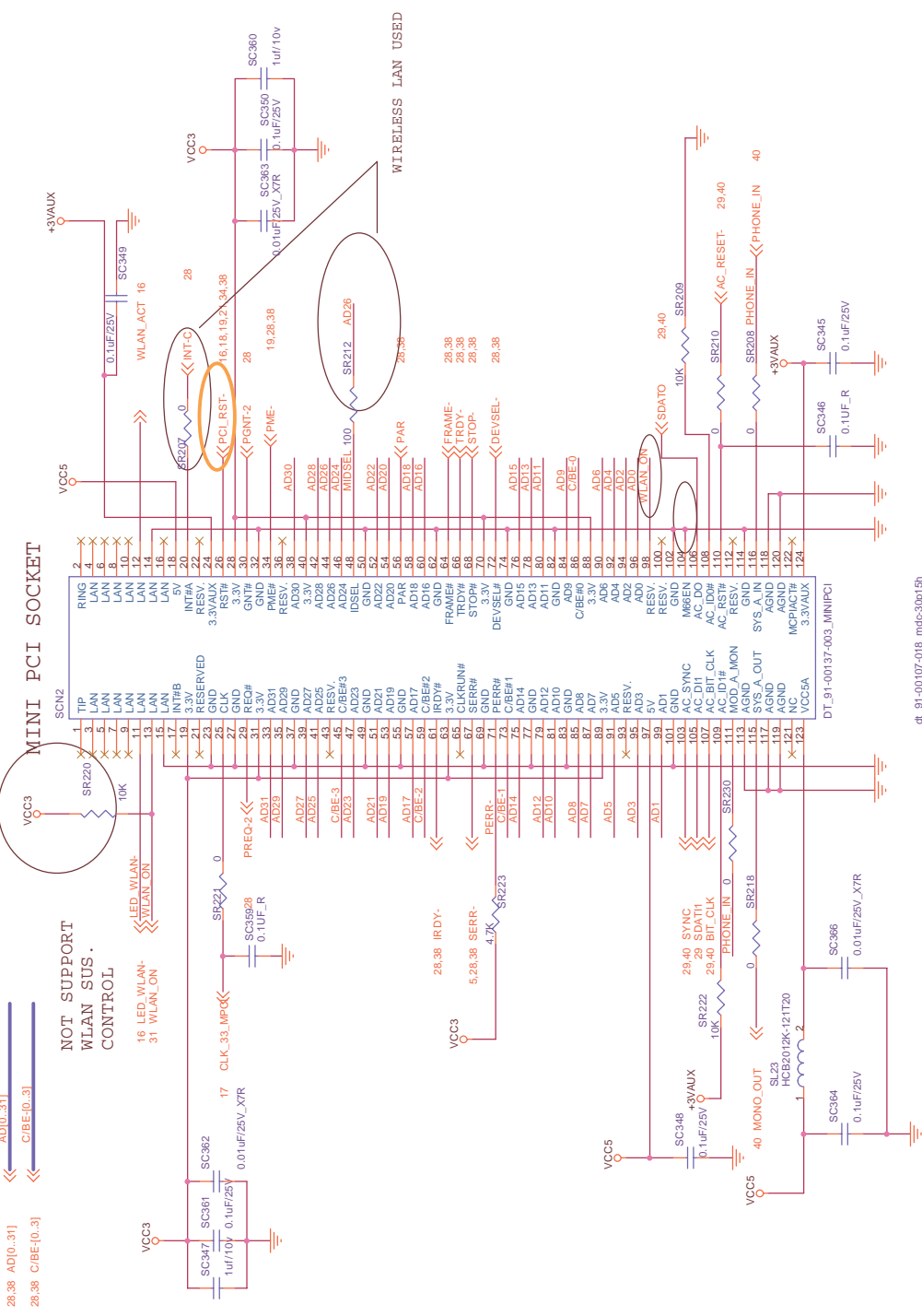
All High=>2N7002 Open=>PM_PWROK_IO

AC_In=>Time Delay min 60us after S5 power to resume reset

Delay min 140ms

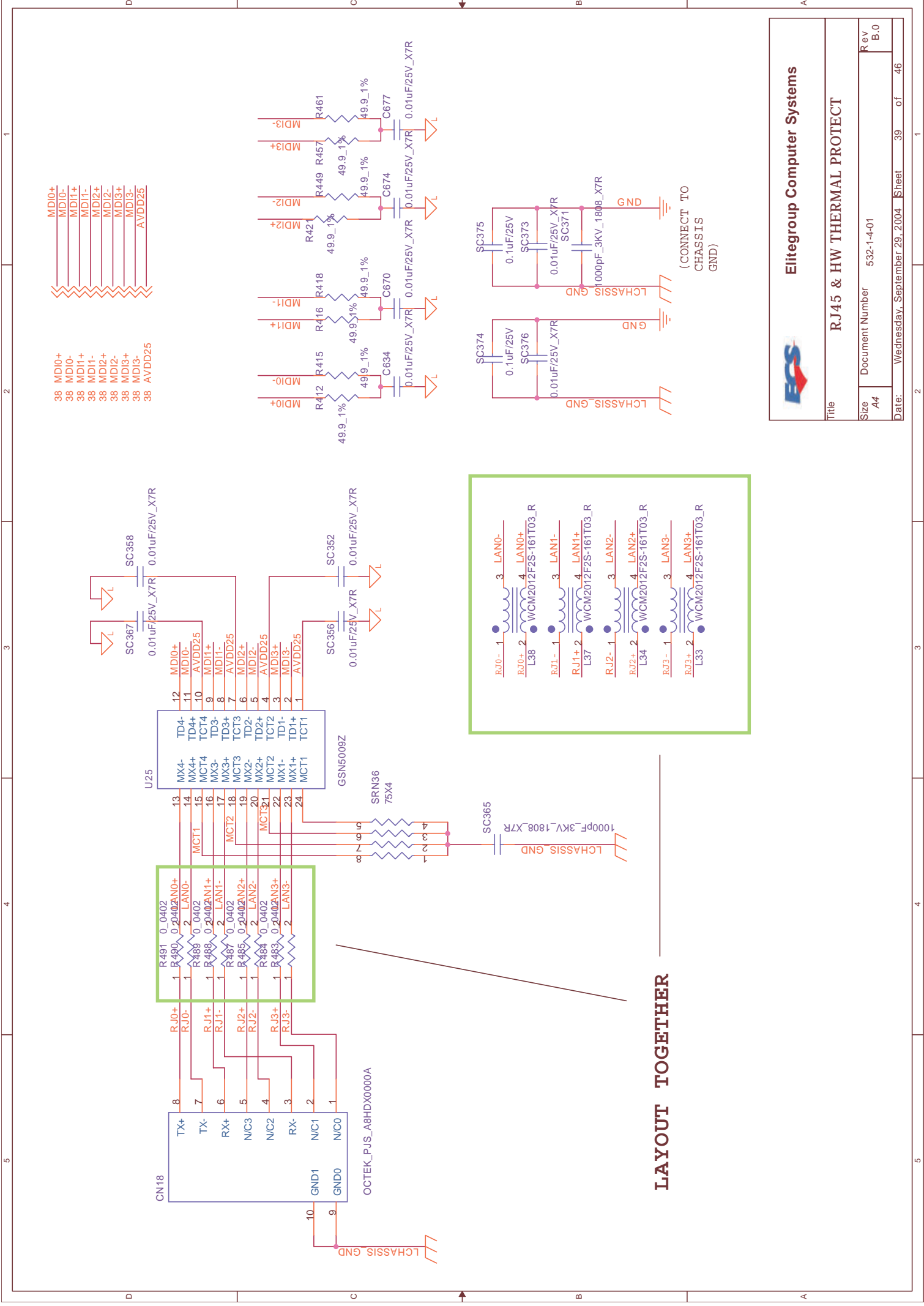
28.38 AD[0..31] << <<
 28.38 C/BE[0..31] << <<

NOT SUPPORT
 WLAN SUS.
 CONTROL



dt_91-00107-018_mdcs30p15h

9/20 MODIFY close to MDC bin 17

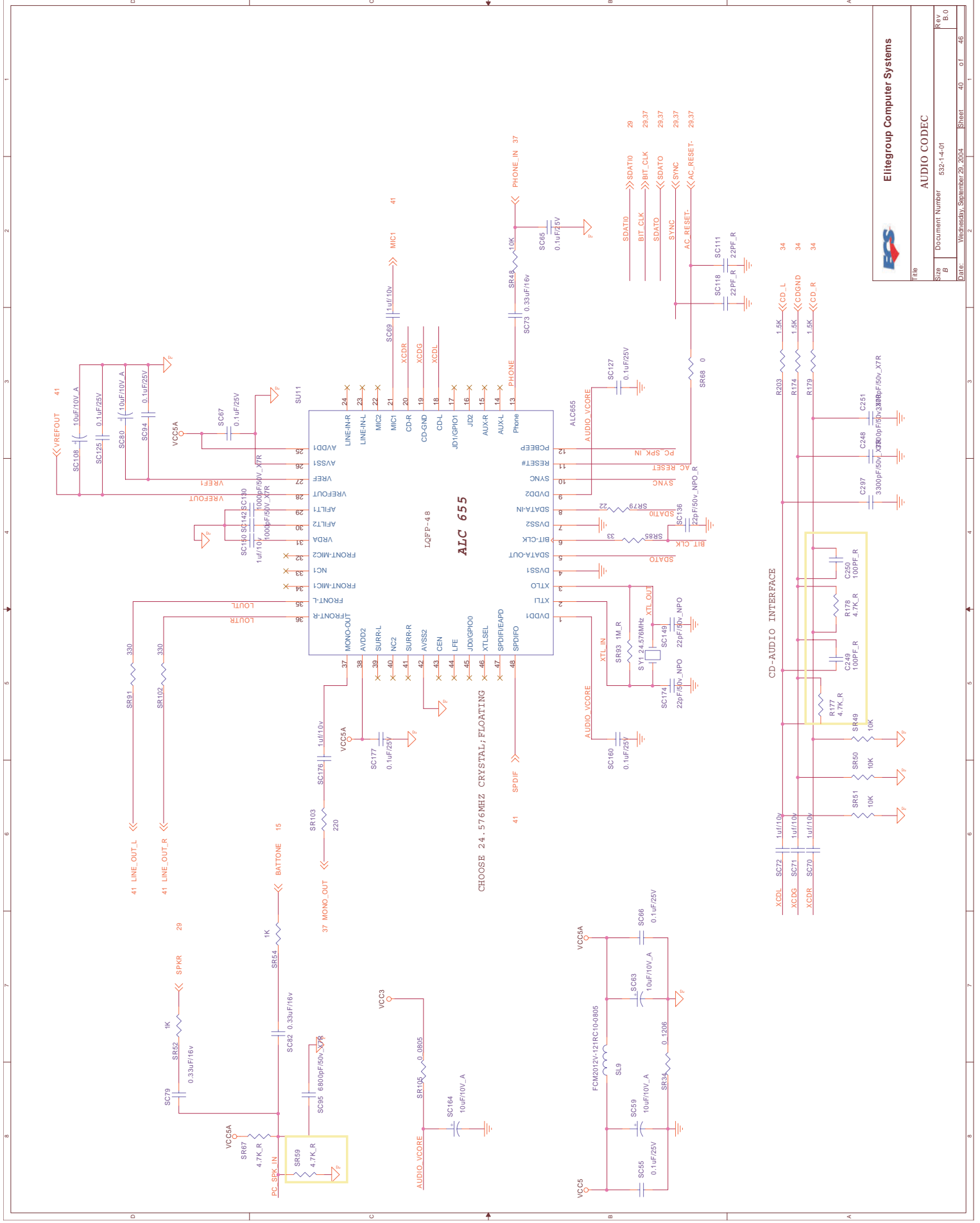


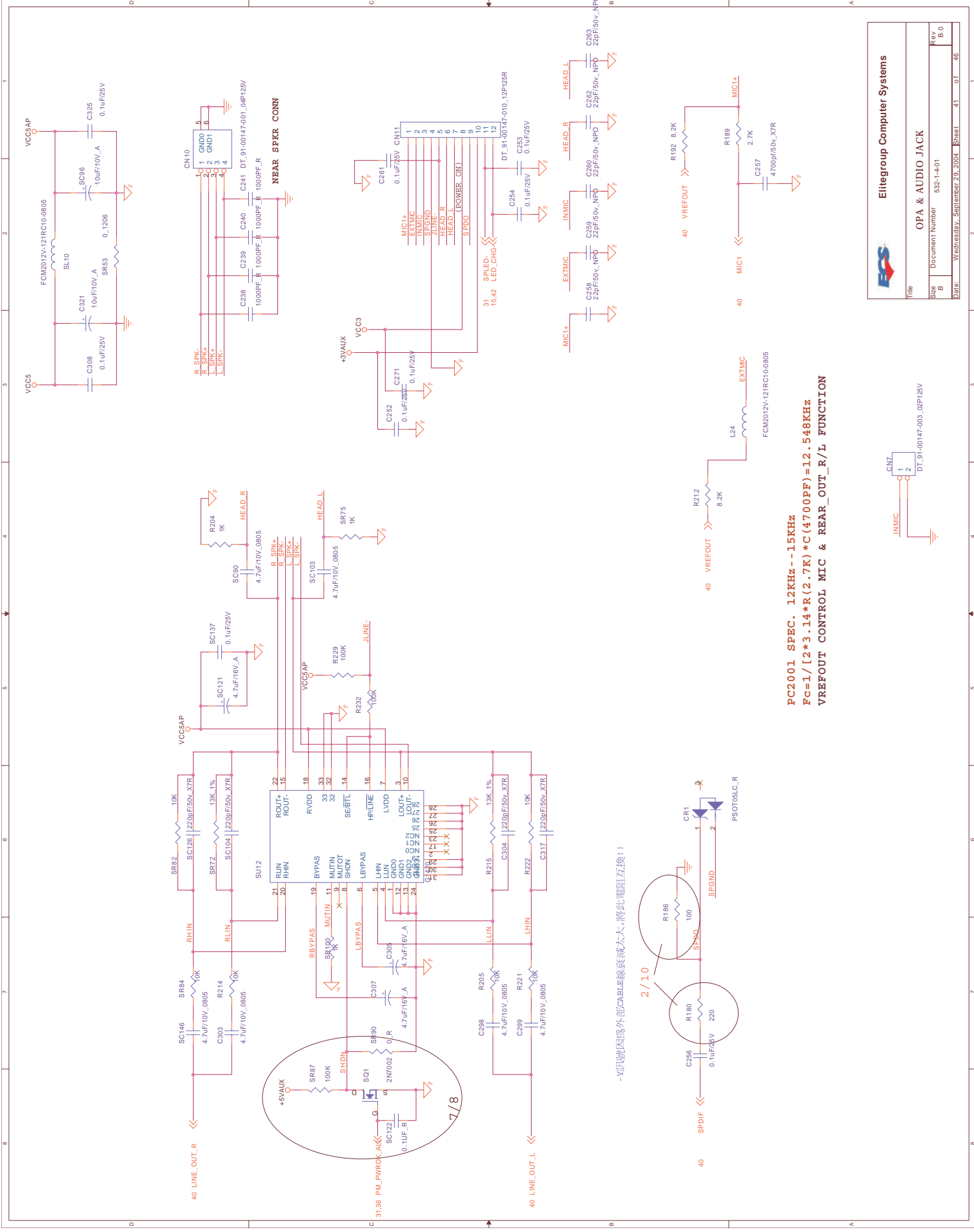
LAYOUT TOGETHER

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RJ45 & HW THERMAL PROTECT

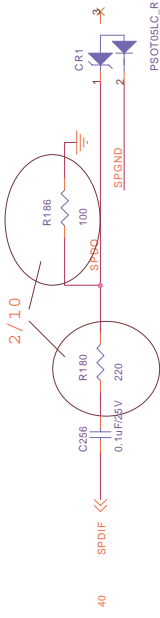
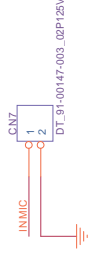
Title		Document Number		Rev	
A4		532-1-4-01		B.0	
Date:	Wednesday, September 29, 2004	Sheet	39	of	46



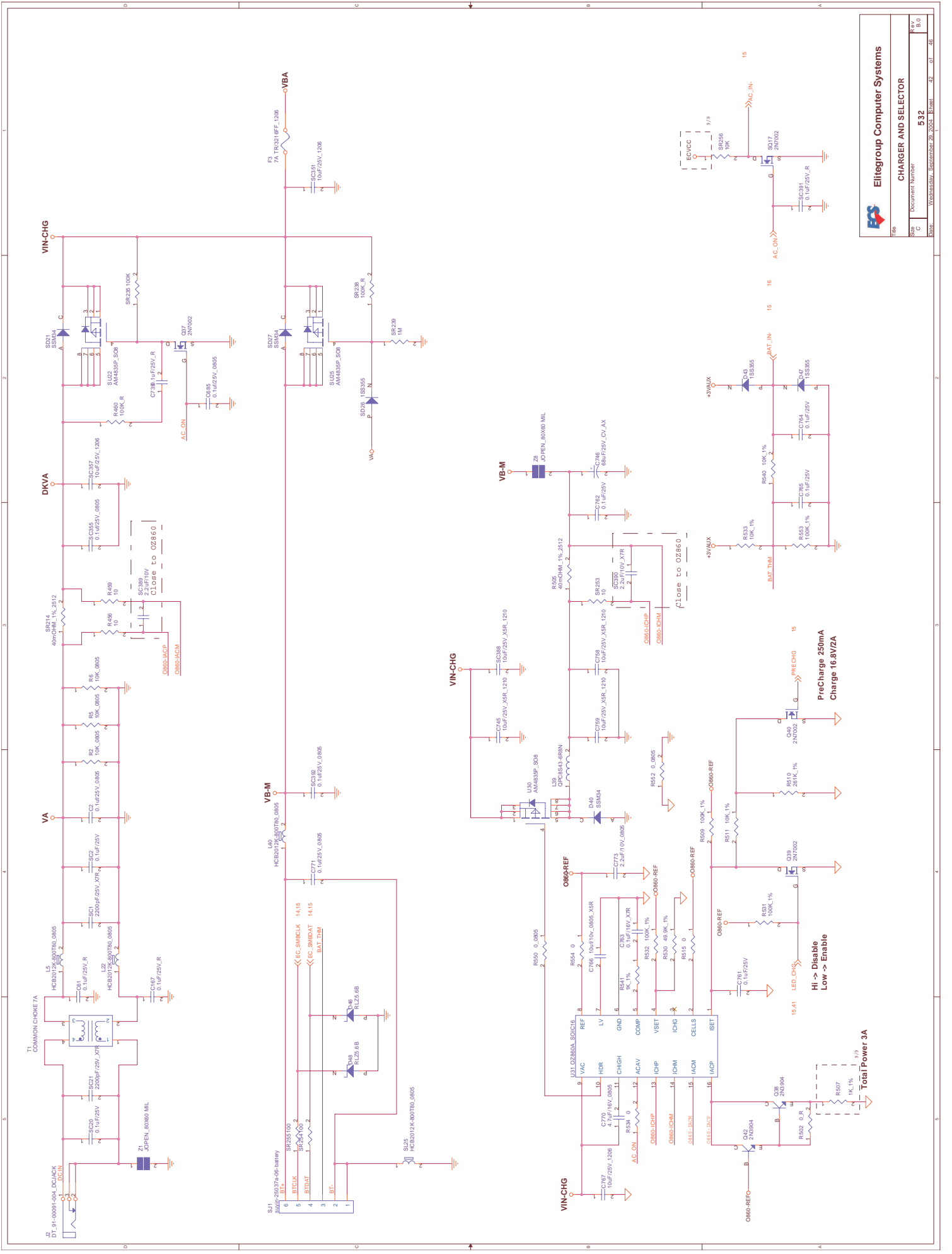


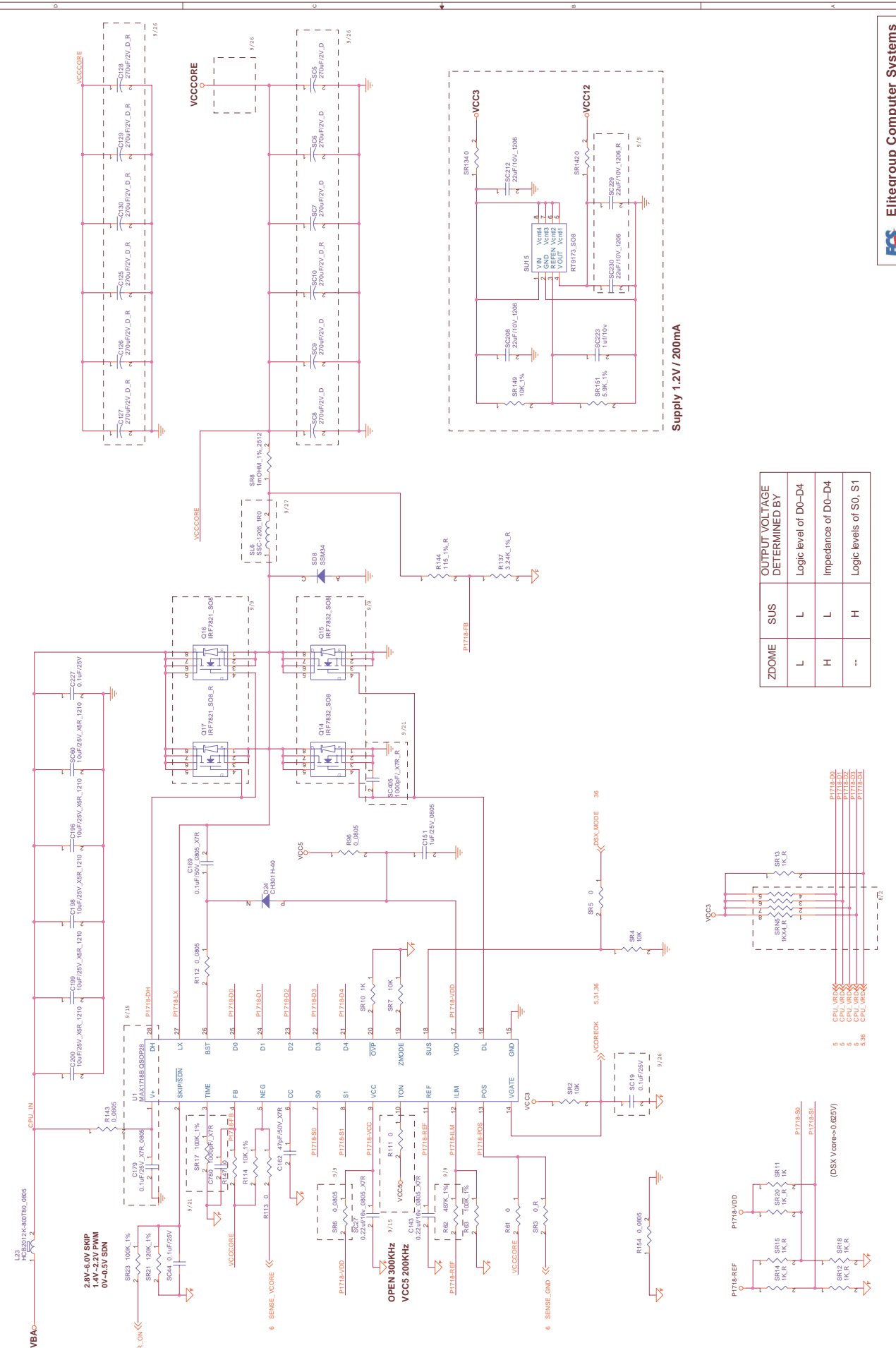
PC2001 SPEC. 12KHZ -- 15KHZ
 $F_c = 1 / [2 * 3.14 * R * (2.7K) * C] (4700PF) = 12.548KHZ$
VREFOUT CONTROL MIC & REAR_OUT_R/L FUNCTION

Elitegroup Computer Systems	
Title OPA & AUDIO JACK	
Size	Document Number 532-1-4-01
B	Rev B.0
Date: Wednesday, September 29, 2004	Sheet 41 of 46

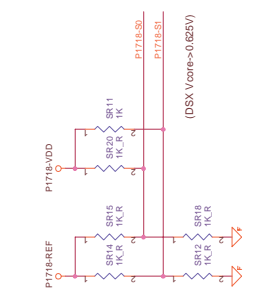
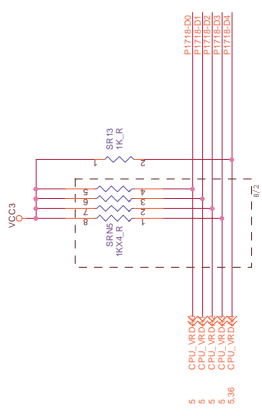


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ZDOME	SUS	OUTPUT VOLTAGE DETERMINED BY
L	L	Logic level of D0-D4
H	L	Impedance of D0-D4
..	H	Logic levels of S0, S1



Supply 1.2V / 200mA

