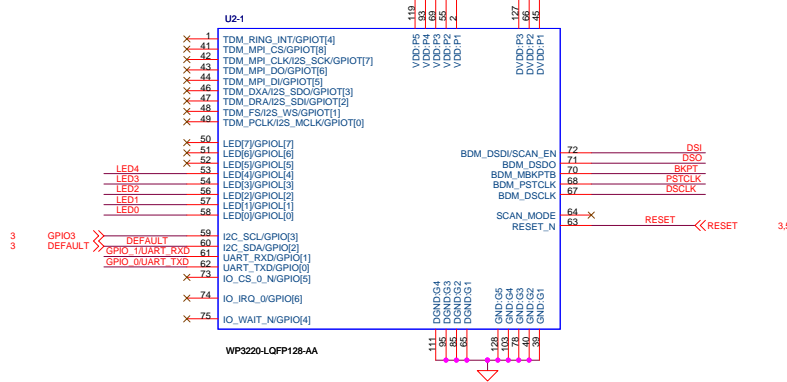
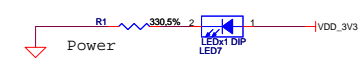
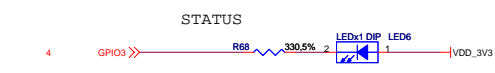
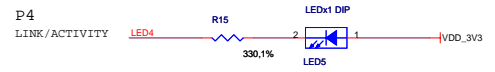
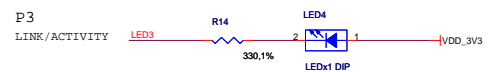
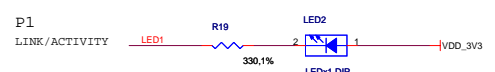
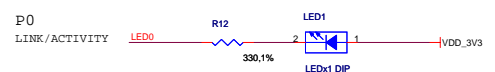


LINK/ACTIVITY:
 ON: LINK
 OFF: UNLINK
 BLINKING: ACTIVITY

SPEED:
 ON: 100M
 OFF: 10M

DUPLEX/COL:
 ON: FULL DUPLEX
 OFF: HALF DUPLEX
 BLINKING: COLLISION



TP1: GPIO UART RXD
 TP2: GPIO UART TXD

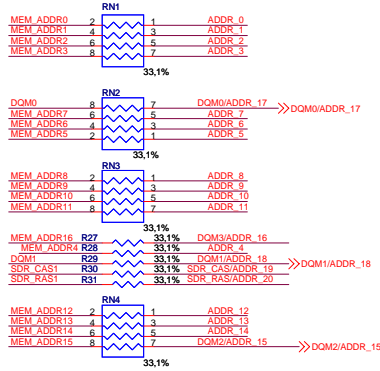
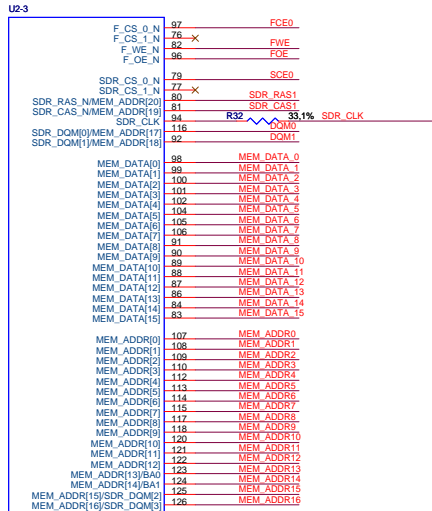
7 ADDR_0[14] << <<

DOM2/ADDR_15 << <<

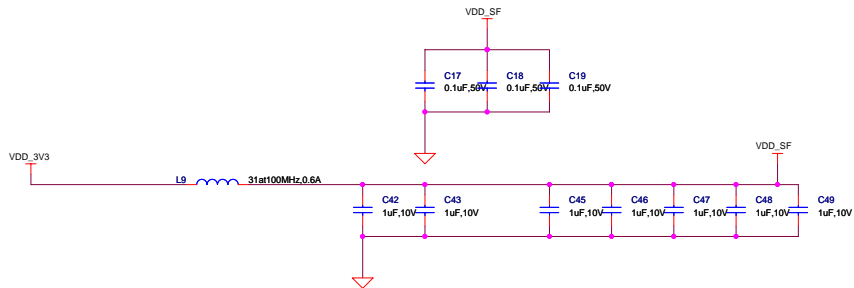
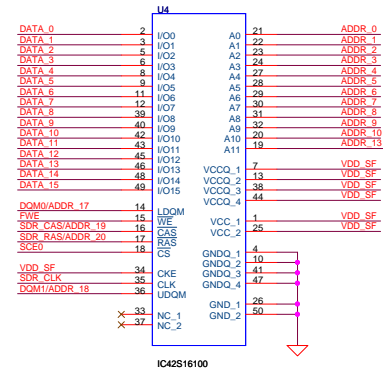
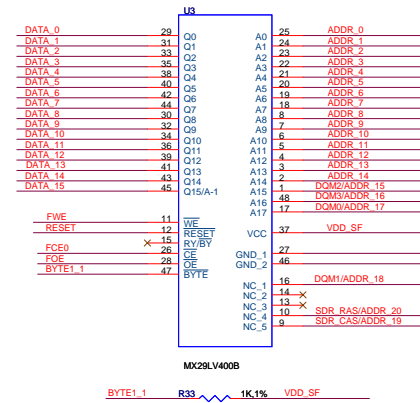
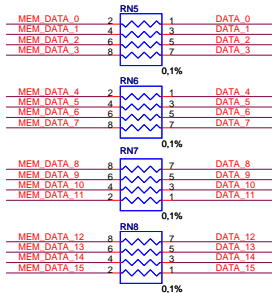
DOM0/ADDR_17 << << DOM0/ADDR_17

DOM1/ADDR_18 << << DOM1/ADDR_18

3.4 RESET >> >> RESET



Near the U1

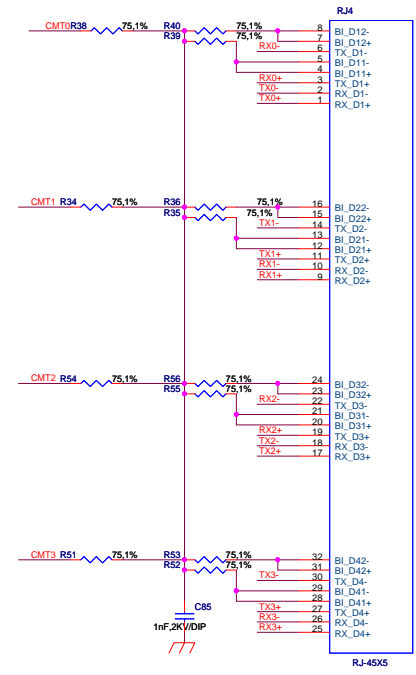
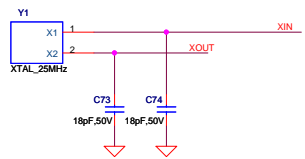
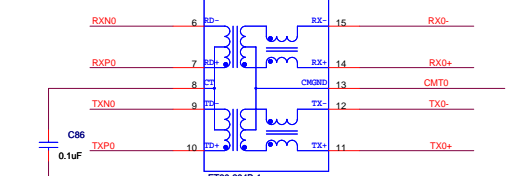
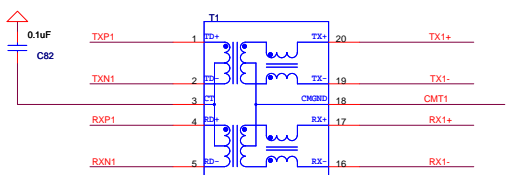
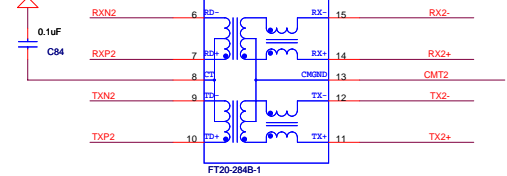
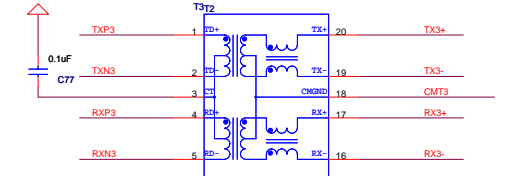
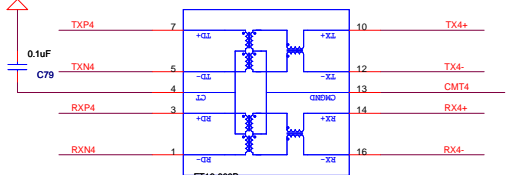
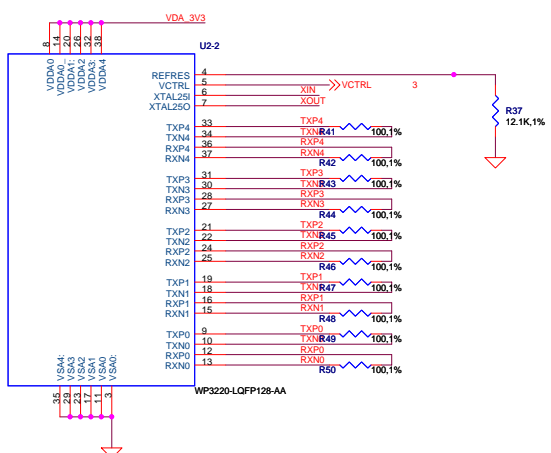
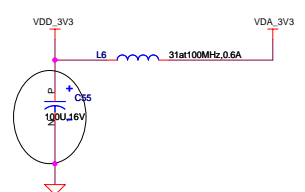
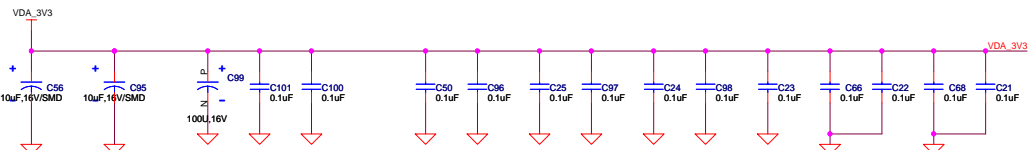


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 6F, No.18, Prosperity Road II, Science-Based Industrial Park,
 Hsinchu 300, Taiwan, R.O.C.
 Designer: Y.S.Liao

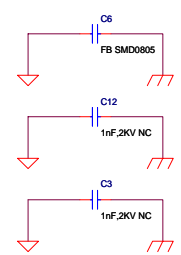
Title: 5 PORT Router Demo BOARD "Flash & SDRAM"

Size: C Document Number: SCH-051202-01 WP3221 AC DMB Rev: 0.4

Date: Tuesday, September 18, 2006 Sheet: 5 of 7

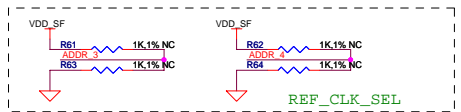
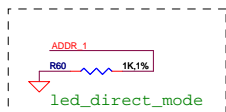


WAN port

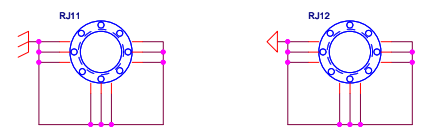


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 Hsinchu 300, Taiwan, R.O.C.
 Designer: Y.S.Liao

Title	5 PORT Router Demo BOARD "Analog & RJ-45"	
Size	Document Number	Rev
C	SCH-051202-01 WP3221 AC DMB	0.4
Date:	Tuesday, September 18, 2006	Sheet 6 of 7



5 ADDR_[0:14] >>



Initial Setting pins:

PIN	Function	Value
ADDR[1]	LED Mode	0: Single LED 1: Matrix Mode
ADDR_[3:4]	Frequency Selection CPU run 175Mhz while R58, R70, R72, R114 DNE	00: 150 MHz 01: 175 MHz (Default)