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		Design ref.:	GS-BT2416C2	File:
		Date:	15-12-05	Rev.: 1
SPG Division - R/D group		Title:	**Block Diagram - System description**	

Simplified Block Diagram :
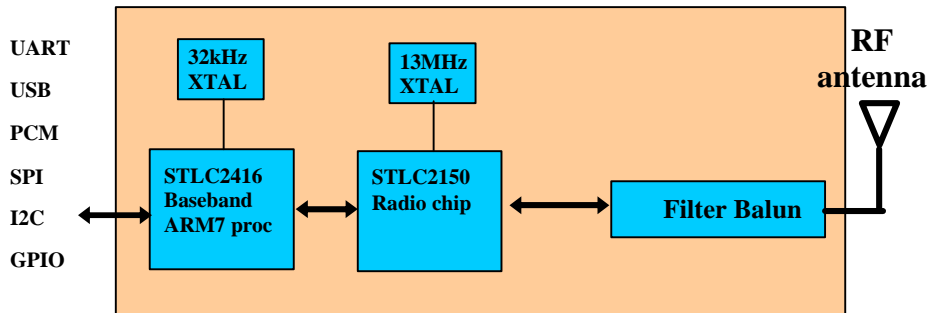
Block Diagram

The module is done by:

- STLC2416 : baseband processor interfacing with the external application by means General purpose   I/O (GPIO) , Uart, USB, PCM, I2C, SPI. The processor interfaces also the RF part of the module exchanging data and commend with it.
  Inside the processor a flash memory is available to download the customer application and the Bluetooth profiles.
  A 32 Khz xtal is used as internal clock

- STLC2150 : RF chip which interfaces the RF channel by means a Filter Balun
   A 13 Mhz Xtal is used as reference and internal clock.

- On module voltage regulators supplying the baseband and rf parts ; the use of internal regulators allows the use of a single 3.3V to supply the module.