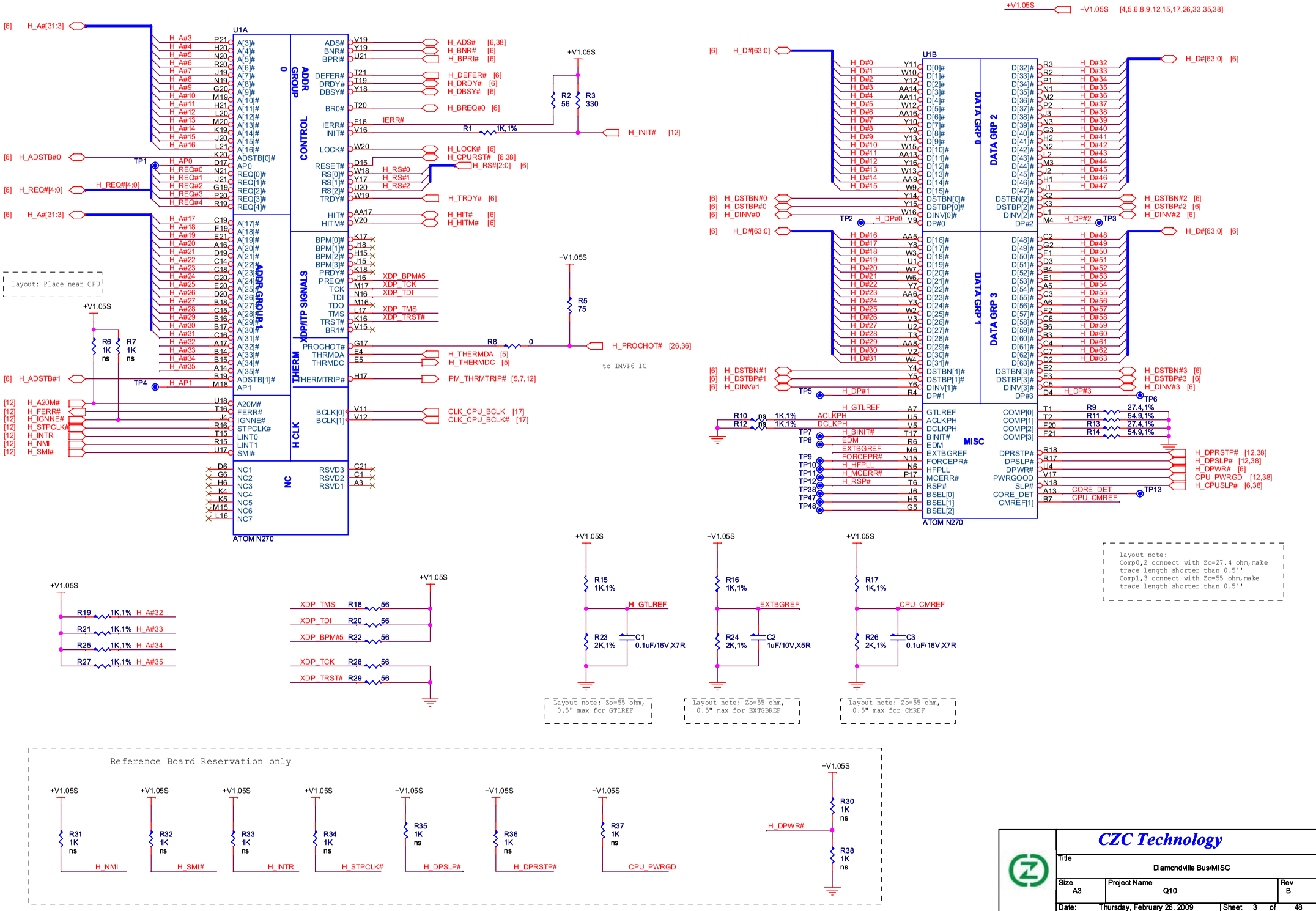
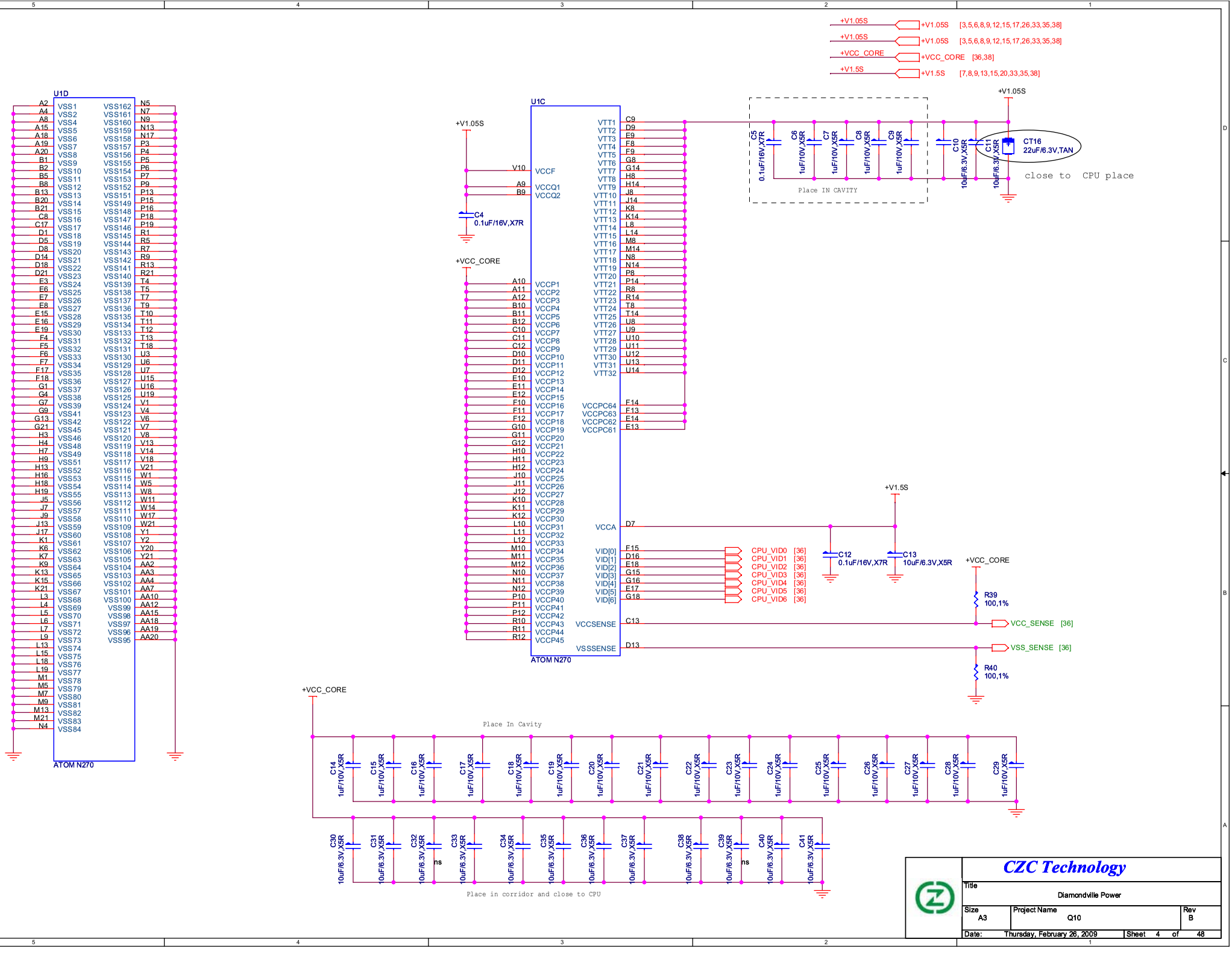
Blank

CZC Technology

Li.wang

Title: Power Block		
Size: A	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 2 of 48	


U1A
ATOM N270
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERM
H CLK
NC
U1B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
ATOM N270
Reference Board Reservation only
CZC Technology
Diamondville Bus/MISC
Size A3
Project Name Q10
Rev B
Date: Thursday, February 26, 2009
Sheet 3 of 48


+V1.05S +V1.05S [3,5,6,8,9,12,15,17,26,33,35,38]
+V1.05S +V1.05S [3,5,6,8,9,12,15,17,26,33,35,38]
+VCC_CORE +VCC_CORE [36,38]
+V1.5S +V1.5S [7,8,9,13,15,20,33,35,38]
U1D
ATOM N270
U1C
ATOM N270
+V1.05S
+VCC_CORE
+V1.5S
C4 0.1uF/16V,X7R
Place IN CAVITY
CT16 22uF/6.3V,TAN
close to CPU place
CPU_VID0 [36]
CPU_VID1 [36]
CPU_VID2 [36]
CPU_VID3 [36]
CPU_VID4 [36]
CPU_VID5 [36]
CPU_VID6 [36]
C12 0.1uF/16V,X7R
C13 10uF/6.3V,X5R
R39 100,1%
R40 100,1%
VCC_SENSE [36]
VSS_SENSE [36]
Place In Cavity
Place in corridor and close to CPU
CZC Technology
Title
Diamondville Power
Size A3
Project Name Q10
Rev B
Date: Thursday, February 26, 2009
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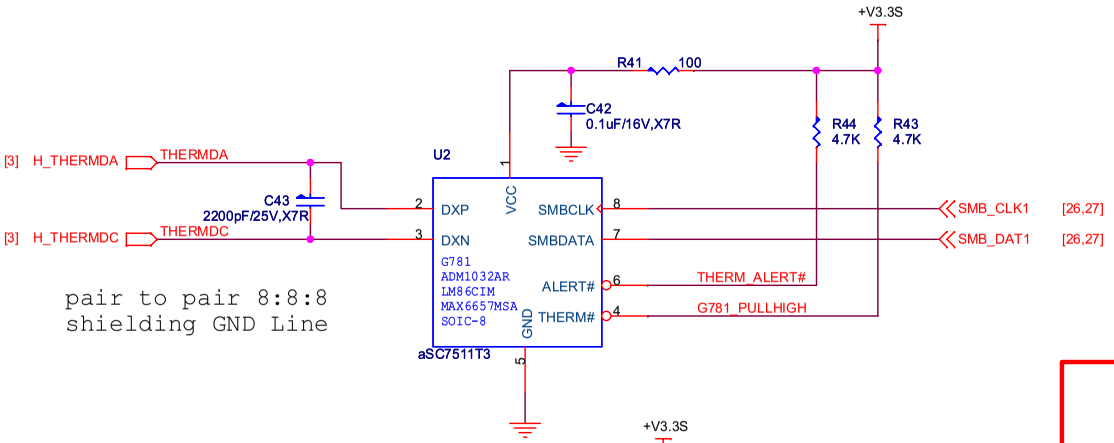
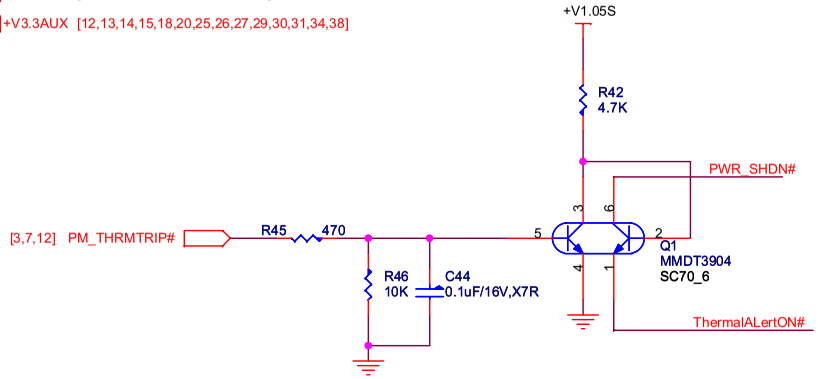
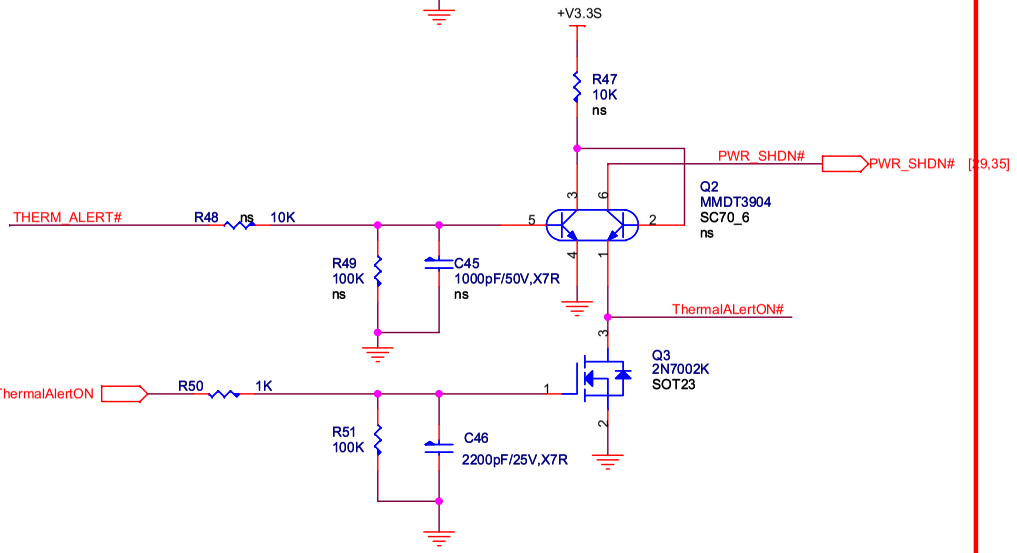
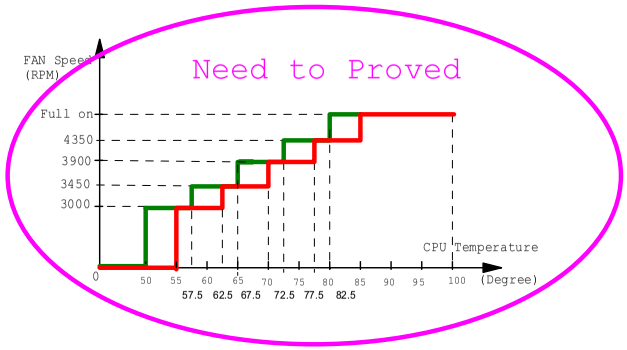
CPU Thermal

+V3.3S +V3.3S [7,8,9,11,12,13,14,15,17,18,20,22,23,25,26,27,28,34,35,36,38]
+V1.05S +V1.05S [3,4,6,8,9,12,15,17,26,33,35,38]
+V3.3AUX +V3.3AUX [12,13,14,15,18,20,25,26,27,29,30,31,34,38]



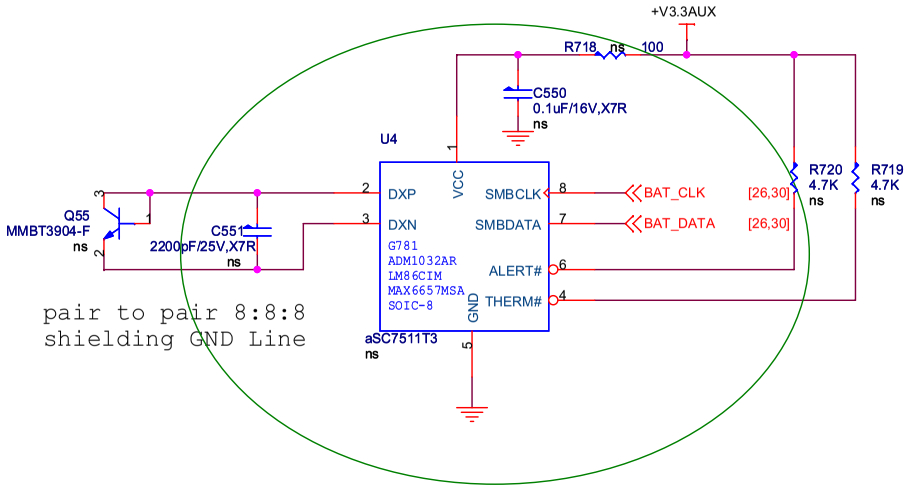






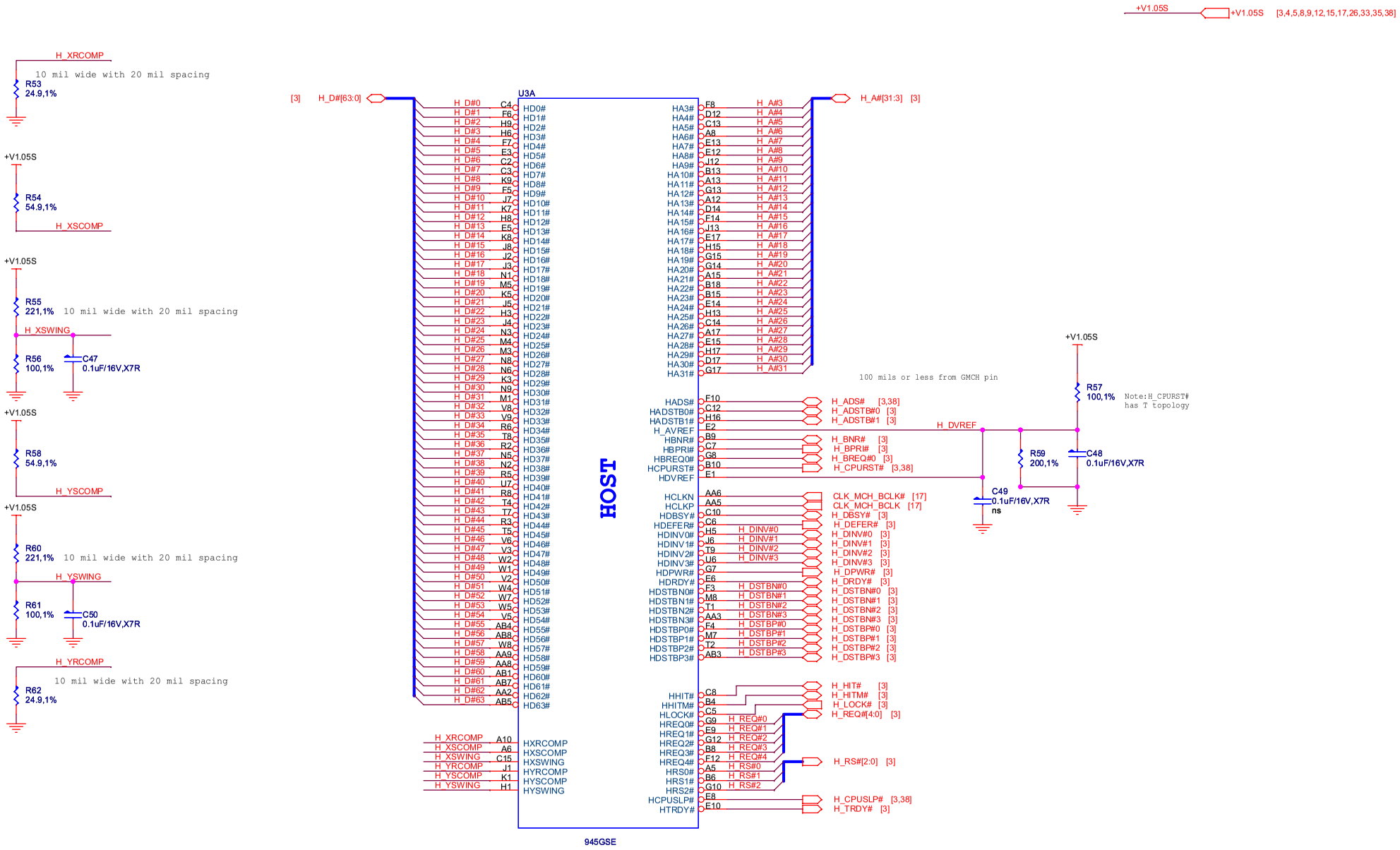
System Thermal

Note: Need be placed near the area of the highest temp



CZC Technology

Title	CPU THERMAL SENSOR	
Size: Custom	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 5 of 48	



CZC Technology		
Title	945GSE FSB	
Size A3	Project Name Q10	Rev B
Date: Thursday, February 26, 2009	Sheet 6 of 48	

MCH_CFG_3	Reserve
MCH_CFG_6	Reserve
MCH_CFG_5	Low=DMIx2 Defalt High=DMIx4

+V1.5S_PCIE [9]
+V1.5S [4,8,9,13,15,20,33,35,38]
+V3.3S [5,8,9,11,12,13,14,15,17,18,20,22,23,25,26,27,28,34,35,36,38]
+V1.8 [9,11,32]

U3B

DMI_TXN0 Y29
DMI_TXN1 Y32
DMI_TXP0 Y28
DMI_TXP1 Y31
DMI_RXN0 V28
DMI_RXN1 V31
DMI_RXP0 V29
DMI_RXP1 V32

SM_CK0 AF33
SM_CK1 AG1
SM_CK2 AJ1
SM_CK3 AM30
SM_CK0# AG33
SM_CK1# AE1
SM_CK2# AK1
SM_CK3# AN30
SM_CKE0 AN21
SM_CKE1 AN22
SM_CKE2 AF26
SM_CKE3 AF25
SM_CS0# AG14
SM_CS1# AF12
SM_CS2# AK14
SM_CS3# AH12
SMOCDCOMP0 AJ21
SMOCDCOMP1 AF11
SM_ODT0 AE12
SM_ODT1 AF14
SM_ODT2 AJ14
SM_ODT3 AJ12
SMRCOMPN AN12
SMRCOMPP AN14
SMVREF0 AA33
SMVREF1 AE1

DMI
DDR2 MUXING
CFG/RSVD
PM
CLK

CFG0 C18
CFG1 E18
CFG2 G20
CFG3 G18
CFG5 J20
CFG6 J18
MCH_RSVD1 K32
MCH_RSVD2 K31
MCH_RSVD7 C17
MCH_RSVD8 F18
MCH_RSVD9 A3

ICHSYNC# E31
BM_BUSY# G21
EXT_TS0# F26
EXT_TS1#/DPRSLPVR H26
THRMTRIP# J15
PWROK AB29
RSTIN# W27

DREF_CLKN A27
DREF_CLKP A26
DREF_SSCLKN J33
DREF_SSCLKP H33
CLKREQB J22

945GSE

[13] DMI_TXN0
[13] DMI_TXN1
[13] DMI_TXP0
[13] DMI_TXP1
[13] DMI_RXN0
[13] DMI_RXN1
[13] DMI_RXP0
[13] DMI_RXP1

[11] M_CLK_DDR0
[11] M_CLK_DDR1
[11] M_CLK_DDR0#
[11] M_CLK_DDR1#
[11] M_CKE0
[11] M_CKE1
[11] M_CS#0
[11] M_CS#1
[11] M_ODT0
[11] M_ODT1

M_RCOMP#
M_RCOMP

+V1.8
R77 10K,1%
M_VREF_MCH
R78 10K,1%
C51 1uF/10V_X5R
C52 0.1uF/16V_X7R
C53 0.1uF/16V_X7R

GMS_CFG5
R65 2.2K ns
R63 2.2K
R66 2.2K ns

MCH_BSEL0 [17]
MCH_BSEL1 [17]
MCH_BSEL2 [17]

R_PM_EXTTS#0 R74 0
PM_EXTTS#1 R75 0
RST_IN#_MCH R76 100

MCH_ICH_SYNC# [13]
PM_BMBUSY# [14]
PM_EXTTS#0 [11]
PM_DPRSLPVR [14,36]
PM_THRMTRIP# [3,5,12]
IMVP_PWROK [14,26,36,38]
PLTRST# [13,14,20,25,26,38]

DREFCLK# [17]
DREFCLK [17]
DREFSSCLK# [17]
DREFSSCLK [17]
MCH_CLKREQ# [17]

U3F

SDVOCTRL_DATA H27
SDVOCTRL_CLK J27
GCLKN Y26
GCLKP AA26

DDCCLK H20
DDCDATA H22
BLUE A24
BLUE# A23
GREEN E25
GREEN# F25
RED C25
RED# D25
VSYNC F27
HSYNC D27
REFSET H25

LBKLT_CTRL H30
LBKLT_EN G29
LCTLA_CLK F28
LCTLB_CLK E28
LDDC_CLK G28
LDDC_DATA H28
LVDD_EN K30
LIBG K27
LVBG J29
LVREFH J30
LVREFL K29

LACLKN D30
LACLKP C30
LBCLKN A30
LBCLKP A29

LADATAN0 G31
LADATAN1 F32
LADATAN2 D31

LADATAP0 H31
LADATAP1 G32
LADATAP2 C31

LBDATAN0 F33
LBDATAN1 D33
LBDATAN2 F30

LBDATAP0 E33
LBDATAP1 D32
LBDATAP2 F29

MISC
VGA
LVDS
SDVO

945GSE

[17] CLK_PCIE_3GPLL#
[17] CLK_PCIE_3GPLL

[23] CRT_DDC_CLK
[23] CRT_DDC_DATA
[23] CRT_BLUE
[23] CRT_GREEN
[23] CRT_RED
[23] CRT_VSYNC
[23] CRT_HSYNC

R70 33
R71 33
CRTREFSET
R72 249,1%

R73 1.5K,1%

[18] L_BKLTCTL
[18] L_BKLTEN
L_CTLA_CLK
L_CTLA_DATA
L_DDC_CLK
L_DDC_DATA
[18] L_VDDEN

[18] LA_CLKN
[18] LA_CLKP

[18] LA_DATAN0
[18] LA_DATAN1
[18] LA_DATAN2

[18] LA_DATAP0
[18] LA_DATAP1
[18] LA_DATAP2

EXP_COMPI R28
EXP_ICOMPO M28
PEG_COMP R64 24.9,1%

SDVO_TVCLKIN# N30
SDVO_INT# R30
SDVO_FLDSTALL# T29

SDVO_TVCLKIN M30
SDVO_INT P30
SDVO_FLDSTALL T30

SDVOB_RED# P28
SDVOB_GREEN# N32
SDVOB_BLUE# P32
SDVOB_CLKN T32

SDVOB_RED N28
SDVOB_GREEN M32
SDVOB_BLUE P33
SDVOB_CLKP R32

TV

TVDAC_A A21
TVDAC_B C20
TVDAC_C E20
TV_REFSET G23
TV_IRTNA B21
TV_IRTNB C21
TV_IRTNC D21

TV_DCONSEL0 G26
TV_DCONSEL1 J26

+V1.5S_PCIE
+V1.5S

R67 150,1% CRT_BLUE
R68 150,1% CRT_GREEN
R69 150,1% CRT_RED

+V1.8
R79 80.6,1%
M_RCOMP#
M_RCOMP
R86 80.6,1%

+V3.3S
R80 10K R_PM_EXTTS#0
R82 10K ns PM_EXTTS#1
R84 10K MCH_CLKREQ#

+V3.3S
R81 10K L_CTLA_CLK
R83 10K L_CTLA_DATA
R85 10K L_DDC_CLK
R87 10K L_DDC_DATA

CZC Technology

Title	945GSE DMI/MISC/VGA/LVDS	
Size A3	Project Name Q10	Rev B
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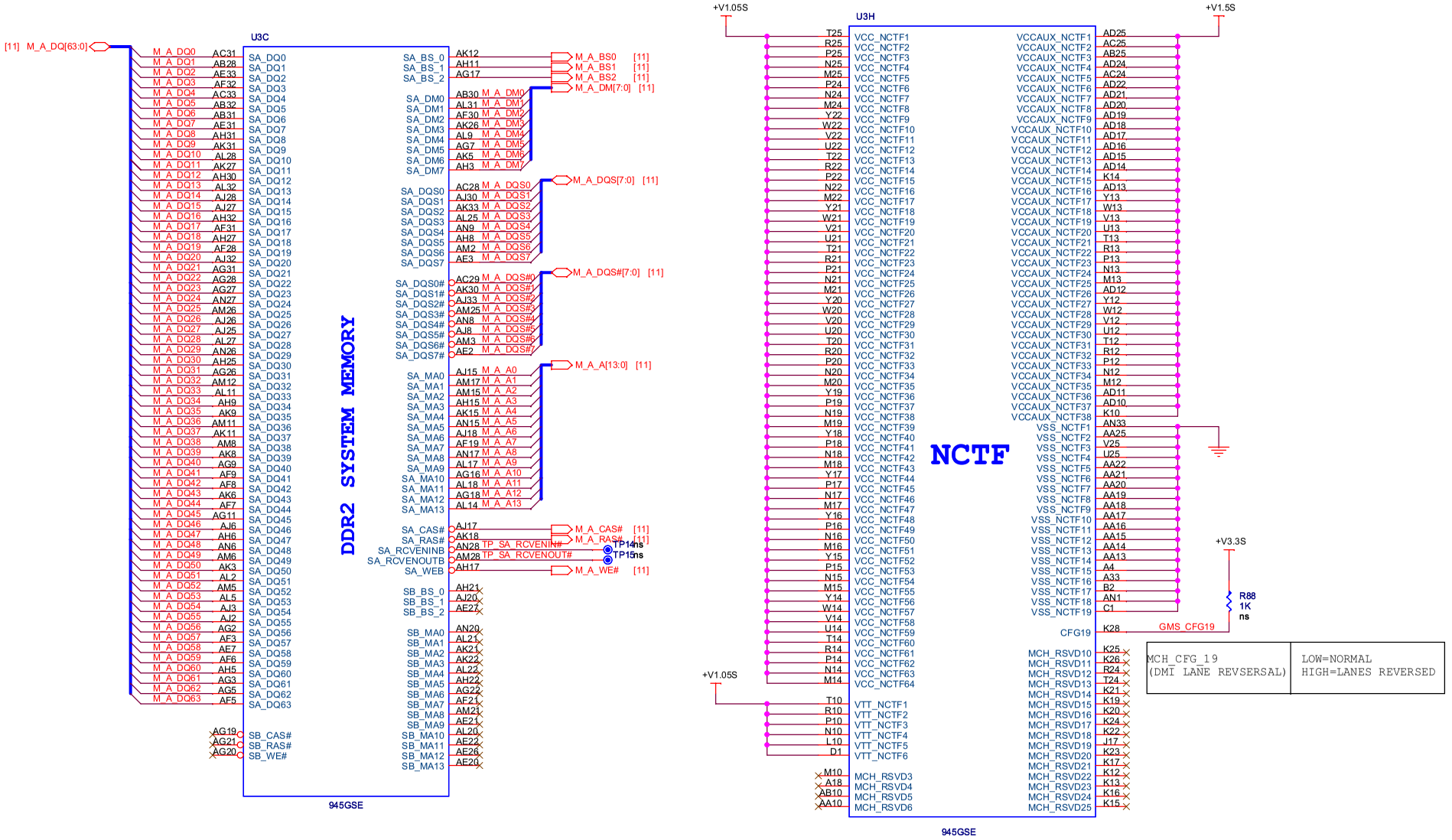
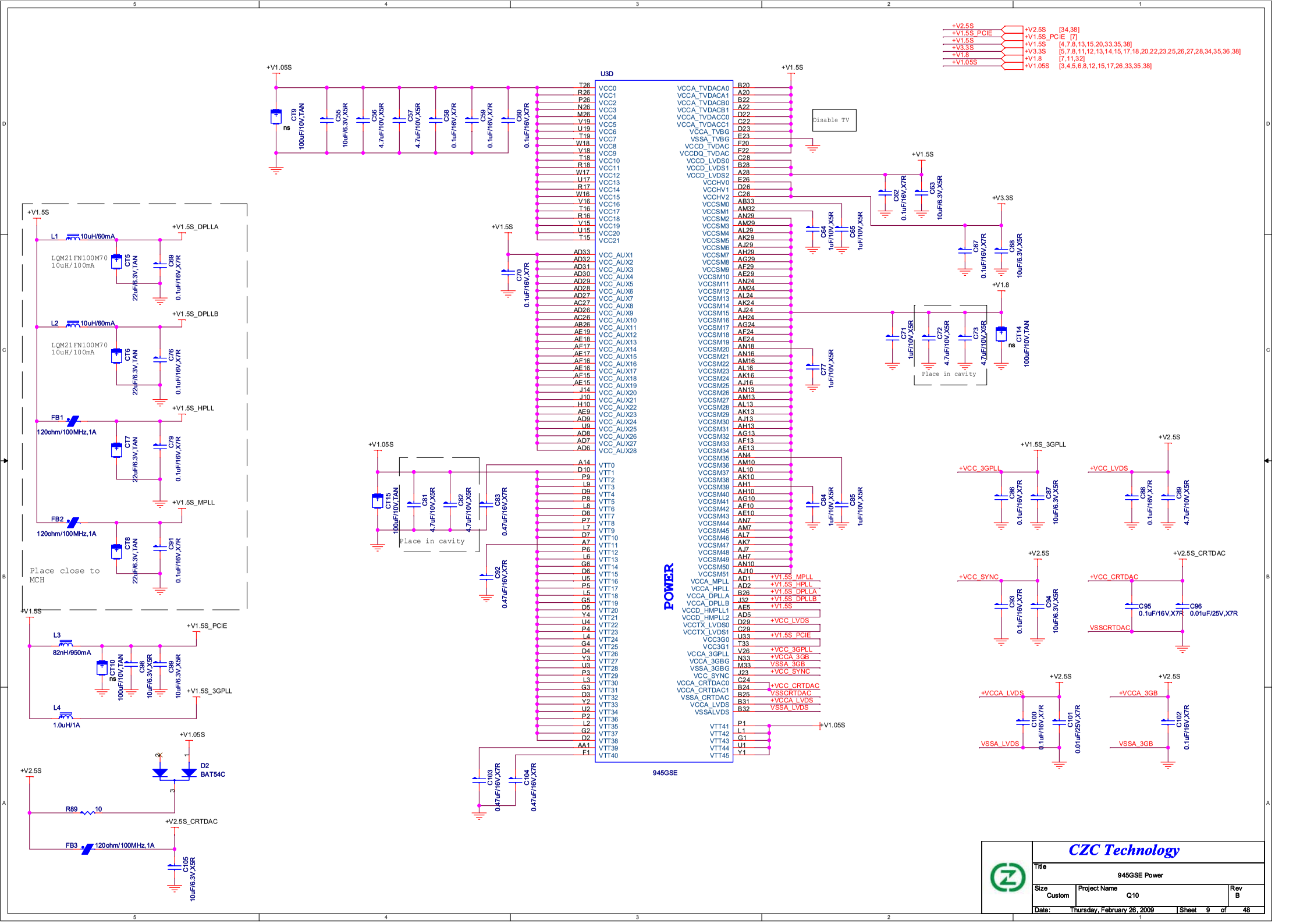
+V1.05S
+V1.5S
+V3.3S

+V1.05S [3,4,5,6,9,12,15,17,26,33,35,38]
+V1.5S [4,7,9,13,15,20,33,35,38]
+V3.3S [5,7,9,11,12,13,14,15,17,18,20,22,23,25,26,27,28,34,35,36,38]



Title	945GSE DDRII	
Size: A3	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 8 of 48	

CZC Technology


+V2.5S [34,38]
+V1.5S_PCIE [7]
+V1.5S [4,7,8,13,15,20,33,35,38]
+V3.3S [5,7,8,11,12,13,14,15,17,18,20,22,23,25,26,27,28,34,35,36,38]
+V1.8 [7,11,32]
+V1.05S [3,4,5,6,8,12,15,17,26,33,35,38]
U3D
945GSE
POWER
Disable TV
Place in cavity
Place close to MCH
LQM21FN100M70 10uH/100mA
120ohm/100MHz,1A
82nH/950mA
1.0uH/1A
BAT54C
CZC Technology
945GSE Power
Custom
Q10
B
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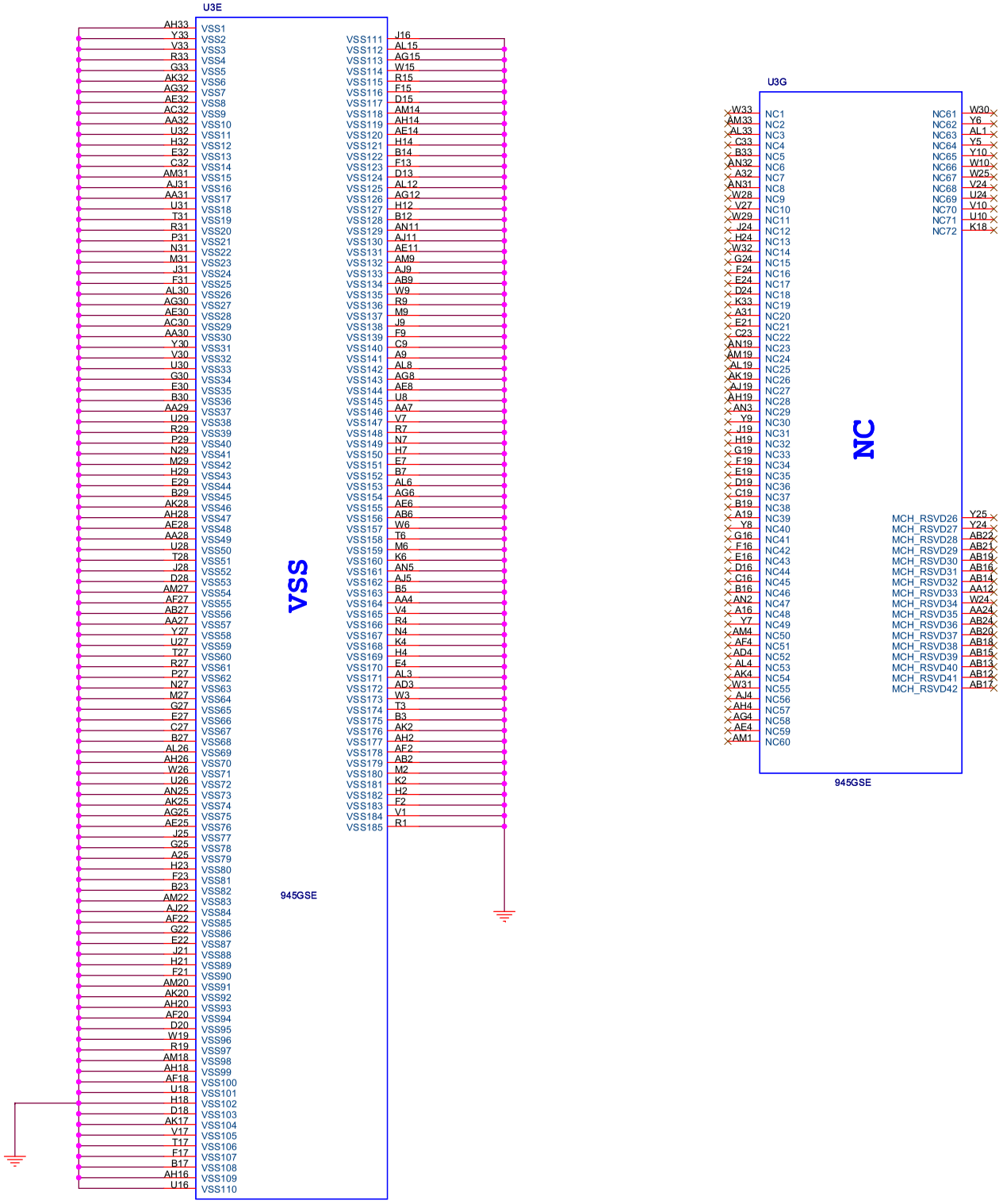
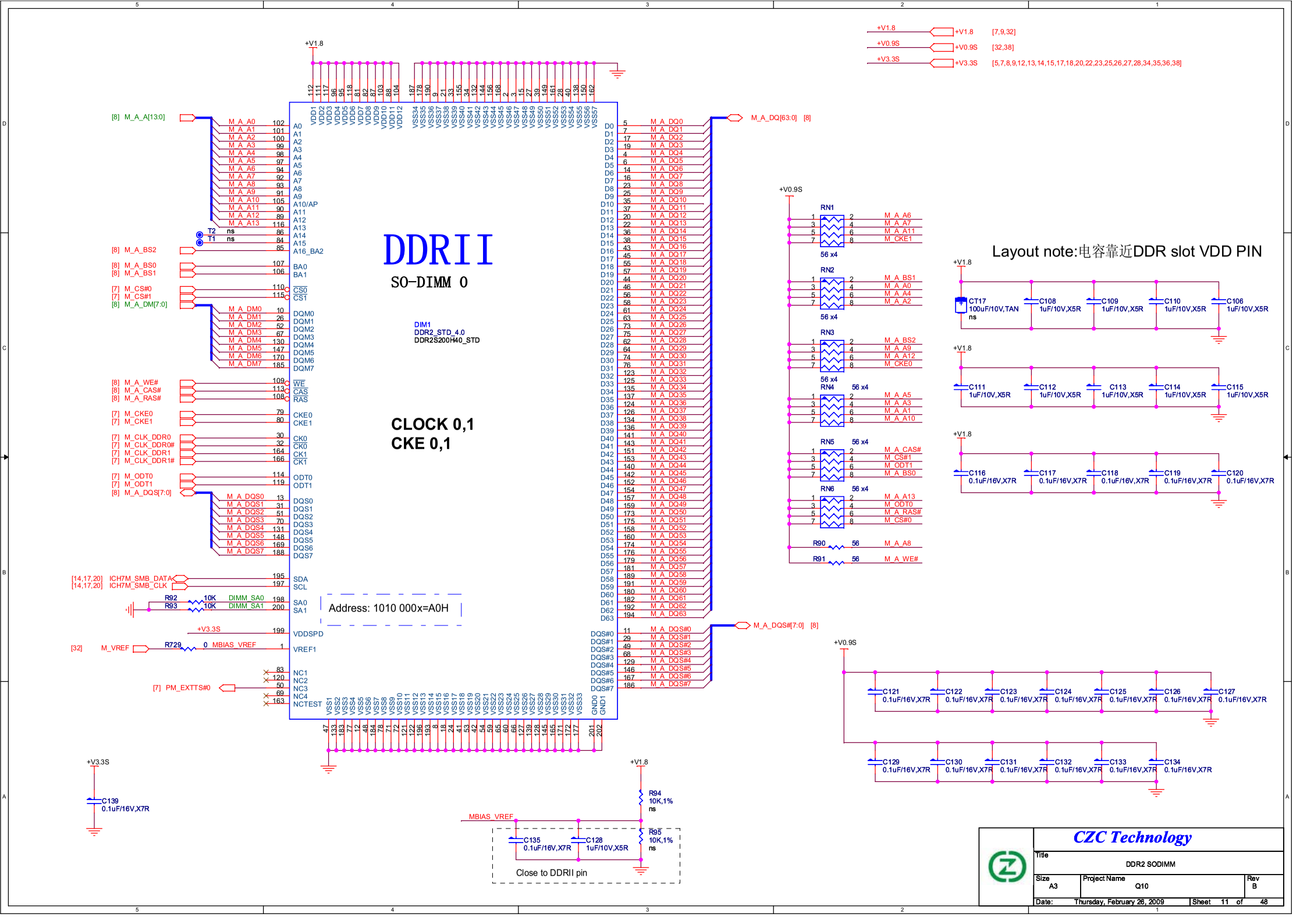


CZC Technology

Title: 945GSE GND		
Size: A3	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 10 of 48	


+V1.8 [7,9,32]
+V0.9S [32,38]
+V3.3S [5,7,8,9,12,13,14,15,17,18,20,22,23,25,26,27,28,34,35,36,38]
DDRII
SO-DIMM 0
DIM1
DDR2_STD_4.0
DDR2S200H40_STD
CLOCK 0,1
CKE 0,1
Address: 1010 000x=A0H
Layout note:电容靠近DDR slot VDD PIN
Close to DDRII pin
M_A_DQ[63:0] [8]
M_A_DQS#[7:0] [8]
[8] M_A_A[13:0]
[8] M_A_BS2
[8] M_A_BS0
[8] M_A_BS1
[7] M_CS#0
[7] M_CS#1
[8] M_A_DM[7:0]
[8] M_A_WE#
[8] M_A_CAS#
[8] M_A_RAS#
[7] M_CKE0
[7] M_CKE1
[7] M_CLK_DDR0
[7] M_CLK_DDR0#
[7] M_CLK_DDR1
[7] M_CLK_DDR1#
[7] M_ODT0
[7] M_ODT1
[8] M_A_DQS[7:0]
[14,17,20] ICH7M_SMB_DATA
[14,17,20] ICH7M_SMB_CLK
R92 10K DIMM_SA0
R93 10K DIMM_SA1
+V3.3S
[32] M_VREF
R729 0 MBIAS_VREF
[7] PM_EXTTS#0
RN1 56 x4
RN2 56 x4
RN3 56 x4
RN4 56 x4
RN5 56 x4
RN6 56 x4
R90 56 M_A_A8
R91 56 M_A_WE#
C139 0.1uF/16V,X7R
R94 10K,1% ns
R95 10K,1% ns
C135 0.1uF/16V,X7R
C128 1uF/10V,X5R
CZC Technology
Title DDR2 SODIMM
Size A3
Project Name Q10
Rev B
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+V1.05S [3,4,5,6,8,9,15,17,26,33,35,38]
+V3.3S [5,7,8,9,11,13,14,15,17,18,20,22,23,25,26,27,28,34,35,36,38]
+V3.3A_RTC [15]
+V3.3AUX [5,13,14,15,18,20,25,26,27,29,30,31,34,38]

U5A

RTC_X1 AB1 RTCX1
RTC_X2 AB2 RTCX2
RTC_RST# AA3 RTCRST#
SM_INTRUDER# Y5 INTRUDER#
ICH_INTVRMEN W4 INTVRMEN
RTC

W1 EE_CS
Y1 EE_SHCLK
Y2 EE_DOUT
W3 EE_DIN

V3 LAN_CLK
U3 LAN_RSTSYNC
U5 LAN_RXD0
V4 LAN_RXD1
T5 LAN_RXD2
U7 LAN_TXD0
V6 LAN_TXD1
V7 LAN_TXD2
LAN

C410 10pF/50V,NPO ns

[22] HDA_BITCLK R101 33 ACZ_BITCLK_R U1 ACZ_BIT_CLK
[22] HDA_SYNC R102 33 ACZ_SYNC_R R6 ACZ_SYNC
[22] HDA_RST# R103 33 ACZ_RST#_R R5 ACZ_RST#
[22] HDA_SDATAIN0 T2 ACZ_SDIN0
T3 ACZ_SDIN1
T1 ACZ_SDIN2
[22] HDA_SDATAOUT R105 33 ACZ_SDATAOUT_R T4 ACZ_SDOUT
[27] SATA_LED# SATA_LED#_R AF18 SATALED#
AC-97/AZALIA

[19] SATA_RXN0 AF3 SATA0RXN
[19] SATA_RXP0 AE3 SATA0RXP
[19] SATA_TXN0 C142 3900pF/50V,X7R SATA_TXN0_C AG2 SATA0TXN
[19] SATA_TXP0 C143 3900pF/50V,X7R SATA_TXP0_C AH2 SATA0TXP

[19] SATA_RXN1 AF7 SATA2RXN
[19] SATA_RXP1 AE7 SATA2RXP
[19] SATA_TXN1 C233 3900pF/50V,X7R SATA_TXN1_C AG6 SATA2TXN
[19] SATA_TXP1 C234 3900pF/50V,X7R SATA_TXP1_C AH6 SATA2TXP

[17] CLK_PCIE_SATA# AF1 SATA_CLKN
[17] CLK_PCIE_SATA AE1 SATA_CLKP

Short pins AH10 and AG10 at the package. Place R within 500mils of ICH7 ball

R108 24.9,1% SATA_RBIAS_PN AH10 SATARBIASN
AG10 SATARBIASP
SATA

AE15 DIOR#
AH15 DIOW#
AF16 DDACK#
IDEREQ AH16 IDEIRQ
IORDY AG16 IORDY
AE15 DDREQ
IDE

NH82801GBM

LAD0 AA6 LPC_AD0 LPC_AD0 [26,27,38]
LAD1 AB5 LPC_AD1 LPC_AD1 [26,27,38]
LAD2 AC4 LPC_AD2 LPC_AD2 [26,27,38]
LAD3 Y6 LPC_AD3 LPC_AD3 [26,27,38]
LDRQ0# AC3 LDRQ0#
LDRQ1#/GPIO23 AA5 LDRQ1#
LFRAME# AB3 LPC_FRAME# [26,27,38]
LPC

A20GATE AE22 CPU_A20GATE- CPU_A20GATE- [26]
A20M# AH28 H_A20M# [3]
CPUSLP# AG27
TP1/DPRSTP# AF24 H_DPRSTP# R_R98 0 H_DPRSTP# [3,38]
TP2/DPSLP# AH25 H_DPSLP# R_R99 0 H_DPSLP# [3,38]
FERR# AG26 H_FERR# H_FERR# [3]
GPIO49/CPUPWRGD AG24 CPU_PWRGD [3,38]
CPU

IGNNE# AG22 H_IGNNE# [3]
INIT3_3V# AG21 FWH_INIT#
INIT# AF22 H_INIT# [3]
INTR AF25 H_INTR [3]
RCIN# AG23 H_RCIN# H_RCIN# [26]
NMI AH24 H_NMI [3]
SMI# AF23 H_SMI#_R R104 0 H_SMI# [3]
STPCLK# AH22 H_STPCLK# [3]
THERMTRIP# AF26 H_THRMTRIP_R R106 24.9,1% PM_THRMTRIP# [3,5,7]

R106 need to place within 2" of ICH7
R104 must be placed within 2" of R129 W/O stub

DD0 AB15
DD1 AE14
DD2 AG13
DD3 AF13
DD4 AD14
DD5 AC13
DD6 AD12
DD7 AC12
DD8 AE12
DD9 AF12
DD10 AB13
DD11 AC14
DD12 AF14
DD13 AH13
DD14 AH14
DD15 AC15

DA0 AH17
DA1 AE17
DA2 AF17

DCS1# AE16
DCS3# AD16

+V3.3A_RTC
R111 332K,1%
ICH_INTVRMEN

+V3.3A_RTC
+V3.3AUX
RTC_RST# R96 20K,1%
C141 1uF/10V,X5R
C140 1uF/10V,X5R
D3 BAT54C SOT23
R97 1M
R100 1K
SM_INTRUDER#
RTCCN1 W-B-2P-R HWS2_1P25R

RTC_RST#
CLRCMOS JOPEN RESISTOR_1 ns
CMOS Settings Clear CMOS Keep CMOS
CLRCMOS: Shunt Open

ACES 85204-02X01

RTC_X1 C144 15pF/50V,NPO
R107 10M
Y1 32.768kHz,10ppm,12.5pF X4S67X15
RTC_X2 C145 15pF/50V,NPO

ICH7 intel VccSus1.05 enable strap

	INTVRMEN		
Enable(default)	1	STUFF	UNSTUFF
Disable	0	UNSTUFF	STUFF

+V1.05S

R110 ns 56 H_DPRSTP#
R112 ns 56 H_DPSLP#
R114 56 H_FERR#
R117 56 PM_THRMTRIP#

R122 ns 1K SATA_RXN1
R121 ns 1K SATA_RXP1

H_DPRSTP# should be routed as "Daisy chain" CMOS topology, routed from ICH to IMVP to CPU in this order exactly

+V3.3S

R113 10K H_RCIN#
R115 10K CPU_A20GATE-
R118 1K ACZ_SDATAOUT_R ns
R119 1K FWH_INIT# ns
R416 10K LDRQ0#
R417 10K LDRQ1#
R562 4.7K IORDY
R430 10K IDEREQ

R118 strap functionality based on ICH_TP3 strap:
XOR chain entrance(ICH_TP3 pulled low)
PCIE port config bit 1(ICH_TP3 not pulled low)

RTCBAT1
RTC Battery with Cable

RTCSPNG1
RTC Battery Sponge

CZC Technology

Title: ICH7M IDE/SATA/LPC/RTC/AUDIO
Size: A3
Project Name: Q10
Rev: B
Date: Thursday, February 26, 2009
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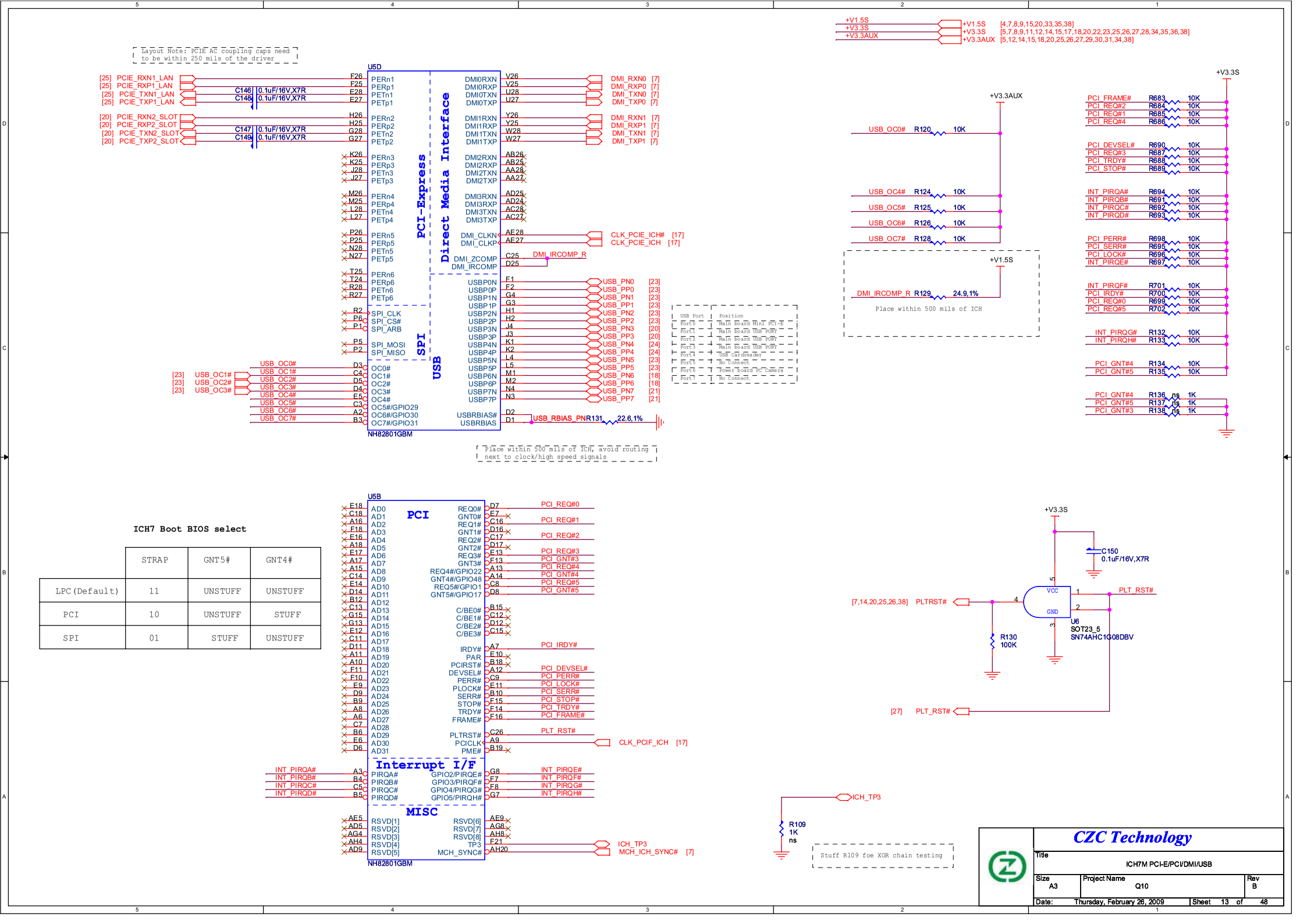
Layout Note: PCIE AC coupling caps need to be within 250 mils of the driver
U5D
PCI-Express
Direct Media Interface
SPI
USB
PERn1
PERp1
PETn1
PETp1
PERn2
PERp2
PETn2
PETp2
PERn3
PERp3
PETn3
PETp3
PERn4
PERp4
PETn4
PETp4
PERn5
PERp5
PETn5
PETp5
PERn6
PERp6
PETn6
PETp6
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
SPI_CLK
SPI_CS#
SPI_ARB
SPI_MOSI
SPI_MISO
OC0#
OC1#
OC2#
OC3#
OC4#
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBRBIAS#
USBRBIAS
NH82801GBM
USB Port
Position
Port0 Main board Mini PCI-E
Port1 Main board USB PORT
Port2 Main board USB PORT
Port3 Main board USB PORT
Port4 USB Cardreader
Port5 No Connect
Port6 Power board PC Camera
Port7 No Connect
Place within 500 mils of ICH, avoid routing next to clock/high speed signals
+V1.5S
+V3.3S
+V3.3AUX
+V1.5S [4,7,8,9,15,20,33,35,38]
+V3.3S [5,7,8,9,11,12,14,15,17,18,20,22,23,25,26,27,28,34,35,36,38]
+V3.3AUX [5,12,14,15,18,20,25,26,27,29,30,31,34,38]
USB_OC0# R120 10K
USB_OC4# R124 10K
USB_OC5# R125 10K
USB_OC6# R126 10K
USB_OC7# R128 10K
DMI_IRCOMP_R R129 24.9,1%
Place within 500 mils of ICH
PCI_FRAME# R683 10K
PCI_REQ#2 R684 10K
PCI_REQ#1 R685 10K
PCI_REQ#4 R686 10K
PCI_DEVSEL# R690 10K
PCI_REQ#3 R687 10K
PCI_TRDY# R688 10K
PCI_STOP# R689 10K
INT_PIRQA# R694 10K
INT_PIRQB# R691 10K
INT_PIRQC# R692 10K
INT_PIRQD# R693 10K
PCI_PERR# R698 10K
PCI_SERR# R695 10K
PCI_LOCK# R696 10K
INT_PIRQE# R697 10K
INT_PIRQF# R701 10K
PCI_IRDY# R700 10K
PCI_REQ#0 R699 10K
PCI_REQ#5 R702 10K
INT_PIRQG# R132 10K
INT_PIRQH# R133 10K
PCI_GNT#4 R134 10K
PCI_GNT#5 R135 10K
PCI_GNT#4 R136 ns 1K
PCI_GNT#5 R137 ns 1K
PCI_GNT#3 R138 ns 1K
ICH7 Boot BIOS select
STRAP
GNT5#
GNT4#
LPC(Default) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
U5B
PCI
REQ0#
GNT0#
REQ1#
GNT1#
REQ2#
GNT2#
REQ3#
GNT3#
REQ4#/GPIO22
GNT4#/GPIO48
REQ5#/GPIO1
GNT5#/GPIO17
C/BE0#
C/BE1#
C/BE2#
C/BE3#
IRDY#
PAR
PCIRST#
DEVSEL#
PERR#
PLOCK#
SERR#
STOP#
TRDY#
FRAME#
PLTRST#
PCICLK
PME#
Interrupt I/F
PIRQA#
PIRQB#
PIRQC#
PIRQD#
GPIO2/PIRQE#
GPIO3/PIRQF#
GPIO4/PIRQG#
GPIO5/PIRQH#
MISC
RSVD[1]
RSVD[2]
RSVD[3]
RSVD[4]
RSVD[5]
RSVD[6]
RSVD[7]
RSVD[8]
TP3
MCH_SYNC#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_GNT#3
PCI_REQ#4
PCI_GNT#4
PCI_REQ#5
PCI_GNT#5
PCI_IRDY#
PCI_DEVSEL#
PCI_PERR#
PCI_LOCK#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
PCI_FRAME#
PLT_RST#
CLK_PCIF_ICH [17]
INT_PIRQA#
INT_PIRQB#
INT_PIRQC#
INT_PIRQD#
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
INT_PIRQH#
ICH_TP3
MCH_ICH_SYNC# [7]
+V3.3S
C150 0.1uF/16V,X7R
[7,14,20,25,26,38] PLTRST#
PLT_RST#
R130 100K
U6 SOT23_5 SN74AHC1G08DBV
[27] PLT_RST#
ICH_TP3
R109 1K ns
Stuff R109 foe XOR chain testing
CZC Technology
Title
ICH7M PCI-E/PCI/DMI/USB
Size A3
Project Name Q10
Rev B
Date: Thursday, February 26, 2009
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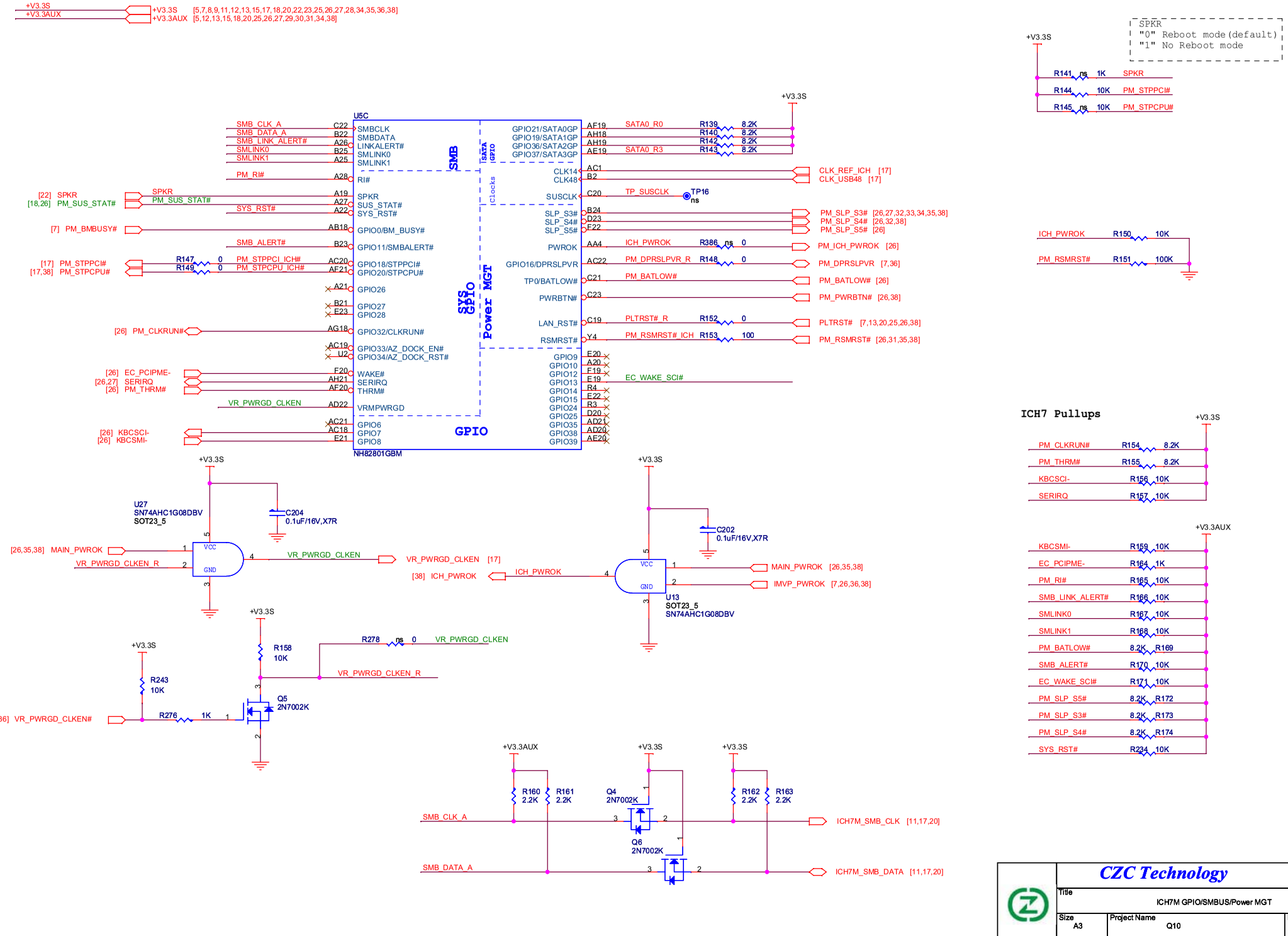
+V3.3S
+V3.3AUX
[5,7,8,9,11,12,13,15,17,18,20,22,23,25,26,27,28,34,35,36,38]
[5,12,13,15,18,20,25,26,27,29,30,31,34,38]
SPKR
"0" Reboot mode(default)
"1" No Reboot mode
R141 ns 1K SPKR
R144 10K PM_STPPCI#
R145 ns 10K PM_STPCPU#
U5C
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
SMB_CLK_A
SMB_DATA_A
SMB_LINK_ALERT#
SMLINK0
SMLINK1
PM_RI#
SPKR
PM_SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
SMB_ALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
NH82801GBM
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
GPIO11/SMBALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
SATA0_R0 R139 8.2K
SATA0_R1 R140 8.2K
SATA0_R2 R142 8.2K
SATA0_R3 R143 8.2K
CLK_REF_ICH [17]
CLK_USB48 [17]
TP_SUSCLK TP16 ns
PM_SLP_S3# [26,27,32,33,34,35,38]
PM_SLP_S4# [26,32,38]
PM_SLP_S5# [26]
ICH_PWROK R386 ns 0 PM_ICH_PWROK [26]
PM_DPRSLPVR_R R148 0 PM_DPRSLPVR [7,36]
PM_BATLOW# PM_BATLOW# [26]
PM_PWRBTN# [26,38]
PLTRST#_R R152 0 PLTRST# [7,13,20,25,26,38]
PM_RSMRST#_ICH R153 100 PM_RSMRST# [26,31,35,38]
EC_WAKE_SCI#
[22] SPKR
[18,26] PM_SUS_STAT#
[7] PM_BMBUSY#
[17] PM_STPPCI#
[17,38] PM_STPCPU#
R147 0 PM_STPPCI_ICH#
R149 0 PM_STPCPU_ICH#
[26] PM_CLKRUN#
[26] EC_PCIPME-
[26,27] SERIRQ
[26] PM_THRM#
VR_PWRGD_CLKEN
[26] KBCSCI-
[26] KBCSMI-
ICH_PWROK R150 10K
PM_RSMRST# R151 100K
ICH7 Pullups
PM_CLKRUN# R154 8.2K
PM_THRM# R155 8.2K
KBCSCI- R156 10K
SERIRQ R157 10K
KBCSMI- R159 10K
EC_PCIPME- R164 1K
PM_RI# R165 10K
SMB_LINK_ALERT# R166 10K
SMLINK0 R167 10K
SMLINK1 R168 10K
PM_BATLOW# 8.2K R169
SMB_ALERT# R170 10K
EC_WAKE_SCI# R171 10K
PM_SLP_S5# 8.2K R172
PM_SLP_S3# 8.2K R173
PM_SLP_S4# 8.2K R174
SYS_RST# R234 10K
U27
SN74AHC1G08DBV
SOT23_5
C204
0.1uF/16V,X7R
[26,35,38] MAIN_PWROK
VR_PWRGD_CLKEN_R
VR_PWRGD_CLKEN
VR_PWRGD_CLKEN [17]
C202
0.1uF/16V,X7R
[38] ICH_PWROK
MAIN_PWROK [26,35,38]
IMVP_PWROK [7,26,36,38]
U13
SOT23_5
SN74AHC1G08DBV
R158
10K
R278 ns 0 VR_PWRGD_CLKEN
R243
10K
R276 1K
Q5
2N7002K
[36] VR_PWRGD_CLKEN#
R160 2.2K
R161 2.2K
Q4
2N7002K
R162 2.2K
R163 2.2K
SMB_CLK_A
SMB_DATA_A
Q6
2N7002K
ICH7M_SMB_CLK [11,17,20]
ICH7M_SMB_DATA [11,17,20]
CZC Technology
Title
ICH7M GPIO/SMBUS/Power MGT
Size A3
Project Name Q10
Rev B
Date: Thursday, February 26, 2009
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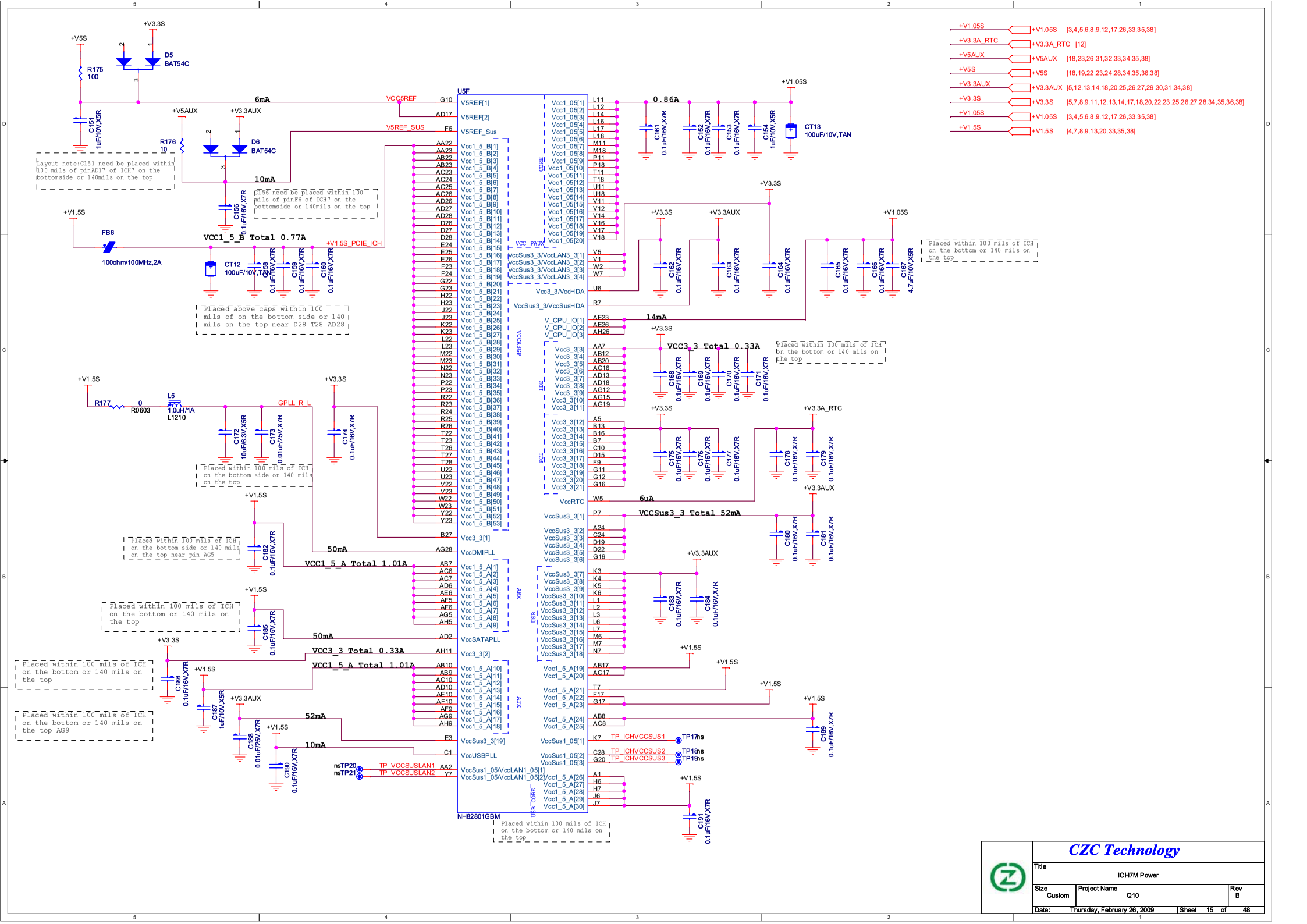
+V1.05S [3,4,5,6,8,9,12,17,26,33,35,38]
+V3.3A_RTC [12]
+V5AUX [18,23,26,31,32,33,34,35,38]
+V5S [18,19,22,23,24,28,34,35,36,38]
+V3.3AUX [5,12,13,14,18,20,25,26,27,29,30,31,34,38]
+V3.3S [5,7,8,9,11,12,13,14,17,18,20,22,23,25,26,27,28,34,35,36,38]
+V1.05S [3,4,5,6,8,9,12,17,26,33,35,38]
+V1.5S [4,7,8,9,13,20,33,35,38]
U5F
NH82801GBM
VCC5REF
V5REF_SUS
VCC1_5_B Total 0.77A
VCC1_5_A Total 1.01A
VCC3_3 Total 0.33A
VCCSus3_3 Total 52mA
0.86A
14mA
6uA
6mA
10mA
50mA
52mA
Layout note:C151 need be placed within 100 mils of pinAD17 of ICH7 on the bottomside or 140mils on the top
C156 need be placed within 100 mils of pinF6 of ICH7 on the bottomside or 140mils on the top
Placed above caps within 100 mils of on the bottom side or 140 mils on the top near D28 T28 AD28
Placed within 100 mils of ICH on the bottom side or 140 mils on the top
Placed within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG5
Placed within 100 mils of ICH on the bottom or 140 mils on the top
Placed within 100 mils of ICH on the bottom or 140 mils on the top
Placed within 100 mils of ICH on the bottom or 140 mils on the top AG9
Placed within 100 mils of ICH on the bottom or 140 mils on the top
Placed within 100 mils of ICH on the bottom or 140 mils on the top
Placed within 100 mils of ICH on the bottom or 140 mils on the top
Placed within 100 mils of ICH on the bottom or 140 mils on the top
Placed within 100 mils of ICH on the bottom or 140 mils on the top
Placed within 100 mils of ICH on the bottom or 140 mils on the top
CZC Technology
Title
ICH7M Power
Size
Custom
Project Name
Q10
Rev
B
Date:
Thursday, February 26, 2009
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of
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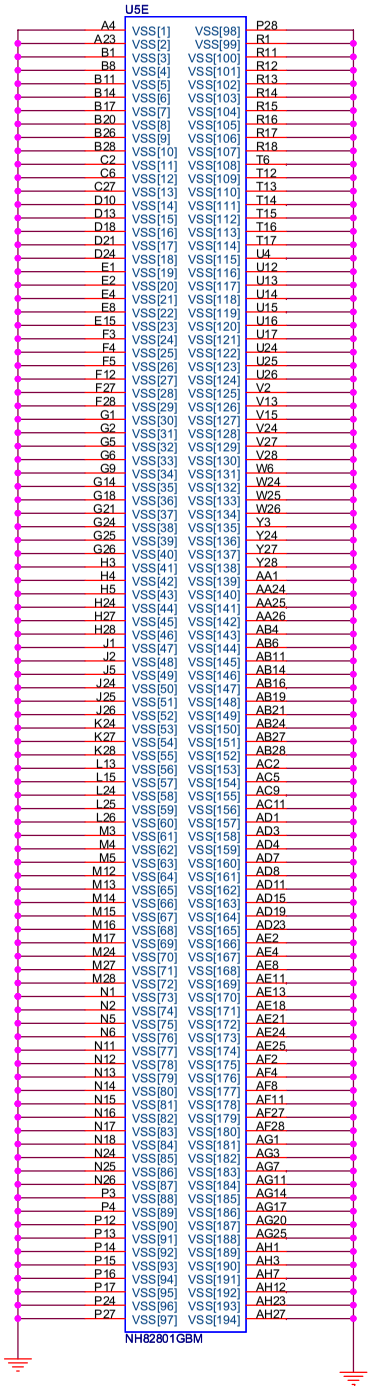
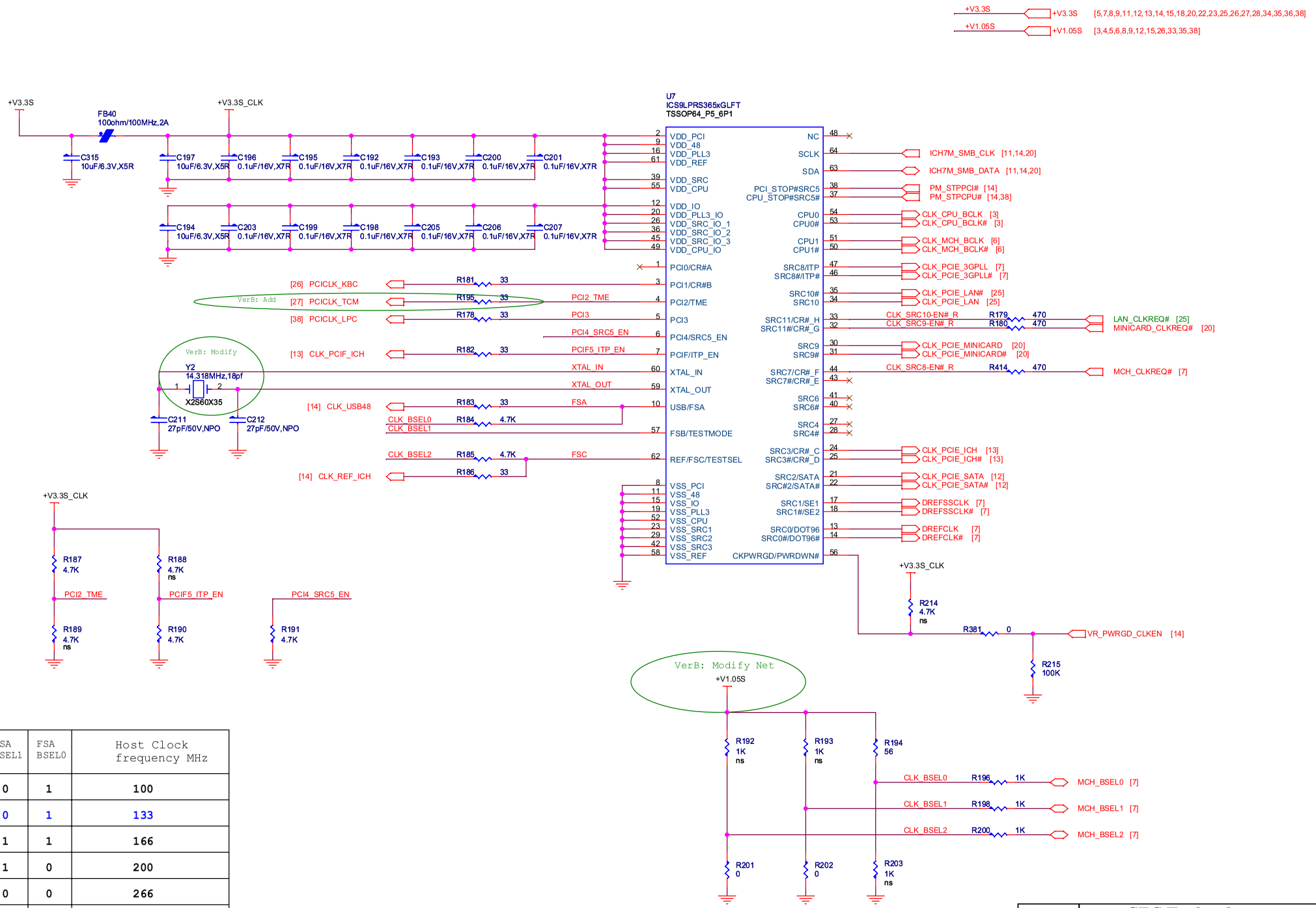


CZC Technology

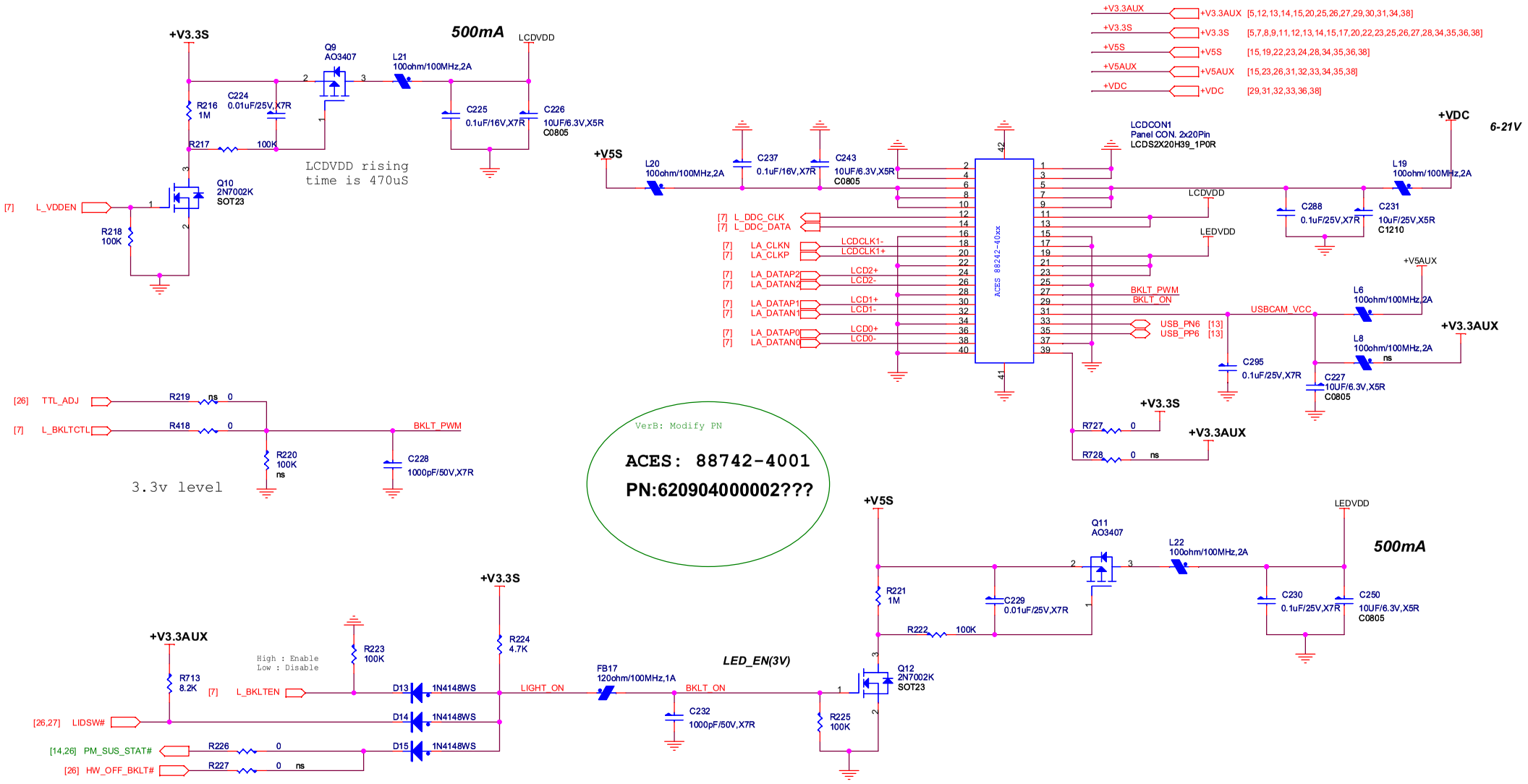
Title: ICH7M GND		
Size: A3	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 16 of 48	



FSC BSEL2	FSA BSEL1	FSA BSEL0	Host Clock frequency MHz
1	0	1	100
0	0	1	133
0	1	1	166
0	1	0	200
0	0	0	266
1	0	0	333
1	1	0	400
1	1	1	Reserved

CZC Technology

Title: CK505		
Size: A3	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 17 of 48	



	10.1 1024x576 Panel Type	VLED	LED_EN(3V)
* 1	HSD101PFW1-A00	5-21V	Need
* 2	CPT CLAA101NA0ACG V0.0	6-21V	Need
* 3	CPT CLAA101NA0ACN V0.0	6-21V	Need
4	AUO B101AW01 V3	5V	Need
* 5	BOE HT101WSB-100 [1024x600]	7-21V	Need
* 6	BOE HT101WSA-100	7-21V	Need
7	12.1 inch CCFL Panel		

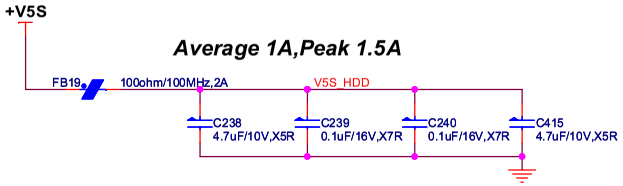
	10.2 1024x600 Panel Type	VLED	LED_EN(3V)
8	CPT CLAA102NA0ACW	5V	No
9	Hannstar HSD100IFW1-A**	5V	No
10			
11			
12			

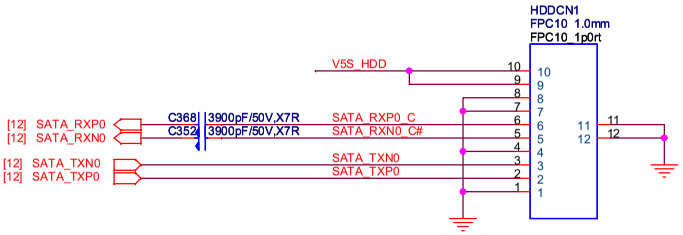
CZC Technology

Title: LVDS Panel		
Size: A3	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 18 of 48	

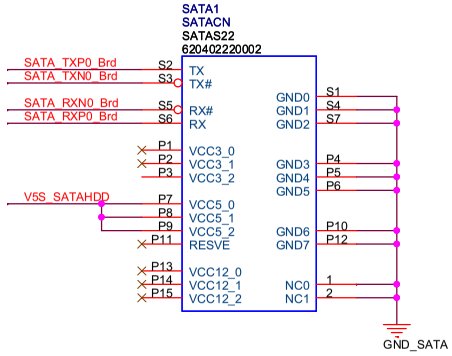
SATA HDD

+V3.3S → +V3.3S [5,7,8,9,11,12,13,14,15,17,18,20,22,23,25,26,27,28,34,35,36,38]
+V5S → +V5S [15,18,22,23,24,28,34,35,36,38]
ECVCC → ECVCC [26,28]
VIN → VIN [27,29,37,38]
+V3.3AUX → +V3.3AUX [5,12,13,14,15,18,20,25,26,27,29,30,31,34,38]



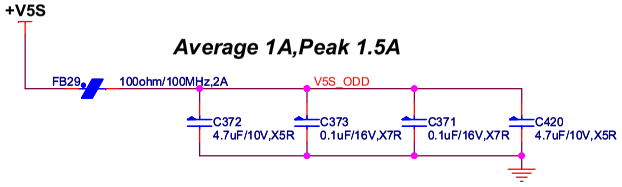


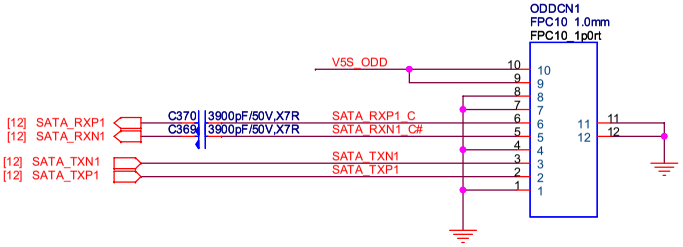
SATA Board

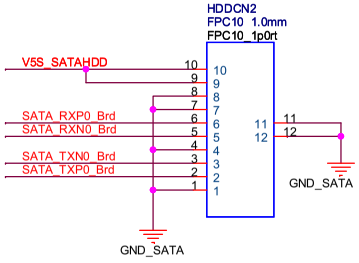


Alltop C16614-122A4-Y

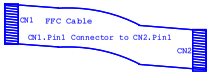
SATA ODD







SATACBL1
SATA 10P 1mmPitch FFC cable XXXmmL



CZC Technology

Title: SATAMISC		
Size: A3	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 19 of 48	

MINIPCIE SLOT

+VDC +VDC [18,29,31,32,33,36,38]
+V3.3S +V3.3S [5,7,8,9,11,12,13,14,15,17,18,22,23,25,26,27,28,34,35,36,38]
+V5S +V5S [15,18,19,22,23,24,28,34,35,36,38]
+V3.3AUX +V3.3AUX [5,12,13,14,15,18,25,26,27,29,30,31,34,38]
+V1.5S +V1.5S [4,7,8,9,13,15,33,35,38]

PCIE1
PCIE MINI CARD 4mm
MINIPCIEH40

+V3.3S_WLAN +V1.5S

[13] USB_PN3
[13] USB_PP3
USB_D-
USB_D+
3.3VAux0
+3.3VAUX
+3.3VAUX1
+1.5V0
+1.5V1
1.5V
LED_WPAN#
LED_WLAN#
LED_WWAN#
TP23
R242 0
R270 0
WIRELESS_LED# [27]
VerB: Add

[17] CLK_PCIE_MINICARD#
[17] CLK_PCIE_MINICARD
REFCLK-
REFCLK+
PERST#
WAKE#
CLKREQ#
PLTRST# [7,13,14,25,26,38]
PCIE_WAKE# [25,26]
MINICARD_CLKREQ# [17]

[13] PCIE_TXN2_SLOT
[13] PCIE_TXP2_SLOT
PETN0
PETP0
SMB_DATA
SMB_CLK
ICH7M_SMB_DATA [11,14,17]
ICH7M_SMB_CLK [11,14,17]

[13] PCIE_RXN2_SLOT
[13] PCIE_RXP2_SLOT
C241 0.1uF/16V,X7R
C242 0.1uF/16V,X7R
PERN0
PERP0
COEX2
COEX1

W_DISABLE#
HW_RATIO_OFF_WLAN# [26]

PCIE mini Card V1.2

+V3.3S_WLAN
RESERVED0/UIM_C8
RESERVED1/UIM_C4
GND15
+3.3VAux2
+3.3VAux3
GND16
RESERVED0
RESERVED1
RESERVED2
RESERVED3

MiniPCIE_H1
Match 4mm Boss

+V3.3Aux
FB45
100ohm/100MHz,2A
ns
+V3.3S
FB46
100ohm/100MHz,2A
+V3.3S_WLAN
VerB:Add
C245 4.7uF/10V,X5R
C246 0.1uF/16V,X7R
C244 0.1uF/16V,X7R

VerB: Add
SIM_VCC
SIM_DAT0
SIM_CLK
SIM_RESET
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP
GND0 GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14

+V1.5S
C247 4.7uF/10V,X5R
C248 0.1uF/16V,X7R
C249 0.1uF/16V,X7R

3GPCIE1
PCIE MINI CARD 4mm
MINIPCIEH40_SL

+V3.3S_3G +V1.5S
VerB:Add
VerB:Modify

[21] USB_PN7_3G
[21] USB_PP7_3G
TP49
R295 0
R292 0
WIRELESS_LED# [27]
R294 0
R293 0
PLTRST# [7,13,14,25,26,38]
PCIE_WAKE# [25,26]
VerB:Add
HW_RATIO_OFF_3G# [26]

+V3.3Aux
FB44
100ohm/100MHz,2A
ns
+V3.3S
FB41
100ohm/100MHz,2A
+V3.3S_3G
VerB:Add
C374 10uF/6.3V,X5R
C376 0.1uF/16V,X7R
C377 0.1uF/16V,X7R

PCIE mini Card V1.2
Support Half Size Card

Full Size Card Stuff
3GPCIE_H1
Match 4mm Boss

Half Size Card Stuff
3GPCIE_H2
Match 4mm Boss
ns

VerB:Add
+V1.5S
C294 4.7uF/10V,X5R
C251 0.1uF/16V,X7R
C287 0.1uF/16V,X7R

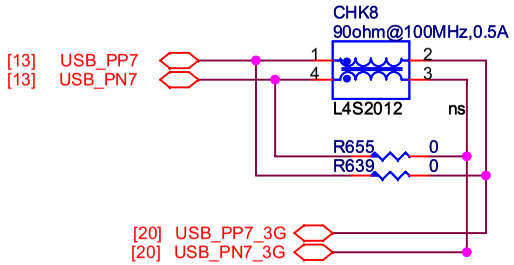
Proconn
SPPN08-A0-5000
1.5mm

SIMreader
SIMreader
sim9h15

SIM_VCC
SIM_VPP
SIM_RESET
SIM_CLK
SIM_DAT0
SIM_RST
SIM_IO
SIM_MCMD
SIM_CDDETECT
SIM_GND0
SIM_GND1
SIM_GND2
SIM_GND3
SIM_GND4

CZC Technology

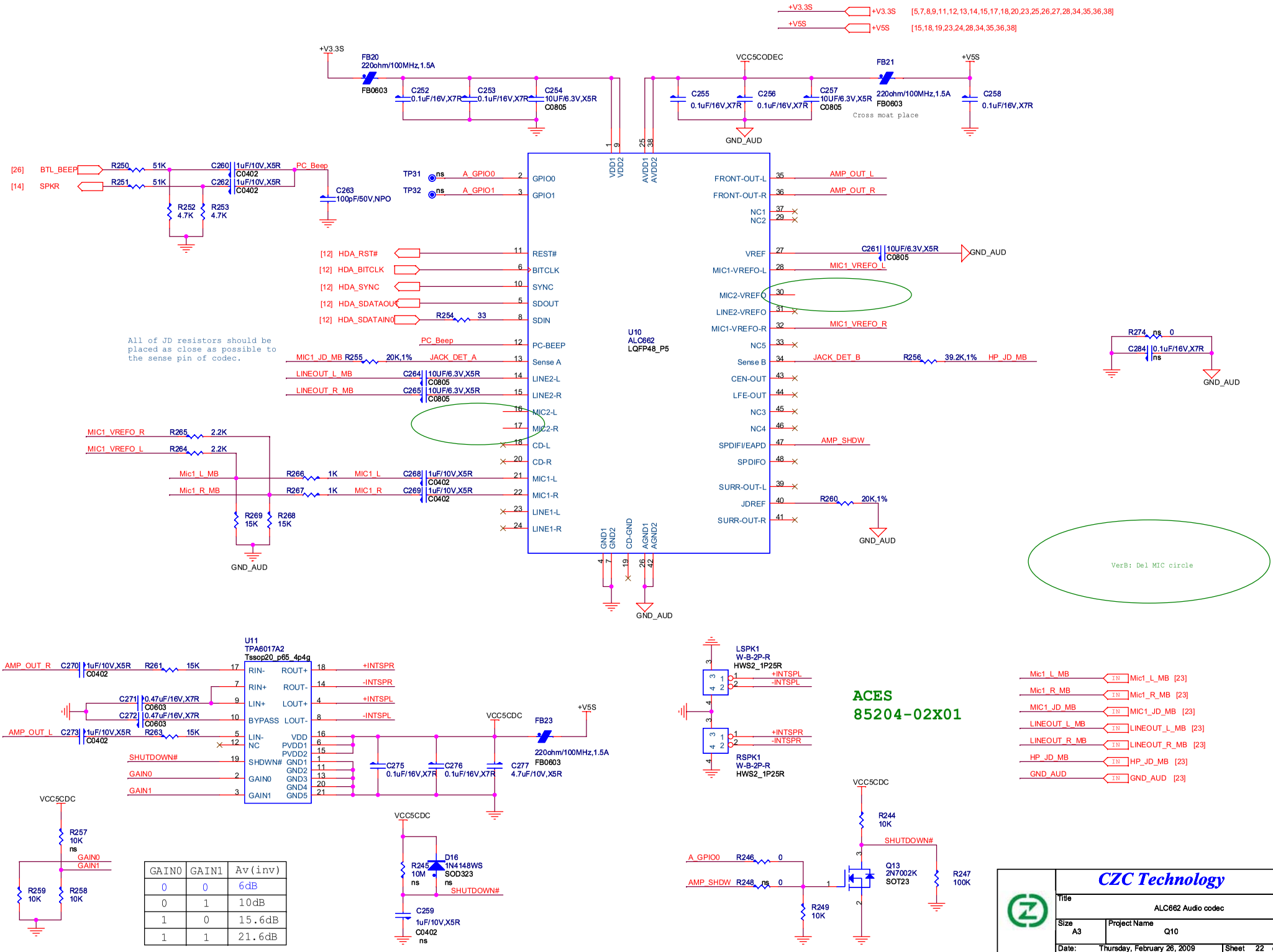
Title: Mini PCIE connect		
Size: A3	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 20 of 48	



VerB: Del Express Card circle

CZC Technology

Title: BLOCK DIAGRAM		
Size: A4	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 21 of 48	



GAIN0	GAIN1	Av(inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

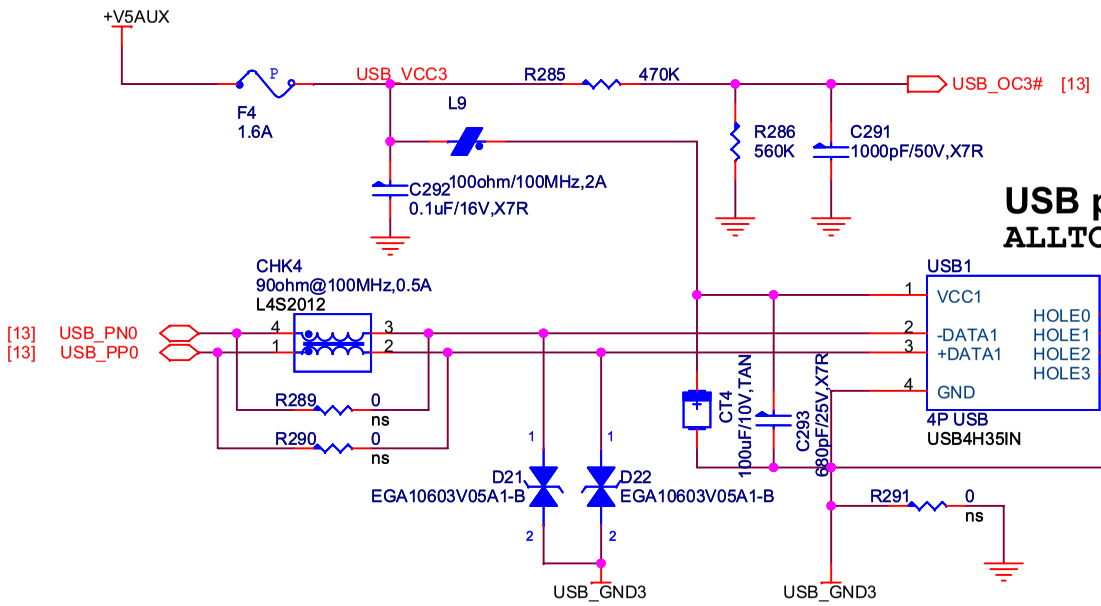
CZC Technology

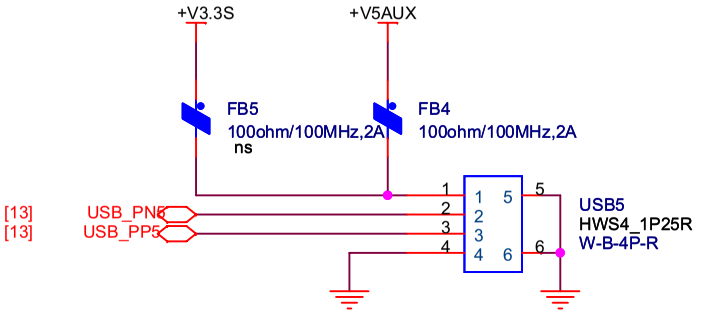
Title: ALC662 Audio codec		
Size: A3	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 22 of 48	

+V3.3S → +V3.3S [5,7,8,9,11,12,13,14,15,17,18,20,22,25,26,27,28,34,35,36,38]

+V5S → +V5S [15,18,19,22,24,28,34,35,36,38]

+V5AUX → +V5AUX [15,18,26,31,32,33,34,35,38]

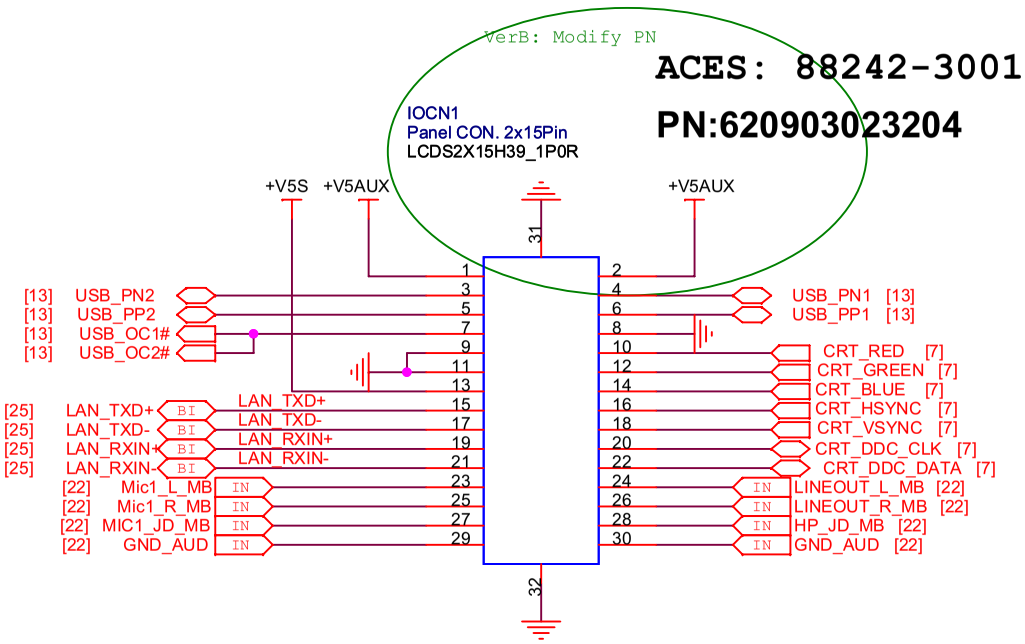


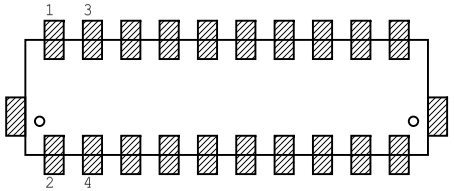


VerB: Modify PN

ACES: 88242-3001

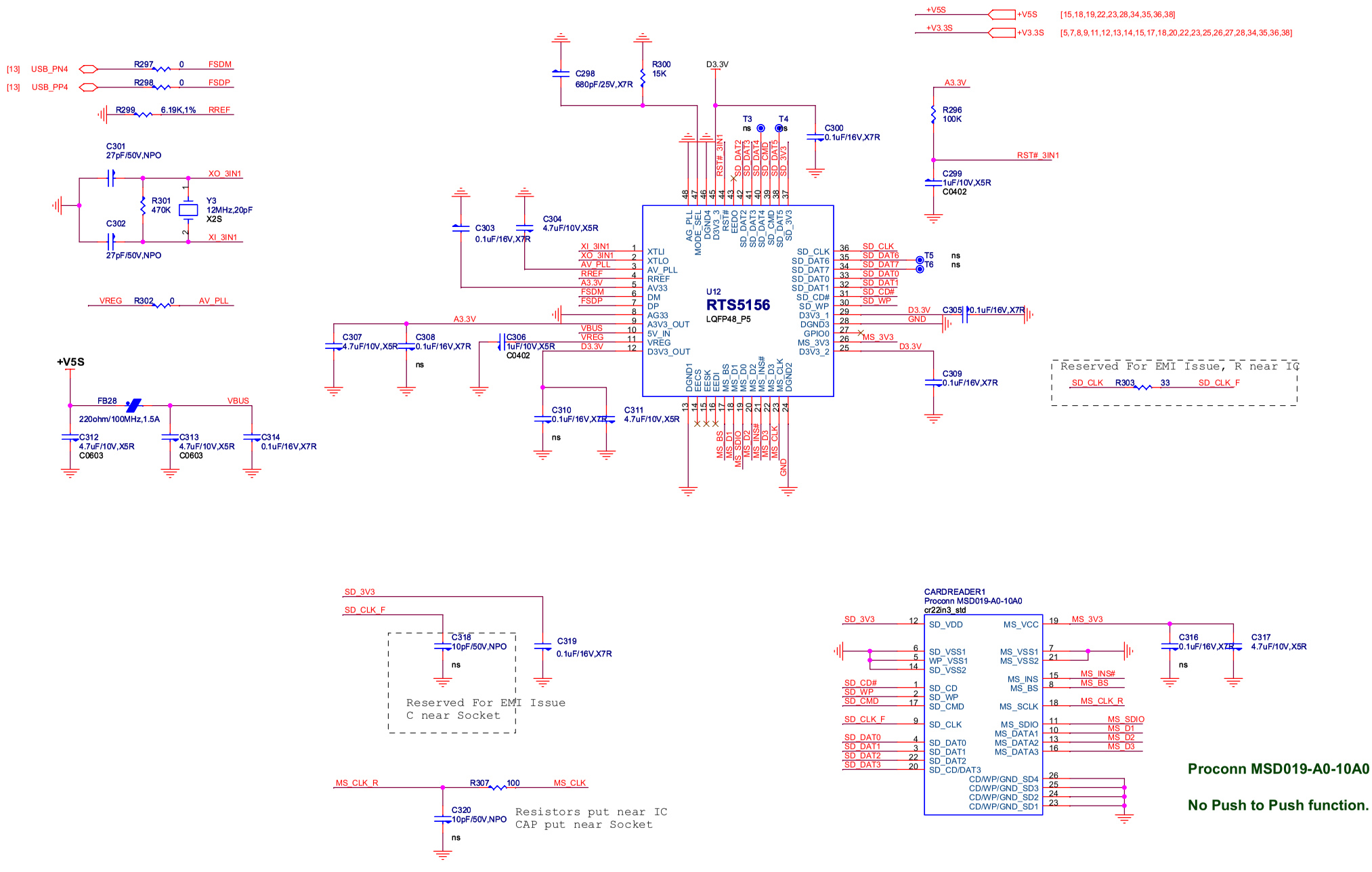
PN:620903023204



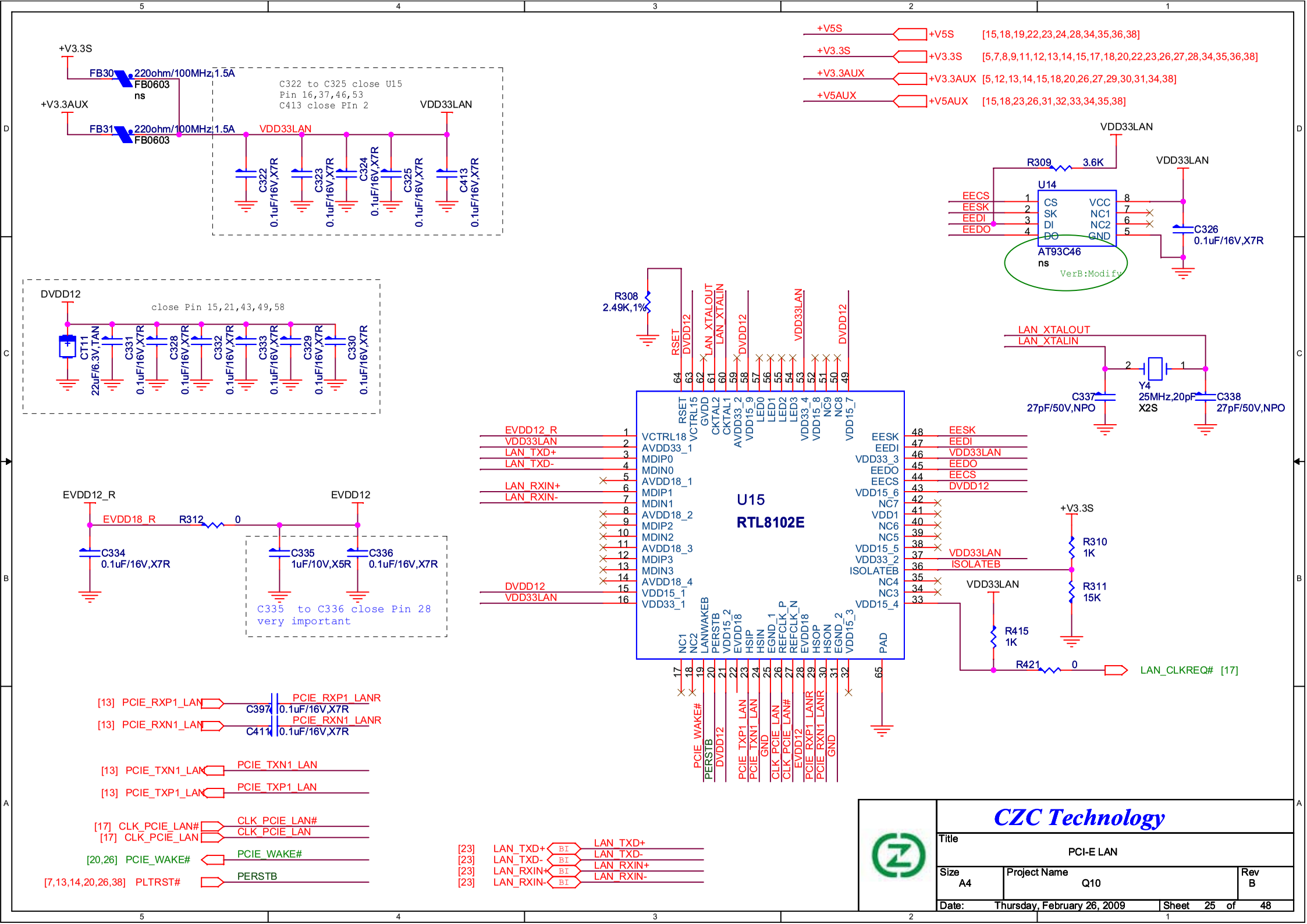


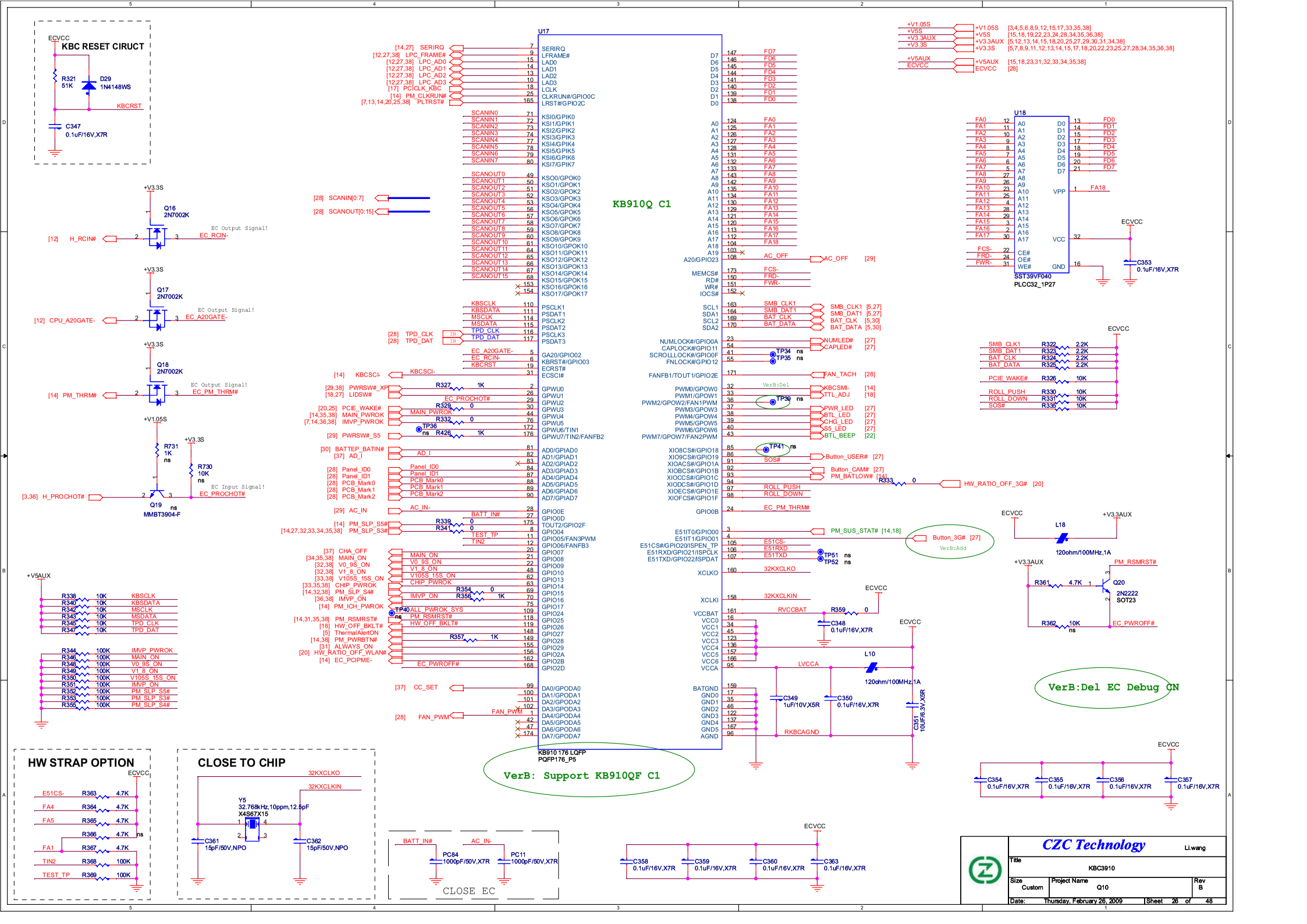
CZC Technology

Title: USB Port & Fan control		
Size: A4	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 23 of 48	



CZC Technology		
Title	Cardreader SD/MMC/MS	
Size A3	Project Name Q10	Rev B
Date: Thursday, February 26, 2009	Sheet 24 of 48	


+V5S +V5S [15,18,19,22,23,24,28,34,35,36,38]
+V3.3S +V3.3S [5,7,8,9,11,12,13,14,15,17,18,20,22,23,26,27,28,34,35,36,38]
+V3.3AUX +V3.3AUX [5,12,13,14,15,18,20,26,27,29,30,31,34,38]
+V5AUX +V5AUX [15,18,23,26,31,32,33,34,35,38]
+V3.3S
FB30 220ohm/100MHz,1.5A FB0603 ns
+V3.3AUX
FB31 220ohm/100MHz,1.5A FB0603
C322 to C325 close U15 Pin 16,37,46,53 C413 close PIn 2
VDD33LAN
C322 0.1uF/16V,X7R
C323 0.1uF/16V,X7R
C324 0.1uF/16V,X7R
C325 0.1uF/16V,X7R
C413 0.1uF/16V,X7R
DVDD12
close Pin 15,21,43,49,58
C11 22uF/6.3V,TAN
C331 0.1uF/16V,X7R
C328 0.1uF/16V,X7R
C332 0.1uF/16V,X7R
C333 0.1uF/16V,X7R
C329 0.1uF/16V,X7R
C330 0.1uF/16V,X7R
EVDD12_R
EVDD18_R
R312 0
EVDD12
C334 0.1uF/16V,X7R
C335 1uF/10V,X5R
C336 0.1uF/16V,X7R
C335 to C336 close Pin 28 very important
R308 2.49K,1%
U15
RTL8102E
RSET
DVDD12
LAN_XTALOUT
LAN_XTALIN
VDD33LAN
VCTRL18
AVDD33_1
MDIP0
MDIN0
AVDD18_1
MDIP1
MDIN1
AVDD18_2
MDIP2
MDIN2
AVDD18_3
MDIP3
MDIN3
AVDD18_4
VDD15_1
VDD33_1
EESK
EEDI
VDD33_3
EEDO
EECS
VDD15_6
NC7
VDD1
NC6
NC5
VDD15_5
VDD33_2
ISOLATEB
NC4
NC3
VDD15_4
PAD
NC1
NC2
LANWAKEB
PERSTB
VDD15_2
EVDD18
HSIP
HSIN
EGND_1
REFCLK_P
REFCLK_N
EVDD18
HSOP
HSON
EGND_2
VDD15_3
PCIE_WAKE#
PERSTB
DVDD12
PCIE_TXP1_LAN
PCIE_TXN1_LAN
GND
CLK_PCIE_LAN
CLK_PCIE_LAN#
EVDD12
PCIE_RXP1_LANR
PCIE_RXN1_LANR
GND
VDD33LAN
R309 3.6K
U14
EECS
EESK
EEDI
EEDO
CS
SK
DI
DO
VCC
NC1
NC2
GND
AT93C46
ns
VerB:Modify
C326 0.1uF/16V,X7R
LAN_XTALOUT
LAN_XTALIN
Y4 25MHz,20pF X2S
C337 27pF/50V,NPO
C338 27pF/50V,NPO
+V3.3S
R310 1K
R311 15K
VDD33LAN
R415 1K
R421 0
LAN_CLKREQ# [17]
EVDD12_R
VDD33LAN
LAN_TXD+
LAN_TXD-
LAN_RXIN+
LAN_RXIN-
DVDD12
VDD33LAN
[13] PCIE_RXP1_LAN
C397 0.1uF/16V,X7R
PCIE_RXP1_LANR
[13] PCIE_RXN1_LAN
C411 0.1uF/16V,X7R
PCIE_RXN1_LANR
[13] PCIE_TXN1_LAN
PCIE_TXN1_LAN
[13] PCIE_TXP1_LAN
PCIE_TXP1_LAN
[17] CLK_PCIE_LAN#
CLK_PCIE_LAN#
[17] CLK_PCIE_LAN
CLK_PCIE_LAN
[20,26] PCIE_WAKE#
PCIE_WAKE#
[7,13,14,20,26,38] PLTRST#
PERSTB
[23] LAN_TXD+ BI LAN_TXD+
[23] LAN_TXD- BI LAN_TXD-
[23] LAN_RXIN+ BI LAN_RXIN+
[23] LAN_RXIN- BI LAN_RXIN-
CZC Technology
Title
PCI-E LAN
Size A4
Project Name Q10
Rev B
Date: Thursday, February 26, 2009
Sheet 25 of 48


KBC RESET CIRUCT
ECVCC
R321 51K
D29 1N4148WS
KBCRST
C347 0.1uF/16V,X7R
U17
KB910Q C1
KB910 176 LQFP
PQFP176_P5
VerB: Support KB910QF C1
U18
SST39VF040
PLCC32_1P27
HW STRAP OPTION
CLOSE TO CHIP
Y5 32.768kHz,10ppm,12.5pF X4S67X15
C361 15pF/50V,NPO
C362 15pF/50V,NPO
CLOSE EC
VerB:Del EC Debug CN
CZC Technology
Li.wang
KBC3910
Custom
Q10
Rev B
Thursday, February 26, 2009
Sheet 26 of 48

ACES
87152-1207L
0.5mm 12P Bottom

PWRBTN1
FFC12
FPC12_P5RT

R723
100K

+V3.3AUX

PWRSWVCC_MBXP
PWRSWVCC_S5
Button_CAM#
Button_USER#
Button_3G#
LIDSW#

PWRSWVCC_MBXP [29,31]
PWRSWVCC_S5 [29,31]
Button_CAM# [26]
Button_USER# [26]
Button_3G# [26]
LIDSW# [18,26]

BTNCN1
W-B-4P-R
HWS4_1P25R

Button_CAM#
Button_USER#

VerB:Del OSPWRBTN2 circle.

+V3.3S [5,7,8,9,11,12,13,14,15,17,18,20,22,23,25,26,28,34,35,36,38]
+V5S [15,18,19,22,23,24,28,34,35,36,38]
VIN [29,37,38]
+V3.3AUX [5,12,13,14,15,18,20,25,26,29,30,31,34,38]

R714 330
R711 330
PWR_LED+
S5_LED+
RED BLUE
PWR1
red blue
LED4_0605

[26] S5_LED
R543 1K
Q52
MMBT3904-F
R712 100K ns

[26] PWR_LED
R716 1K
Q53
MMBT3904-F
R717 100K ns

R741 330
R742 330
CHARGE_LED
3BAT_STATE_LED
RED BLUE
CHARGE
red blue
LED4_0605

[26] BTL_LED
R743 1K
Q57
MMBT3904-F

[26] CHG_LED
R744 1K
Q58
MMBT3904-F

[12] SATA_LED#
[26] NUMLED#
[26] CAPLED#
[20] WIRELESS_LED#

SATA_LED# IDE Blue LED2_0603 IDE+ R715 330
NUMLED# NUMLK Blue LED2_0603 NUM+ R738 330
CAPLED# CAPSLK Blue LED2_0603 CAP+ R739 330
WIRELESS_LED# WIRELS Blue LED2_0603 WIRE+ R740 330

S5_LED+ C545 1000pF/50V,X7R
PWR_LED+ C546 1000pF/50V,X7R
IDE+ C547 1000pF/50V,X7R
NUM+ C555 1000pF/50V,X7R
CAP+ C556 1000pF/50V,X7R
WIRE+ C557 1000pF/50V,X7R
BAT_STATE_LED C558 1000pF/50V,X7R
CHARGE_LED C559 1000pF/50V,X7R

VCC_TCM1
VCC_TCM
+V3.3S
+V3.3AUX

FB75 220ohm/100MHz,1.5A FB0603
FB77 220ohm/100MHz,1.5A FB0603
FB72 220ohm/100MHz,1.5A ns FB0603

C696 0.1uF/16V,X7R
C695 0.1uF/16V,X7R
C698 2.2uF/6.3V,X7R
C694 0.1uF/16V,X7R

U42
SSX44B
qfn40_p5

[14,26] SERIRQ
[12,26,38] LPC_AD0
[12,26,38] LPC_AD1
[12,26,38] LPC_AD2
[12,26,38] LPC_AD3
[12,26,38] LPC_FRAME#
[13] PLT_RST#
[17] PCICLK_TCM
[14,26,32,33,34,35,38] PM_SLP_S3#

R750 0
R754 0
R816 4.7K ns
R755 0

TP37 ns
TP46 ns
TP53 ns

BADD0 R817 10K ns
BADD1 R818 10K ns

C697 1uF/10V,X7R

VerB: Add TCM

BA0/1 Address
00---EE/EF
01--7E/7F
10--2E/2F
11--4E/4F(Default)

IICCN1
W-B-4P-R
HWS4_1P25R

FB76
220ohm/100MHz,1.5A
FB0603

SMB_CLK1 [5,26]
SMB_DAT1 [5,26]

VerB: Add I2C bus Interface

Q10预留

LEDCN1
FFC12
FPC12_P5RT

FB33 220ohm/100MHz,1.5A FB0603
FB34 220ohm/100MHz,1.5A FB0603

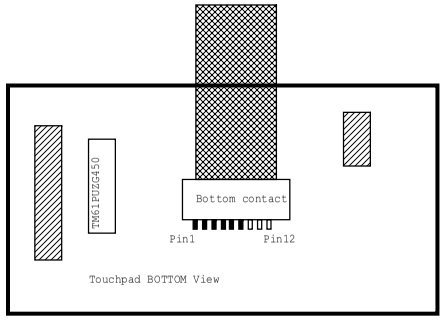
LEDT12 ns
LEDT11 ns
LEDT10 ns
LEDT9 ns
LEDT8 ns
LEDT7 ns
LEDT6 ns
LEDT5 ns
LEDT4 ns
LEDT3 ns
LEDT1 ns

SATA_LED#
NUMLED#
CAPLED#
WIRELESS_LED#
CHG_LED
BTL_LED
PWR_LED
S5_LED

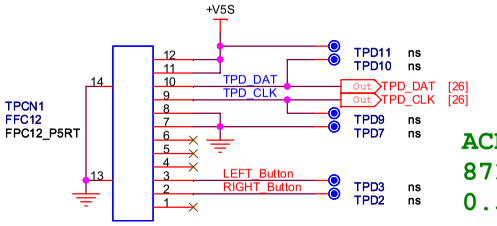
ACES
87152-1207L
0.5mm 12P Bottom

CZC Technology
Li.wang

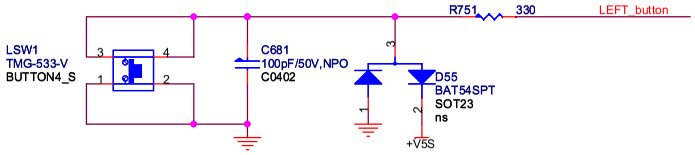
Title: System LED and button connect
Size: A3
Project Name: Q10
Rev: B
Date: Thursday, February 26, 2009
Sheet 27 of 48

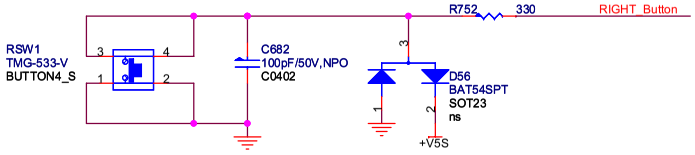


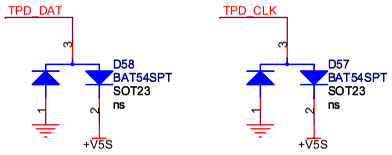
Synaptics : TM-00450-001
Was TM61PUZG450
Up.

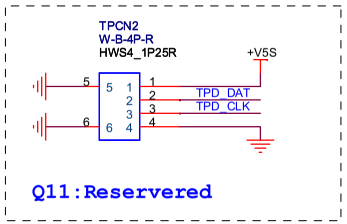


ACES
87152-1207L
0.5mm 12P Bottom

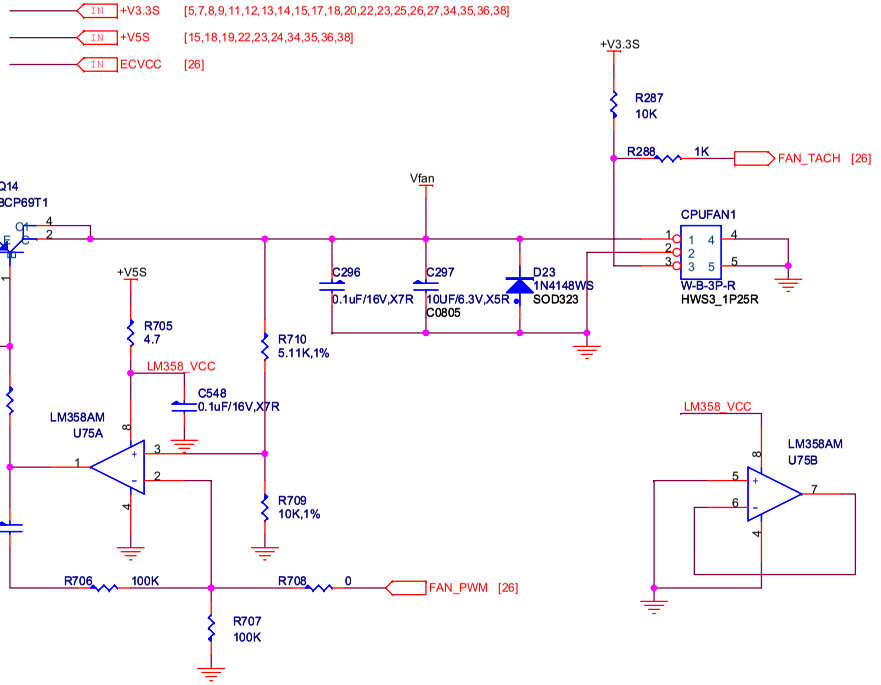


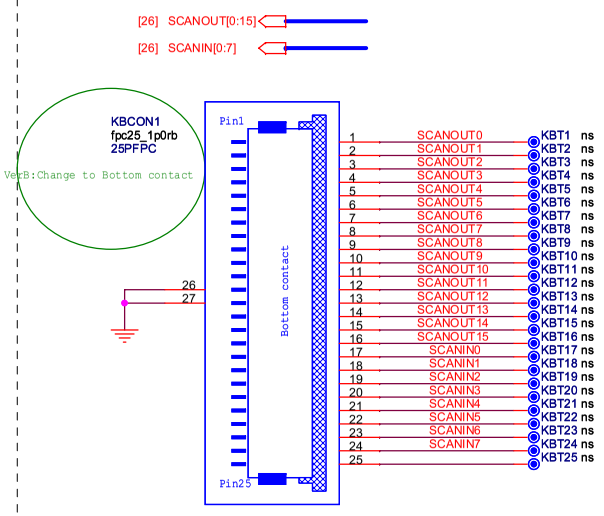






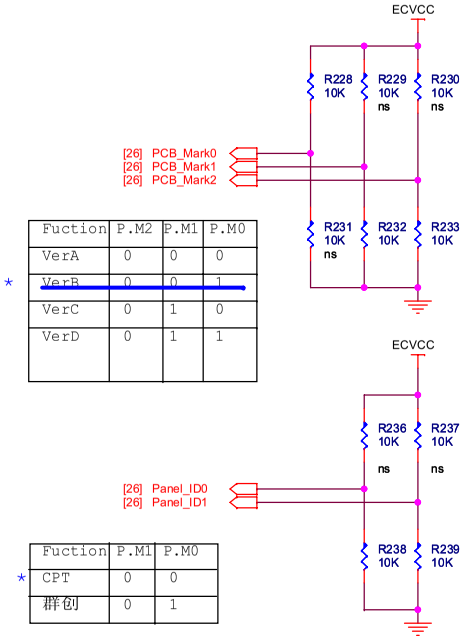
ACES
85204-04X01





ACES
85202-25x61
1.0mm Bottom 25P

精模
V0761EMBK1 US

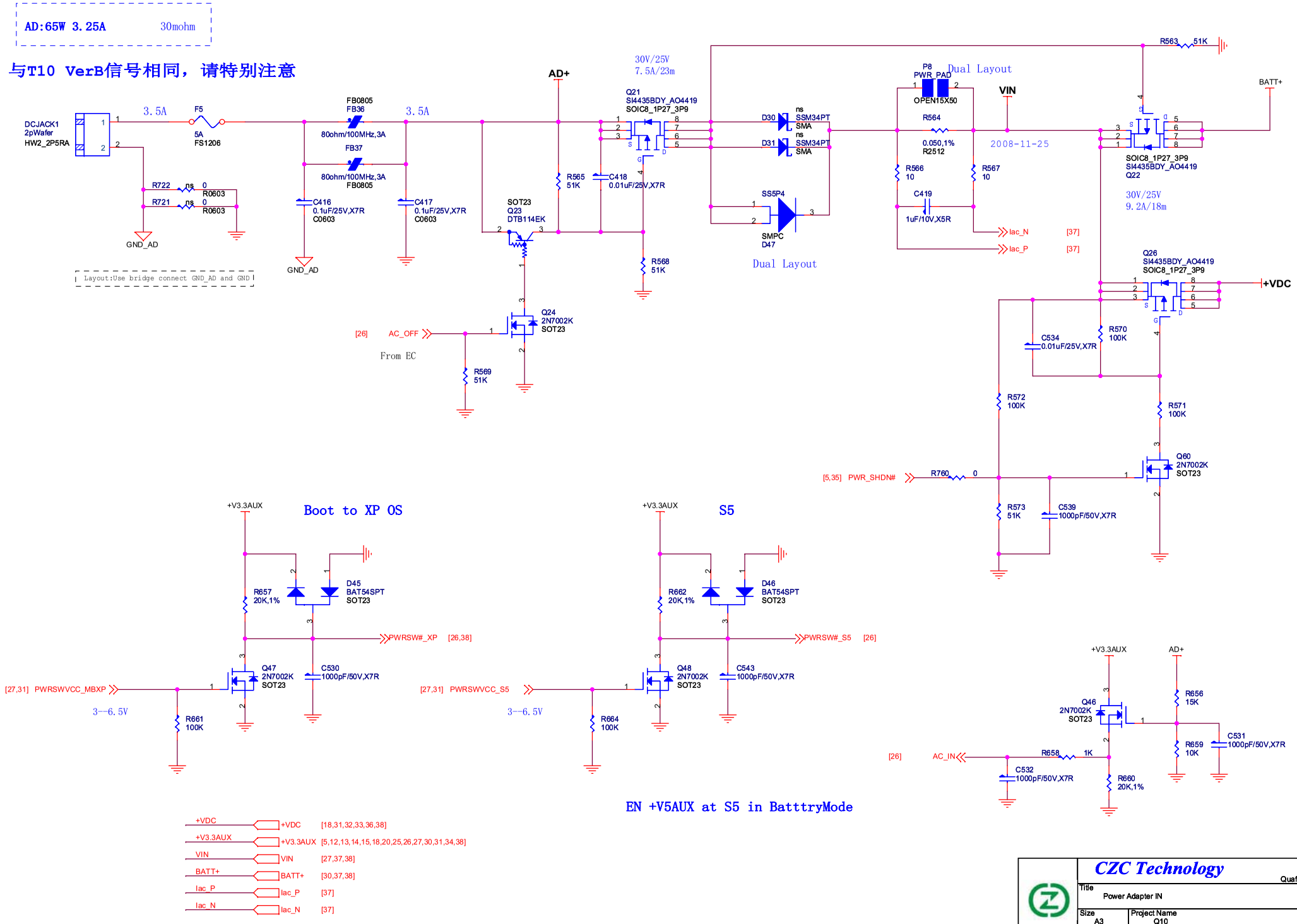


Title	Touchpad & Keyboard & FAN Connector
Size	A3
Project Name	Q10
Rev	B
Date:	Thursday, February 26, 2009
Sheet	28 of 48

CZC Technology
Li.wang

AD:65W 3.25A 30mohm

与T10 VerB信号相同，请特别注意



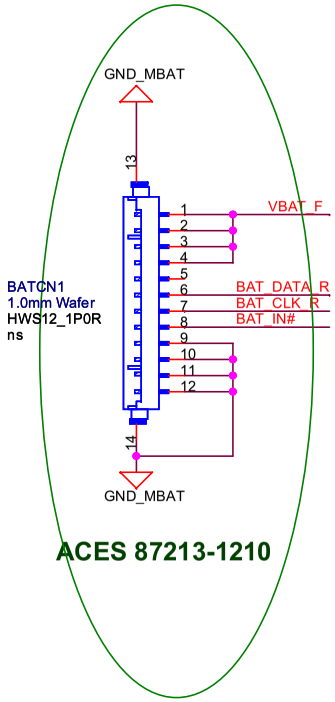
CZC Technology

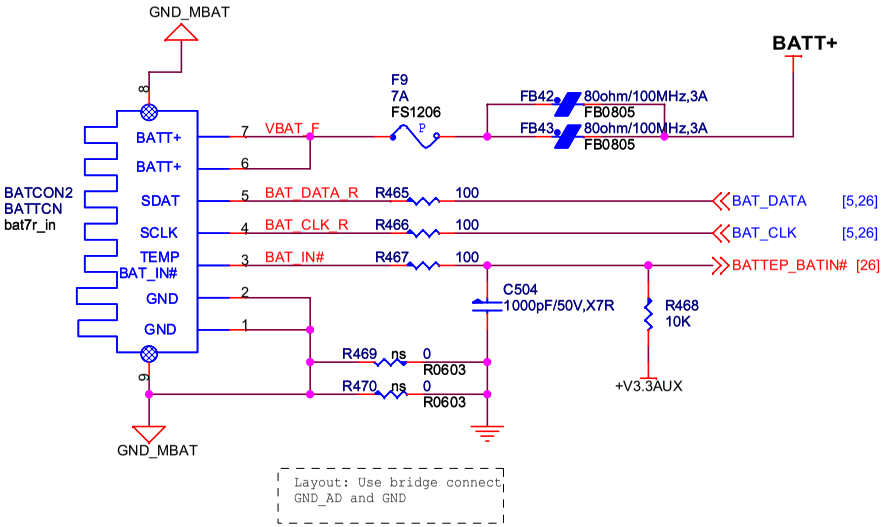
Quaf

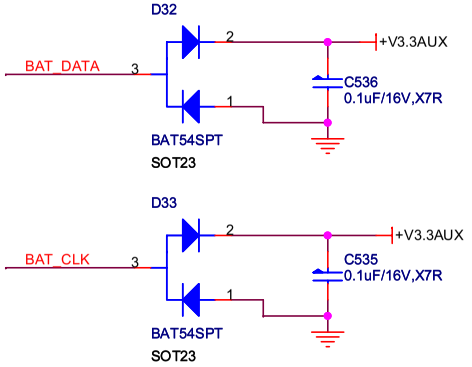
Title: Power Adapter IN

Size: A3 | Project Name: Q10 | Rev: B

Date: Thursday, February 26, 2009 | Sheet 29 of 48







BATT+ BATT+ [29,37,38]

+V3.3AUX +V3.3AUX [5,12,13,14,15,18,20,25,26,27,29,31,34,38]

RTC MF52 D 103 F 3950

Temperature	Voltage	RT
-15	3.0	74.18K
70	0.5	1.740K

BAT_TEM	
0.5-3.0V	Battery OK
<0.5V or >3.0V	Battery Fail

BATT_IN#	
3.3V	No Battery
0V	Battery In

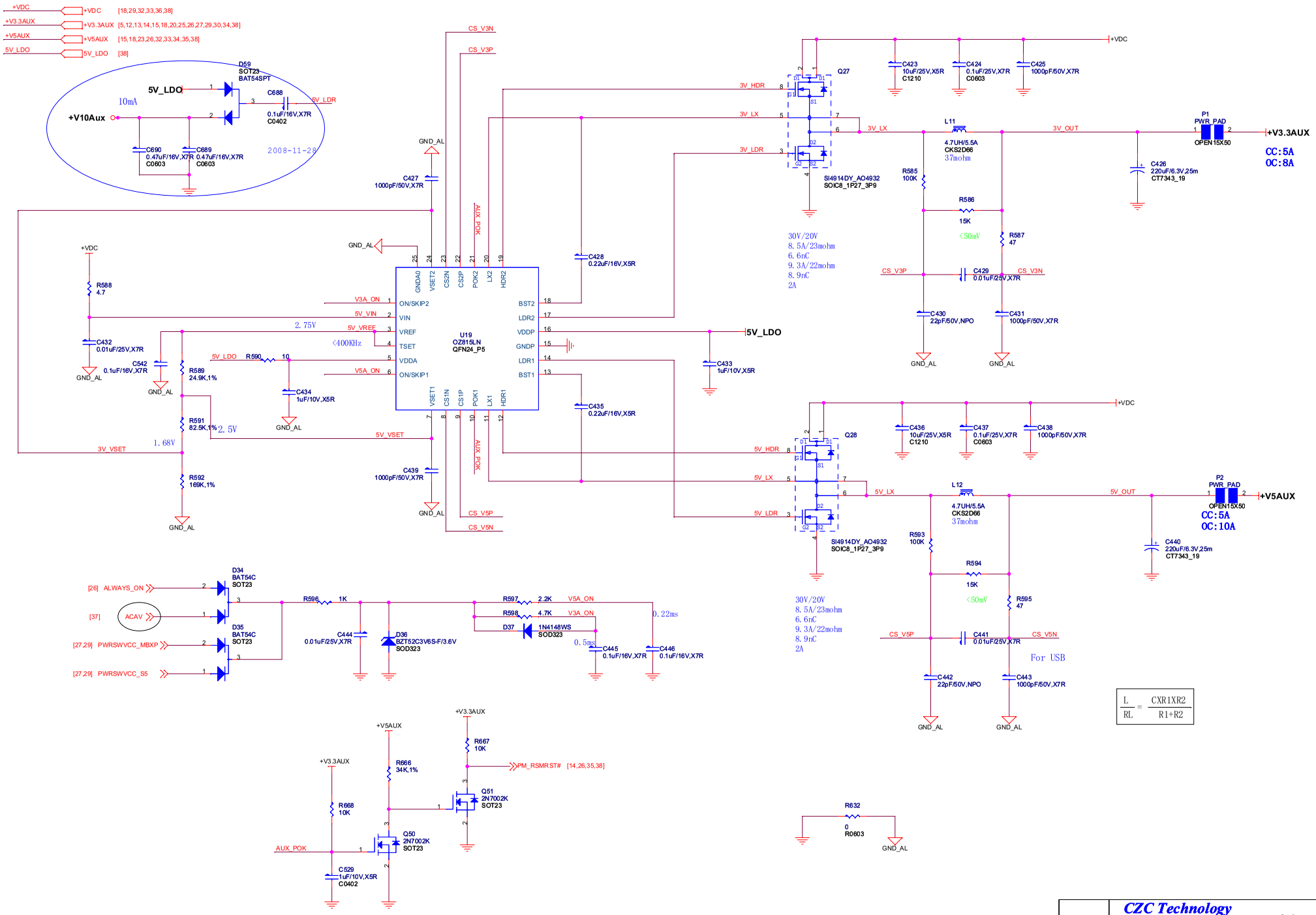
CZC Technology

Quaf

Title: Power Battery IN

Size	Project Name	Rev
Custom	Q10	B

Date: Thursday, February 26, 2009 Sheet 30 of 48


+VDC [18,29,32,33,36,38]
+V3.3AUX [5,12,13,14,15,18,20,25,26,27,29,30,34,38]
+V5AUX [15,18,23,26,32,33,34,35,38]
5V_LDO [38]
D59 SOT23 BAT54SPT
5V_LDO
10mA
+V10Aux
C688 0.1uF/16V,X7R C0402
5V_LDR
C690 0.47uF/16V,X7R C0603
C689 0.47uF/16V,X7R C0603
2008-11-28
CS_V3N
CS_V3P
GND_AL
C427 1000pF/50V,X7R
AUX_POK
C428 0.22uF/16V,X5R
U19 OZ815LN QFN24_P5
GNDA0 VSET2 CS2N CS2P POK2 LX2 HDR2
ON/SKIP2 VIN VREF TSET VDDA ON/SKIP1
BST2 LDR2 VDDP GNDP LDR1 BST1
V3A_ON 5V_VIN 5V_VREF 5V_LDO V5A_ON
VSET1 CS1N CS1P POK1 LX1 HDR1
+VDC
R588 4.7
C432 0.01uF/25V,X7R
C542 0.1uF/16V,X7R
R589 24.9K,1%
2.75V
<400KHz
R590 10
C434 1uF/10V,X5R
R591 82.5K,1%
2.5V
1.68V
3V_VSET
R592 169K,1%
5V_VSET
C439 1000pF/50V,X7R
C435 0.22uF/16V,X5R
C433 1uF/10V,X5R
5V_LDO
3V_HDR
3V_LX
3V_LDR
Q27
SI4914DY_AO4932 SOIC8_1P27_3P9
C423 10uF/25V,X5R C1210
C424 0.1uF/25V,X7R C0603
C425 1000pF/50V,X7R
+VDC
L11 4.7UH/5.5A CKS2D66 37mohm
3V_OUT
P1 PWR_PAD OPEN15X50
+V3.3AUX
CC:5A
OC:8A
C426 220uF/6.3V,25m CT7343_19
R585 100K
R586 15K
<50mV
R587 47
CS_V3P
C429 0.01uF/25V,X7R
CS_V3N
C430 22pF/50V,NPO
C431 1000pF/50V,X7R
GND_AL
30V/20V
8.5A/23mohm
6.6nC
9.3A/22mohm
8.9nC
2A
5V_HDR
5V_LX
5V_LDR
Q28
SI4914DY_AO4932 SOIC8_1P27_3P9
C436 10uF/25V,X5R C1210
C437 0.1uF/25V,X7R C0603
C438 1000pF/50V,X7R
+VDC
L12 4.7UH/5.5A CKS2D66 37mohm
5V_OUT
P2 PWR_PAD OPEN15X50
+V5AUX
CC:5A
OC:10A
C440 220uF/6.3V,25m CT7343_19
R593 100K
R594 15K
<50mV
R595 47
CS_V5P
C441 0.01uF/25V,X7R
CS_V5N
For USB
C442 22pF/50V,NPO
C443 1000pF/50V,X7R
30V/20V
8.5A/23mohm
6.6nC
9.3A/22mohm
8.9nC
2A
[26] ALWAYS_ON
[37] ACAV
[27,29] PWRSWVCC_MBXP
[27,29] PWRSWVCC_S5
D34 BAT54C SOT23
D35 BAT54C SOT23
R596 1K
C444 0.01uF/25V,X7R
D36 BZT52C3V6S-F/3.6V SOD323
R597 2.2K
R598 4.7K
V5A_ON
V3A_ON
D37 1N4148WS SOD323
0.22ms
0.5ms
C445 0.1uF/16V,X7R
C446 0.1uF/16V,X7R
+V3.3AUX
+V5AUX
R667 10K
PM_RSMRST# [14,26,35,38]
R666 34K,1%
R668 10K
Q51 2N7002K SOT23
Q50 2N7002K SOT23
AUX_POK
C529 1uF/10V,X5R C0402
R632 0 R0603
L / RL = CXR1XR2 / R1+R2
CZC Technology
Quaf
Title
Power +V3.3Aux +V5Aux +10V
Size Custom
Project Name Q10
Rev B
Date: Thursday, February 26, 2009
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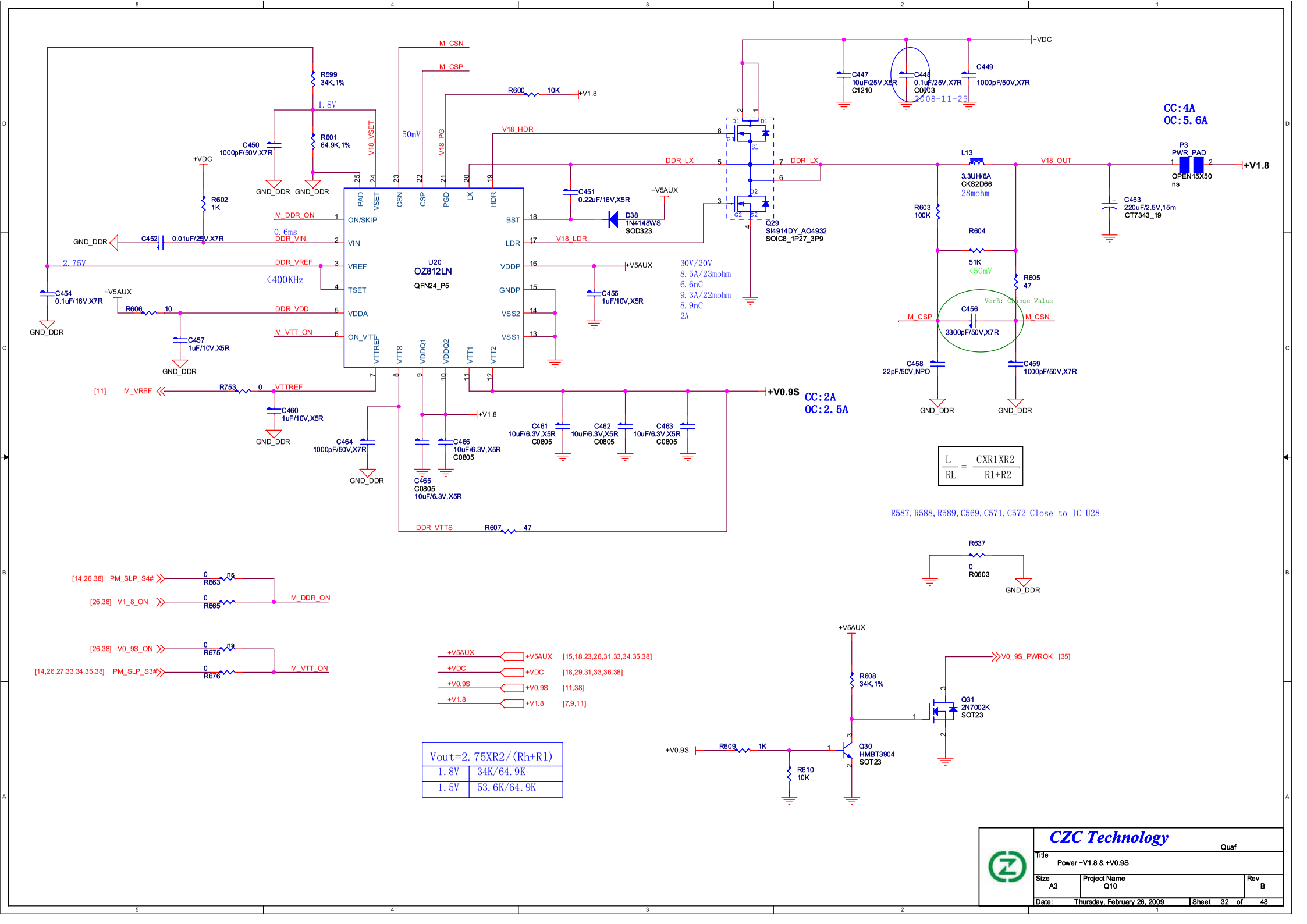


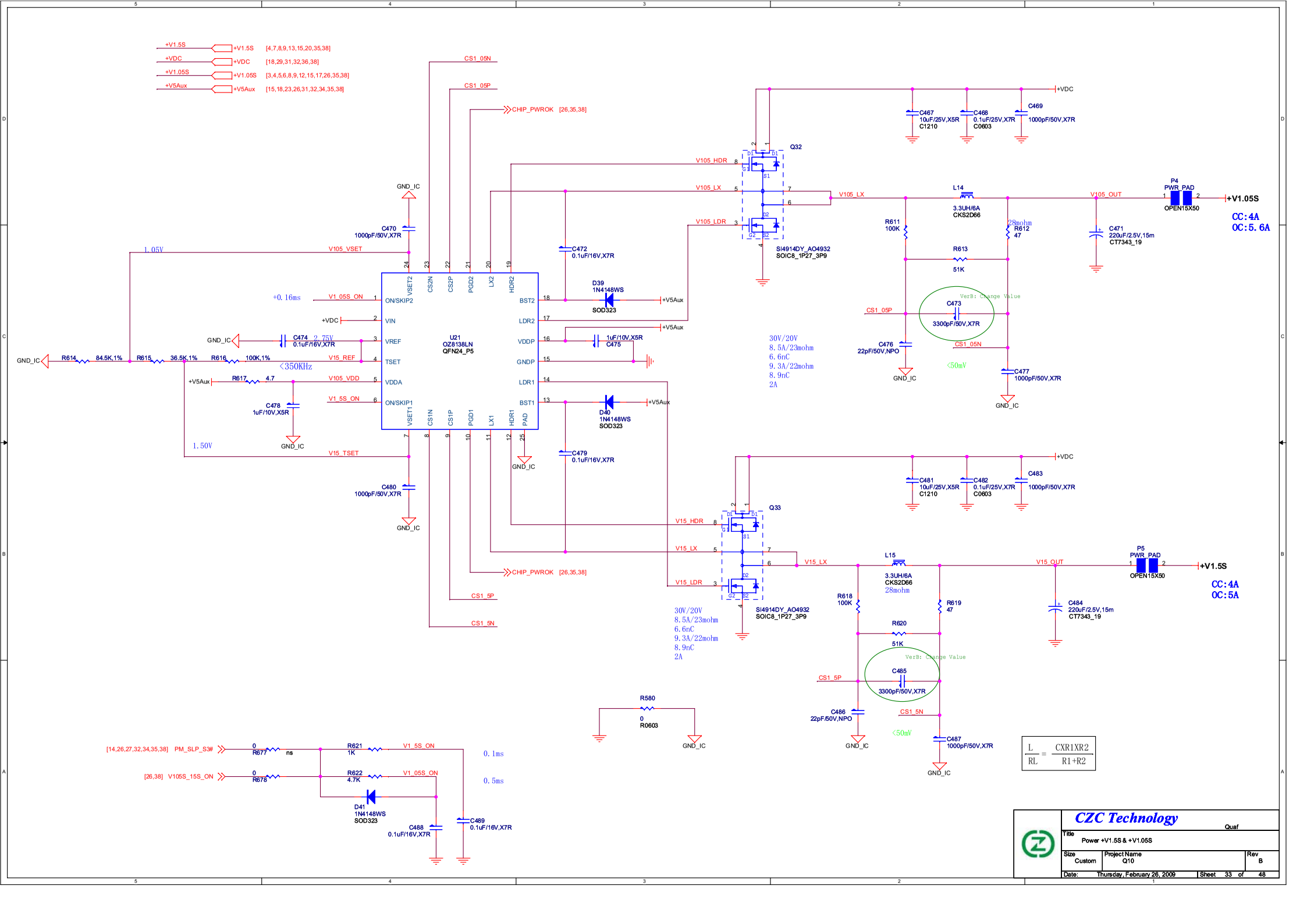
CZC Technology

Quaf

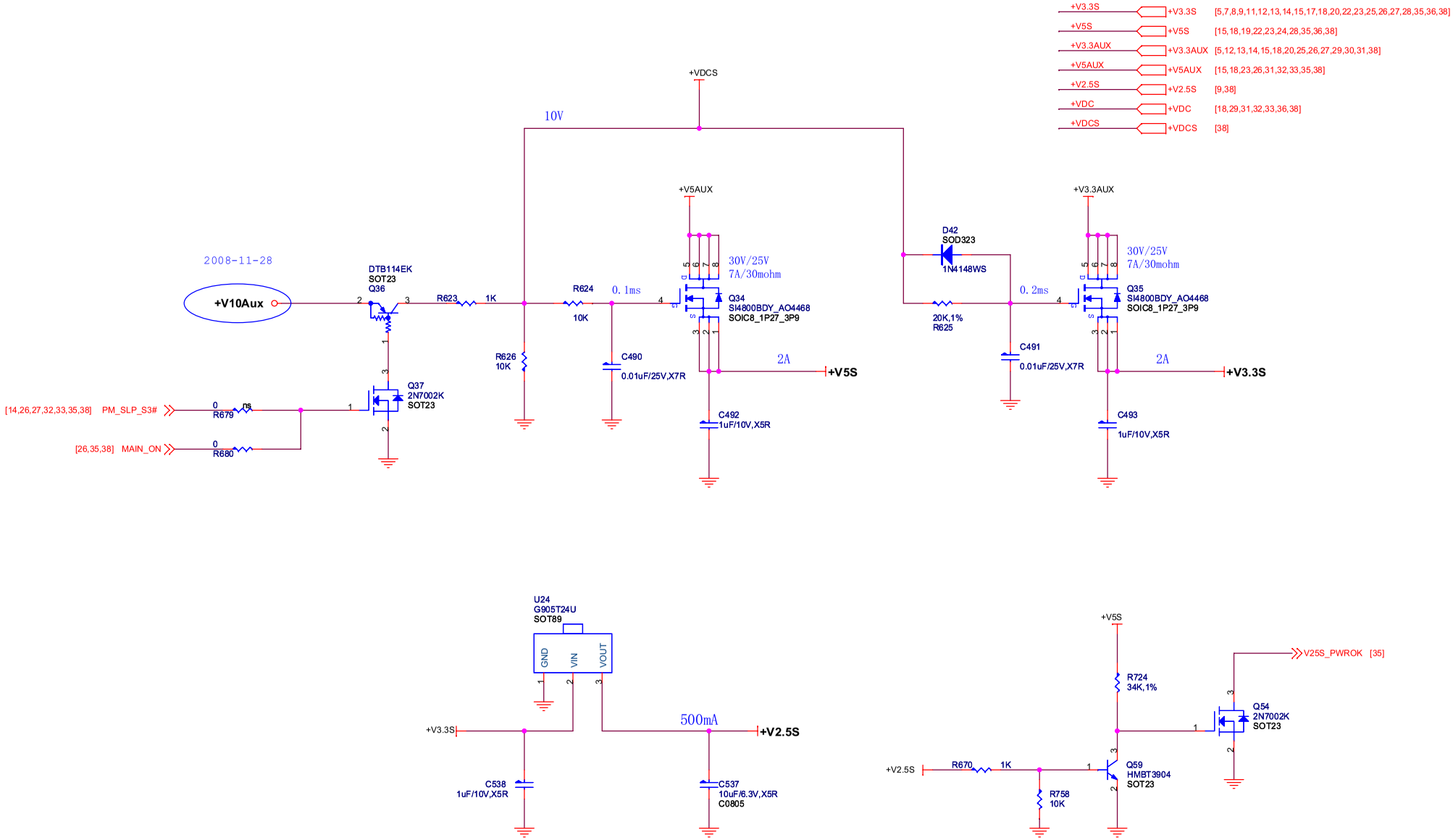
Title: Power +V1.8 & +V0.9S

Size: A3 | Project Name: Q10 | Rev: B

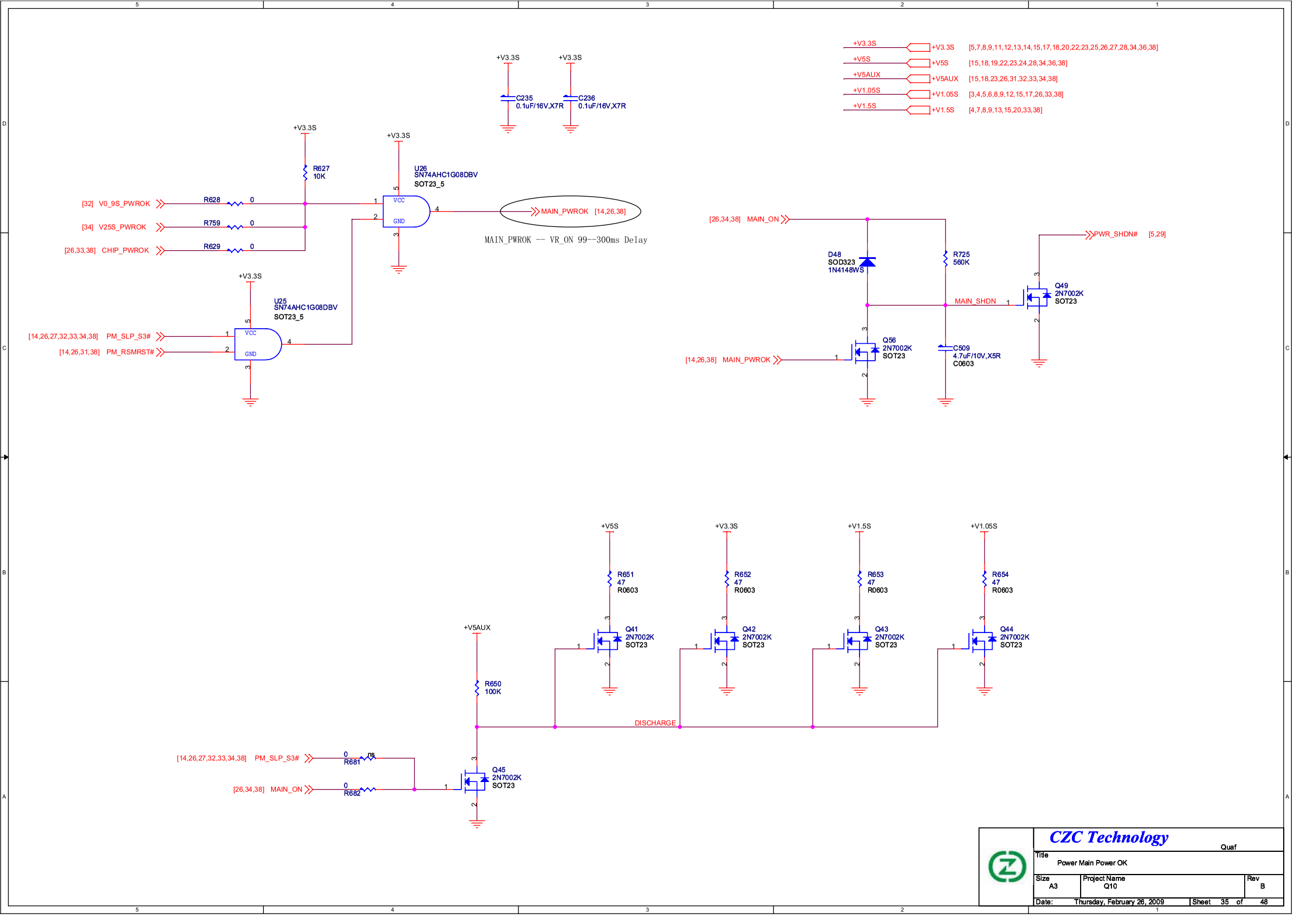
Date: Thursday, February 26, 2009 | Sheet 32 of 48



CZC Technology		Quaf	
Title: Power +V1.5S & +V1.05S			
Size: Custom	Project Name: Q10		Rev: B
Date: Thursday, February 26, 2009		Sheet 33 of 48	



CZC Technology		Quaf
Title: Power +V5S & +V3.3S & +V25S		
Size: A3	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 34 of 48	


+V3.3S [5,7,8,9,11,12,13,14,15,17,18,20,22,23,25,26,27,28,34,36,38]
+V5S [15,18,19,22,23,24,28,34,36,38]
+V5AUX [15,18,23,26,31,32,33,34,38]
+V1.05S [3,4,5,6,8,9,12,15,17,26,33,38]
+V1.5S [4,7,8,9,13,15,20,33,38]
C235 0.1uF/16V,X7R
C236 0.1uF/16V,X7R
R627 10K
U26 SN74AHC1G08DBV SOT23_5
[32] V0_9S_PWROK
[34] V25S_PWROK
[26,33,38] CHIP_PWROK
R628 0
R759 0
R629 0
MAIN_PWROK [14,26,38]
MAIN_PWROK -- VR_ON 99--300ms Delay
U25 SN74AHC1G08DBV SOT23_5
[14,26,27,32,33,34,38] PM_SLP_S3#
[14,26,31,38] PM_RSMRST#
[26,34,38] MAIN_ON
D48 SOD323 1N4148WS
R725 560K
PWR_SHDN# [5,29]
Q49 2N7002K SOT23
MAIN_SHDN
Q56 2N7002K SOT23
[14,26,38] MAIN_PWROK
C509 4.7uF/10V,X5R C0603
R651 47 R0603
R652 47 R0603
R653 47 R0603
R654 47 R0603
Q41 2N7002K SOT23
Q42 2N7002K SOT23
Q43 2N7002K SOT23
Q44 2N7002K SOT23
R650 100K
DISCHARGE
[14,26,27,32,33,34,38] PM_SLP_S3#
[26,34,38] MAIN_ON
R681 0 ns
R682 0
Q45 2N7002K SOT23
CZC Technology
Quaf
Title
Power Main Power OK
Size A3
Project Name Q10
Rev B
Date: Thursday, February 26, 2009
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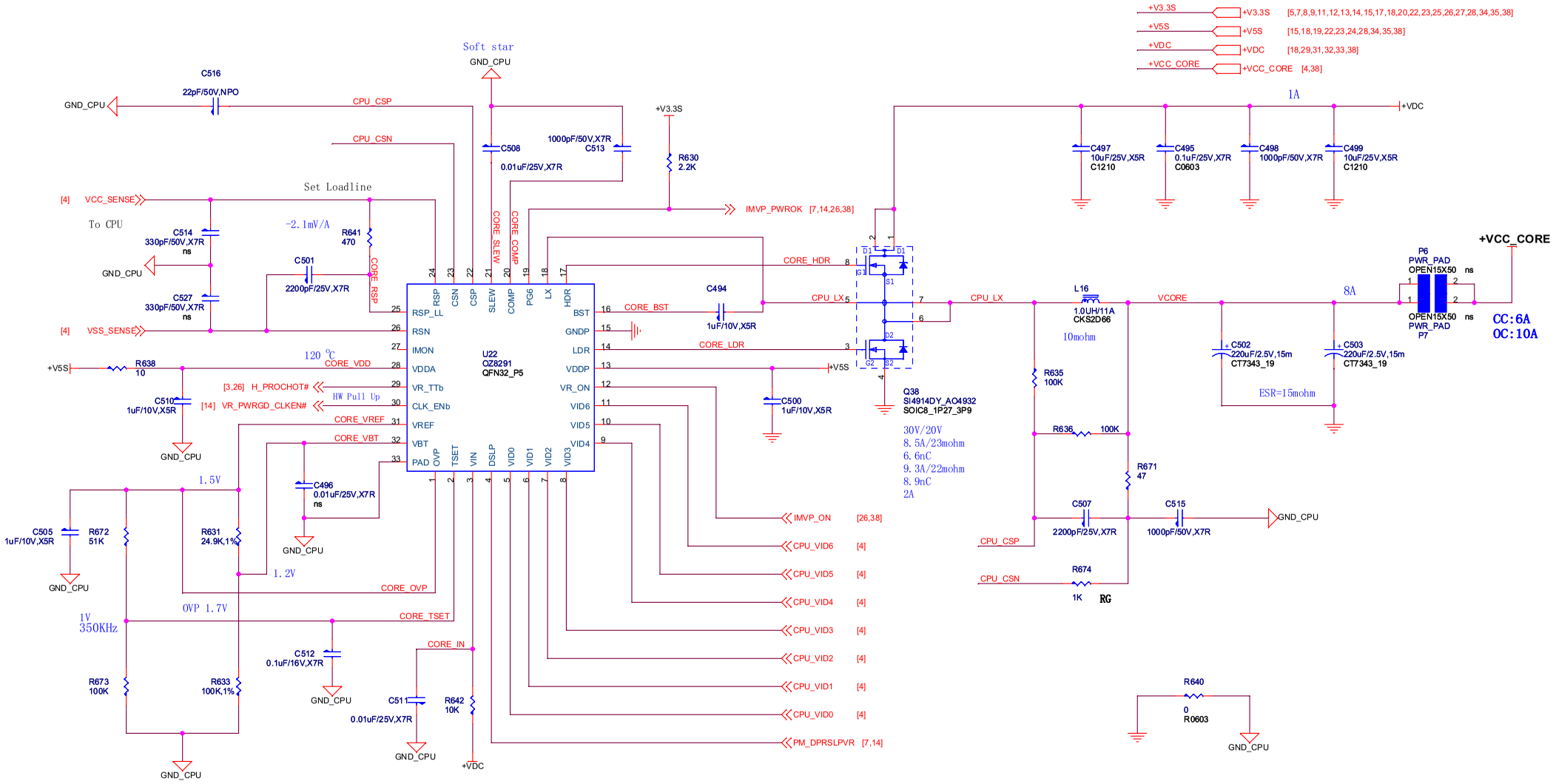
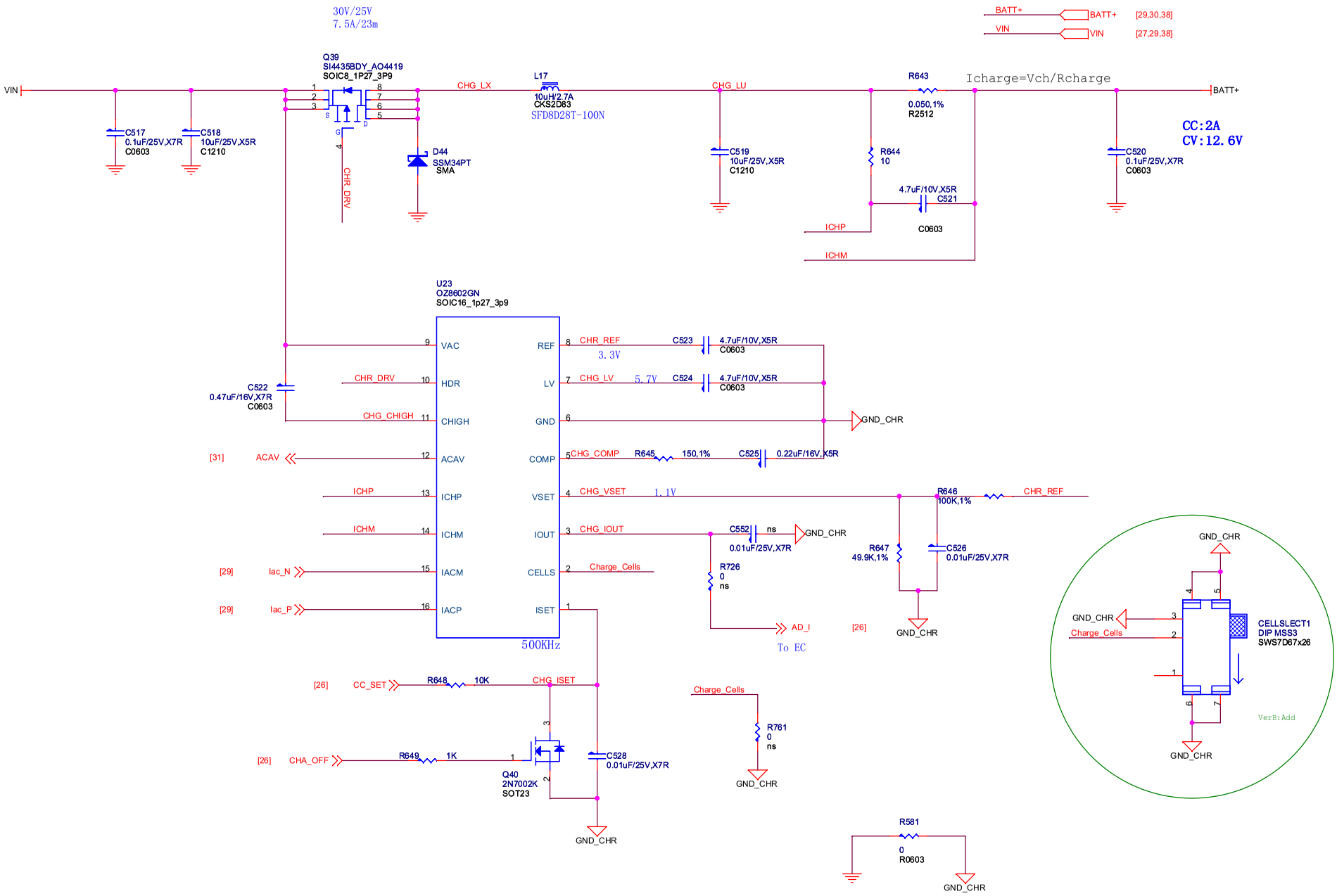


CPU Core Debug

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vout
0	0	1	1	0	0	0	1.2000V
0	1	1	0	0	0	0	0.9000V

CZC Technology			Quaf
Title: Power CPU			
Size: Custom	Project Name: Q10		Rev: B
Date: Thursday, February 26, 2009		Sheet 36 of 48	



CC_SET	Charge Current
3.0V	2.0A
1.5V	1.0A
0.45V	300mA
<0.15V	=CHA_OFF

State	SET_I	Charge Current
S0	1.5V	1A
S3 S5	3.0V	2A
Pre-Charge	0.3V	200mA

State	CELLS
High	3
LOW	2

CZC Technology

Quaf

Title: Power Charger OZ8602

Size: A3 | Project Name: Q10 | Rev: B

Date: Thursday, February 26, 2009 | Sheet 37 of 48

H_S1 BOSSC237PT276D118 MH24X40X65 ns
H_S2 BOSSC237PT276D118 MH24X40X65 ns
H_S3 BOSSC237PT276D118 MH24X40X65 ns
H_S4 BOSSC237PT276D118 MH24X40X65 ns
H_S11 BOSSC237PT276D118 MH24X40X65 ns
H_S12 BOSSC237PT276D118 MH24X40X65 ns
USB_GND3
VerB:ADD

FD1 FD2 FD3 FD4 FD5 FD6 FD7 FD8
FMARKC ns

H_S5 BOSSC237PT276D118 MH24X40X65 ns
H_S7 BOSSC237PT276D118 MH24X40X65 ns
H_S8 BOSSC237PT276D118 MH24X40X65 ns
H_S9 BOSSC237PT276D118 MH24X40X65 ns
H_S10 BOSSC237PT276D118 MH24X40X65 ns
GND_MBat

+V3.3S
LPC_DEBUG
FPC10 1.0mm
FPC10_1p0rt
[12,26,27] LPC_AD0
[12,26,27] LPC_AD1
[12,26,27] LPC_AD2
[12,26,27] LPC_AD3
[12,26,27] LPC_FRAME#
[7,13,14,20,25,26] PLTRST#
[17] PCICLK_LPC
MB pin10----DB pin1

[27,29,37] VIN → VIN TestP TPC60 ns
[18,29,31,32,33,36] +VDC → VDC TestP TPC60 ns
[29,30,37] BATT+ → VBAT TestP TPC60 ns
[31] 5V_LDO → V5LDO TestP TPC60 ns
[5,12,13,14,15,18,20,25,26,27,29,30,31,34] +V3.3AUX → V33AL TestP TPC60 ns
[15,18,23,26,31,32,33,34,35] +V5Aux → V5AL TestP TPC60 ns
[11,32] +V0.9S → V09S1 TestP TPC60 ns
[34] +VDCS → VDCS TestP TPC60 ns
[15,18,19,22,23,24,28,34,35,36] +V5S → V5S1 TestP TPC60 ns
[5,7,8,9,11,12,13,14,15,17,18,20,22,23,25,26,27,28,34,35,36] +V3.3S → V33S TestP TPC60 ns
[9,34] +V2.5S → V25S TestP TPC60 ns
[4,7,8,9,13,15,20,33,35] +V1.5S → V15S1 TestP TPC60 ns
[3,4,5,6,8,9,12,15,17,26,33,35] +V1.05S → V105S1 TestP TPC60 ns
[4,36] +VCC_CORE → CPUCORE TestP TPC60 ns

[26,29] PWRSW#_XP → PWRSWN TPC30 ns
[14,26,31,35] PM_RSMRST# → RSMRSTN TPC30 ns
[14,26] PM_PWRBTN# → PWRBTNN TPC30 ns
[14,26,32] PM_SLP_S4# → SLPS4N TPC30 ns
[14,26,27,32,33,34,35] PM_SLP_S3# → SLPS3N TPC30 ns
[26,32] V1_8_ON → DDR2ON TPC30 ns
[26,34,35] MAIN_ON → MAINON TPC30 ns
[26,32] V0_9S_ON → VTTON TPC30 ns
[14,26,35] MAIN_PWROK → MAINPWROK TPC30 ns
[26,33] V105S_15S_ON → V105S15SON TPC30 ns
[26,33,35] CHIP_PWROK → V105S15SPWROK TPC30 ns
[26,36] IMVP_ON → IMVPON TPC30 ns
[7,14,26,36] IMVP_PWROK → IMVPPWROK TPC30 ns
[14] ICH_PWROK → ICHPWROK TPC30 ns
[3,12] CPU_PWRGD → CPUPWROK TPC30 ns
[3,6] H_CPURST# → CPURSTN TPC30 ns
[7,13,14,20,25,26] PLTRST# → PCIRSTN TPC30 ns

[3,12] H_DPRSTP# → CPUDPRSTPN ns
[3,12] H_DPSLP# → CPUDPSLPN ns
[3,6] H_CPUSLP# → CPUSLPN ns
[3,6] H_ADS# → CPUADS ns
[14,17] PM_STPCPU# → CPUSTPCLKN ns
[12,26,27] LPC_FRAME# → LPCFRAMEN ns

+V3.3Aux
C541
0.1uF/16V,X7R

VerB: Del PWROKLED circle.

Layout note:
This Test point must be place same side and follow CPU side.

CZC Technology
Title: SCREW HOLE
Size: A3
Project Name: Q10
Rev: B
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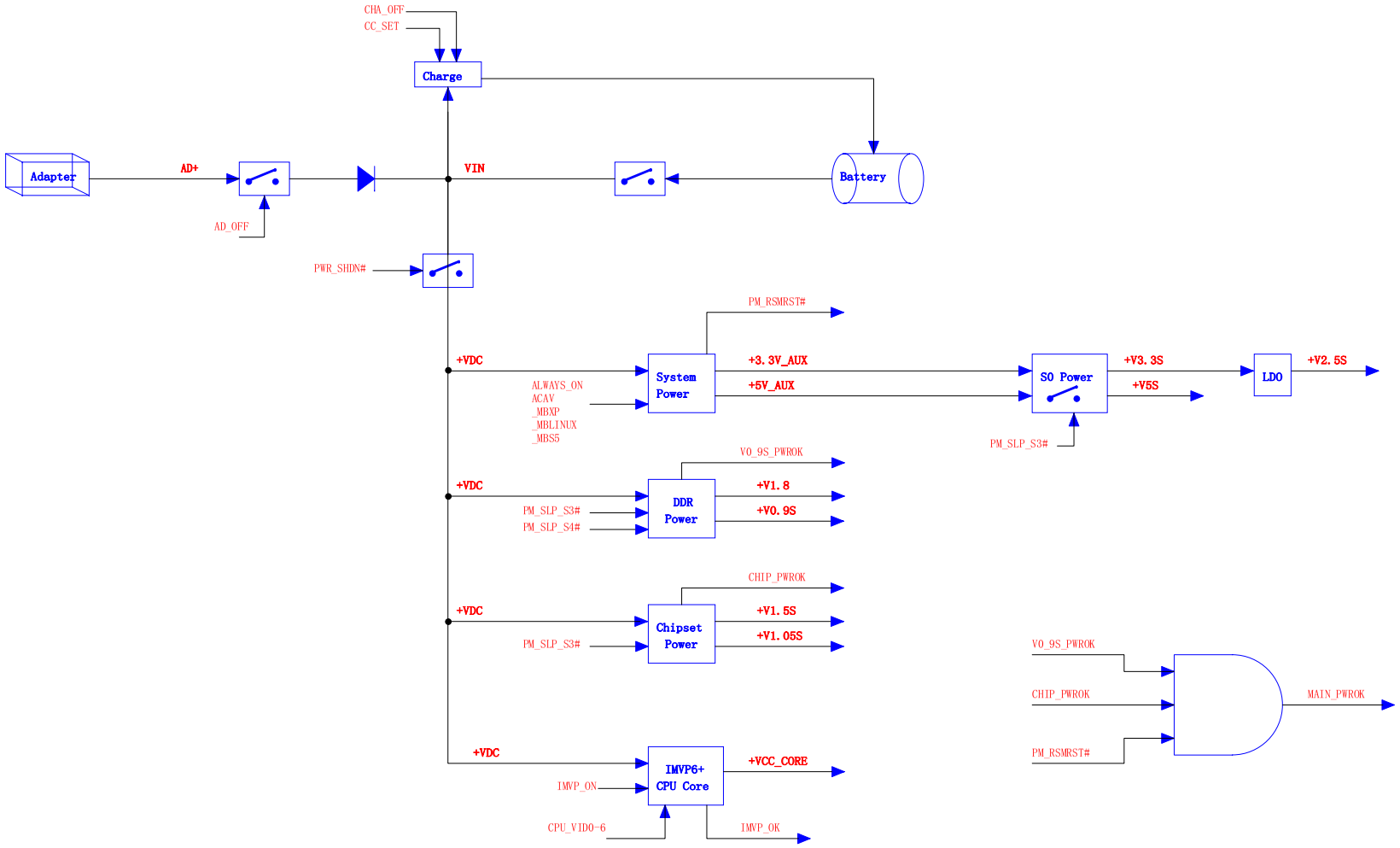

Power Plane	Voltage	Active In	Control Signal
AD+	19V +/-10%	S0 S3 S4 S5	Adapter Plug In
VIN	9-19V	S0 S3 S4 S5	Adapter or Battery Plug In
BATT+	9-12.6V	S0 S3 S4 S5	Battery Plug In
+VDC	9-19V	S0 S3 S4 S5	Adapter or Battery In and PWR_SHDN#
+5V_AUX	5V +/-5%	S0 S3 S4 S5	ALWAYS_ON/ACAV/_MBXP/_MBLINUX/_MBS5
+V5S	5V +/-5%	S0	PM_SLP_S3#
+3.3V_AUX	3.3V +/-5%	S0 S3 S4 S5	ALWAYS_ON/ACAV/_MBXP/_MBLINUX/_MBS5
+V3.3S	3.3V +/-5%	S0	PM_SLP_S3#
+V1.8	1.8V +/-5%	S0 S3	PM_SLP_S4#
+V0.9S	0.9V +/-5%	S0	PM_SLP_S3#
+V1.5S	1.5V +/-5%	S0	PM_SLP_S3#
+V1.05S	1.05V +/-5%	S0	PM_SLP_S3#
+V2.5S	2.5V +/-5%	S0	+V3.3S
+VCC_CORE	0.35-1.77V	S0	IMVP_ON

Anfeng

Power Map

Custom Q10

Size: B

Project Name

Rev

Date: Thursday, February 26, 2009

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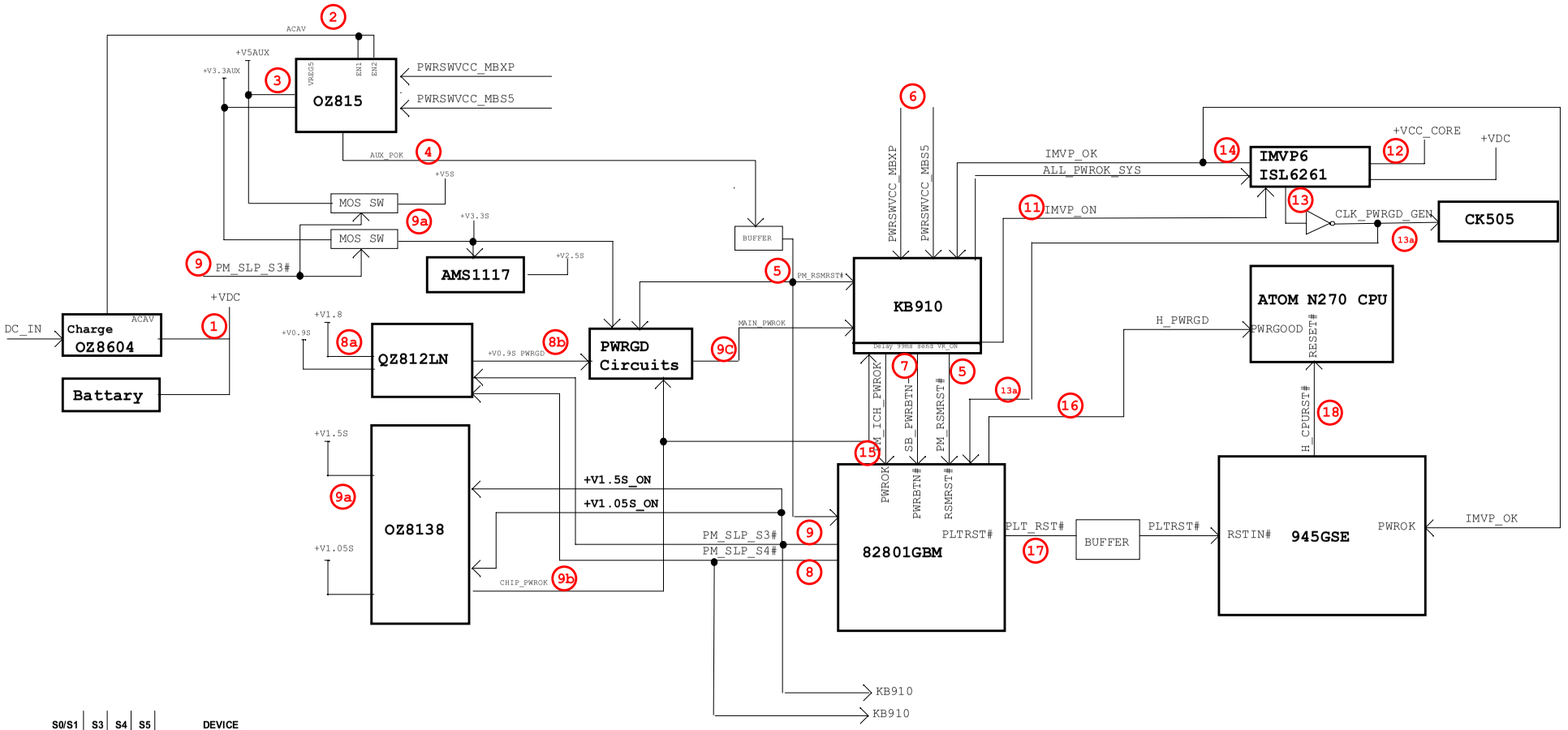


S0/S1	S3	S4	S5	DEVICE
X				VCORE
X				+V1.05S
X	X	X	X	5VAUX(AC)
X	X	X		5VAUX(BATT)
X	X	X	X	3.3VAUX(AC)
X	X	X		3.3VAUX(BATT)
X	X	X	X	ECVCC(AC)
X	X	X		ECVCC(BATT)
X				5V
X				3.3V
X				1.5V
X	X			1.8VDIMM
X				0.9V
X				VCCA
X				2.5V
X				LCDVDD,LEDVDD

CZC Technology

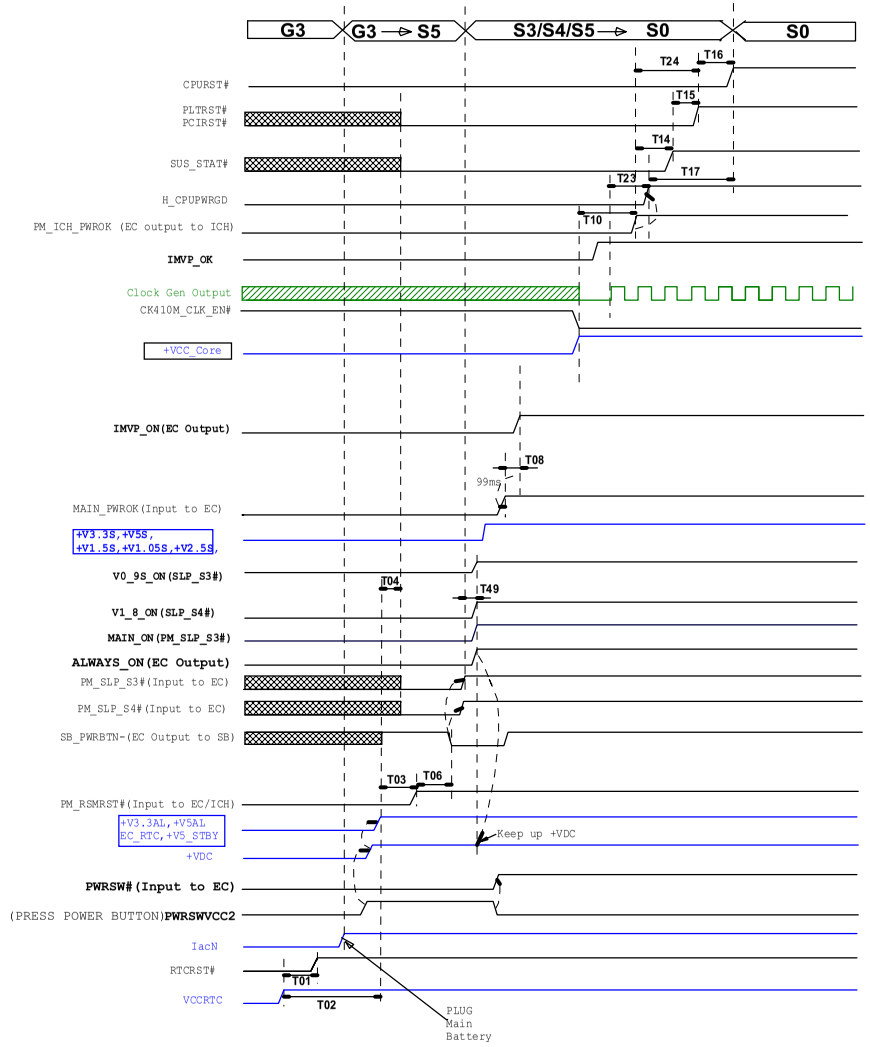
Title: Power block

Size: Custom | Project Name: Q10 | Rev: B

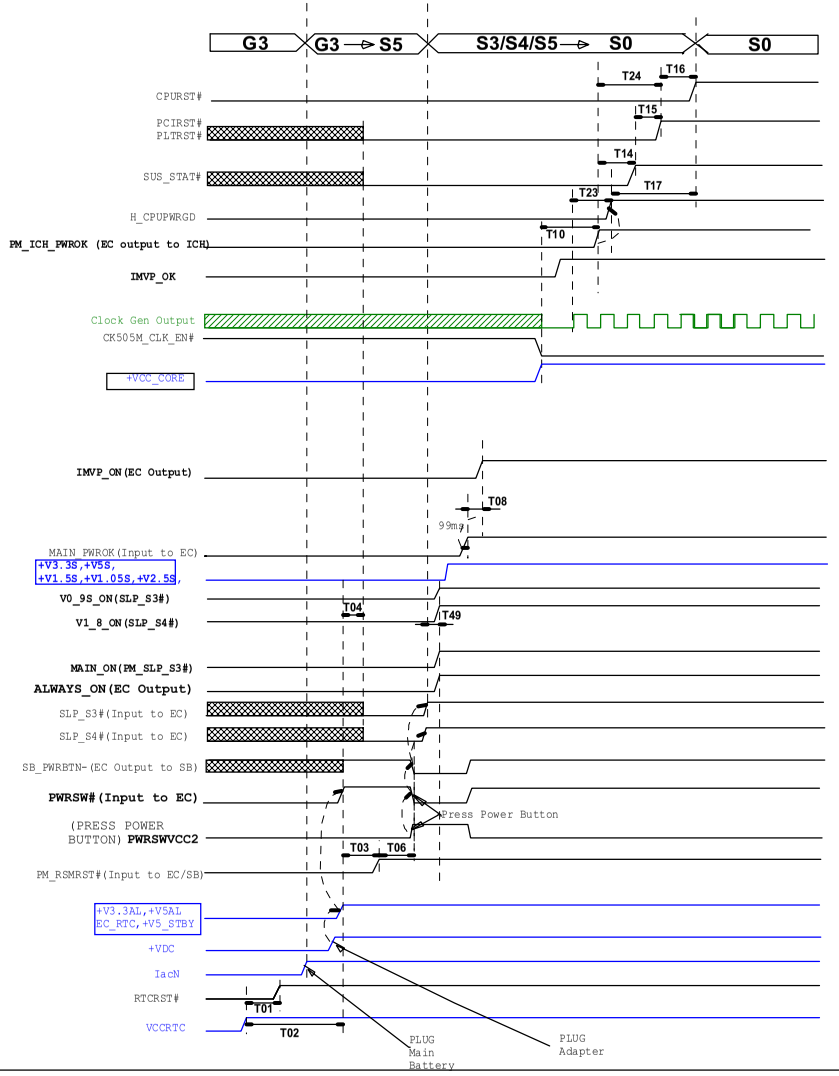
Date: Thursday, February 26, 2009 | Sheet 40 of 48

5. Power on Sequence:

Power On Sequence(Battery mode)

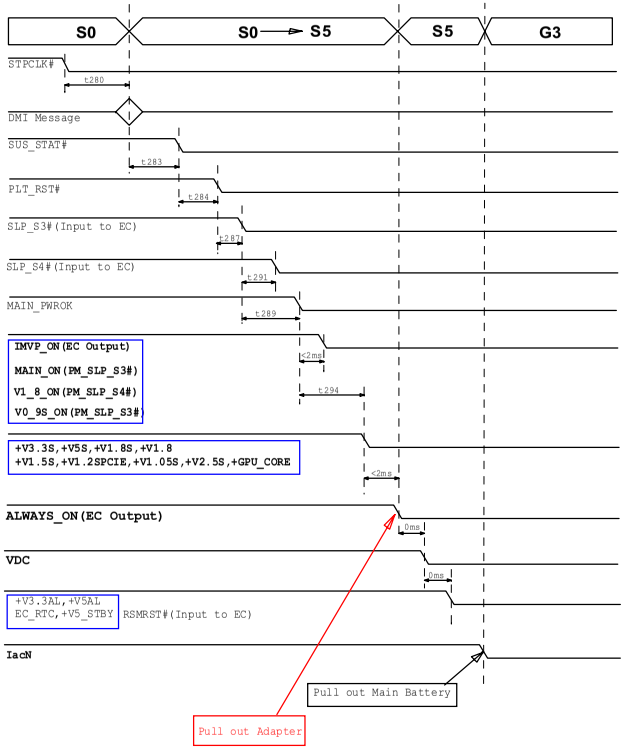


Power On Sequence(Adapter mode)



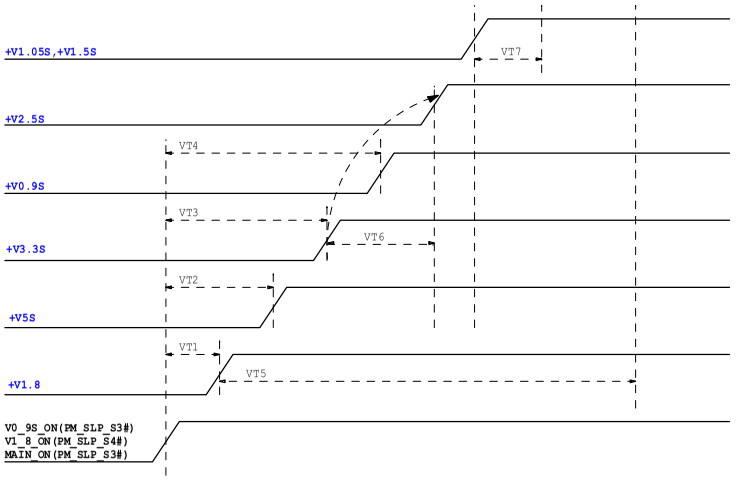
CZC Technology		Li.wang
Title: Power ON Sequence		
Size: A3	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 41 of 48	

5. Power on & off Sequence;



Detail of VCC Power on

+V3.3S,+V5S,+V1.8S,+V1.8
+V1.5S,+V1.2SPCIE,+V1.05S,+V2.5S,+GPU_CORE



CZC Technology

Li.wang

Title: Power OFF Sequence		
Size: A3	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 42 of 48	

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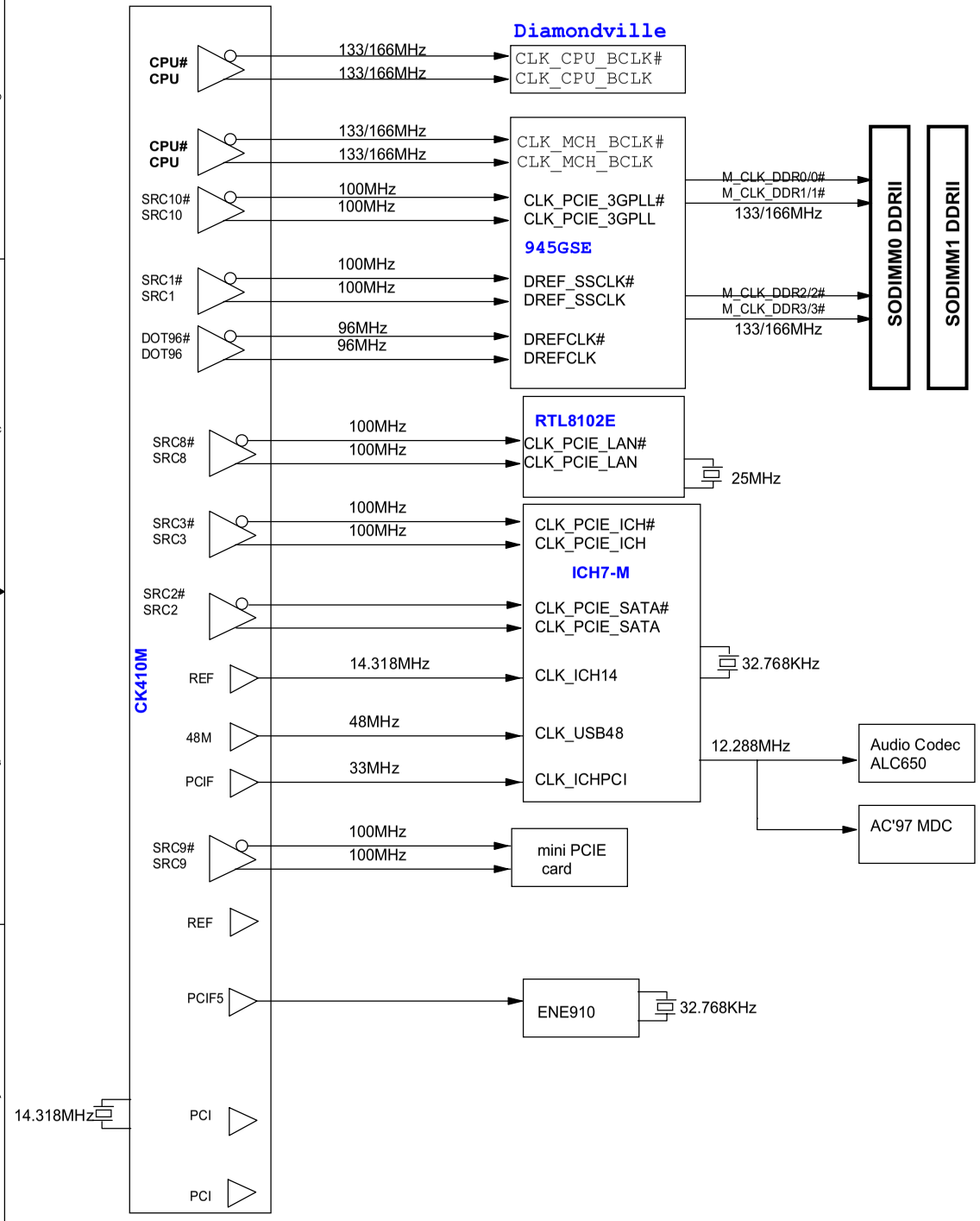
CZC Technology

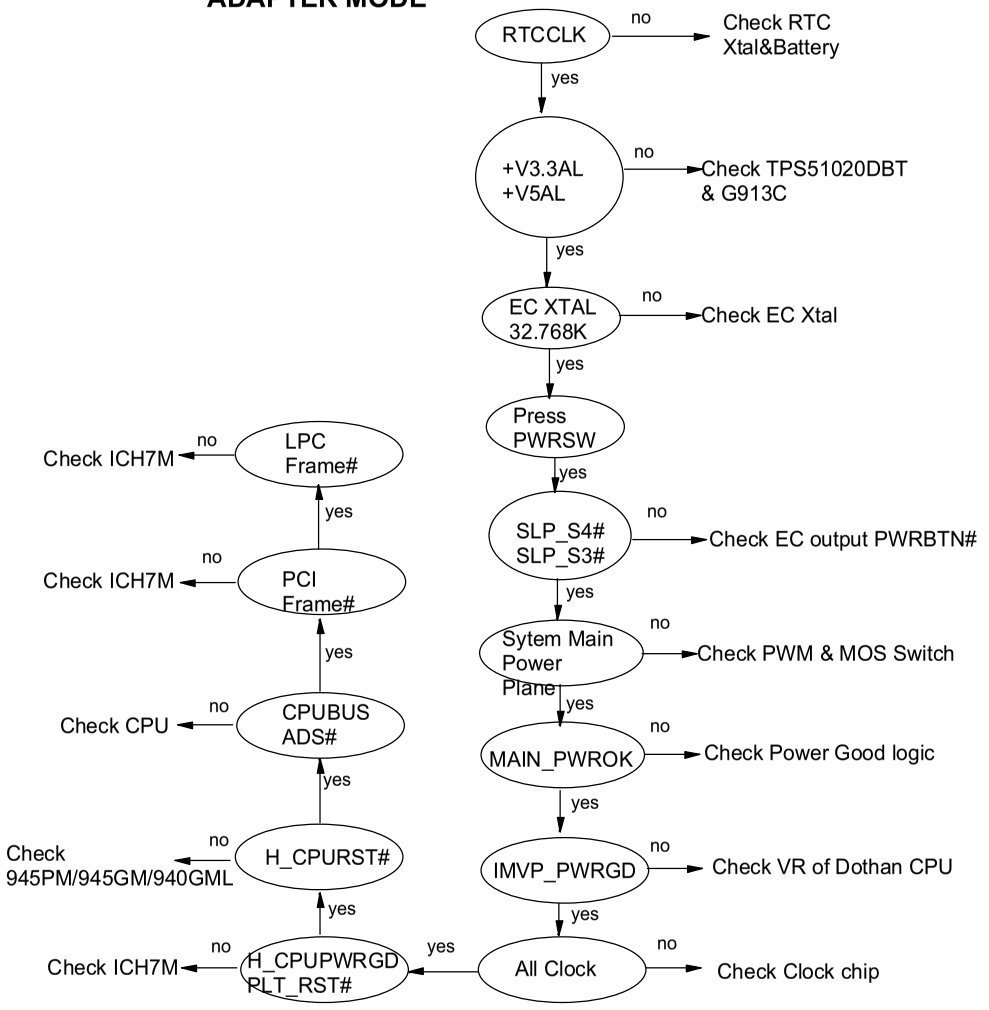
Li.wang

Title: ACPI Sequence		
Size: A	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 43 of 48	

CLOCK Distribution:



ADAPTER MODE



CLOCK Distribution			
Size	Project Name		Rev
Date: Thursday, February 26, 2009	Sheet 44	of 48	

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CZC Technology		Li.wang
Title: Notes and Annotations		
Size: A4	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 45 of 48	

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CZC Technology		Li.wang
Title: PCB Block		
Size: A4	Project Name: Q10	Rev: B
Date: Thursday, February 26, 2009	Sheet 46 of 48	

VerA To VerB List：

1. MiniPCIE 4.0mm高度的BOSS铜柱PCB板孔径要加大，不加大无法打上螺丝，参考T11
2. 需要兼容四种10.1的Panel 1024X576：HSD101PFW1,CLAA101NA0ACG亮面；CLAA101NA0ACN雾面；B101AW01 V3
3. CLK部分调FSB的需要增加上拉为+V1.05S
4. 增加EC I2Cbus输出;
5. Q10原理图和BOM中的VGA P/N改为DSUB03151005D：620501510002
6. Match 4.0mm的MiniPCIE的Boss图纸要更新，孔径太大了。
7. IO连接器上的30Pin应该用88742-3001；料号为620903023204
8. 3GPCIE1的连接器为5.6mm的MiniPCIE SLOT，Alltop C15702
9. LAN的93C46不上
10. EC要换成KB910Q C1版本的
11. KB要改成下接触的，同时PCB信号要同VERA垂直镜像。
12. PWRBTN1链接器考虑增加一个按钮信号。
13. 删去OSPWRBTN2相关电路
14. 删去PWROKLED相关电路
15. PCB版本改为B版：R228装上，R231不装；
16. 支持半卡的3G卡，参考MiniPCIE Ver1.2
17. 预留支持TCM功能
18. 将电源部分的电容默认上Sanyo POSCAP，MOSFET上AOS；
19. 将ＰＡＮＥＬ连接器更换成４０ＰＩｎ的，满足支持3种Panel的要求。

20. (2009.2.17) 除了SATAHDD板之外，将其它小板做成单独的拼板。

	Title: History1		
	Size: A	Project Name: Q10	Rev: B
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Blank

Title: History2			
Size: A	Project Name: Q10		Rev: B
Date: Thursday, February 26, 2009		Sheet 48 of 48	