LS100W Board Block Design

POWER,reset CONTROL

LED CONTROL

EEPROM (512B)

89C51ED2 (29.4912Mhz)sor

Flash ROM (64KB)

RAM (256B)

SRAM (32KB)

Wireless LAN Transceiver 802.11b

Serial Transceiver for Console

RF Antenna

DB9 Connector
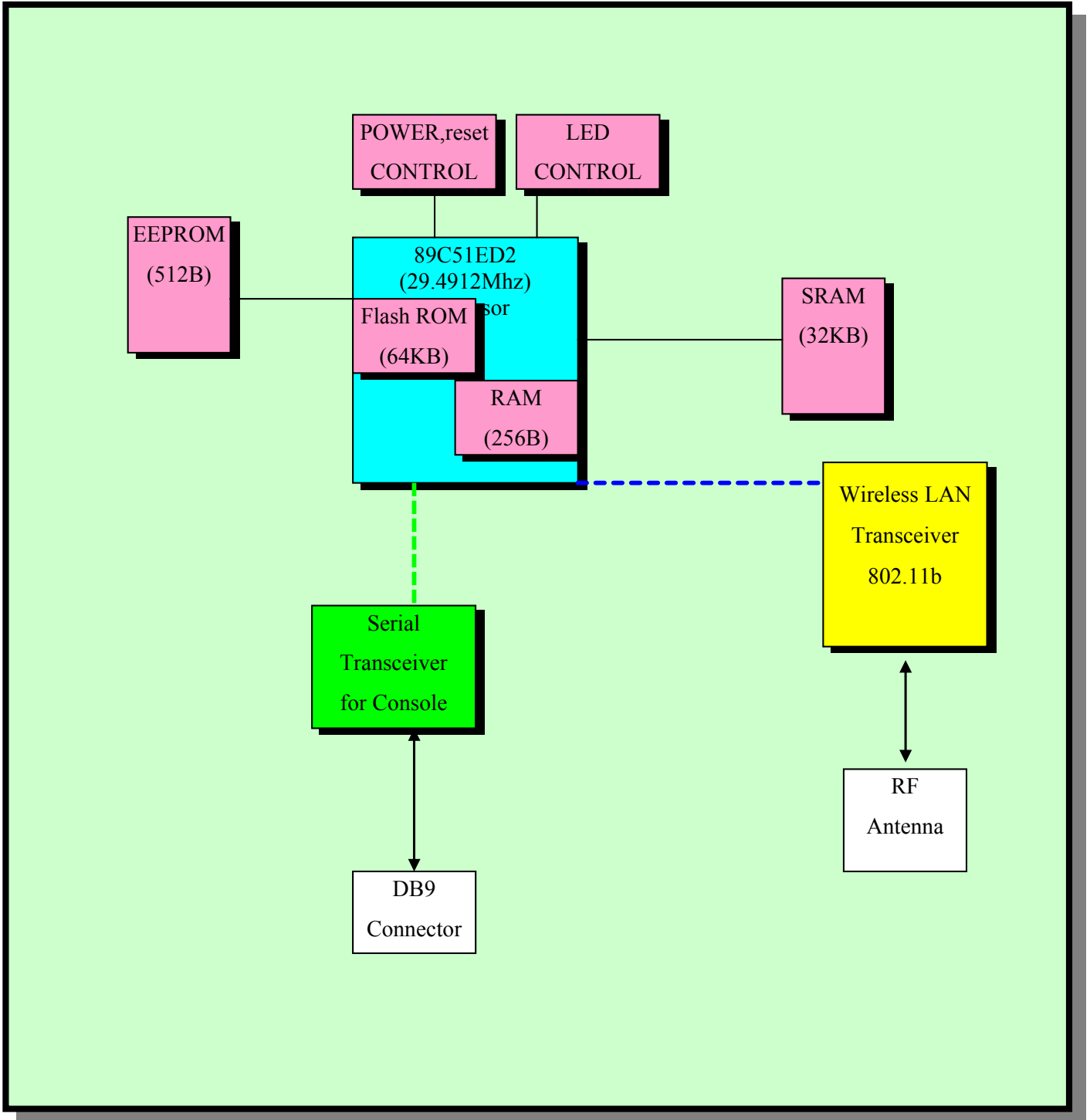
The LS100W uses Atmega 89C51ED2 CPU that is based on 8051 core specifications, and supports one Console/Serial port, and one 802.11b interface.

The LS100W board consists of

1.   Processor interface using 89C51ED2 CPU

2.   Memory interface using external RAM, and On-chip RAM

3.   Wireless LAN interface that is compliant to 802.11b specification

4.   Serial Transceiver interface that performs UART and Console operations

5.   Control interface that consists of 3.3V Power regulator and Reset control

6.   Display Interface that consists Operating status LEDs

89C51ED2 Processor interface consists of

1.   A module by using 11Mbps wireless LAN,

2.   UART module that performs UART/console operation and

3.   ISP module that writes the program into the internal flash memory.

Memory interface is included with

1.   flash memories that consists of booting program and application program,

2.   serial EEPROM that consists of Wireless LAN system information and board serial number,

3.   external RAM using the Wireless LAN data buffer, and

4.   embedded main local memory.

Wireless LAN interface is connected to the LS100W Board by using a wireless LAN transceiver and HRS connector. Further, Wireless LAN interface supports IEEE 802.11b LLC, MAC and PHY functionalities.

Control interface uses a power regulator and supports Watchdog, 5.0/3.3V power supply, and Reset timing.

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Hardware Architecture

1 Hardware Block Diagram

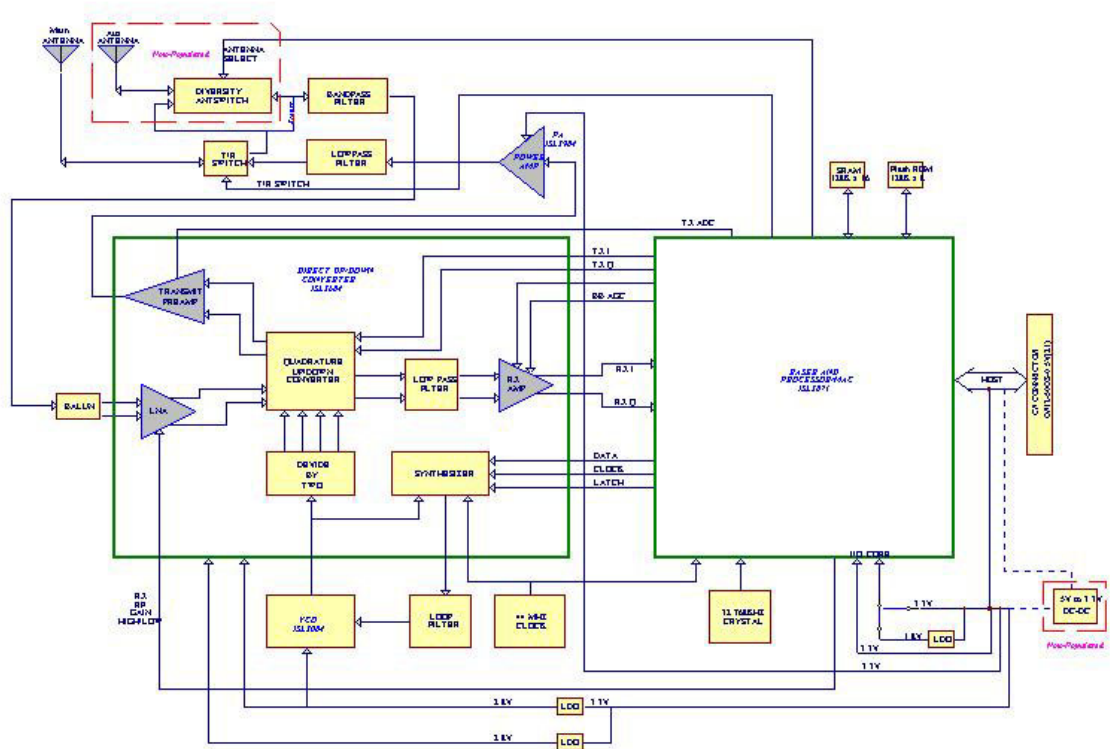The major internal components and external interfaces of the KCJ are illustrated in Figure 1.

Figure 1 KCJ Major Component and System Interface

2 Main Chipset Information

Item	Vender	Model #
MAC/BBP	Intersil	ISL3871IK18
5GHz VCO	Intersil	ISL3084
Direct Down Conversion Transceiver	Intersil	ISL3684A
RF PA	Intersil	ISL3984

2.1 MAC/Baseband Processor

The Intersil ISL3871 Wireless LAN Integrated Medium Access Controller with Integrated Baseband Processor is part of PRISM 2.4 GHz radio chip set. Protocol and PHY support are implemented in firmware. Differential phase shift keying modulation schemes DBPSK and DQPSK, with data scrambling capability, are available with Complementary Code

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Keying to provide a variety of data rates. Both Receive and Transmit AGC functions with 7-bit AGC control obtain maximum performance in the analog portions of the transceiver.

2.2 5GHz VCO

The ISL3084 is a 5GHz SiGe monolithic VCO circuit designed to simplify and reduce the cost and size of miniature wireless transceivers.

2.3 Direct Down Conversion Transceiver

The Intersil ISL3684A is a highly integrated UHF2 process, direct down conversion transceiver and is part of the PRISM 3, 2.4GHz 11Mbps, 802.11b compliant radio chipset. The ISL3684A directly interfaces with the Intersil's Integrated LAN medium access controller (MAC) with baseband processor (ISL3871). The addition of the ISL3984 Intersil power amplifier completes the LAN radio application.

2.4 Power Amplifier and Detector

The ISL3984 is a 2.4GHz monolithic SiGe Power Amplifier designed to operate in the ISM Band.

3 Pin Definition

| Pin Number	Pin Name	Pin I/O Type	Description
1	RF_VCC	Power, 0.35A	DC Power Supply 3.3V ±5%
2	RF_VCC	Power, 0.35A	DC Power Supply 3.3V ±5%
3	RF_VCC	Power, 0.35A	DC Power Supply 3.3V ±5%
4	RF_VCC	Power, 0.35A	DC Power Supply 3.3V ±5%
5	A00	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Address Input, Bits 0
6	D00	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 0
7	A01	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Address Input, Bits 1
8	D01	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 1
9	A02	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Address Input, Bits 2
10	D02	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 2
11	A03	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Address Input, Bits 3
12	D03	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 3
13	A04	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Address Input, Bits 4
14	D04	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 4
15	A05	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Address Input, Bits 5
16	D05	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 5
17	A06	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Address Input, Bits 6
18	D06	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 6

19	A07	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Address Input, Bits 7
20	D07	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 7
21	A08	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Address Input, Bits 8
22	GND	Ground	Digital Ground
23	A09	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Address Input, Bits 9
24	D08	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 8
25	GND	Ground	Digital Ground
26	D09	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 9
27	OE#	5V tol, BiDir, 2mA, 50K Pull Up	Host PC Card Memory Attribute Space Output Enable
28	D10	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 10
29	WE#	5V tol, COMS, Input, 50K Pull Up	Host PC Card Memory Attribute Space Write Enable
30	D11	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 11
31	IORD#	5V tol, BiDir, 2mA, 50K Pull Up	Host PC Card I/O Space Read Strobe
32	D12	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 12
33	IOWR#	5V tol, BiDir, 2mA, 50K Pull Up	Host PC Card Space I/O Write Strobe
34	D13	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 13
35	CE1#	5V tol, BiDir, 2mA, 50K Pull Up	Host PC Card Select, Low Byte
36	D14	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 14
37	CE2#	5V tol, BiDir, 2mA, 50K Pull Up	Host PC Card Select, High Byte
38	D15	5V tol, BiDir, 2mA, 50K Pull Down	Host PC Card Data Bus, Bits 15
39	GND	Ground	Digital Ground
40	GND	Ground	Digital Ground
41	RESET	5V tol, COMS, ST (Schmitt Trigger) Input, 50K Pull Up	Hardware Reset,
42	IREQ#	5V tol, BiDir, 2mA, 50K Pull Up	Host PC Card interrupt Request (I/O Mode), also used as WLAN module Ready (Memory Mode) output which is asserted to indicate module initialization is complete
43	REG#	5V tol, BiDir, 2mA, 50K Pull Up	Host PC Card Attribute Space Select Memory mode: H for common memory, L for attribute memory. The signal must be low during I/O cycles when the I/O address is on the bus.

44	WAIT#	COMS Output, 4mA, 50K Pull Up	Host Wait,
45	RF_LED#	Input, 9mA	LED cathode
46	IOIS16#	Pull Low, Output	8 Bits or 16 Bits I/O Card selected L: 16 bit or odd byte only operation
47	STSCHG#	COMS Output, 4mA 50K Pull Up	Host PC Card Status Change To show the BVD1 (Battery Voltage Detect), BVD2, WP (Write Protect), or Ready status changed.
48	CD1#	Pull Low, Output	Card Detect
49	GND	Ground	Digital Ground
50	INPACK#	CMOS BiDir, 2mA, 50K Pull Up	Host PC Card I/O Decode Confirmation It is asserted by the module when it is selected and responding to an I/O read cycle. It is used to control the HBA (Host Bus Adaptor) tri-state buffer on/off)

4 LED connection suggestion:
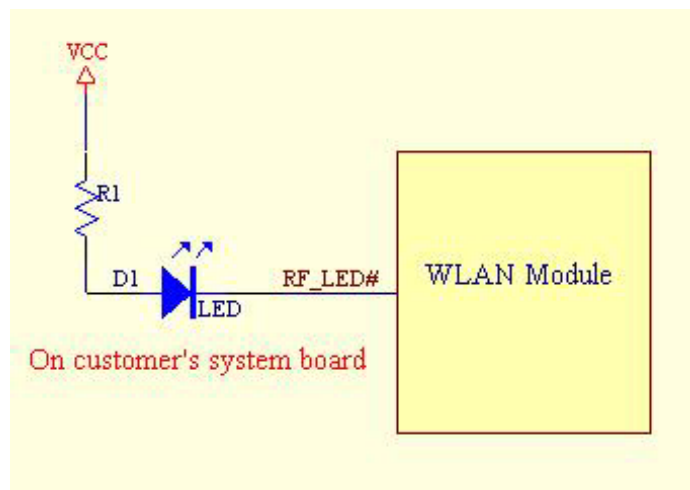
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5 LED behavior

	Infrastructure Mode		802.11b Ad Hoc Mode	System Standby
	Seeking for connection	Connected		
LED	Blinking	On	On	Blinking

6 Antenna Interface

   a. Impedance: 50 ohm
   b. Connector Type: HRS U.FL-R-SMT, Mating connector: U.FL-LP
   c. External antenna adopted SMA connector type with a left-handed connector structure,so that common SMA connector can not be connected.