BCM-860S Schematic Descriptions

Bellwave

1. Introduction

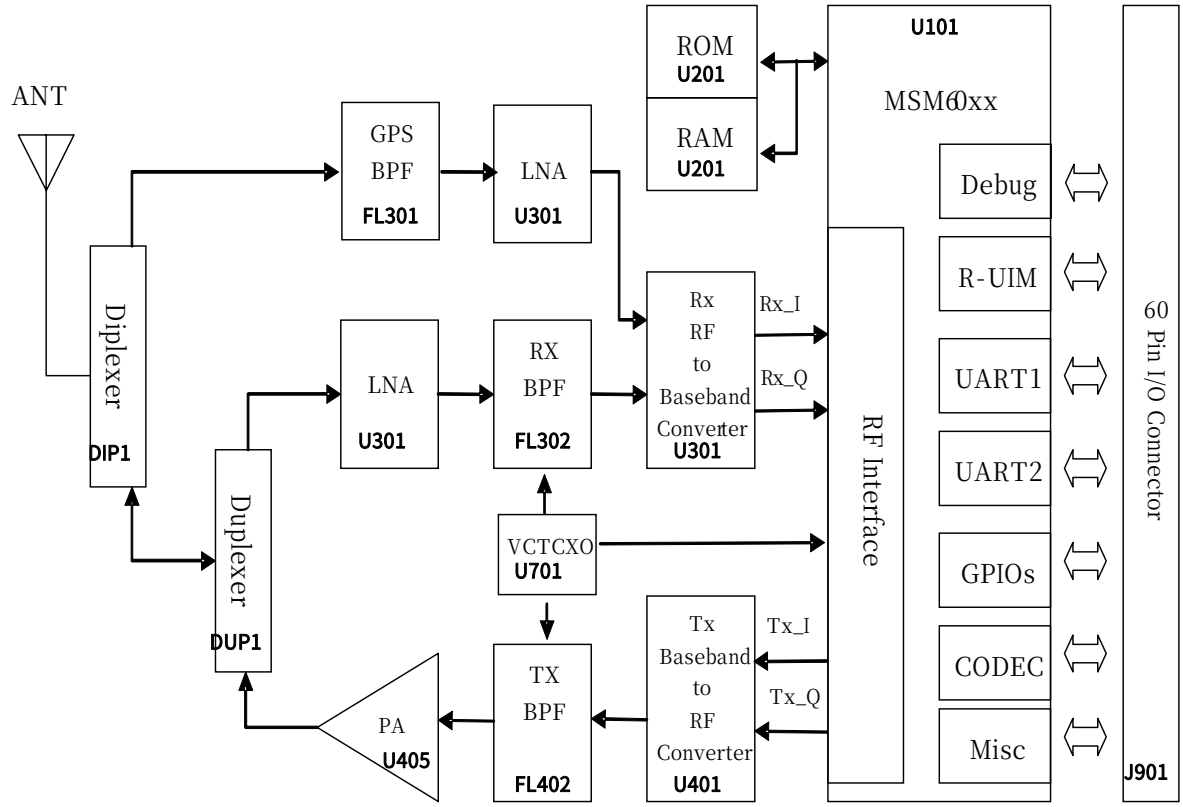


Figure 1-1. BCM-860S Blcok Diagram

This document describes BCM-860S Cellular CDMA Module. BCM-860S is a Cellular CDMA Module including GPS function(gpsOne), using the radioOne chipsets. The radioOne chipsets(Qualcomm's Zero-IF chipsets) implement direct conversions from RF to baseband and vice versa, completely eliminating receive and transmit intermediate frequencies to reduce component count and space. This radio architecture is referred to as Zero-IF (or ZIF), emphasizing that there is no IF or that IF is really baseband, centered at zero hertz. The Cellular CDMA radioOne chipset eliminates even more components by integrating the LNA and VCO functionality into only one receiver chip.

Figure 1-1 shows the block diagram of the BCM -860S cellular CDMA module.

2. Functional Descriptions

2.1 Diplexer (DIP1)

The BCM-860S Cellular CDMA module equipped a common antenna port and a diplexer for receiving CDMA and GPS signals and radiating CDMA signal.
A diplexer allows multiple operating bands to share the same antenna. In the BCM-860S Celluar CDMA module, a common antenna serves both bands - cellular CDMA and GPS, using a diplexer to separate the bands. The diplexer combines the signal paths from cellular CDMA and GPS bands into a common port. One antenna collects Cellular base station and GPS satellite forward link signals and radiates the handset Cellular reverse link signal.

- CDMA Freauency Band: 824MHz ~ 894MHz
- GPS Frequency Band : 1570MHz ~ 1580MHz

2.2 Duplxer (DUP1)

A duplexer splits a single operating band into receive and transmit paths. The duplexer provides input selectivity for the receiver, output filtering for the transmitter, and isolates between CDMA RX and TX signals.

- Center Frequency TX : 836.50MHz
- Center Frequency RX : 881.50MHz

2.3 LNA (U301)

There are two LNAs(Low Noise Amplifier) in the RFR6125 Receiver IC(U301). One is used for Cellular CDMA, the other is used for GPS. Cellular CDMA and GPS receive signals are amplified by the LNAs then pass through bandpass filters before being applied to the RFR6125 Receiver ICAll receive signals are downconverted directly from RF to baseband within the Receiver IC.

2.4 GPS Band Pass Filter(FL301)

The GPS RF filter is located before its LNA(U301). BCM-860S CDMA module does not include a GPS transmitter so there are no Tx-band leakage attenuation requirements. Using a single-ended filter will improve GPS sensitivity.

- Pass band Frequency : 1574.42 - 1576.42 MHz

- Center Frequency : 1575.42 MHz

2.5 Rx Bandpass Filter(FL302)

A Cellular Rx Bandpass filter(FL302) is located between its LNA and mixer(U301).
The transmitter channel power, although attenuated by the duplexer(DUP1), still presents a cross-modulation threat in combination with Rx-band jammers. The RF filter(FL302) must provide rejection of this Tx-band leakage.
Rx Bandpass filter(FL302) takes a single-ended output from the LNA and provides differential outputs.

- Pass band Frequency : 869 ~ 894 MHz
- Center Frequency : 881.5 MHz

2.6 TX Bandpass Filter(FL402)

The transmitter RF BPF(FL402) rejects out-of-band spurious signals and RFT6120 broadband noise to assure compliance with the applicable emissions standards.

- Pass badn Frequency : 824 - 849 MHz
- Center Frequency : 836.5 MHz

2.7 RX RF Receiver IC-RFR6125(U301)

The RFR6125 IC (U301) provides the Zero-IF receiver signal paths for Cellular and GPS signals. The Cellular path begins with a four gain-state LNA, followed by the external Cellular RX bandpass filter(FL302) that provides transformation between the single-ended 50-Ohm LNA output and the differential second-stage amplifier input.
An external filter is not required between the LNA and downconverter in the GPS path, so only the GPS LNA input is accessible. The GPS input signal level has a relatively narrow range, requiring significantly less dynamic range than the Cellular path and allowing a fixed gain LNA.
Amplifier outputs drive the RF ports of the quadrature RF-to-baseband downconverters (a dedicated downconverter for each band)(U301). The downconverted baseband outputs are multiplexed and routed to lowpass filters (one I and one Q) whose passband and stopband characteristics are multiplexed and routed to lowpass filters (one I and one Q) whose passband and stopband characteristics are mode dependent. The filter outputs are buffered and routed to the MSM6050 device for further processing.

Numerous secondary functions are integrated on-chip as well: the Rx LO generation and distribution circuits, Cellular and GPS VCO circuits, and various interface, control and status circuits

There are two integrated VCOs on-chip, one for Cellular operation and one for GPS. The VCOs are tuned via the RFT6120's Rx PLL when active, and share an output buffer amplifier to deliver the PLL feedback signal to the RFT device. The active VCO signal is processed by the LO generation and distribution circuits to create the appropriate LO signal (Cellular-CDMA or GPS). In all cases, the LO signals applied at the mixer ports are at a frequency different than the VCO frequency. This assures that the VCO frequency is different than the RF frequency, an important consideration for Zero-IF processing.

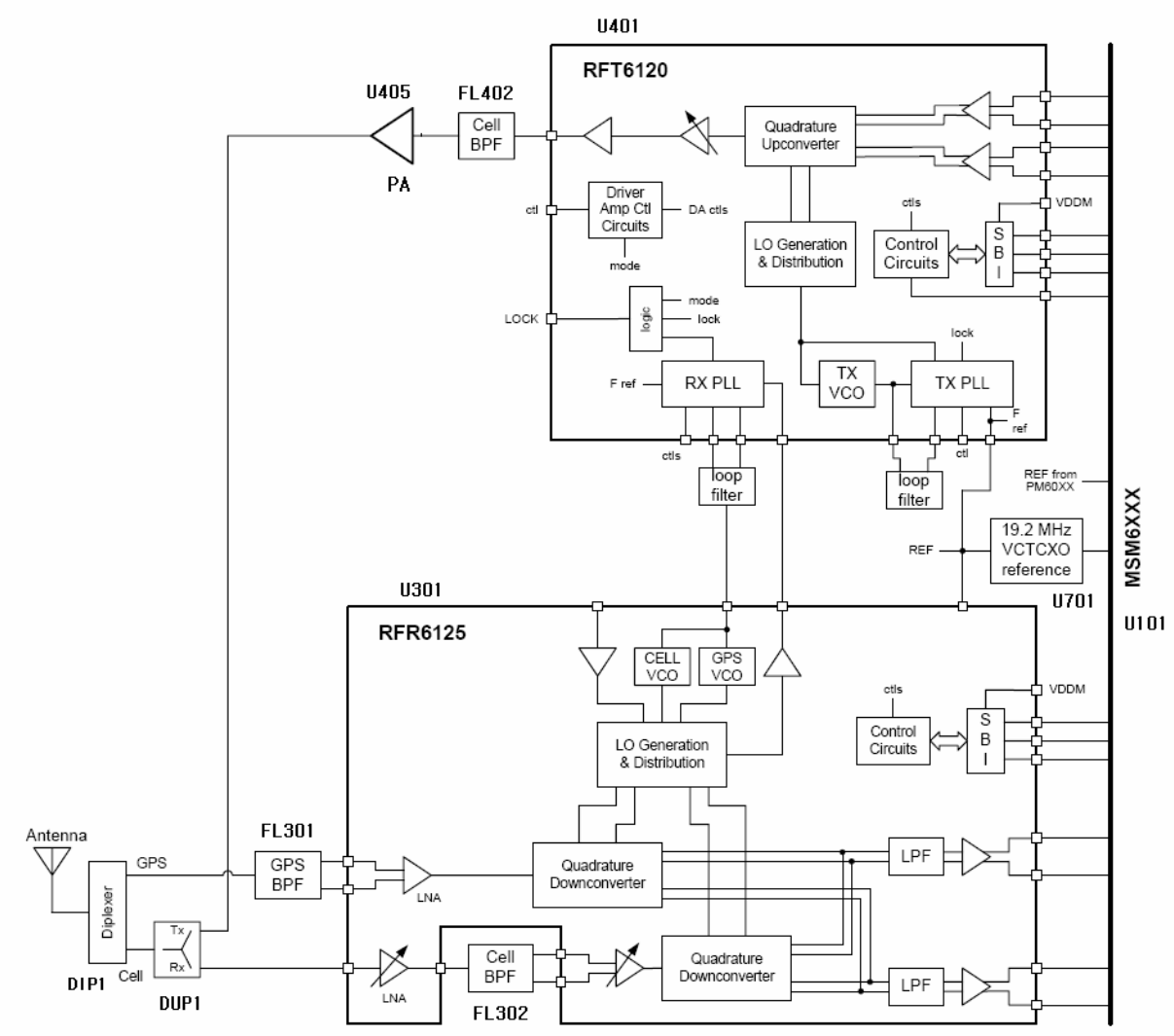


Figure 2-1. Cellular CDMA and GPS Functional Block Diagram

2.7 TX RF Transmitter IC – RFT6120(U401)

The RFT6120 IC (U401) provides the Zero-IF transmitter signal path, from analog baseband to RF driver amplifiers, for Cellular CDMA-only handsets. The MSM device provides I and Q differential CDMA baseband signals; these analog input signals are amplified and applied to the upconverter mixers(U401). The RF circuits include multiple variable gain stages that provide transmit AGC under MSM device control.

The RFT6120 IC(U401) includes a number of secondary functions in addition to the transmit signal path: a reference for the transmit DACs, two phase-locked loop circuits (Tx LO and Rx LO), the Tx VCO circuit, Tx LO generation and distribution circuits, and various interface, control and status circuits.

Virtually the entire transmitter LO synthesizer is included within the RFT6120 IC(U401); only the loop filter(is off-chip. The phase-locked loop (PLL) circuits include a reference divider, phase detector, charge pump, feedback divider, and digital logic that generate LOCK status. The entire Tx VCO is on-chip as well.

The RFT6120 IC integrates significant Tx LO generation and distribution circuits on-chip. These circuits operate in various modes to yield a highly flexible quadrature Tx LO output that drives the Cellular upconverter(U401). A separate phase-locked loop circuit, identical to the PLL portion of the Tx LO synthesizer, is integrated on-chip to support the receivers' RF-to-baseband downconverter.

2.8 Power Amplifier (U405)

This is a key component in the transmitter chain and must complement the RFT6120 IC.

PA(U405) takes a CDMA RF output from the TX BPF(FL402) and provides a amplified output to the antenna port. The transmitter output power depends upon the operating band class and mobile station class per the applicable standard.

There are two control lines from the MSM6050 IC(U101) to the power amplifier(U405).

PA_R1 (pin E16) connected to the VMODE pin of the Power Amplifier, sets the output power range (reducing DC dissipation when high Tx output power is not required).

PA_ON[0] (pin H16) – the Power Amplifier on/off control signal.

2.9 VCTCXO(U701)

The Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO) provides the reference frequency for all RF IC synthesizers as well as clock generation functions within the MSM6050 IC. The MSM6050(U101) requires a **19.2 MHz** nominal VCTCXO frequency**.** The oscillator frequency is controlled by the MSM6050's TRK_LO_ADJ pulse density modulated signal.
The filtered PDM signal results in an analog control signal into the VCTCXO tuning port whose voltage is directly proportional to the density of the digital bit stream. The MSM device varies the pulse density to change the analog control voltage that sets the oscillator frequency.

2.10 Receiver PLL

Rx LO functional blocks are distributed between the RFR6125 IC(U301), RFT6120 IC(U401) and loop filter components(C402, C403, R402, R403). A Cellular VCO and a GPS VCO are inside the RFR6125 IC(U301). The internal VCOs are enabled within the RFR6125 IC via SBI. Using only the selected VCO signal, the RFR6125 Rx LO generation and distribution circuits create the necessary LO signals for the active quadrature downconverter.
A sample of the active VCO is buffered and routed from RFR6125 pin 16 (LO_OUT) to RFT6120 pin 15 (RX_LO_IN). A series capacitor(C309) provides an adequate match between the RFICs.
Most Rx PLL circuits are included within the RFT6120 IC(U401): reference divider, phase detector, charge pump, feedback divider, and digital logic that generate LOCK status. The buffered 19.2 MHz TCXO(U701) signal provides the synthesizer input (REF), the frequency reference to which the PLL is phase and frequency locked. The reference is divided by the R-Counter to create a fixed frequency input to the phase detector, FR. The other phase detector input (FV) varies as the loop acquires lock, and is generated by dividing the active VCO frequency using the feedback path's N-Counter. The closed loop will force FV to equal FR when locked. If the loop is not locked, the error between FV and FR will create an error signal at the output of the charge pump. This error signal is filtered by the loop filter and applied to the VCO, tuning the output frequency such that the error is decreased. Ultimately the loop forces the error to approach zero and the PLL is phase and frequency locked.

2.11 Transmitter PLL

All Tx LO functional blocks are integrated into the RFT6120 IC(U401) except the loop filter components. On-chip circuits include reference divider, phase detector, charge pump, Tx VCO, feedback divider, and digital logic that generate LOCK status. The off-chip loop filter allows optimization of key PLL performance characteristics (stability, transitory response, settling time, and phase noise) for different applications.

2.12 MEMORY(U201)

In the BCM-860S Cellular CDMA module, a MCP memory is used which integrates a Flash ROM and a pSRAM in the single package.

- Flash ROM size : 64Mbits
- pSRAM size : 16Mbits

3. Matching Networks

3.1 Cellular Path

The Cellular path (Figure 3-1) begins with the RFR6125 LNA that requires matching at its input port (pin40, CLNA_IN) and output port (pin3, CLNA_OUT). RF circuits can be matched to optimize various performance parameters such as power transfer, IIP3, impedance, or noise figure, but the final implementation is usually a compromise that provides adequate performance of all parameters but may not optimize any one.

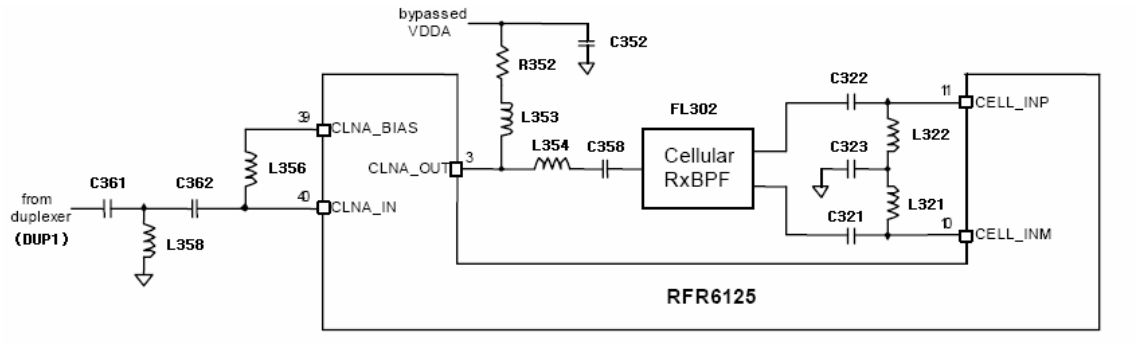


Figure 3-1. Cellular path matching Networks

The LNA input circuit provides a shunt inductor(L356) that serves a dual purpose: it is part of the matching network and provides a DC bias path from the CLNA_BIAS pin to the CLNA_IN pin. A shunt inductor(L358) and a series capacitor(C362) complete the input-matching network.

The LNA output circuit also includes a dual-purpose shunt inductor(L353), affecting the RF match and providing a DC bias path. The bias current flows through the resistor(R352) and the required L353 inductor into the LNA output pin.

A differential configuration is used at the Cellular-band's second-stage amplifier input (CELL_INP and CELL_INM) to improve isolation relative to single-ended implementations. Furthermore, Cellular operation requires a high selectivity filter to reject Tx leakage, thereby suppressing cross-modulation. A bandpass filter that transforms its single-ended input to a differential output fulfills both these requirements. The differential configuration into the Cellular second-stage is required.

Common-mode rejection and second-order non-linearity is improved using well-balanced, differential mixer input, LO, and output ports. The RFR6125(U301) Cellular second-stage amplifier input is essentially the RF port of the downconversion mixer. The balance between

the complementary signals is critical and must be maintained from the RF filter outputs all the way into the IC pins. The complementary inputs, plus and minus, require a low impedance path for low frequency distortion products. This is accomplished using an inductor from each pin, connected to a common bypass capacitor to ground. The capacitor (C323) provides RF ground, but its more critical function is to shunt the low frequency distortion terms to ground.

3.2 GPS path

GPS input filter requirements are greatly reduced (compared with the Cellular path), eliminating the need to filter the LNA output before applying it to the downconversion circuits. Hence, pins accessing an external filter are not required between the GPS LNA and downconverter(U301). This reduces the GPS matching requirements to a single interface – the GPS LNA input.

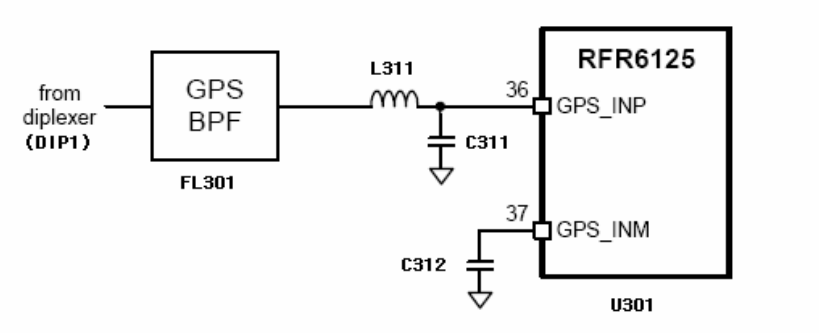


Figure 3-2. GPS path

Although a differential configuration (when implemented properly) improves isolation, common-mode rejection, and second-order non-linearity, it also introduces loss. A single-ended filter may reduce insertion loss.

While the Cellular second-stage differential input required a low frequency/low impedance path to ground from each pin, this is not required at the GPS LNA input. The GPS mixer is embedded further inside the IC, eliminating this requirement – a single inductor without a center-tap capacitor is sufficient.

4. MSM6050 and RF Infaces

4.1 SBI Interfaces

MSM6050(U101) controls RFR6125 IC(U301) operating modes and circuit parameters through the proprietary 3-line Serial Bus Interface (SBI). A separate, auxiliary SBI interface is used to control the RFT6120 IC, avoiding corruption of transmit signals through noise and transients from the RFR.

SBIs provide efficient initialization, control of device operating modes and parameters, and verification of programmed parameters. The MSM device's SBI controllers are the Masters while the RFICs are Slaves. The three SBI and auxiliary SBI signals have dedicated functions

- The Serial Bus Strobe signal (SBST) is used to initiate serial data transfers
- The Serial Bus Data line (SBDT) is a bi-directional data line that transfers data into and out of the ICs. All ICs configure this line as a tri-state driver for output functions and as a CMOS gate for input functions.
- The Serial Bus Clock (SBCK) is the clock signal that synchronizes data transfers.

4.2 Transmitter Functions

The RFT6120 transmitter (U401) parameters, MSM-controlled via the auxiliary SBI, include the following:

- Operating mode (Power down, Tx puncture, or Tx).
- Circuit gains, bias conditions, and output drive levels.
- Puncture internal controls.
- Tx PLL and on-chip VCO (for Cellular Tx LOs).
- Rx PLL (for Cellular Rx and GPS LOs).
- Tx LO generation mode and parameters.
- Tx VCO controls.

In addition to auxiliary SBI controls there are two dedicated control lines from the MSM6050(U101) to the RFT6120 IC(U401):

1. A digital line that controls Tx puncturing, pin E14 (TX_ON). This is a direct connection between the two ICs; it should be routed as directly as possible while avoiding sensitive analog, LO, and RF signal traces and circuits.
2. An analog control signal formed by filtering a PDM signal from the MSM6050 IC (pin E15, TX_AGC_ADJ). The filtered control signal is applied to the RFT6120 pin 21

(VCONTROL) to implement CDMA transmit gain control.

A filtered pulse density modulated (PDM) signal is used to provide analog control of the transmitter gain as follows: the MSM6050 IC (U101) outputs a stream of digital pulses, varying the density of pulses within the stream. A series resistor(R101) followed by a shunt capacitor(C118) lowpass filters the pulse stream to remove its high frequency components and pass its low frequency and DC components. If the stream held a constant pulse density the DC component at the filter output would be proportional to its average density.

The MSM6050(U101) and RFT6120(U401) ICs include a four-line interface for Tx analog baseband signals. These four lines are configured as two differential pairs – one pair for the in-phase component and one pair for the quadrature component(,). The MSM device in-phase component has a positive(TX_I+) and a negative (TX_I-) output, as does the quadrature component (TX_Q+ and TX_Q-).
The transmit baseband signals are generated by digital-to-analog converter (DAC) circuits within the MSM6050 IC.

The RFT6120 IC(U401) includes two phase-locked loop (PLL) circuits that synthesize the necessary LO signals for the handset receivers and transmitter. The handset supports Cellular and GPS bands, and different channels within the Cellular band, by tuning the LO signals in response to MSM programming of the PLLs via the SBI.
In addition to SBI controls, the PLLs report their status using the dedicated RFT6120 LOCK signal. The status of all active RFT6120 PLLs factor into the single LOCK indication. If all active PLLs are locked, the LOCK signal is high. If any active PLL is not locked, the LOCK signal is low. The MSM modulator requires LOCK signal to be high for transmission.

4.3 Receiver Functions

Both the Cellular and GPS receivers employ the radioOne Zero-IF architecture that converts RF signals directly to baseband. The RFR6125 receiver parameters MSM-controlled via the SBI include the following:

- Operating band (Cellular or GPS).
- Operating mode (Sleep, Warm-up, Rx, or Rx/Tx).
- Circuit gains, bias conditions, and output drive levels.
- LO generation circuit controls.

■ Cellular and GPS VCO controls.

The RFR6125 baseband receive signal output pins connect directly to the MSM60xx input pins. Recognize that the I and Q baseband outputs are configured as differential pairs: the in-phase component has a plus (RX_I+) and a minus (RX_I-) output, as does the quadrature component (RX_Q+ and RX_Q-).

5. DC power Distribution

The DC power circuits use an external supply or the handset's battery to establish the phone's raw DC power. The raw power is applied to regulator circuits, filters, and bypass capacitors that provide clean DC power to all the other handset functions.

+3.0V_MSMP – MSM Pad Voltage, also used to power RFIC digital I/O circuits.

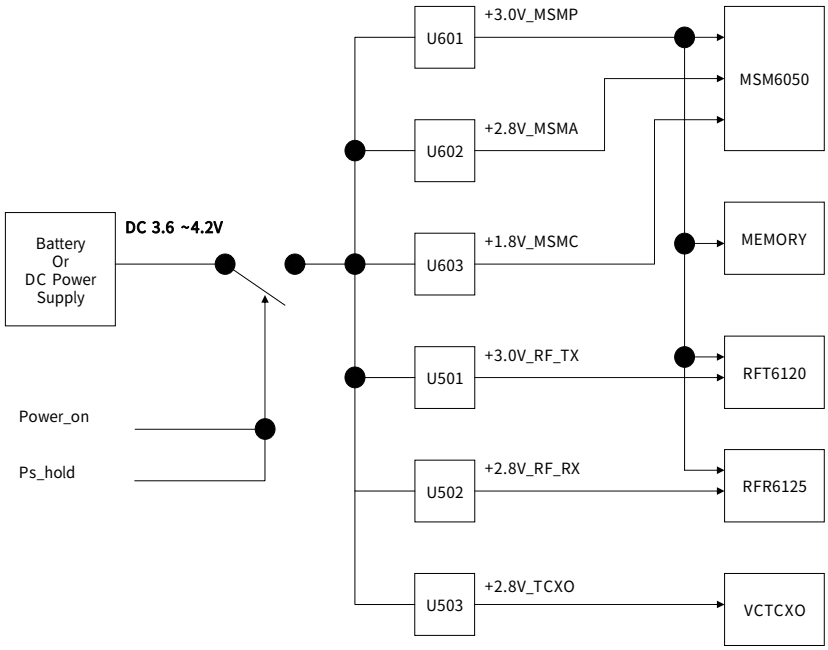
+2.7V_MSMA – MSM Analog Voltage

+1.8V_MSMC – MSM Core Voltage

+2.8V_RF_RX – Supply voltage for most receiver circuits (RFR6125).

+3.0V_RF_TX – Supply voltage for most RFT6120 transmitter circuits.

+2.8V_TCXO – Supply voltage for the VCTCXO



Fugure 5-1 DC power Distribution

Table 5-1 defines RFIC supply voltage requirements versus handset operating modes. If a table cell entry is "ON", that supply voltage must be on for that handset mode. If a table cell entry is "OFF", that supply voltage should be turned off for that handset mode. The RFICs are automatically programmed to operating states that reduce power consumption in each handset mode.

Table 5-1 RFIC Supply Voltages Per Operating Mode

Operationg Mode	+3.0V_MSMP +2.7V_MSMA +1.8V_MSMC	+2.8V_TCXO	+2.8V_RF_RX	+3.0V_RF_TX
Cellular CDMA Sleep	ON	OFF	OFF	OFF
Cellular CDMA Warmup	ON	ON	ON	OFF
Cellular CDMA Rx	ON	ON	ON	OFF
Cellular CDMA Rx/Tx	ON	ON	ON	ON
gpsOne Sleep	ON	OFF	OFF	OFF
gpsOne Rx Warmup	ON	ON	ON	OFF
gpsOne Rx	ON	ON	ON	OFF

REFERENCES

[1] 80-V5766-1 Rev. A, Cellular CDMA-only radioOne Chipset, Qualcomm Inc.

[2] CL93-V2920-1, radioOne Zero-IF Receiver Architecture, Qualcomm Inc.

[3] CL93-V2685-1, radioOne Zero-IF Transmitter Architecture, Qualcomm Inc.

[4] 80-V5759-1, RFR6125 RF Receiver , Qualcomm Inc.

[5] 80-V5229-1, RFT6120 Baseband-to-RF Transmitter, Qualcomm Inc.

[6] 93-V1091-1 Rev. E, PM6050 Device Specification, Qualcomm Inc.