

	瑞 声 科 技 AAC Technologies	NO. AT2530A
Module Specification		
TITLE: Module, ZigBee, 14.9 x 21.9 x 2.65mm, 45 I/O, Edge Castellated, SMD		
REVISION DATE: 22 May 2013	ISSUE: 0	PAGE: 1 of 28

ISSUE	DESCRIPTION OF CHANGES	DATE
O	Initial Release	22 nd May 2013

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1.0 Description and Application

1.1 Description

AT2530A module is based on the TI CC2530 ZigBee compliant SOC IC. The IC is a 2.4GHz, IEEE 802.15.4 compliant transceiver with an industry-standard enhanced 8051 MCU, 256 KB of flash and 8 KB of integrated RAM memory. The module is 14.9mm x 21.9mm x 2.65mm in dimensions with 45 I/O edge castellated interconnect.

1.2 Application

The custom module support user-defined applications, peripherals include five-channel DMA, integrated Op-Amp and ultralow-power comparator, general-purpose timers, 12-Bit ADC, USART as well as up to 21 GPIOs. The target applications include Home/Building automation and control, lighting systems, Industrial control and monitoring, Consumer Electronics, Health care and General ZigBee wireless sensor networking.

1.3 Module Block Diagram

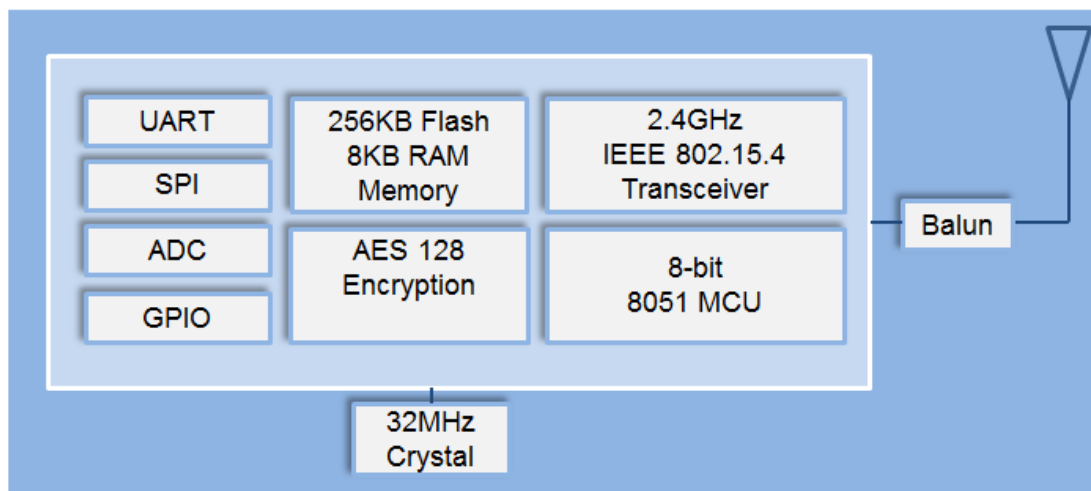


Figure 1: Module Block Diagram

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2.0 Mechanical Specifications

2.1 Module Dimensions (mm)

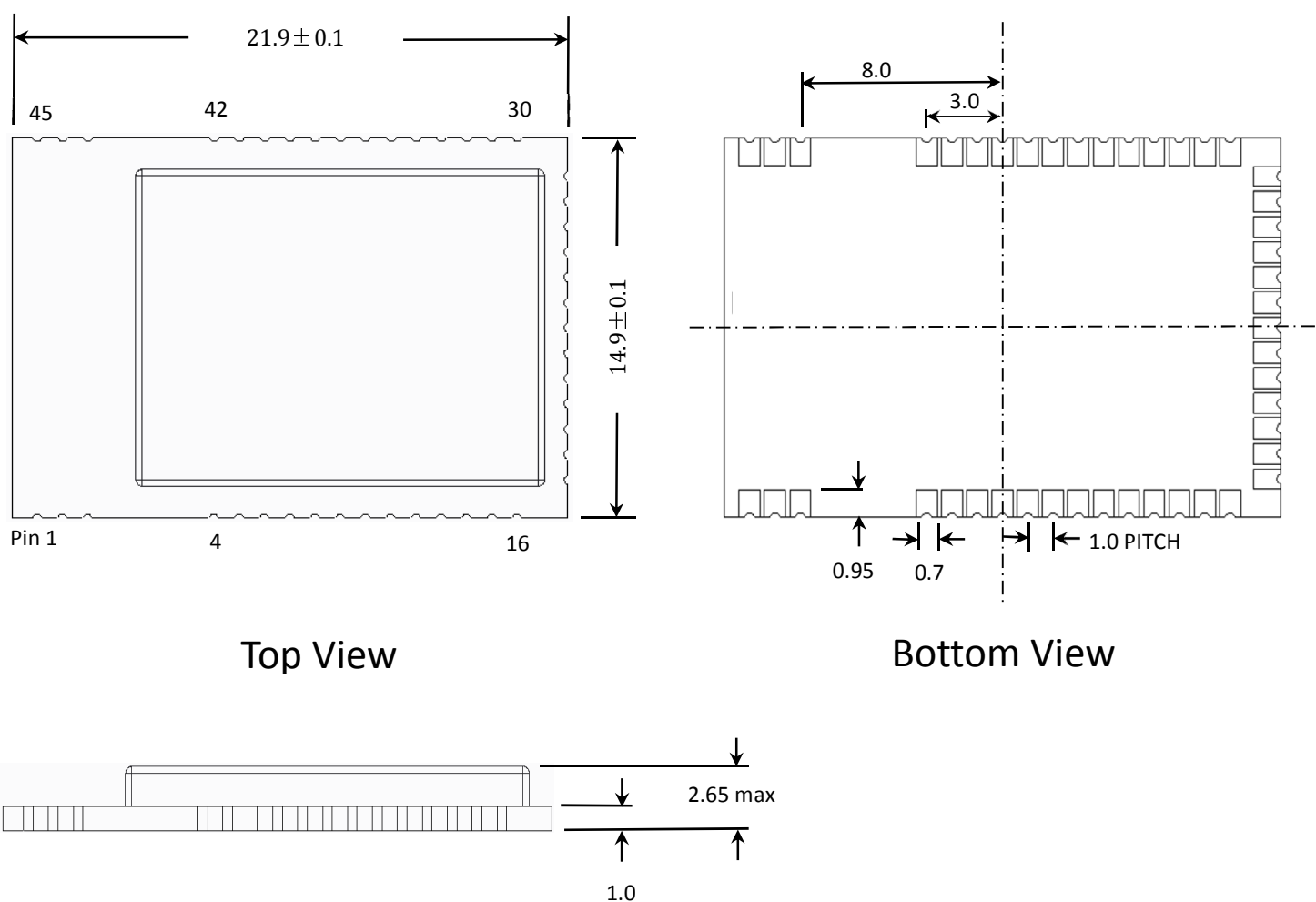


Figure 2: Module Top, Bottom and Side View

Figure 3: Module Footprint



2.3 Recommended Main PCB Copper Ground Design

(Only applicable to module with internal antenna)

Dimension in mm

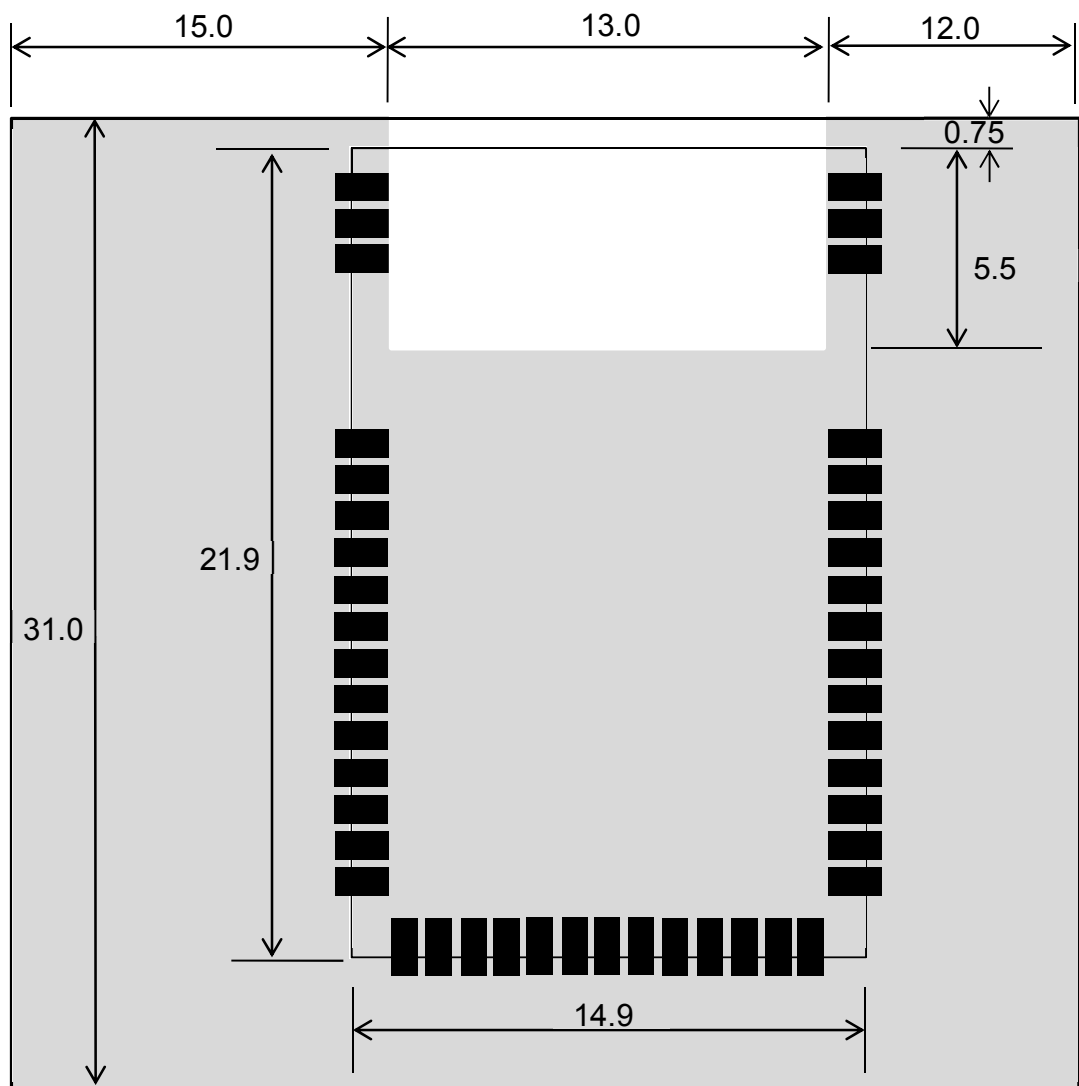


Figure 4: Recommended main PCB Copper design



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2.4 Module Mounting Location

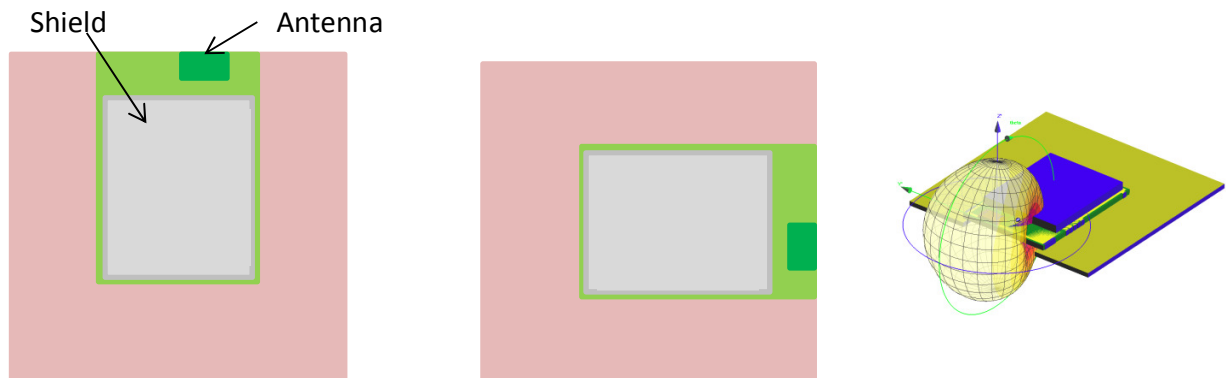


Figure 5: Recommended Locations in XY-Plane

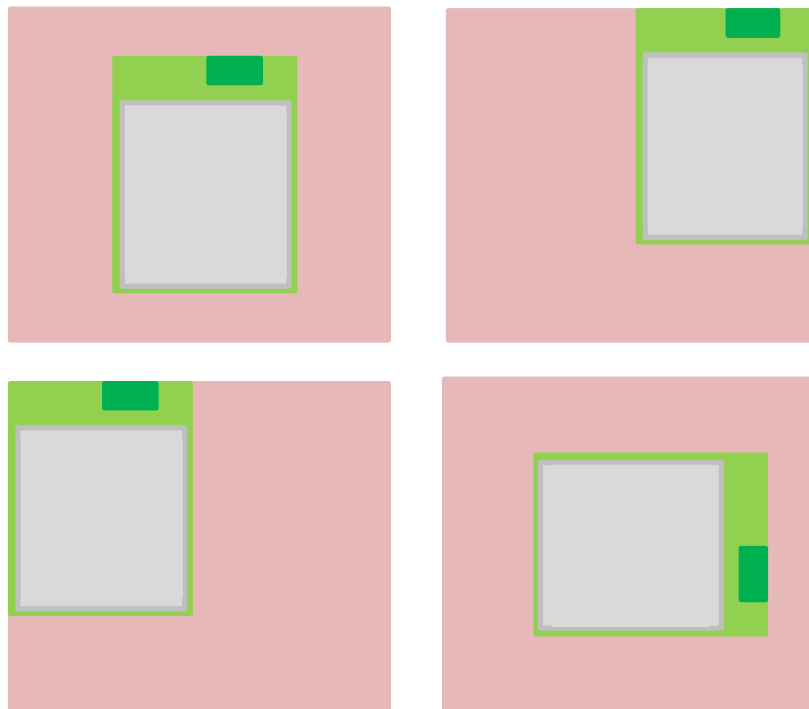


Figure 6: Locations Not Recommended in XY-Plane



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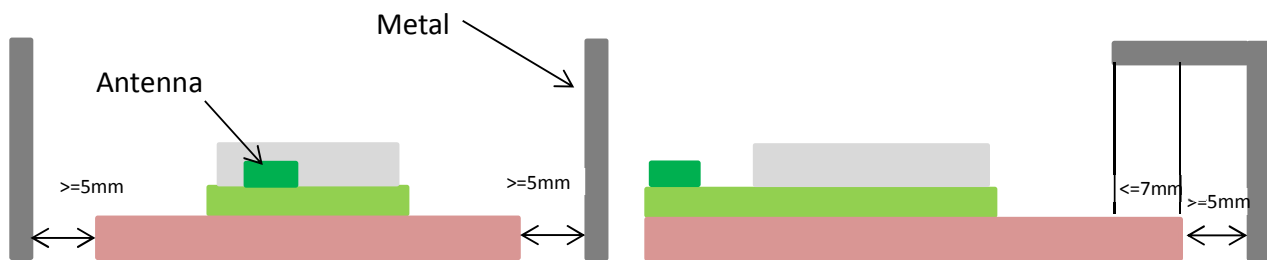


Figure 7: Locations of Metal Allowed in Z-Plane



Figure 8: Locations of Metal Not Allowed in Z-Plane



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2.5 Module Pin-Out

Module Pin	Pin Name	Pin Type	Description
1	GND	GND	Ground
2	GND	GND	Ground
3	GND	GND	Ground
4	GND	GND	Ground
5	VDD	Power	2.0V - 3.6V Power Supply
6	GND	GND	Ground
7	GND	GND	Ground
8	GND	GND	Ground
9	GND	GND	Ground
10	P2_4/XOSC32K_Q1	Digital I/O, Analog I/O	Port2.4/32.768 khz XOSC
11	P2_3/XOSC32K_Q2	Digital I/O, Analog I/O	Port2.3/32.768 khz XOSC
12	GND	GND	Ground
13	P2_2	Digital I/O	Port 2.2 - DC (debug clock)
14	P2_1	Digital I/O	Port 2.1 - DD (debug data)
15	P2_0	Digital I/O	Port 2.0
16	GND	GND	Ground
17	GND	GND	Ground
18	P1_7	Digital I/O	Port 1.7
19	P1_6	Digital I/O	Port 1.6
20	NC	NC	No Connection
21	NC	NC	No Connection
22	P1_5	Digital I/O	Port 1.5
23	P1_4	Digital I/O	Port 1.4
24	P1_3	Digital I/O	Port 1.3
25	P1_2	Digital I/O	Port 1.2
26	P1_1	Digital I/O	Port 1.1 - 20mA drive capability
27	P1_0	Digital I/O	Port 1.0 - 20mA drive capability
28	P0_7	Digital I/O	Port 0.7
29	GND	GND	Ground
30	GND	GND	Ground
31	P0_6	Digital I/O	Port 0.6
32	P0_5	Digital I/O	Port 0.5
33	P0_4	Digital I/O	Port 0.4
34	P0_3	Digital I/O	Port 0.3
35	P0_2	Digital I/O	Port 0.2

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36	P0_1	Digital I/O	Port 0.1
37	P0_0	Digital I/O	Port 0.0
38	RESET_N	Digital Input	Reset, active-low
39	GND	GND	Ground
40	GND	GND	Ground
41	GND	GND	Ground
42	GND	GND	Ground
43	GND	GND	Ground
44	GND	GND	Ground
45	GND	GND	Ground

Table 1: Module Signal Description

Notes:

(1) The serial UART connections RXD, TXD, CTS and RTS are P0_2, P0_3, P0_4 and P0_5 respectively.



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3.0 Electrical Specifications

3.1 Absolute Maximum Ratings

PARAMETER	Min	Max	Unit
Supply voltage, VDD	-0.3	3.9	V
Voltage on any digital pin	-0.3	VDD+0.3, ≤ 3.9	V
Input RF level		10	dBm
Storage Temperature	-40	85	°C

Table 2: Absolute Maximum Ratings

3.2 Environmental Characteristics

PARAMETER	MIN	MAX	UNIT
ESD on any pad (human body model)		2	kV
ESD on any pad (charged device model)		500	V
Moisture Sensitivity Level		3	

Table 3: Environment Characteristics

3.3 Operating Conditions

PARAMETER	Min	Typ	Max	Unit
Power supply	2.0	3.0	3.6	V
Operating Temperature	-40	25	85	°C

Table 4: Operating Conditions

3.4 DC characteristics

TA = 25°C, VDD = 3V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Unit
Receive Mode	32MHz XOSC running, radio in RX mode at -100 dBm input power, no peripherals active, CPU idle		25.5		mA
Transmit Mode	32MHz XOSC running, radio in TX mode, 4.5 dBm output power, no peripherals active, CPU idle		35.2		mA
Sleep Mode	Power mode 2. Digital regulator off, 16MHz RCOSC and 32MHz crystal oscillator off; 32.768KHz XOSC, POR and sleep timer active; RAM and register retention		1	2	uA

Table 5: DC characteristics

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3.5 RF Characteristics

(VDD = 3V, TA = 25°C, Normal Mode measured at the RF connector with 50Ω termination)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	PER = 1%		-97	-92	dBm
Saturation (max input level)	PER =1%		10		dBm
High-Side Adjacent Channel Rejection	Wanted signal -82dBm, adjacent modulated channel at 5MHz, PER =1%		49		dB
Low-Side Adjacent Channel Rejection	Wanted signal -82dBm, adjacent modulated channel at -5MHz, PER =1%		49		dB
2 nd High-Side Adjacent Channel Rejection	Wanted signal -82dBm, adjacent modulated channel at 10MHz, PER =1%		57		dB
2 nd Low-Side Adjacent Channel Rejection	Wanted signal -82dBm, adjacent modulated channel at -10MHz, PER =1%		57		dB
Co-channel rejection	Wanted signal at -82dBm. Undesired signal is an IEEE 802.15.4 modulated at the same frequency as the desired signal. Signal level for PER = 1%		-3		dB
Spurious emission 30 ~ 1000MHz 1 ~ 12.75GHz			-88		dBm
			-75		dBm

Table 6: Rx Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power	Maximum output-power setting	0	4.5	8	dBm
Programmable output power range			32		dB
Error vector magnitude (EVM)	Measured using maximum-recommended output-power setting		2		%
2 nd Harmonic 3 rd Harmonic	Max recommended output power setting		-62 -78		dBm
Spurious emission 30 ~ 1000 MHz 1 ~ 2.5 GHz 2.5 ~ 12.7 GHz (outside restricted bands)	Max recommended output power setting		-56		dBm
			-68		dBm
			-69		dBm

Table 7: Tx Characteristics



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3.6 Transmit Power Characteristics

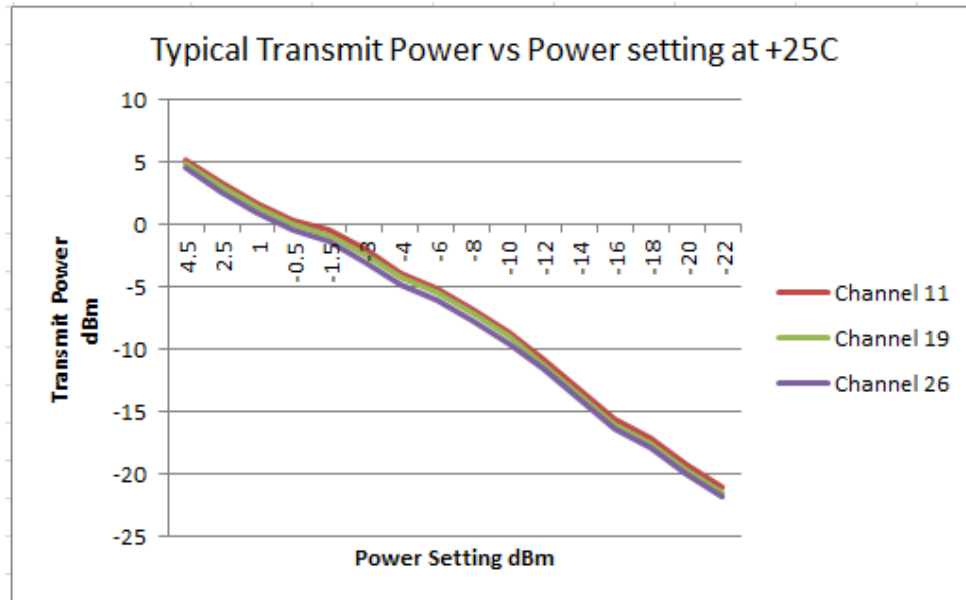


Figure 9: Transmit Power vs Power Setting

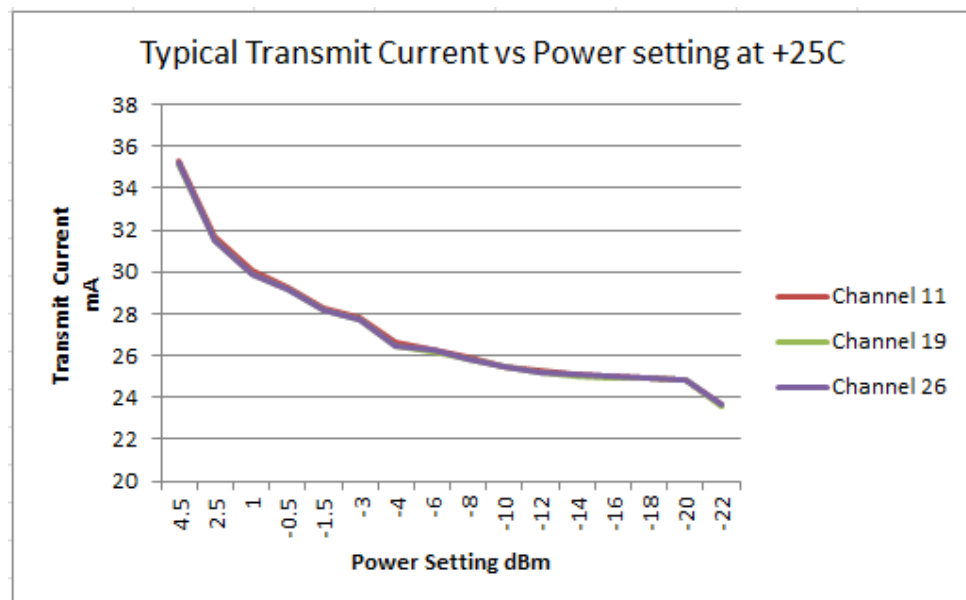


Figure 10: Transmit Current vs Power Setting

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4.0 Assembly Information

4.1 Lead-Free soldering reflow profile

Condition	Exposure
Average ramp-up rate (200°C to 250°C)	< 3 °C / second
> 217°C	60-120 seconds
Peak temperature	250 +0/-5°C
Time within 5°C of peak	20-30 seconds
Ramp-down rate (Peak to 50°C)	Less than 6°C / second

Table 8: Reflow Profile Recommendation

5.0 Reliability Tests

No.	Test item	Test condition
1	Reflow Thermal Cycle	Normal Pbfree reflow Condition 2 times
2	Thermal Shock Cycle	30min. at -40°C, 30min. at 85°C , 100Cycles Recovery Time 1hours
3	Vibration Test	JESD22-B103-B Service Condition 5, 5Hz -> 500Hz, Acceleration 0.3g, 4min/Cycle. Total 4 cycles per axis
4	High Temperature Storage Test	96 hours at 85°C, Recovery Time 1hours
5	Low Temperature Storage Test	96 hours at -40°C, Recovery Time 1hours
6	High Temperature & Humidity Storage Test	96 hours at 60°C & 90%RH±2%RH. Recovery Time 1hours
7	Drop Test	Height min 76 cm, All sides onto metal plate

Table 9: Reliability Tests



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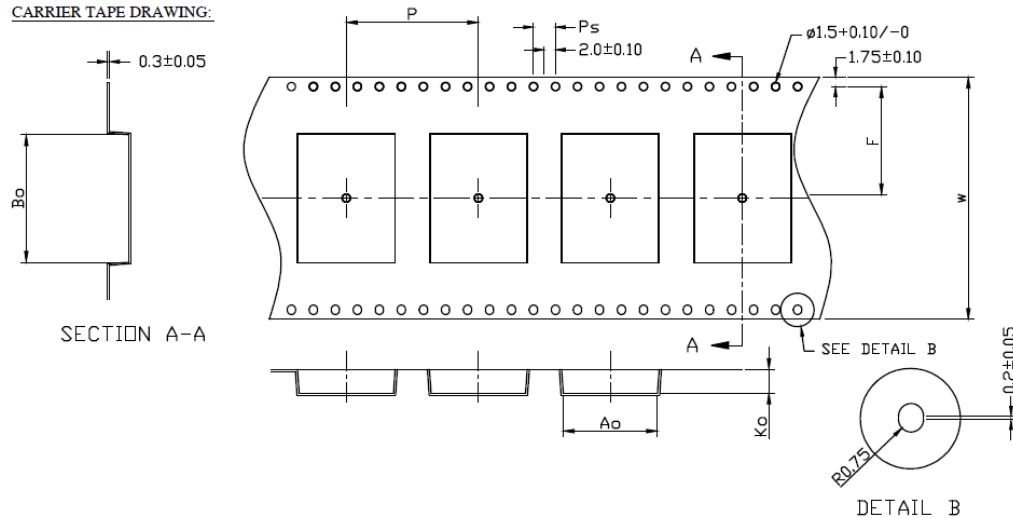
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6.0 Packaging Information

6.1 Tape and Reel specification

CARRIER TAPE DRAWING:



DIMENSIONS	W	P	Ao	A1	Bo	B1	Ko	K1	Ps	F
SPECS' Nominal	44.00	24.00	15.50	NA	22.50	NA	3.20	NA	4.00	20.20
Tolerance +/-	0.30	0.10	0.10	NA	0.10	NA	0.10	NA	0.10	0.10

All dimensions in mm.

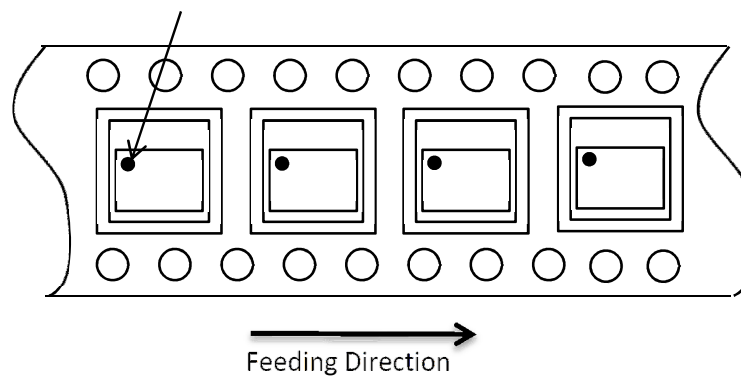
6.2 Component Orientation

Tape Width: 44 mm

Tape Pitch (part to part): 24 mm

Reel Diameter: 330 mm

Pin 1 Orientation (Not to Scale)



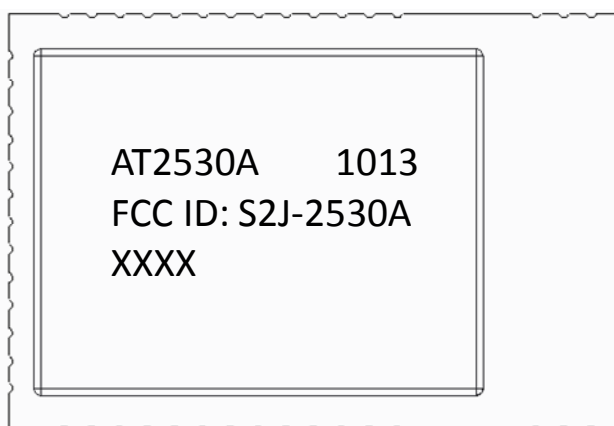
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6.3 Module Marking

AT2530A - Module Model Number

1013 - Date Code (Example: 10-Workweek, 13-Year)

XXXX - Customer Program information



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7.0 Regulatory Information

7.1 FCC Notice

This module complies with Part 15 of the FCC rules and regulations. Compliance with the labeling requirements, FCC notice and antenna usage guideline is required.

The OEM must comply with the following regulations:

1. The OEM integrator must ensure that the text on the external label provided with this device is placed on the outside of the final product.
2. AT2530A module may only be used with antenna that have been tested and approved for use with this module.

FCC Caution: Any changes or modifications not expressly approval by the party responsible for compliance could void the user's authority to operate this device.

7.2 OEM Labeling Requirements

The Original Equipment Manufacturing (OEM) must ensure that FCC labeling requirements are met. This includes a clearly visible label on the outside of the finished product specifying the AT2530A FCC identifier (**FCC ID: S2J-2530A**).

Below FCC label statements are required for OEM products containing AT2530A Module.

Contains FCC ID: S2J-2530A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference and (2) This device must accept any interference received, including interference that may cause undesired operation.

7.3 RF Exposure

This module has been certified for remote and base radio applications and is not intended to be operated within 20cm of the body. If the module will be used for portable applications, the OEM or OEM integrator is responsible for passing additional SAR (Specific Absorption Rate) testing in accordance with FCC Rules 2.1093.

The preceding statement must be included as a CAUTION statement in OEM product manuals in order to alert users of FCC RF exposure compliance.

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To satisfy FCC RF exposure requirements, a separation distance of 20cm or more should be maintained between the antenna of this device and persons during device operation. To ensure compliance, operation at closer than this distance is not recommended. The antenna used for this transmitter must not be co-located or operating in conjunction with other antennas or transmitters.

7.4 FCC Approved Power Settings

Table 15 shows approved channels of operations with the corresponding maximum output power steps settings.

	Channel 11-25	Channel 26
AT2530A	+4.5dBm	-0.5dBm

Table 15: Maximum Power Settings for FCC Compliance

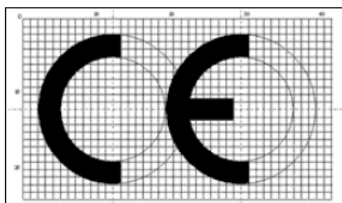
7.5 CE Notice

The AT2530A module has been tested and certified for use in the European Union. If this module is to be incorporated into a product, the OEM must ensure compliance of the final product to the European Harmonized EMC and low voltage/safety standards. A Declaration of Conformity must be issued for each of these standards and kept on file as described in Annex II of the R&TTE Directive. The final product must not exceed the specified power ratings, antenna specifications and installation requirements as specified in this user manual. If any of these specifications are exceeded in the final product then a submission must be made to a notified body for compliance testing to all of the required standards.

7.6 OEM Labeling Requirements

1. The CE conformity marking must consist of the initials CE taking the following form:

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If the CE conformity marking is reduced or enlarged the proportions given in the above graduated drawing must be respected

2. Where the directive concerned does not impose specific dimensions, the CE marking must have a height of at least 5 mm.

3. The CE marking must be affixed to the product or to its data plate. However, where this is not possible or not warranted on account of the nature of the product, it must be affixed to the packaging, if any, and to the accompanying documents, where the directive concerned provides for such documents.

4. The CE marking must be affixed visibly, legibly and indelibly.

For more information please refer to <http://ec.europa.eu/enterprise/faq/ce-mark.htm>. Customers assume full responsibility for learning and meeting the required guidelines for each country in their distribution market.

7.7 CE Compliance Power Settings

Table 16 shows approved channels of operations with the corresponding maximum output power steps settings.

	Channel 11-26
AT2530A	+4.5dBm

Table 16: Maximum Power Settings for Europe (ESTI)

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8.0 RoHS Declaration

Based on our supplier declarations, this product does not contain substances that are banned by Directive 2002/95/EC or contains a maximum concentration of 0.1% or 1000 ppm by weight in homogeneous materials for:

- Lead and lead compounds
- Mercury and mercury compounds
- Chromium (VI)
- PBB (polybrominated biphenyl)
- PBDE (polybrominated biphenyl ether)

And a maximum concentration of 0.01% or 100 ppm by weight in homogeneous materials for:

- Cadmium and cadmium compounds

9.0 Ordering Information

Module	Description	QTY/Reel	Order Number
AT2530A	+4.5dBm Output Power ZigBee Module • Based on TI CC2530F256 • AAC AT Style Command Interpreter • TI Z-Stack • Integrated Antenna	600	R001

Note:

All Modules are pre-programmed with AAC AT style command interpreter based on the TI Z-stack. Customers who are using their own firmware will be able to erase and write to the flash memory of the CC2530.

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Appendix A: ZigBee Light Link

The ZigBee Light Link ZLL devices are divided into two categories:

- Lighting devices (Target): These are used in ZLL light nodes such as a lamp.
- Controller devices (Initiator): These are used in ZLL controller nodes such as a remote control unit.

Ordering Information

Module	Description
AT2530A_LB	Module with integrated antenna, pre-programmed as Light Link Target
AT2530A_LR	Module with integrated antenna, pre-programmed as Light Link Initiator

Lighting Link Target Reference Module Pin-Out

Module Pin	Pin Name	Pin Type	Description
1	GND	GND	Ground
2	GND	GND	Ground
3	GND	GND	Ground
4	GND	GND	Ground
5	VDD	Power	2.0V - 3.6V Power Supply
6	GND	GND	Ground
7	GND	GND	Ground
8	GND	GND	Ground
9	GND	GND	Ground
10	P2_4/XOSC32K_Q1	Digital I/O, Analog I/O	Port2.4/32.768 kHz XOSC
11	P2_3/XOSC32K_Q2	Digital I/O, Analog I/O	Port2.3/32.768 kHz XOSC
12	GND	GND	Ground
13	P2_2	Digital I/O	Port 2.2 - DC (debug clock)
14	P2_1	Digital I/O	Port 2.1 - DD (debug data)
15	P2_0/ ZLL_FUNC	Digital Input	Use to trigger the following events: 1. Input Pulse < 1 sec: Permit join for 60 secs 

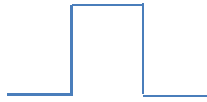


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			2. Input Pulse > 1sec and < 5 secs : Reset to factory New  3. Input Pulse > 5 secs: Classical commissioning 
16	GND	GND	Ground
17	GND	GND	Ground
18	P1_7	Digital I/O	Port 1.7
19	P1_6	Digital I/O	Port 1.6
20	NC	NC	No Connection
21	NC	NC	No Connection
22	P1_5	Digital I/O	Port 1.5
23	P1_4	Digital I/O	Port 1.4
24	P1_3	Digital I/O	Port 1.3
25	P1_2	Digital I/O	Port 1.2
26	P1_1	Digital I/O	Port 1.1 - 20mA drive capability
27	P1_0	Digital I/O	Port 1.0 - 20mA drive capability
28	P0_7	Digital I/O	Port 0.7
29	GND	GND	Ground
30	GND	GND	Ground
31	P0_6/WHITE	Digital Output	White LED PWM
32	P0_5/GREEN	Digital Output	GREEN LED PWM
33	P0_4/BLUE	Digital Output	BLUE LED PWM
34	P0_3/RED	Digital Output	RED LED PWM
35	P0_2	Digital I/O	Port 0.2
36	P0_1	Digital I/O	Port 0.1
37	P0_0	Digital I/O	Port 0.0
38	RESET_N	Digital Input	Reset, active-low

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39	GND	GND	Ground
40	GND	GND	Ground
41	GND	GND	Ground
42	GND	GND	Ground
43	GND	GND	Ground
44	GND	GND	Ground
45	GND	GND	Ground

Lighting Link Initiator Reference Module Pin-Out

Module Pin	Pin Name	Pin Type	Description
1	GND	GND	Ground
2	GND	GND	Ground
3	GND	GND	Ground
4	GND	GND	Ground
5	VDD	Power	2.0V - 3.6V Power Supply
6	GND	GND	Ground
7	GND	GND	Ground
8	GND	GND	Ground
9	GND	GND	Ground
10	P2_4/XOSC32K_Q1	Digital I/O, Analog I/O	Port2.4/32.768 kHz XOSC
11	P2_3/XOSC32K_Q2	Digital I/O, Analog I/O	Port2.3/32.768 kHz XOSC
12	GND	GND	Ground
13	P2_2	Digital I/O	Port 2.2 - DC (debug clock)
14	P2_1	Digital I/O	Port 2.1 - DD (debug data)
15	P2_0	Digital Output	Port 2.0
16	GND	GND	Ground
17	GND	GND	Ground
18	P1_7/COL_7	Digital Output	Key matrix column 7
19	P1_6/COL_6	Digital Output	Key matrix column 6
20	NC	NC	No Connection
21	NC	NC	No Connection
22	P1_5/COL_5	Digital Output	Key matrix column 5
23	P1_4/COL_4	Digital Output	Key matrix column 4
24	P1_3/COL_3	Digital Output	Key matrix column 3
25	P1_2/COL_2	Digital Output	Key matrix column 2

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26	P1_1/COL_1	Digital Output	Key matrix column 1
27	P1_0/COL_0	Digital Output	Key matrix column 0
28	P0_7/ROW_7	Digital Input	Key matrix row 7
29	GND	GND	Ground
30	GND	GND	Ground
31	P0_6/ROW_6	Digital Input	Key matrix row 6
32	P0_5/ROW_5	Digital Input	Key matrix row 5
33	P0_4/ROW_4	Digital Input	Key matrix row 4
34	P0_3/ROW_3	Digital Input	Key matrix row 3
35	P0_2/ROW_2	Digital Input	Key matrix row 2
36	P0_1/ROW_1	Digital Input	Key matrix row 1
37	P0_0/ROW_0	Digital Input	Key matrix row 0
38	RESET_N	Digital Input	Reset, active-low
39	GND	GND	Ground
40	GND	GND	Ground
41	GND	GND	Ground
42	GND	GND	Ground
43	GND	GND	Ground
44	GND	GND	Ground
45	GND	GND	Ground

Lighting Link Initiator Key Matrix Table

Row	Column							
		COL_0	COL_2	COL_3	COL_4	COL_5	COL_6	COL_7
	ROW_0	KEY1	KEY2	KEY3	KEY4	KEY5	KEY6	KEY7
	ROW_1	KEY8	KEY9	KEY10	KEY11	KEY12	KEY13	KEY14
	ROW_2	KEY15	KEY16	KEY17	KEY18	KEY19	KEY20	KEY21
	ROW_3	KEY22	KEY23	KEY24	KEY25	KEY26	KEY27	KEY28
	ROW_4	KEY29	KEY30	KEY31	KEY32	-	KEY33	KEY34
	ROW_5	KEY35	KEY36	KEY37	KEY38	-	KEY39	KEY40
	ROW_6	KEY41	KEY42	KEY43	KEY44	KEY45	KEY46	KEY47
	ROW_7	KEY48	KEY49	KEY50	KEY51	KEY52	KEY53	KEY54



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Lighting Link Initiator Key Functions

KEYS	ZigBee Light link Command Description
KEY1	Enhanced move hue
KEY2	Remove group
KEY3	Get scene membership
KEY4	Remove all groups
KEY5	Remove scene
KEY6	Identify
KEY7	Remove all scenes
KEY8	Enhanced step hue
KEY9	Enhanced move to hue(RED)
KEY10	Add group if identifying
KEY11	Enhanced move to hue(GREEN)
KEY12	Enhanced move to hue(YELLOW)
KEY13	Step Level(On/Off)
KEY14	Enhanced move to hue(BLUE)
KEY15	Swap mode
KEY16	Store scene
KEY17	Mode Utility(Inc/Dec)
KEY18	Add scene
KEY19	Level Utility(Inc/Dec)
KEY20	Color Y Utility(Inc/Dec)
KEY21	Recall scene
KEY22	Reset Utility
KEY23	Scene 1 Select
KEY24	Transition time Utility(Inc/Dec)
KEY25	Scene 2 Select
KEY26	Variant Utility(Inc/Dec)
KEY27	Color X Utility(Inc/Dec)
KEY28	Scene 3 Select
KEY29	Group 4 Select
KEY30	Saturation Utility(Inc/Dec)
KEY31	Group 6 Select
KEY32	Copy scene
KEY33	Group 5 Select
KEY34	Unicast Address Select
KEY35	Group 1 Select
KEY36	Hue Utility(Inc/Dec)
KEY37	Group 3 Select
KEY38	Color loop set



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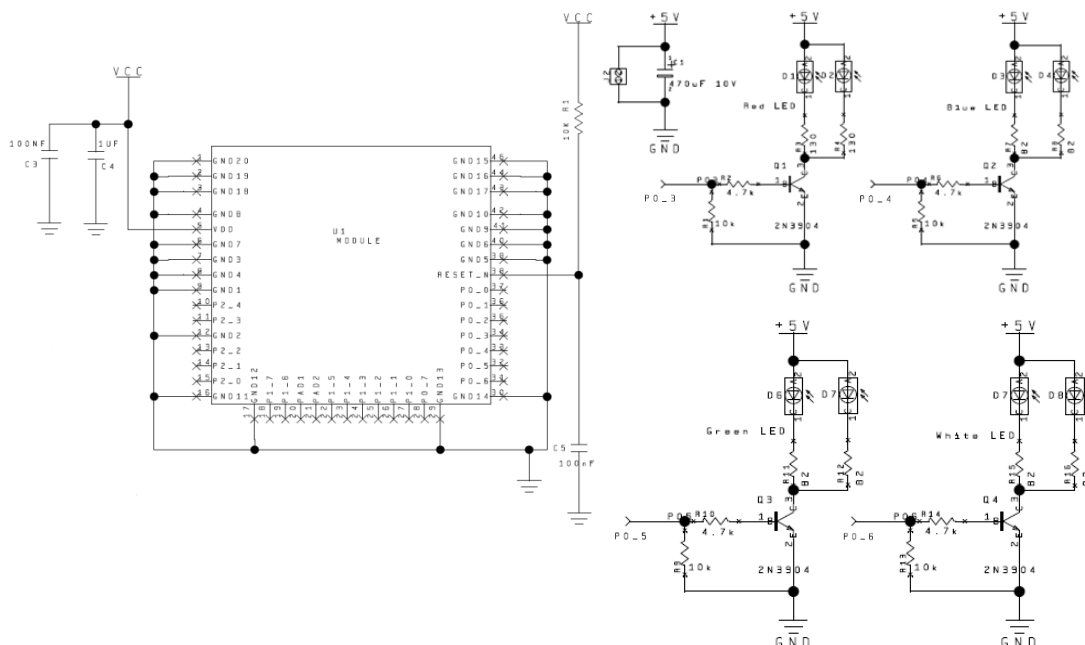
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KEY39	Group 2 Select
KEY40	Broadcast Address Select
KEY41	Factory Reset
KEY42	Stop move step
KEY43	Send Factory Reset
KEY44	Enhanced move to hue and saturation
KEY45	Enhanced add scene
KEY46	Classical commissioning
KEY47	Move Color
KEY48	Device Select down
KEY49	On
KEY50	Device Select up
KEY51	Touch Link
KEY52	Channel Change
KEY53	Add group
KEY54	Off

Lighting Link Target Reference Schematic



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