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HPS-110 Operational Description

RF Transmitter

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot which results in a controlled modulation index. A digital baseband transmit filter provides the required spectral shaping. The output power is typically +16dBm.

RF Receiver

The receiver features a near-zero Intermediate Frequency architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier input allows the radio the be used in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. The use of a digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows HPS-110 to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes or LC resonators.

Baseband and Logic

The microcontroller, interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit RISC microcontroller is used for low power consumption and efficient use of memory.

The MMU provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimize the overheads on the processor during data transfers.

During radio transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM.

Physical Layer Hardware Engine DSP is used to perform Forward error correction, Header error control, Cyclic redundancy check, Encryption, Data whitening, and Access code correlation.