FCC ID: RS4-77926

Technical Description :

The brief circuit description is listed as follows :
- nRF24L01 acts as 2.4 GHz RF Module.
- U101 GPRT5508A acts as MCU.
- U103 W588D120 acts as Sound Synthesizer and Head Flashing LED Control Unit.
- U104 GPC11160C acts as Cap Sensor IC.
- MEMBRANE FOR CAPSENSOR TRIGGER PAD acts as Cap Sensors.
- Q401 acts as Light Sensor.
- MIC acts as Microphone.
- S101 to S104 act as 4 Position Keys.
- S601 acts as Slide Switch.
- GYP0030A and associated circuit act as Audio Amplifier.
- S1 acts as Talk Key.
- S111 acts as Reset Key.
- SPK acts as Speaker.

Antenna Used :

An integral antenna (internal) has been used.

1. INTRODUCTION

Roomtech items are using 2.4GHz RF for the command communication. In each Roomtech item, it is equipped with a Nordic nRF24L01 2.4GHz RF module.

When the talk key in the Roomtech item is pressed, the nRF24L01 2.4GHz RF module will be activate. The Roomtech item can transmit or receive 2.4GHz RF Signal.

The nRF24L01 is normally in receive mode for listening. the nRF24L01 will transmit RF Signal for 0.5s when the user input the relative command to the Roomtech item. After the transmission, the nRF24L01 will return receive mode.

2. GENERAL INFORMATION

a. RF Channel Frequency Table

3 frequencies in 2.4G ISM band are used in RoomTech

Frequency	2402 MHz	2404 MHz	2406 MHz
Channel	Channel 1	Channel 2	Channel 3

b. Modulation

The radio font end uses GFSK modulation

c. Date Structure

Preamble	Address	Pack Control Field	Payload	CRC
1 byte	5 bytes	9 bits	8 bytes	2 bytes

3. TRANSMISSION OPRATION

a. Transmission Pattern

During the transmission time, the PTX sends the data packets in the following sequence last for 0.5s.

Ch1 -> Ch1 -> Ch1 -> Ch2 -> Ch2 -> Ch2 -> Ch3 -> Ch3 -> Ch3 ->
Ch1 -> Ch1 -> Ch1 -> Ch2 -> Ch2 -> Ch2 -> Ch3 -> Ch3 -> Ch3 ->
...
.....
.....
Ch1 -> Ch1 -> Ch1 -> Ch2 -> Ch2 -> Ch2 -> Ch3 -> Ch3 -> Ch3

NORDIC SEMICONDUCTOR

nRF24L01
Single Chip 2.4GHz Transceiver

Product Specification

Key Features

- Worldwide 2.4GHz ISM band operation
- Up to 2Mbps on air data rate
- Ultra low power operation
- 11.3mA TX at 0dBm output power
- 12.3mA RX at 2Mbps air data rate
- 900nA in power down
- 22µA in standby-I
- On chip voltage regulator
- 1.9 to 3.6V supply range
- Enhanced ShockBurst™
- Automatic packet handling
- Auto packet transaction handling
- 6 data pipe MultiCeiver™
- Air compatible with nRF2401A, 02, E1 and E2
- Low cost BOM
- ±60ppm 16MHz crystal
- 5V tolerant inputs
- Compact 20-pin 4x4mm QFN package

Applications

- Wireless PC Peripherals
- Mouse, keyboards and remotes
- 3-in-one desktop bundles
- Advanced Media center remote controls
- VoIP headsets
- Game controllers
- Sports watches and sensors
- RF remote controls for consumer electronics
- Home and commercial automation
- Ultra low power sensor networks
- Active RFID
- Asset tracing systems
- Toys

July 2007

1 Introduction

The nRF24L01 is a single chip 2.4GHz transceiver with an embedded baseband protocol engine (Enhanced ShockBurst™), designed for ultra low power wireless applications. The nRF24L01 is designed for operation in the world wide ISM frequency band at 2.400 - 2.4835GHz. An MCU (microcontroller) and very few external passive components are needed to design a radio system with the nRF24L01.

The nRF24L01 is configured and operated through a Serial Peripheral Interface (SPI.) Through this interface the register map is available. The register map contains all configuration registers in the nRF24L01 and is accessible in all operation modes of the chip.

The embedded baseband protocol engine (Enhanced ShockBurst™) is based on packet communication and supports various modes from manual operation to advanced autonomous protocol operation. Internal FIFOs ensure a smooth data flow between the radio front end and the system's MCU. Enhanced ShockBurst™ reduces system cost by handling all the high-speed link layer operations.

The radio front end uses GFSK modulation. It has user configurable parameters like frequency channel, output power and air data rate.

The air data rate supported by the nRF24L01 is configurable to 2Mbps. The high air data rate combined with two power saving modes makes the nRF24L01 very suitable for ultra low power designs.

Internal voltage regulators ensure a high Power Supply Rejection Ratio (PSRR) and a wide power supply range.

1.1 Features

Features of the nRF24L01 include:

- Radio
  - Worldwide 2.4GHz ISM band operation
  - 126 RF channels
  - Common RX and TX pins
  - GFSK modulation
  - 1 and 2Mbps air data rate
  - 1MHz non-overlapping channel spacing at 1Mbps
  - 2MHz non-overlapping channel spacing at 2Mbps
- Transmitter
  - Programmable output power: 0, -6, -12 or -18dBm
  - 11.3mA at 0dBm output power
- Receiver
  - Integrated channel filters
  - 12.3mA at 2Mbps
  - -82dBm sensitivity at 2Mbps
  - -85dBm sensitivity at 1Mbps
  - Programmable LNA gain
- RF Synthesizer
  - Fully integrated synthesizer
  - No external loop filer, VCO varactor diode or resonator
  - Accepts low cost ±60ppm 16MHz crystal
- Enhanced ShockBurst™
  - 1 to 32 bytes dynamic payload length
  - Automatic packet handling
  - Auto packet transaction handling
  - 6 data pipe MultiCeiver™ for 1:6 star networks
- Power Management
  - Integrated voltage regulator
  - 1.9 to 3.6V supply range
  - Idle modes with fast start-up times for advanced power management
  - 22uA Standby-I mode, 900nA power down mode
  - Max 1.5ms start-up from power down mode
  - Max 130us start-up from standby-I mode
- Host Interface
  - 4-pin hardware SPI
  - Max 8Mbps
  - 3 separate 32 bytes TX and RX FIFOs
  - 5V tolerant inputs
- Compact 20-pin 4x4mm QFN package

1.2 Block diagram

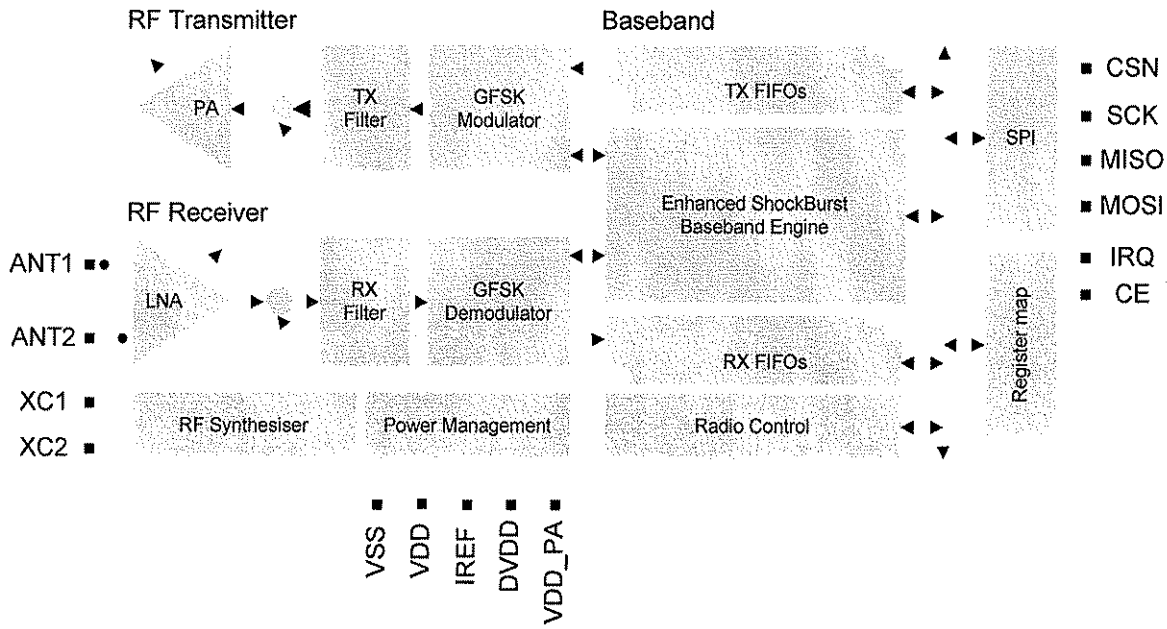


Figure 1. nRF24L01 block diagram

6 Radio Control

This chapter describes the different modes the nRF24L01 radio transceiver can operate in and the parameters used to control the radio.

The nRF24L01 has a built-in state machine that controls the transitions between the different operating modes of the chip. The state machine takes input from user defined register values and internal signals.

6.1 Operational Modes

The nRF24L01 can be configured in four main modes of operation. This section describes these modes.

6.1.1 State diagram

The state diagram (Figure 3.) shows the modes the nRF24L01 can operate in and how they are accessed. The nRF24L01 is undefined until the VDD becomes 1.9V or higher. When this happens nRF24L01 enters the Power on reset state where it remains in reset until it enters the Power Down mode. Even when the nRF24L01 enters Power Down mode the MCU can control the chip through the SPI and the Chip Enable (CE) pin Three types of states are used in the state diagram. "Recommended operating mode" is a state that is used during normal operation. "Possible operating mode" is a state that is allowed to use, but it is not used during normal operation. "Transition state" is a time limited state used during start up of the oscillator and settling of the PLL.

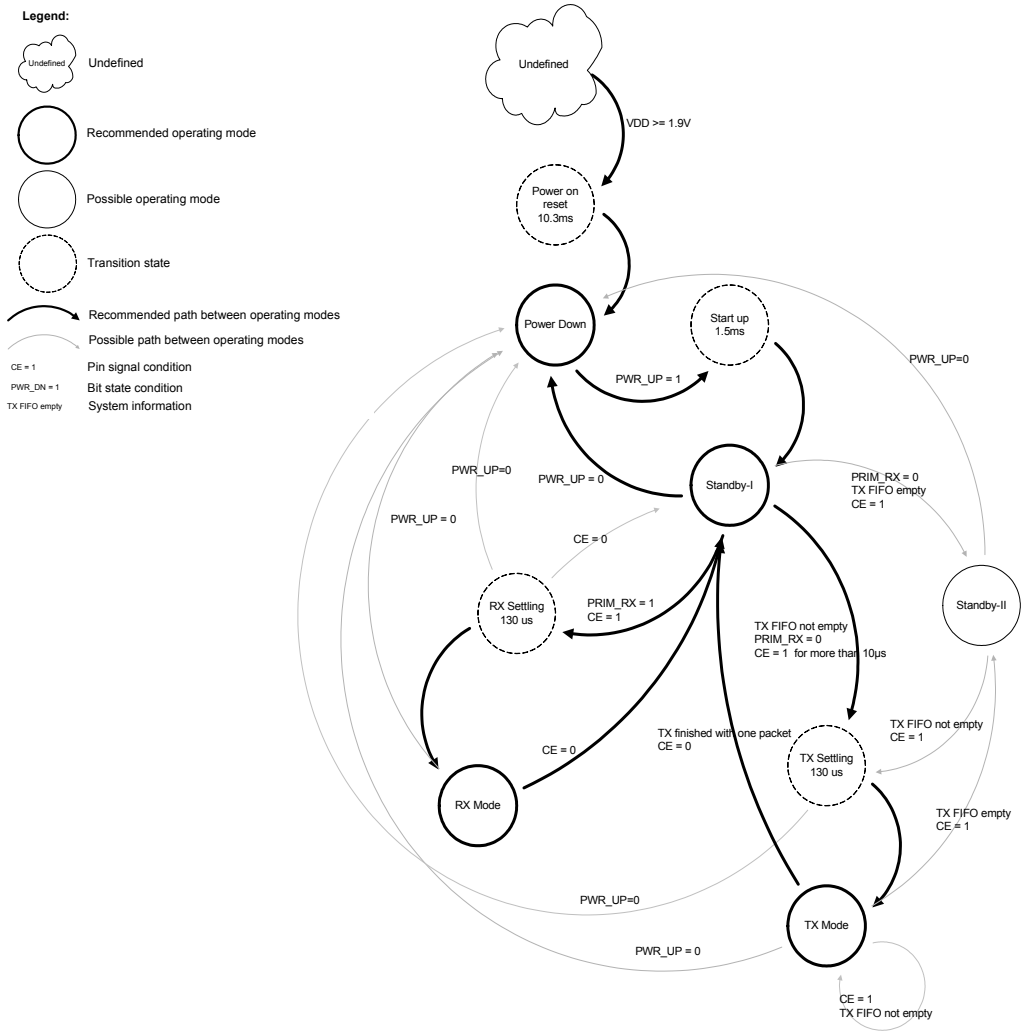


Figure 3. Radio control state diagram

6.1.2 Power Down Mode

In power down mode nRF24L01 is disabled with minimal current consumption. In power down mode all the register values available from the SPI are maintained and the SPI can be activated. For start up time see Table 13. on page 22. Power down mode is entered by setting the `PWR_UP` bit in the `CONFIG` register low.

6.1.3 Standby Modes

By settting the `PWR_UP` bit in the `CONFIG` register to 1, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start up times. In this mode part of the crystal oscillator is active. This is the mode the nRF24L01 returns to from TX or RX mode when **`CE`** is set low.

In standby-II mode extra clock buffers are active compared to standby-I mode and much more current is used compared to standby-I mode. Standby-II occurs when **`CE`** is held high on a PTX device with empty TX FIFO. If a new packet is uploaded to the TX FIFO, the PLL starts and the packet is transmitted.

The register values are maintained during standby modes and the SPI may be activated. For start up time see Table 13. on page 22.

6.1.4 RX mode

The RX mode is an active mode where the nRF24L01 radio is a receiver. To enter this mode, the nRF24L01 must have the PWR_UP bit set high, PRIM_RX bit set high and the CE pin set high.

In this mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFO. If the RX FIFO is full, the received packet is discarded.

The nRF24L01 remains in RX mode until the MCU configures it to standby-I mode or power down mode. If the automatic protocol features (Enhanced ShockBurst™) in the baseband protocol engine are enabled, the nRF24L01 can enter other modes in order to execute the protocol.

In RX mode a carrier detect signal is avaliable. The carrier detect is a signal that is set high when a RF signal is detected inside the receiving frequency channel. The signal must be FSK modulated for a secure detection. Other signals can also be detected. The Carrier Detect (CD) is set high when an RF signal is detected in RX mode, otherwise CD is low. The internal CD signal is filtered before presented to CD register. The RF signal must be present for at least 128µs before the CD is set high. How to use the CD is described in Appendix E on page 74.

6.1.5 TX mode

The TX mode is an active mode where the nRF24L01 transmits a packet. To enter this mode, the nRF24L01 must have the PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO and, a high pulse on the CE for more than 10µs.

The nRF24L01 stays in TX mode until it finishes transmitting a current packet. If CE = 0 nRF24L01 returns to standby-I mode. If CE = 1, the next action is determined by the status of the TX FIFO. If the TX FIFO is not empty the nRF24L01 remains in TX mode, transmitting the next packet. If the TX FIFO is empty the nRF24L01 goes into standby-II mode.The nRF24L01 transmitter PLL operates in open loop when in TX mode. It is important to never keep the nRF24L01 in TX mode for more than 4ms at a time. If the auto retransmit is enabled, the nRF24L01 is never in TX mode long enough to disobey this rule.

6.1.6 Operational modes configuration

The following table (Table 12.) describes how to configure the operational modes.

Mode	PWR_UP register	PRIM_RX register	CE	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data in TX FIFO. Will empty all levels in TX FIFO[a].
TX mode	1	0	minimum 10µs high pulse	Data in TX FIFO.Will empty one level in TX FIFO[b].
Standby-II	1	0	1	TX FIFO empty
Standby-I	1	-	0	No ongoing packet transmission
Power Down	0	-	-	-

a. In this operating mode if the CE is held high the TX FIFO is emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the CE is still high, nRF24L01 enters standby-II mode. In this mode the transmission of a packet is started as soon as the CSN is set high after a upload (UL) of a packet to TX FIFO.
b. This operating mode pulses the CE high for at least 10µs. This allows one packet to be transmitted. This is the normal operating mode. After the packet is transmittet, the nRF24L01 enters standby-I mode.

Table 12. nRF24L01 main modes

6.1.7 Timing Information

The timing information in this section is related to the transitions between modes and the timing for the CE pin. The transition from TX mode to RX mode or vice versa is the same as the transition from standby-I to TX mode or RX mode,Tstby2a.

Name	nRF24L01	Max.	Min.	Comments
Tpd2stby	Power Down → Standby mode	1.5ms		Internal crystal oscillator
Tpd2stby	Power Down → Standby mode	150µs		With external clock
Tstby2a	Standby modes → TX/RX mode	130µs		
Thce	Minimum CE high		10µs	
Tpece2csn	Delay from CE pos. edge to CSN low		4µs	

Table 13. Operational timing of nRF24L01

When nRF24L01 is in power down mode it must settle for 1.5ms before it can enter the TX or RX modes. If an *external clock* is used this delay is reduced to 150µs, see Table 13. on page 22. The settling time must be controlled by the MCU.

Note: The register value is lost if VDD is turned off. In this case, nRF24L01 must be configured before entering the TX or RX modes.

6.2 Air data rate

The air data rate is the modulated signaling rate the nRF24L01 uses when transmitting and receiving data.

The air data rate can be 1Mbps or 2Mbps. The 1Mbps data rate gives 3dB better receiver sensitivity compared to 2Mbps. High air data rate means lower average current consumption and reduced probability of on-air collisions.

The air data rate is set by the RF_DR bit in the RF_SETUP register.

A transmitter and a receiver must be programmed with the same air data rate to be able to communicate with each other.

For compatibility with nRF2401A, nRF24E1, nRF2402 and nRF24E2 the air data rate must be set to 1Mbps.

6.3 RF channel frequency

The RF channel frequency determines the center of the channel used by the nRF24L01. The channel occupies a bandwidth of 1MHz at 1Mbps and 2MHz at 2Mbps. nRF24L01 can operate on frequencies from 2.400GHz to 2.525GHz. The resolution of the RF channel frequency setting is 1MHz.

At 2Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2Mbps mode, the channel spacing must be 2MHz or more. At 1Mbps the channel bandwidth is the same as the resolution of the RF frequency setting.

The RF channel frequency is set by the RF_CH register according to the following formula:

$F_0 = 2400 + RF\_CH$ [MHz]

A transmitter and a receiver must be programmed with the same RF channel frequency to be able to communicate with each other.

6.4 PA control

The PA control is used to set the output power from the nRF24L01 power amplifier (PA). In TX mode PA control has four programmable steps, see Table 14.

The PA control is set by the RF_PWR bits in the RF_SETUP register.

SPI RF-SETUP (RF_PWR)	RF output power	DC current consumption
11	0dBm	11.3mA
10	-6dBm	9.0mA
01	-12dBm	7.5mA
00	-18dBm	7.0mA

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27°C, Load impedance = 15Ω+j88Ω.

Table 14. RF output power setting for the nRF24L01

6.5 LNA gain

The gain in the Low Noise Amplifier (LNA) in the nRF24L01 receiver is controlled by the LNA gain setting. The LNA gain makes it possible to reduce the current consumption in RX mode with 0.8mA at the cost of 1.5dB reduction in receiver sensitivity.

The LNA gain has two steps and is set by the LNA_HCURR bit in the RF_SETUP register.

6.6 RX/TX control

The RX/TX control is set by PRIM_RX bit in the CONFIG register and sets the nRF24L01 in transmit/ receive.

1. GENERAL DESCRIPTION

The W588Dxxx is a powerful embedded microprocessor (uP) dedicated to speech and melody synthesis applications. This series chips are suitable for plush toys, educational Q&A toys, or interactive application. W588Dxxx can synthesize multi-channel speech and melody. 3-track of synthesized speech can be in different kinds of format, for example ADPCM and MDPCM. Regarding synthesized melody, W588Dxxx can provide 2-track of Tone melody (T-melody), or 3-track of High-Quality melody (HQ-melody) that can emulate the characteristics of musical instruments. In general speaking, W588Dxxx series can accomplish multi-tasking requirements easily and make toys with more complicated than traditional *PowerSpeech*.

The W588Dxxx provides at most 8 input pins & 24 bi-directional I/Os, maximum 512 bytes RAM, IR carrier, Serial Interface Management, and 32KHz-Divider for more and more sophisticated applications, such as interactive toys, cartridge toys and final count down function. 3 LED output pins with 256-level control means that numerous combination of RGB colors may result in a versatility of colorful effects. W588Dxxx has two kinds of power saving modes: one is Slow mode and the other is STOP mode. In addition, W588Dxxx also provides PWM mode output to save power during playback and Watch Dog Timer to prevent latch-up situation occurring.

ITEM	W588D003	W588D006	W588D009	W588D012	W588D015
*Duration	4 sec.	6 sec.	12 sec.	15 sec.	19 sec.
ITEM	**W588D020**	**W588D025**	**W588D030**	**W588D035**	**W588D040**
*Duration	25 sec.	29 sec.	32 sec.	44 sec.	50 sec.
ITEM	**W588D045**	**W588D050**	**W588D055**	**W588D060**	**W588D070**
*Duration	53 sec.	58 sec.	62 sec.	66 sec.	86 sec.
ITEM	**W588D080**	**W588D100**	**W588D120**	**W588D150**	**W588D170**
*Duration	100 sec.	118 sec.	134 sec.	169 sec.	203 sec.
ITEM	**W588D210**	**W588D260**	**W588D300**	**W588D350**	**W588D400**
*Duration	237 sec.	271 sec.	313 sec.	358 sec.	407 sec.

Note:

*: The duration time is based on 5-bit MDPCM at 6 KHz sampling rate. The firmware library and program code have been excluded from user's ROM space for the duration estimation.

2. FEATURE

- Wide range of operating voltage:
  - 8 M Hz @ 3.0 volt ~ 5.5 volt
  - 6 M Hz @ 2.4 volt ~ 5.5 volt
- Provide power management to save current consumption:
  - 4 ~ 8 MHz system clocks, with Ring type or crystal type.
  - Slow mode to save power.
  - Stop mode for stopping all IC operations.
- F/W speech synthesis:
  - Multiple format parser that supports
    - ✓ 6-bit MDPCM, 5-bit MDPCM, 4-bit ADPCM, 8-bit Log PCM algorithm can be used
  - Pitch shippable ADPCM for voice changer application
  - Programmable sample rate
- F/W melody synthesizer
  - 2 tracks Tone melody which can emulate envelope of music instruments
  - 3 tracks High-Quality melody that can emulate characteristic of musical instruments
  - Voice melody can be implemented in 2 octaves
- Built-in 3 timers for speech/melody synthesis
  - 3 tracks speech
  - 1 speech channel plus dual-tone melody
  - 3 tracks High-Quality melody
- Harmonized synchronization among MIDI, Speech, LED, and Motor
- I/O configuration:
  - W588D003~D060: 16 I/O pins
  - W588D070~D260: 24 I/O pins
  - W588D300~D400: 8 input pins and 24 I/O pins
- Built-in IR carrier generation circuit for simplification firmware IR application
- Built-in IR receiver counting circuit for simplifying IR decoding
- Build-in 3 LED outputs with 256-level control of brightness.
- Built-in TimerG1 for general purpose applications
- Built-in Watch-Dog Timer (WDT) and Low Voltage Reset (LVR)
- Built-in 32 KHz crystal oscillator with divider for time-keeping application
- Provide serial interface
  - W55Fxx, W551Cxx
  - SPI flash
- Built-in Serial Interface Manager (SIM) in all W588Dxxx series
- 13-bit Current type digital-to-analog converters (DAC) to drive speaker output

- Direct-drive 12-bit PWM output to save power consumption
- Support ***PowerScript***^{TM} for developing codes in easy way.
- Full-fledged development system
  - Source-level ICE debugger (Assembly & ***PowerScript***^{TM} format)
  - ***Ultra I/O***^{TM} tool for event synchronization mechanism
  - ICE system with USB port
  - User-friendly GUI environment
- Available package form:
  - COB is essential

REPEATER FOR LEARNING LANGUAGE

1. GENERAL DESCRIPTION

The GPRT5508A is a high-integrity, high-performance integrated circuit for systems. Its low cost, combined with its complete array of functions, makes it the ideal choice for speech recording /playback application. The GPRT5508A consists of a 16-bits *μ'nSP*™ CPU and a 10-bits DAC/ADC. With a minimum of components, the GPRT5508A incorporated A2000 algorithm (16Kbps) to perform high quality voice encoding/decoding. It provides a wide range of functions, including voice activity detection, stereo tape input driver, repeating with changed speed, LED drivers, and SDRAM interface.

2. FEATURES

- GENERALPLUS 16-bit *μ'nSP*™ CPU
  - — SRAM 1.75K x 16 bits
  - — ROM 20K x 16 bits
- Clock
  - — build in 3.58MHz/455KHz crystal driver
  - — An internal PLL for CPU clock (28MHz/35MHz/43MHz)
- Operating voltage
  - — CPU operating voltage : 2.4V - 3.6V
  - — ADC/DAC/AGC operating voltage: 2.7V - 3.6V
- Operation Modes
  - — Operating mode, Halt mode and Standby mode
- Timer/Counter
  - — One 16-bit timer/counter
  - — One 8-bit timer/counter for ADC sample rate
- Power management for system reliability
  - — Low-Voltage-Reset function (Mask Option)
  - — Power-On-Reset function
  - — Watchdog reset
- Analog Front End
  - — 10bits ADC with 8K/16K sample rate
  - — AGC with 26dB dynamic range
  - — Microphone input driver
  - — Stereo Tape input driver
- Speaker driver
  - — Left channel speaker driver for 8Ω/0.5W speaker
  - — Right channel speaker driver for 32Ω/32mW earphone
- 9 Interrupt / Wakeup Sources (INT / WP)
  - — IOB[7:6] edge-triggered
  - — SDRAM read/write finished
  - — Timer overflow
  - — T16KHz, T8K,T2KHz, T128Hz, T8Hz
- SDRAM interface
  - — support 64M/128M bits SDRAM with 1/2/4/8 bits data bus.
- Up to 22 I/O pins
  - — IOA[7:0]:NMOS open drain output, CMOS input with pull low Resistor
  - — IOB[7:0]:COMS input / output,
- A2000 16Kbps compression algorithm for recording operation
  - — Object code of A2000 encoder/decoder provided
- Miscellaneous
  - — Multiplication with cumulative addition for user's digital filters

3. APPLICATION FIELD

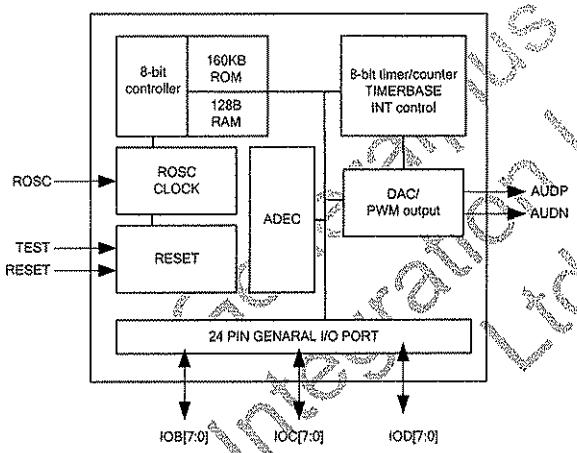
- High quality language repeater
- Language repeater with changed speed
- High quality voice recorder

SOUND CONTROLLER WITH 160KB ROM

1. GENERAL DESCRIPTION

The GPC11160C, a speech/wavetable synthesizer, equips an 8-bit CMOS microprocessor, and 160K-byte Working ROM, 128-byte working SRAM. Other primary features include two 8-bit Timer/Counters and can cascade to one 16-bit timer/counter, 24 Software Selectable I/Os, One 8-bit DAC and a pair of PWM output. It operates at a wide voltage range of 2.4V - 5.5V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 8MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The GPC11160C loads, not only the latest technology, but also the full commitment and technical support of Generalplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 160K bytes ROM
- 128-byte working SRAM
- Software-based audio processing
- Wide operating voltage: 2.4V - 5.5V @ 6.0MHz
  3.6V - 5.5V @ 8.0MHz
- Supports ROSC only
- Max. CPU clock: 6.0MHz @ 3.0V, 8MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings. Max. 2.0μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- 24 general I/Os (include 4 high brightness LED driving I/O)
- Low Voltage Reset (LVR) function
- Two 8-bit timer/counters and can cascade to one 16-bit timer/counter
- Six INT sources
- Key wake -up function
- IR function, crystal clock generator made by IO port
- External feedback input
- Watch dog function
- One DAC and A pair of PWM output

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- Advanced toy controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No	Type	Description
VDD1	1	I	Digital Power Pad
VSS1	10	I	Digital Ground
VDD2	19	I	Digital Power Pad
VSS2	15	I	Digital Ground
VDD3	20	I	Digital Power Pad
VSS3	37	I	Digital Ground
PVDD	12	I	PWM Power Pad
PVSS	13	I	PWM Ground
ROSC	18	I	ROSC Resistor input (Resistor must be connected to VDD)
RESET	17	I	Reset pin, active low to reset whole system
TEST	16	I	Test pin, NC
AUDP	14	O	Audio OUTPUT1
AUDN	11	O	Audio OUTPUT2
IOB0	21	I/O	Nibble-controlled programmable I/O pins
IOB1	22	I/O	In input mode, port B can be either pure or pull-low states. In output mode, port B can
IOB2	23	I/O	be buffer.
IOB3	24	I/O	
IOB4	25	I/O	
IOB5	26	I/O	
IOB6	27	I/O	
IOB7	28	I/O	
IOC0	29	I/O	Nibble-controlled programmable I/O pins
IOC1	30	I/O	In input mode, port C can be either pure or pull-low states. In output mode, port C can
IOC2	31	I/O	be buffer.
IOC3	32	I/O	IOC[3:0] can drive high brightness LED
IOC4	33	I/O	
IOC5	34	I/O	
IOC6	35	I/O	
IOC7	36	I/O	
IOD0	2	I/O	Bit-controlled programmable I/O pins
IOD1	3	I/O	In input mode, port D can be either pure or pull-low states
IOD2	4	I/O	In output mode, port D can be buffer
IOD3	5	I/O	Port D are the key wakeup I/O pins
IOD4	6	I/O	IOD4: feedback input of clock generator
IOD5	7	I/O	IOD5: feedback output of clock generator
IOD6	8	I/O	IOD6 : external interrupt
IOD7	9	I/O	IOD7: IR transmitter

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in GPC11160C is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

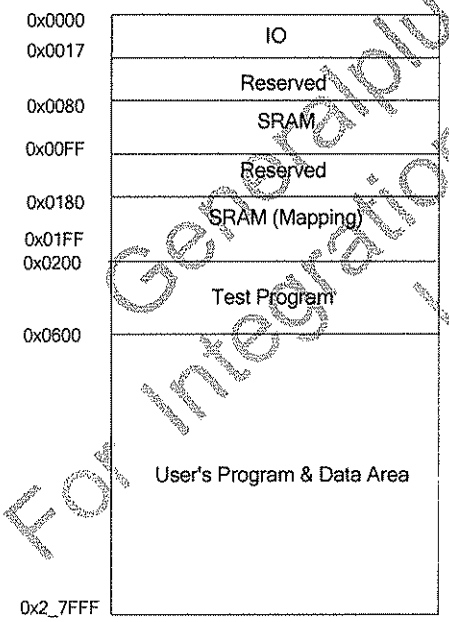
6.2. RAM Area

The total RAM size is 128-bytes (including Stack) starting from address $0080 through $00FF or mapping to $0180 through $01FF.

6.3. ROM Area

The GPC11160C provides a 160K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.4. Map of Memory and I/Os



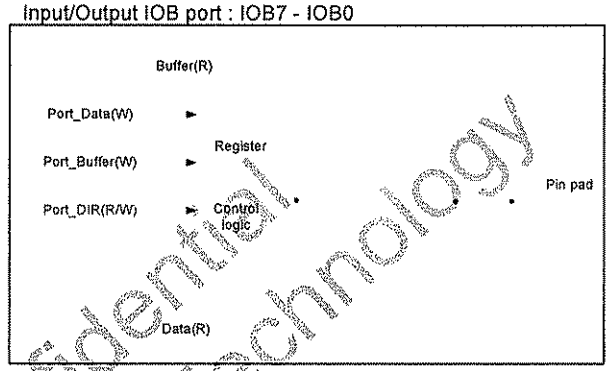
6.5. I/O Port

There are 24 IOs (IODB7-0, IOC7-0 and IOD7-0) in the GPC11160C. IOB7-0 and IOC7-0 are nibble-controlled IOs, but IOD7-0 are bit-controlled IOs. They can be programmed as input (pure input or pull-low) or output buffer. As pull-low input IOD7-0 keep a less impedance to get good noise immunity. While pressing the key (IOD7-0 to VDD), a large impedance remained to save the DC power. IOD4, IOD5 can be programmed as a RC or crystal clock generator by adding external resistor and capacitor. IOD6 can be programmed as an external interrupt source. IOD7 can be programmed as an IR transmitter.

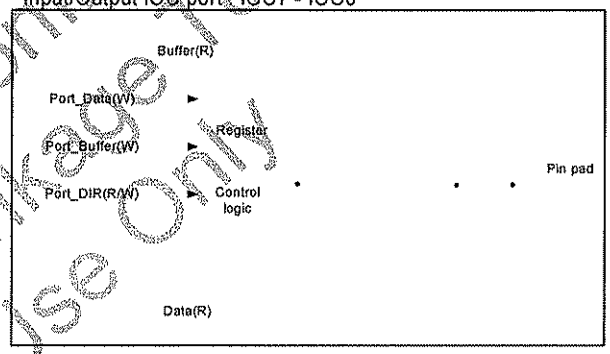
IOC[3:0] can sink high current to drive high brightness LED.

IO port configuration:

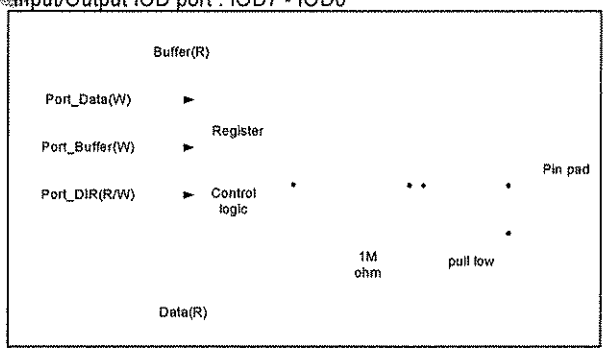
Input/Output IOB port : IOB7 - IOB0



Input/Output IOC port : IOC7 - IOC0



Input/Output IOD port : IOD7 - IOD0



6.6. Power Saving Mode

The GPC11160C includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awaken. Port IOD7-0 is the only wake-up source in the GPC11160C. After the GPC11160C is awaken, the internal CPU will go to the RESET State (Tw ≧ 64 x T1) and continue to execute program. Wakeup Reset will not