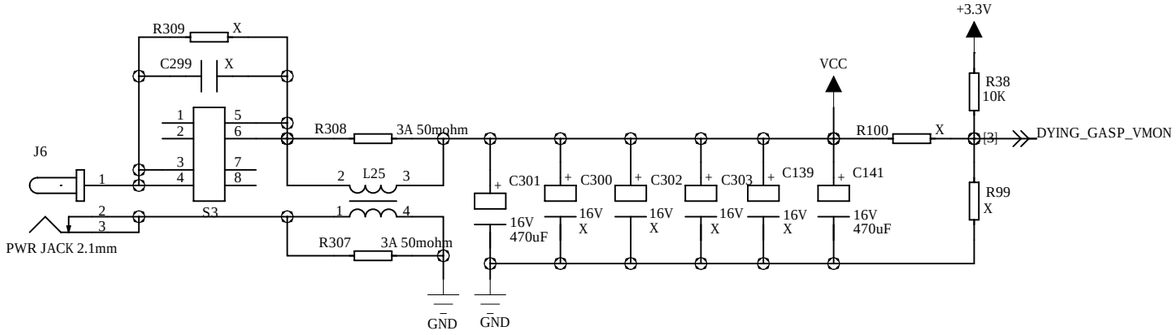
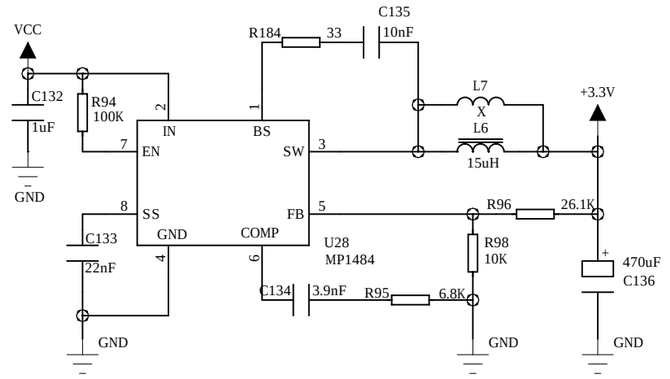
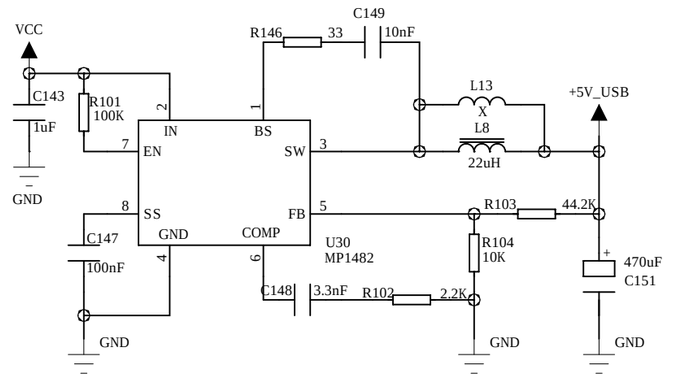
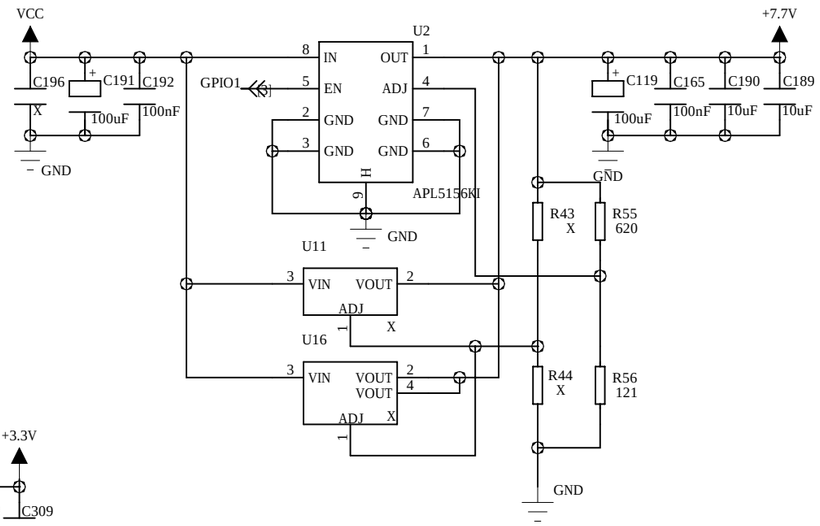




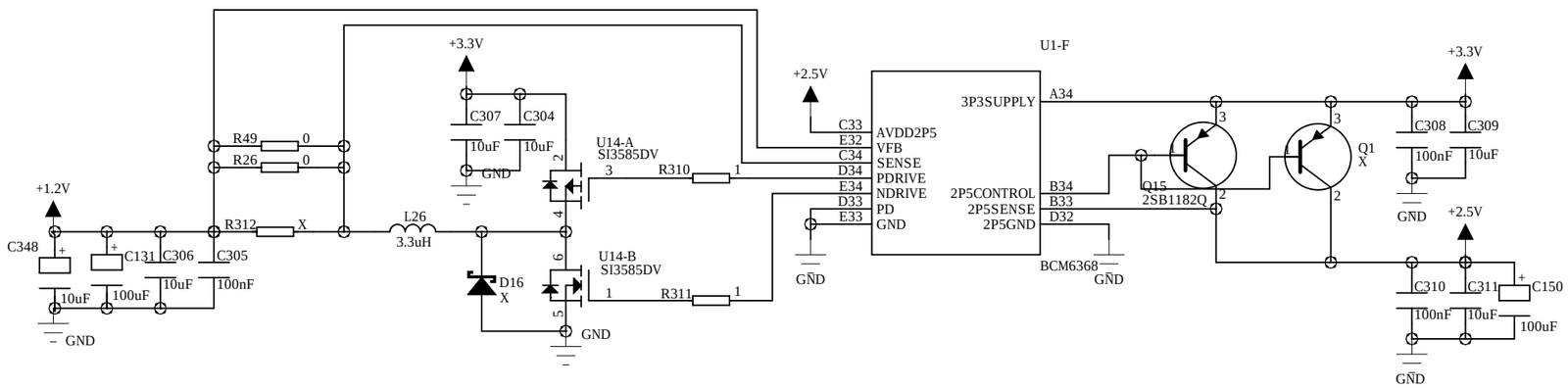


BCM6302 driver supply (7.7V) 500mA

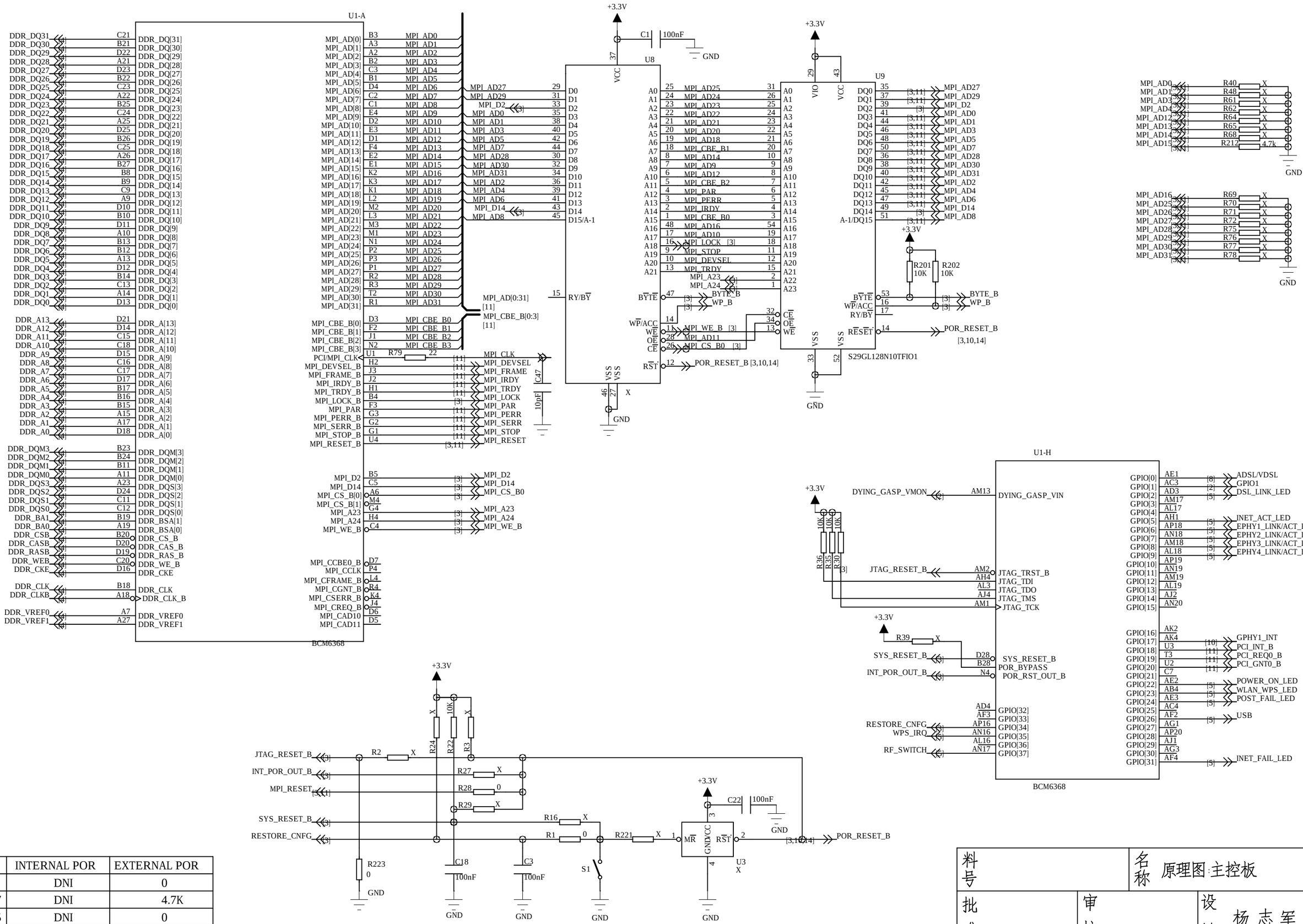


Digital I/O ring supply (2.5V) 655mA

Digital Core Logic Supply (1.2V) 1.214A

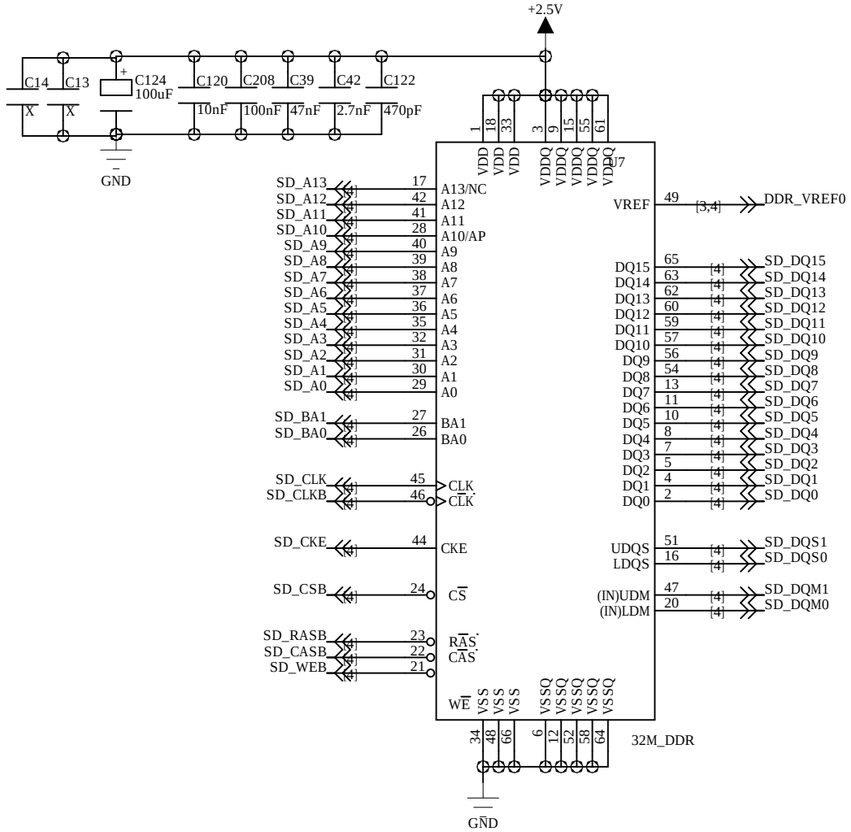


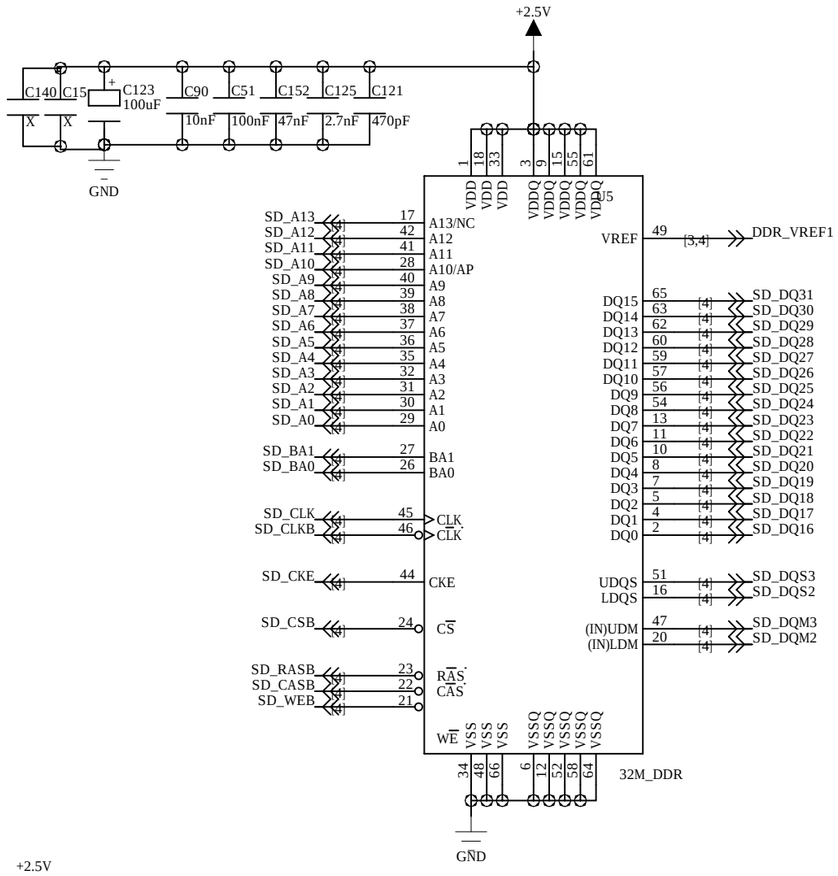
料号		名称	原理图:主控板
批准		审核	设计 杨志军

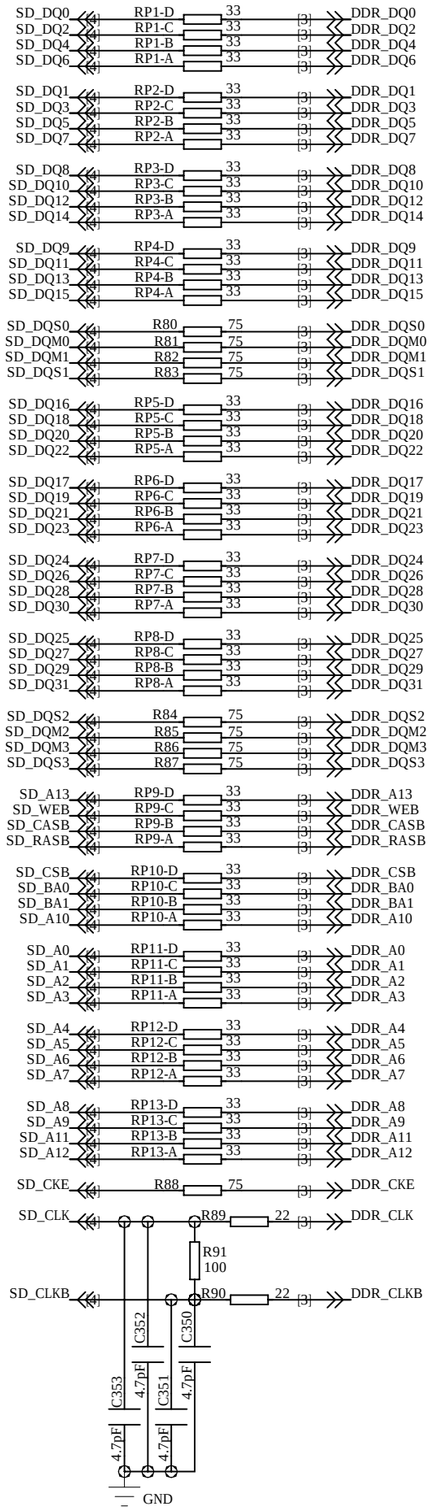


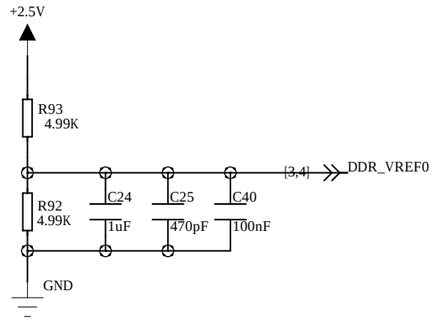
	INTERNAL POR	EXTERNAL POR
U3	DNI	0
R27	DNI	4.7K
R15	DNI	0
R14	0	DNI

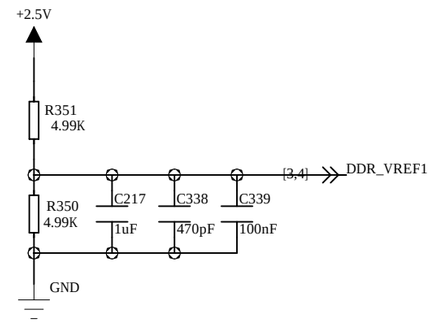
料号		名称	原理图:主控板
批准		审核	设计 杨志军

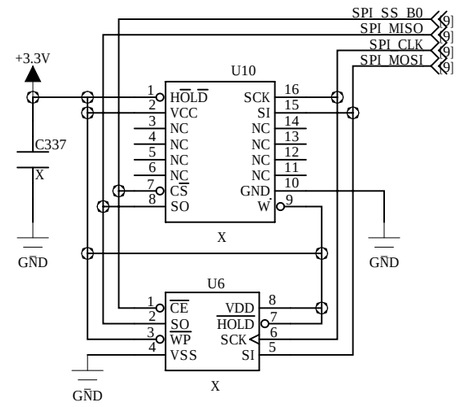








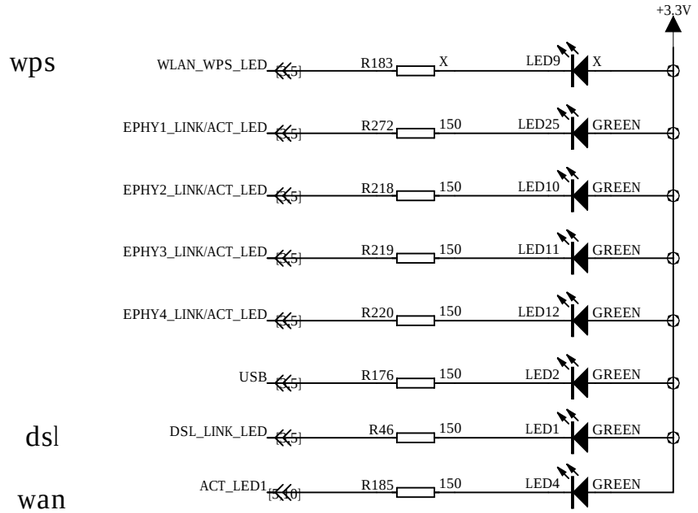


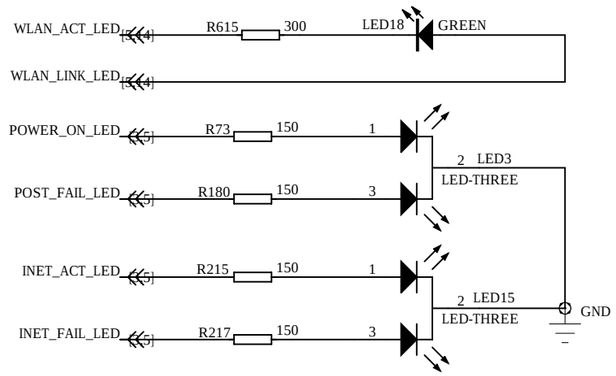


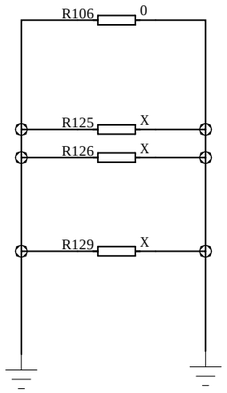
DDR SDRAM layout rules:

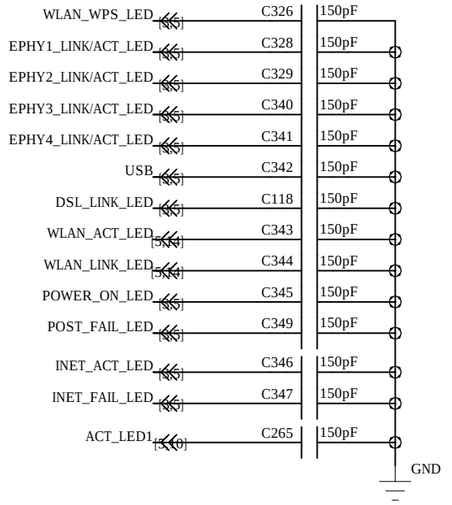
1. CLK/CLKb should be a matched differential pair with a length < 4"
2. Address and control should be +/- 0.75"(or 100ps)
3. DQS and DQM should be +/-0.75"(or 100ps)
4. All DQs should match corresponding byte lane DQS/DQMs Within +/-0.20"(or 30ps)
5. Trace impedances should be 60 ohms +/-10% (54-66ohms)
6. Route REF with 30-mil trace and at least 1 high quality ceramic bypass capacitor for each connection to a device
7. All traces should have a >=3 to 1 spacing ratio from the reference GND/PWR layer.(e.g. 15 mil line to line spacing for a 5 mil dielectric thickness

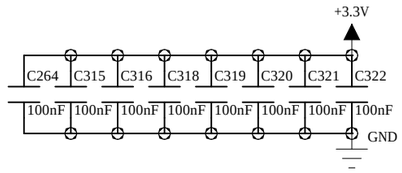
料号		名称	原理图:主控板
批准		审核	
设计	杨志军		

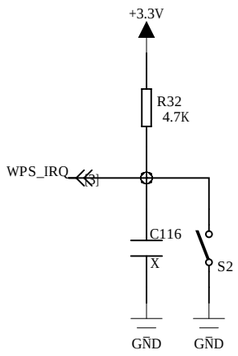


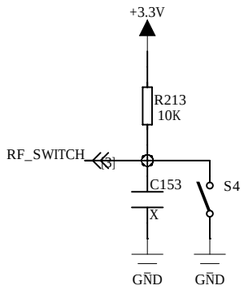




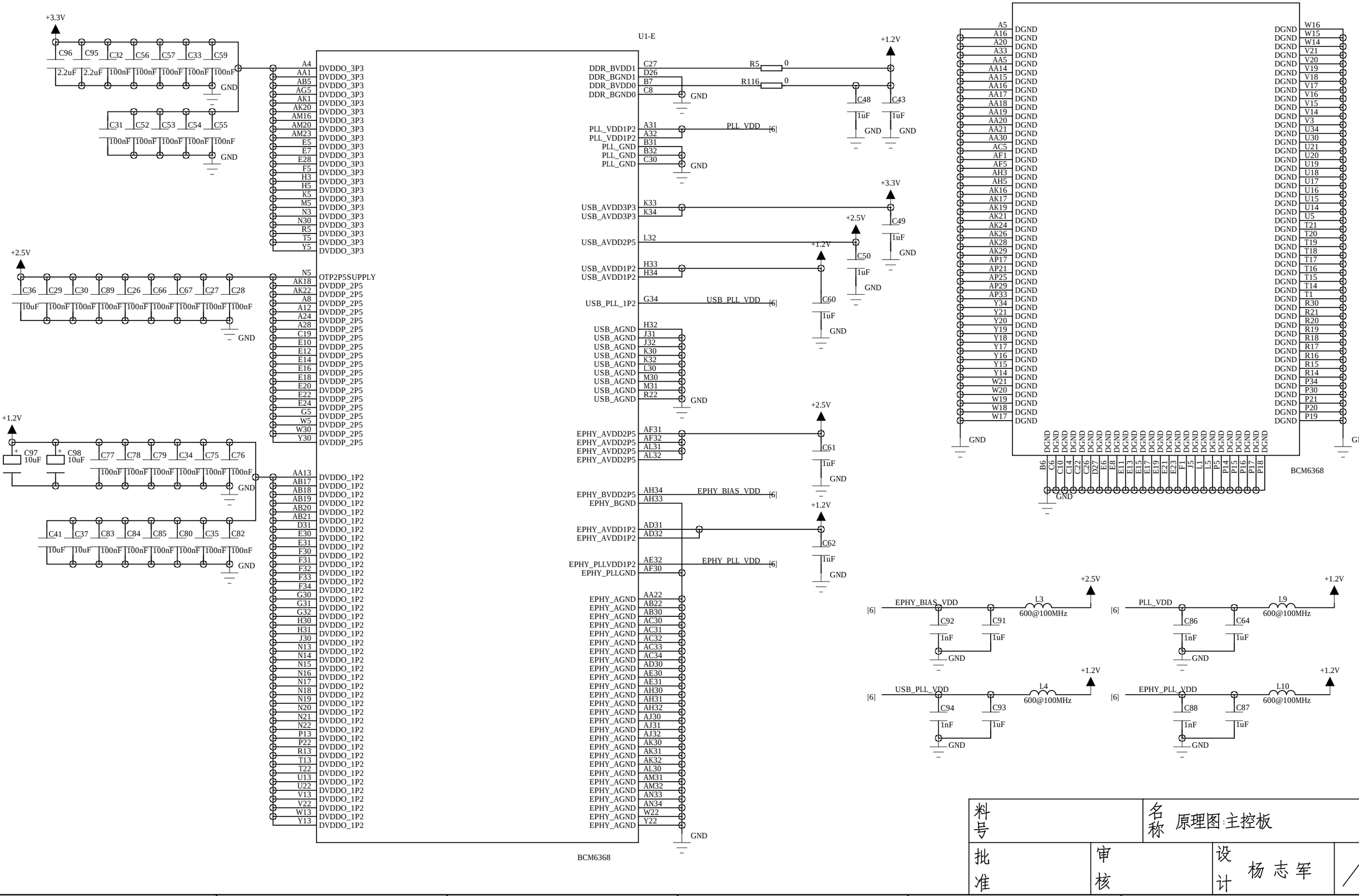






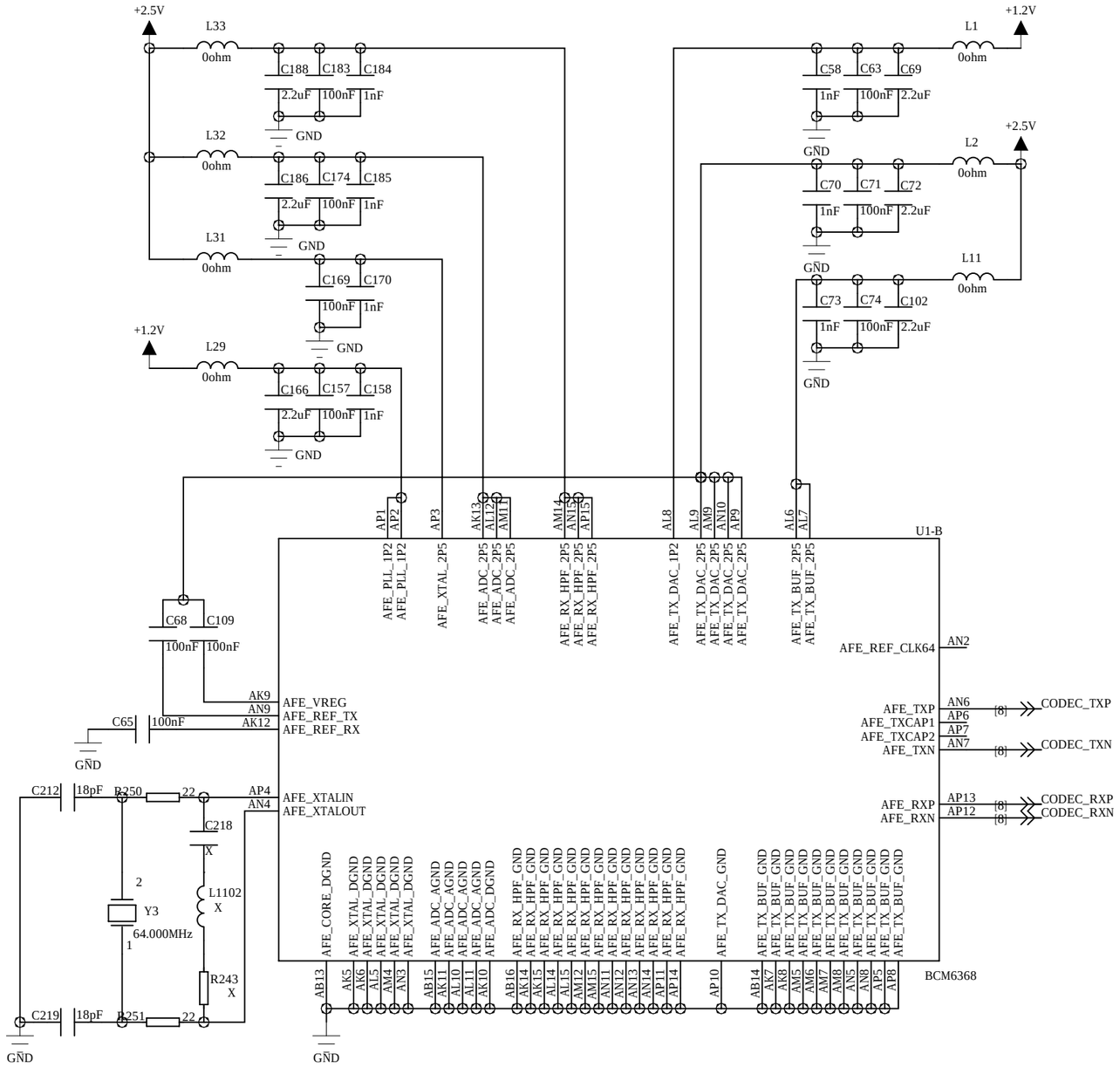


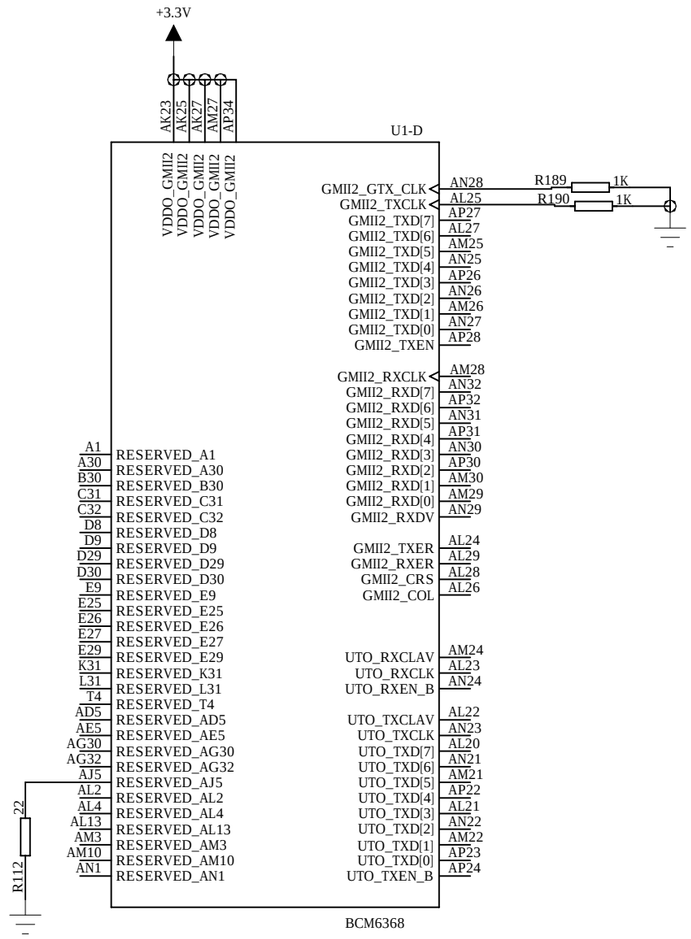
料号		名称	原理图:主控板
批准		审核	设计 杨志军

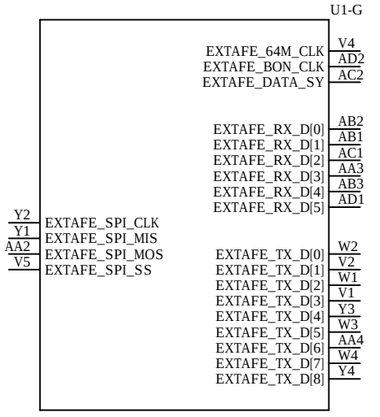

U1-E
U1-I
BCM6368
BCM6368
+3.3V
+2.5V
+1.2V
GND
DVDDO_3P3
DVDDP_2P5
DVDDO_1P2
OTP2P5SUPPLY
DDR_BVDD1
DDR_BGND1
DDR_BVDD0
DDR_BGND0
PLL_VDD1P2
PLL_GND
USB_AVDD3P3
USB_AVDD2P5
USB_AVDD1P2
USB_PLL_1P2
USB_AGND
EPHY_AVDD2P5
EPHY_BVDD2P5
EPHY_BGND
EPHY_AVDD1P2
EPHY_PLLVDD1P2
EPHY_PLLGND
EPHY_AGND
DGND
PLL_VDD
USB_PLL_VDD
EPHY_BIAS_VDD
EPHY_PLL_VDD
L3 600@100MHz
L4 600@100MHz
L9 600@100MHz
L10 600@100MHz
料号
名称 原理图:主控板
批准
审核
设计 杨志军

Connect VDDO_GMII2 to 3.3V used in GMII ,MII or UTOPIA MODE

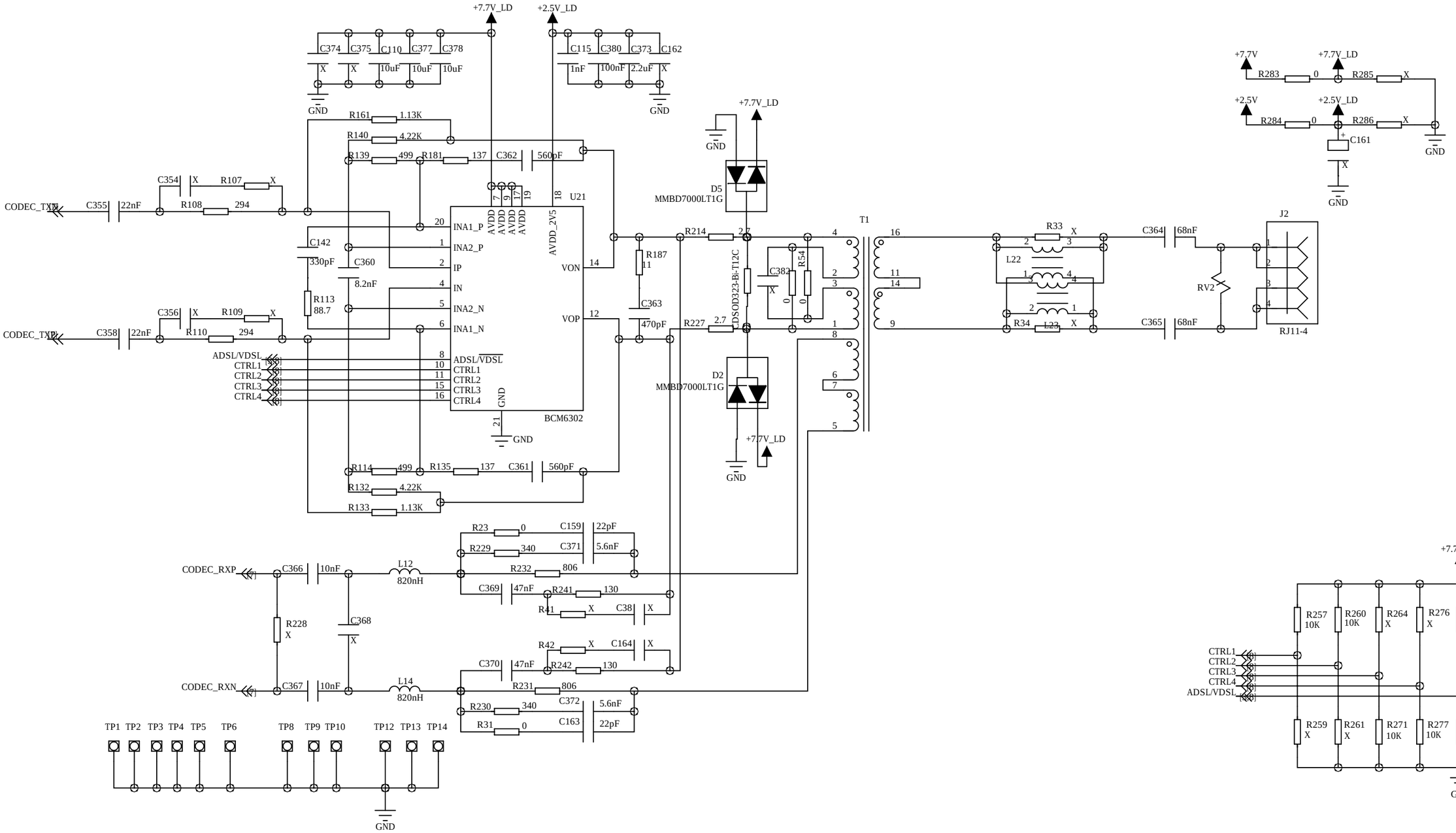
Connect VDDO_GMII2 to 2.5V when used in RGMII MODE







料号		名称	原理图:主控板
批准		审核	设计 杨志军

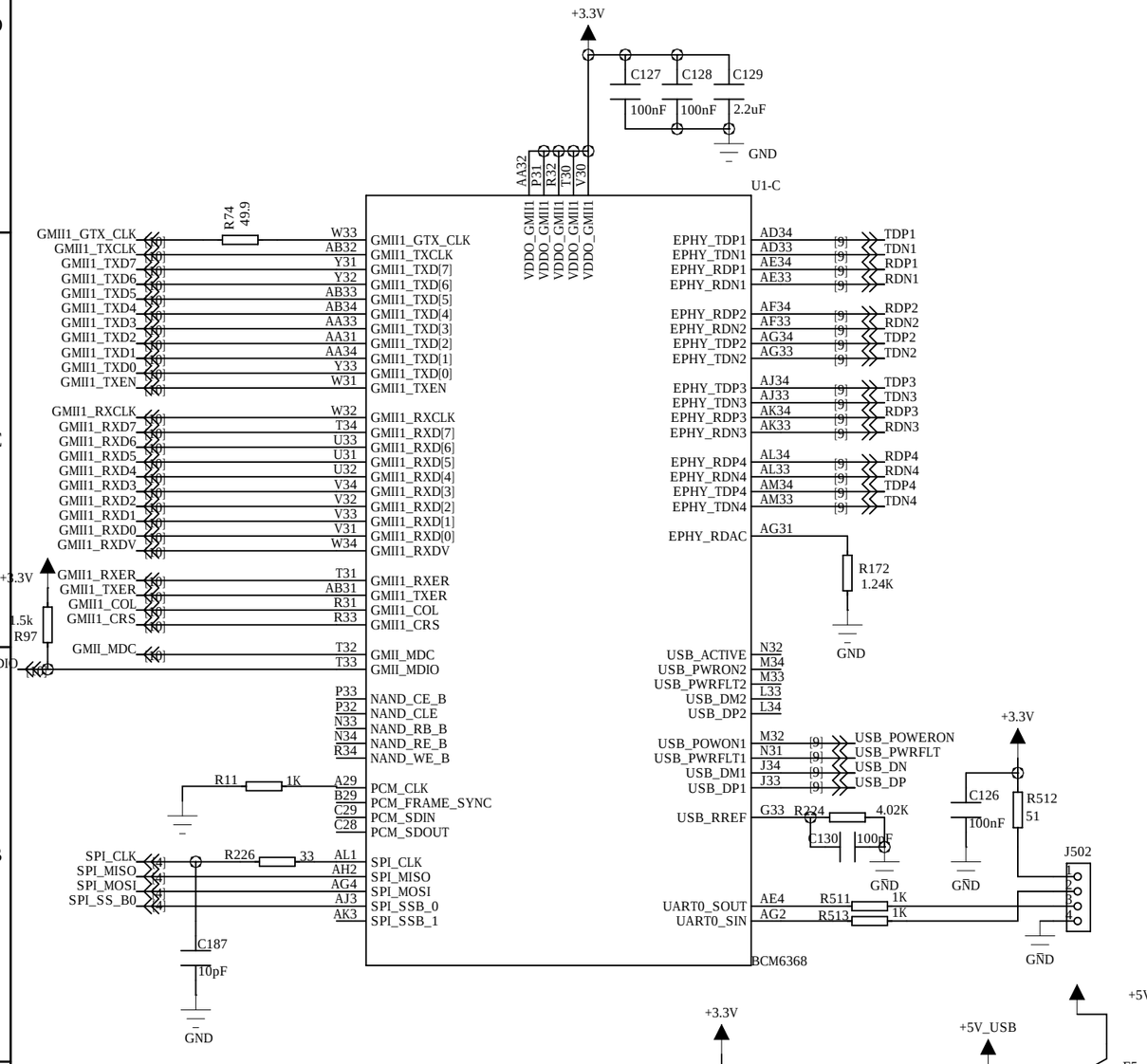


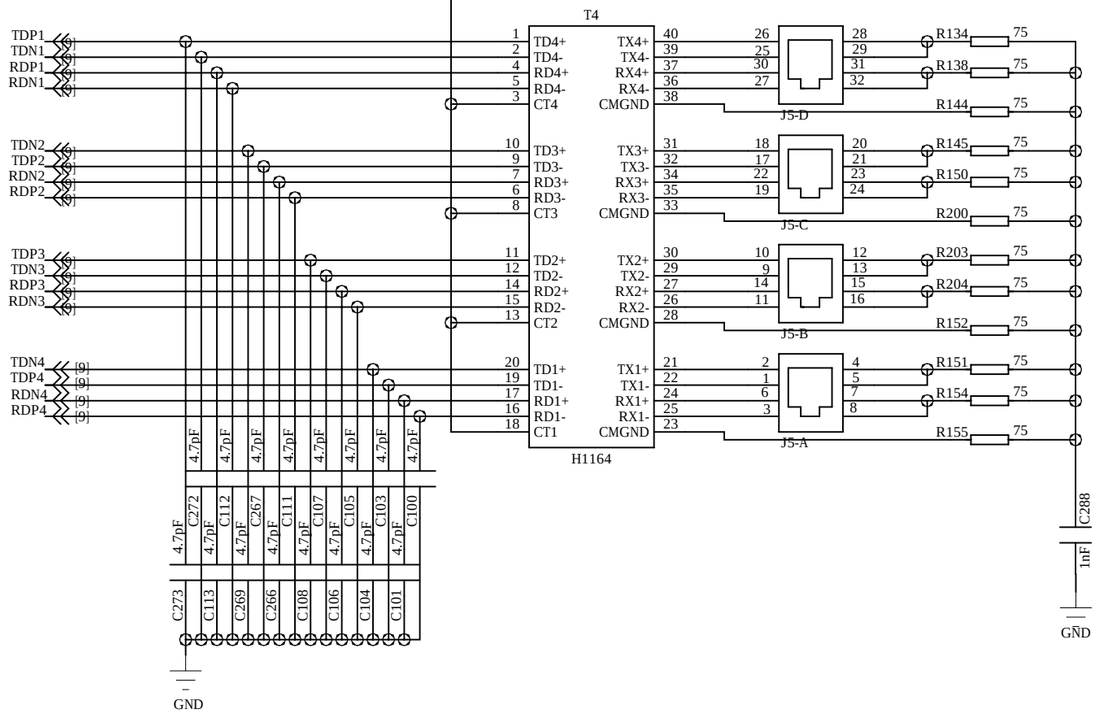
	Logic High	Logic Low	VIH	VIL
ADSL/VDSL	Set mode to ADSL Enable low pass filter	Set mode to VDSL Disable low pass filter	2.2V-8.1V	0V-3V
CTRL1	Norminal VDSL bias current	Reduce bias current by 20%	2.2V-8.1V	0V-3V
CTRL2	Norminal ADSL bias current	Reduce bias current by 20%	2.2V-8.1V	0V-3V
CTRL3	---	Always tie low	---	AVSS
CTRL4	Adds 8mA from AVDD to allow for additional slewing	---	AVDD	AVSS

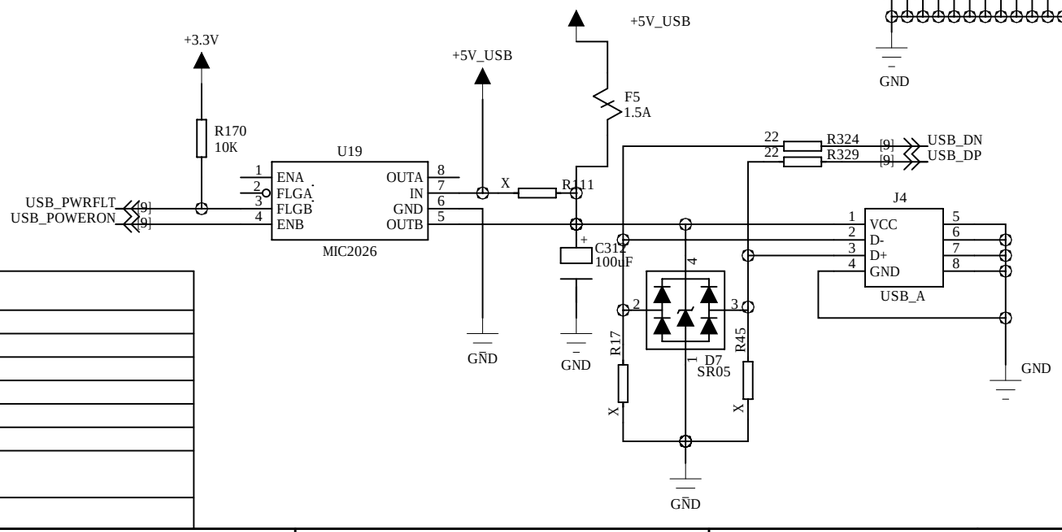
料号		名称	原理图:主控板
批准	审核	设计	杨志军

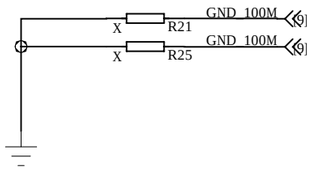
Connect VDDO_GMII1 to 3.3V when used in GMII,MII or nand mode

Connect VDDO_GMII1 to 2.5V when used in RGMII mode









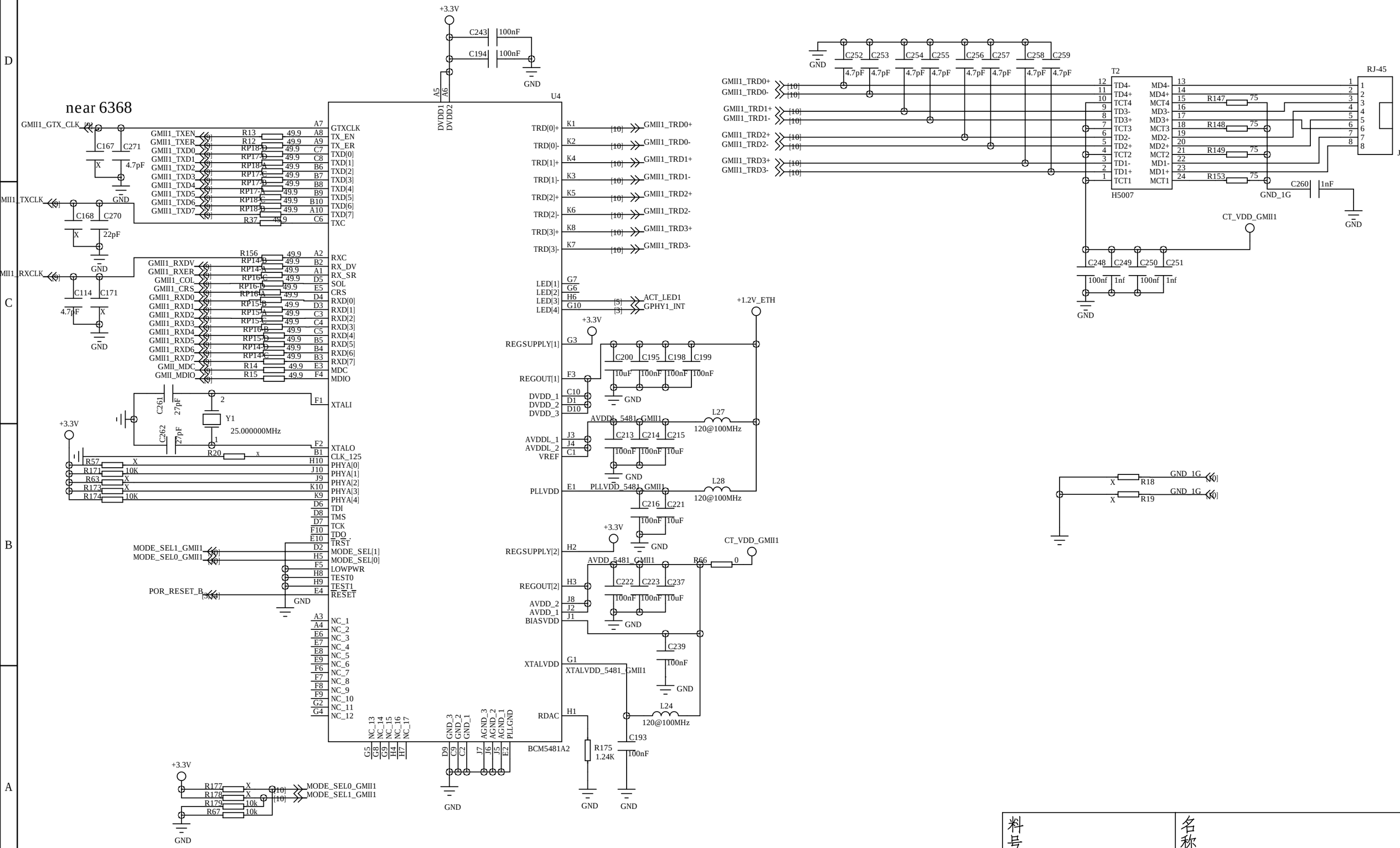
USB2.0 - Layout Guidelines & Notes

1. The Dp and Dn traces are length matched,with max differential skew,within 20mils.
2. Differential trace length must be less than 5 inchs.
3. No more than 2 vias per trace,perfer zero.
4. Never split the ground plane under differential pair routing
5. Route differential pairs above the GND plane.
6. Differential impendance is 90 ohms for USB.
7. Adjacent differential pairs should be separated by at least 3 times the trace width.
   9e.g. 7.5 mil trace ,leave >22.5mils between adjacent diff pairs)
8. Stitch GND vias around each differential pair, but NOT between a given pair.

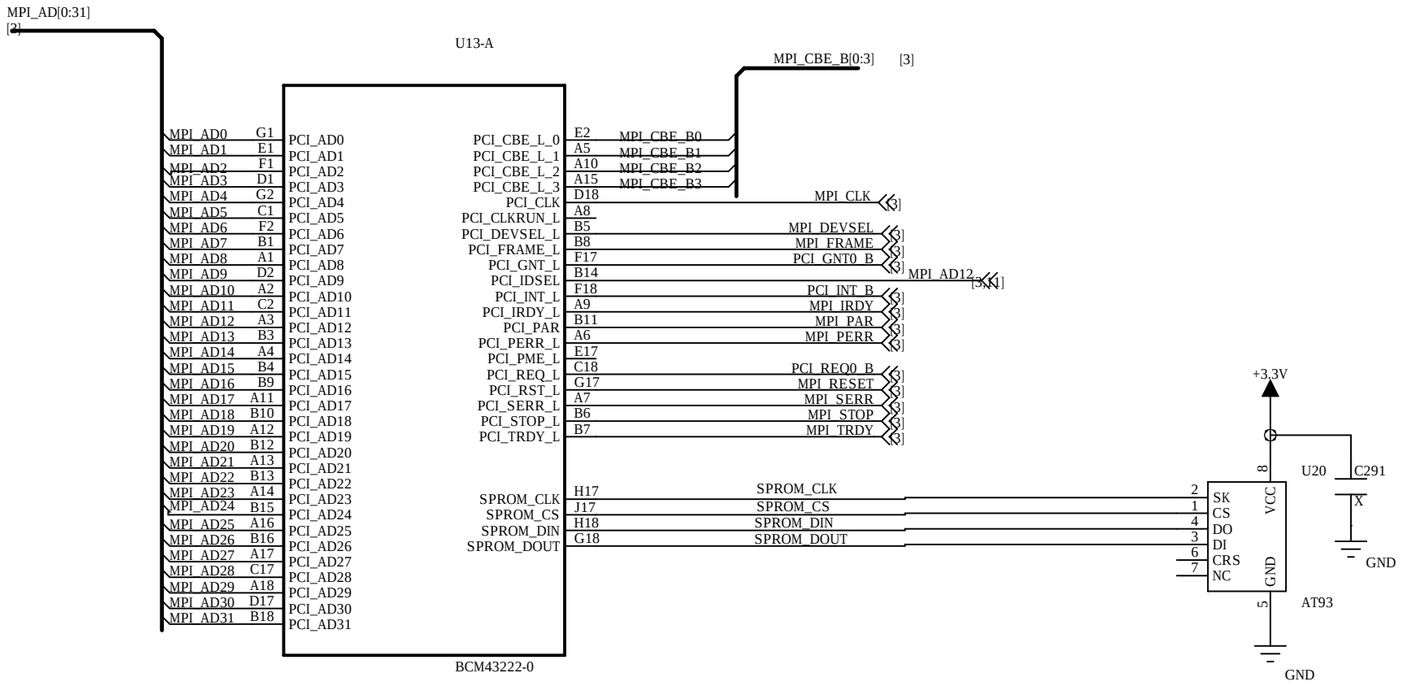
料号		名称	原理图:主控板
批准		审核	设计 杨志军

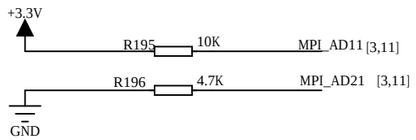
Route TRD+/- pairs with 100ohm differential trace immpedance

near 6368

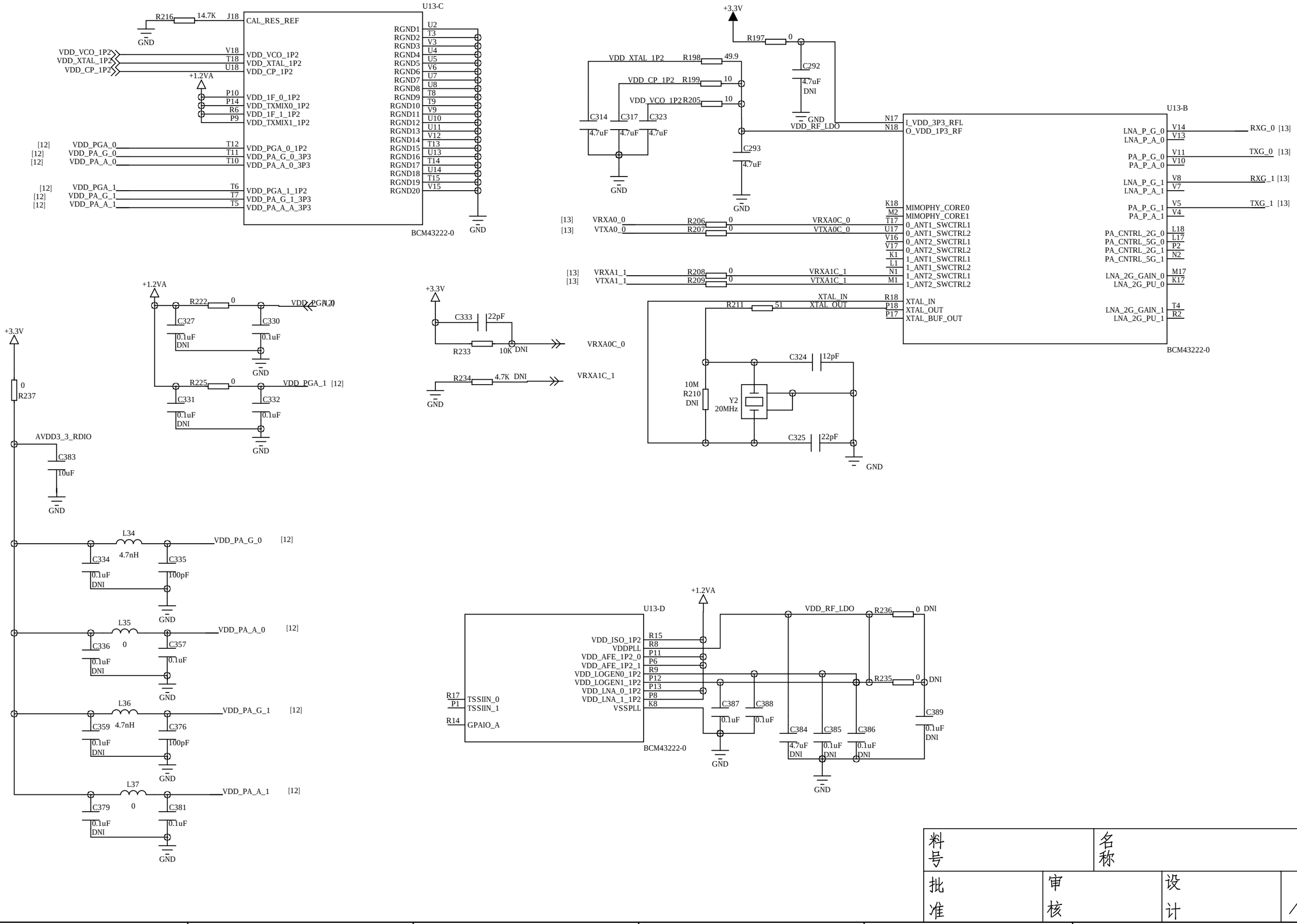


料号		名称	
批准	审核	设计	

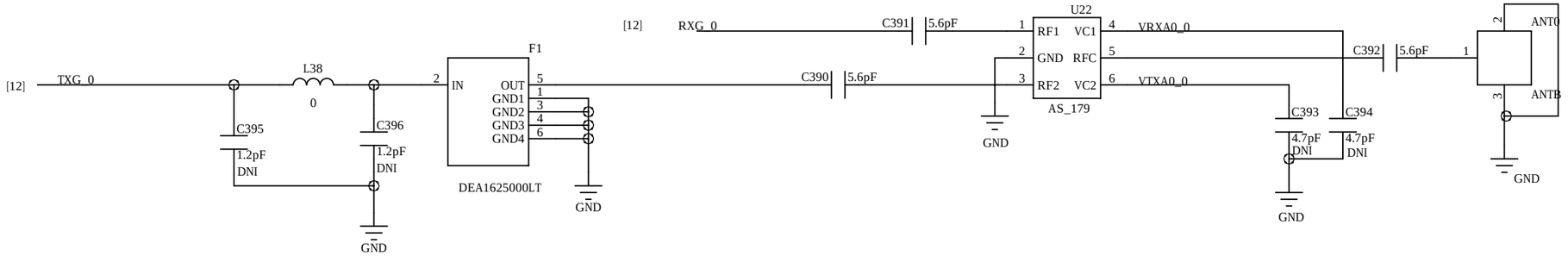

MPI_AD[0:31]
[3]
U13-A
MPI_CBE_B[0:3] [3]
MPI_AD0 G1
MPI_AD1 E1
MPI_AD2 F1
MPI_AD3 D1
MPI_AD4 G2
MPI_AD5 C1
MPI_AD6 F2
MPI_AD7 B1
MPI_AD8 A1
MPI_AD9 D2
MPI_AD10 A2
MPI_AD11 C2
MPI_AD12 A3
MPI_AD13 B3
MPI_AD14 A4
MPI_AD15 B4
MPI_AD16 B9
MPI_AD17 A11
MPI_AD18 B10
MPI_AD19 A12
MPI_AD20 B12
MPI_AD21 A13
MPI_AD22 B13
MPI_AD23 A14
MPI_AD24 B15
MPI_AD25 A16
MPI_AD26 B16
MPI_AD27 A17
MPI_AD28 C17
MPI_AD29 A18
MPI_AD30 D17
MPI_AD31 B18
PCI_AD0
PCI_AD1
PCI_AD2
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
PCI_AD28
PCI_AD29
PCI_AD30
PCI_AD31
PCI_CBE_L_0 E2 MPI_CBE_B0
PCI_CBE_L_1 A5 MPI_CBE_B1
PCI_CBE_L_2 A10 MPI_CBE_B2
PCI_CBE_L_3 A15 MPI_CBE_B3
PCI_CLK D18 MPI_CLK [3]
PCI_CLKRUN_L A8
PCI_DEVSEL_L B5 MPI_DEVSEL [3]
PCI_FRAME_L B8 MPI_FRAME [3]
PCI_GNT_L F17 PCI_GNT0_B [3]
PCI_IDSEL B14 MPI_AD12 [3,11]
PCI_INT_L F18 PCI_INT_B [3]
PCI_IRDY_L A9 MPI_IRDY [3]
PCI_PAR B11 MPI_PAR [3]
PCI_PERR_L A6 MPI_PERR [3]
PCI_PME_L E17
PCI_REQ_L C18 PCI_REQ0_B [3]
PCI_RST_L G17 MPI_RESET [3]
PCI_SERR_L A7 MPI_SERR [3]
PCI_STOP_L B6 MPI_STOP [3]
PCI_TRDY_L B7 MPI_TRDY [3]
SPROM_CLK H17 SPROM_CLK
SPROM_CS J17 SPROM_CS
SPROM_DIN H18 SPROM_DIN
SPROM_DOUT G18 SPROM_DOUT
BCM43222-0
+3.3V
U20
C291
X
SK
CS
DO
DI
CRS
NC
VCC
GND
AT93
GND
GND

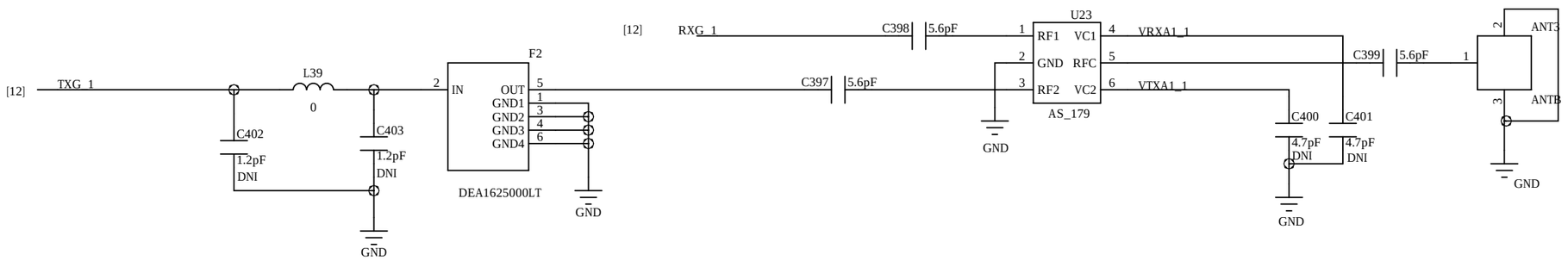

+3.3V
R195 10K MPI_AD11 [3,11]
R196 4.7K MPI_AD21 [3,11]
GND

料号		名称	
批准	审核	设计	

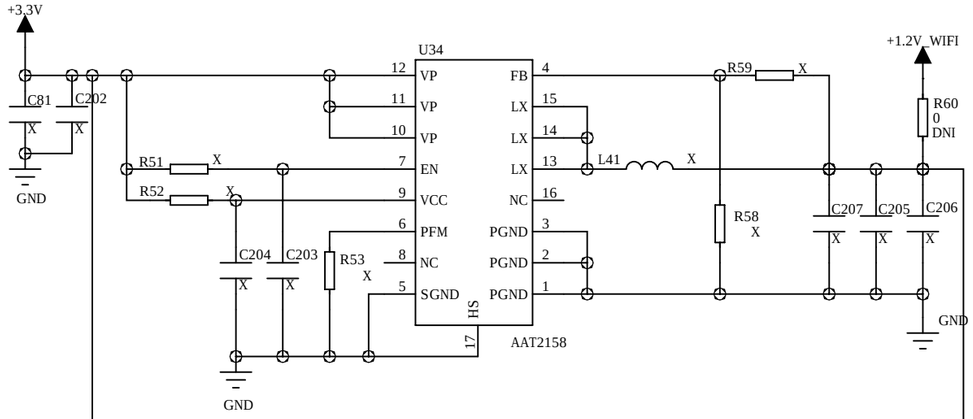

U13-C
R216 14.7K J18 CAL_RES_REF
GND
VDD_VCO_1P2 V18 VDD_VCO_1P2
VDD_XTAL_1P2 T18 VDD_XTAL_1P2
VDD_CP_1P2 U18 VDD_CP_1P2
+1.2VA
P10 VDD_1F_0_1P2
P14 VDD_TXMIX0_1P2
R6 VDD_1F_1_1P2
P9 VDD_TXMIX1_1P2
[12] VDD_PGA_0 T12 VDD_PGA_0_1P2
[12] VDD_PA_G_0 T11 VDD_PA_G_0_3P3
[12] VDD_PA_A_0 T10 VDD_PA_A_0_3P3
[12] VDD_PGA_1 T6 VDD_PGA_1_1P2
[12] VDD_PA_G_1 T7 VDD_PA_G_1_3P3
[12] VDD_PA_A_1 T5 VDD_PA_A_A_3P3
RGND1 U2
RGND2 T3
RGND3 V3
RGND4 U4
RGND5 U5
RGND6 V6
RGND7 U7
RGND8 U8
RGND9 T8
RGND10 T9
RGND11 V9
RGND12 U10
RGND13 U11
RGND14 V12
RGND15 T13
RGND16 U13
RGND17 T14
RGND18 U14
RGND19 T15
RGND20 V15
BCM43222-0
GND
+3.3V
R197 0
C292 4.7uF DNI
VDD_XTAL_1P2 R198 49.9
VDD_CP_1P2 R199 10
VDD_VCO_1P2 R205 10
C314 C317 C323 4.7uF 4.7uF 4.7uF
C293 4.7uF
VDD_RF_LDO
N17 I_VDD_3P3_RFL
N18 O_VDD_1P3_RF
U13-B
K18 MIMOPHY_CORE0
M2 MIMOPHY_CORE1
T17 0_ANT1_SWCTRL1
U17 0_ANT1_SWCTRL2
V16 0_ANT2_SWCTRL1
V17 0_ANT2_SWCTRL2
K1 1_ANT1_SWCTRL1
L1 1_ANT1_SWCTRL2
N1 1_ANT2_SWCTRL1
M1 1_ANT2_SWCTRL2
LNA_P_G_0 V14 RXG_0 [13]
LNA_P_A_0 V13
PA_P_G_0 V11 TXG_0 [13]
PA_P_A_0 V10
LNA_P_G_1 V8 RXG_1 [13]
LNA_P_A_1 V7
PA_P_G_1 V5 TXG_1 [13]
PA_P_A_1 V4
PA_CNTRL_2G_0 L18
PA_CNTRL_5G_0 L17
PA_CNTRL_2G_1 P2
PA_CNTRL_5G_1 N2
LNA_2G_GAIN_0 M17
LNA_2G_PU_0 K17
LNA_2G_GAIN_1 T4
LNA_2G_PU_1 R2
[13] VRXA0_0 R206 0 VRXA0C_0
[13] VTXA0_0 R207 0 VTXA0C_0
[13] VRXA1_1 R208 0 VRXA1C_1
[13] VTXA1_1 R209 0 VTXA1C_1
XTAL_IN R18
R211 51 XTAL_OUT P18
XTAL_BUF_OUT P17
BCM43222-0
C324 12pF
10M R210 DNI
Y2 20MHz
C325 22pF
GND
+1.2VA
R222 0 VDD_PGA_0 [12]
C327 0.1uF DNI
C330 0.1uF
R225 0 VDD_PGA_1 [12]
C331 0.1uF DNI
C332 0.1uF
+3.3V
C333 22pF
R233 10K DNI
VRXA0C_0
R234 4.7K DNI
VRXA1C_1
+3.3V
0 R237
AVDD3_3_RDIO
C383 10uF
L34 4.7nH
VDD_PA_G_0 [12]
C334 0.1uF DNI
C335 100pF
L35 0
VDD_PA_A_0 [12]
C336 0.1uF DNI
C357 0.1uF
L36 4.7nH
VDD_PA_G_1 [12]
C359 0.1uF DNI
C376 100pF
L37 0
VDD_PA_A_1 [12]
C379 0.1uF DNI
C381 0.1uF
U13-D
VDD_ISO_1P2 R15
VDDPLL R8
VDD_AFE_1P2_0 P11
VDD_AFE_1P2_1 P6
VDD_LOGEN0_1P2 R9
VDD_LOGEN1_1P2 P12
VDD_LNA_0_1P2 P13
VDD_LNA_1_1P2 P8
VSSPLL K8
R17 P1 TSSIIN_0
TSSIIN_1
R14 GPAIO_A
BCM43222-0
+1.2VA
VDD_RF_LDO
R236 0 DNI
R235 0 DNI
C387 0.1uF
C388 0.1uF
C384 4.7uF DNI
C385 0.1uF DNI
C386 0.1uF DNI
C389 0.1uF DNI
GND

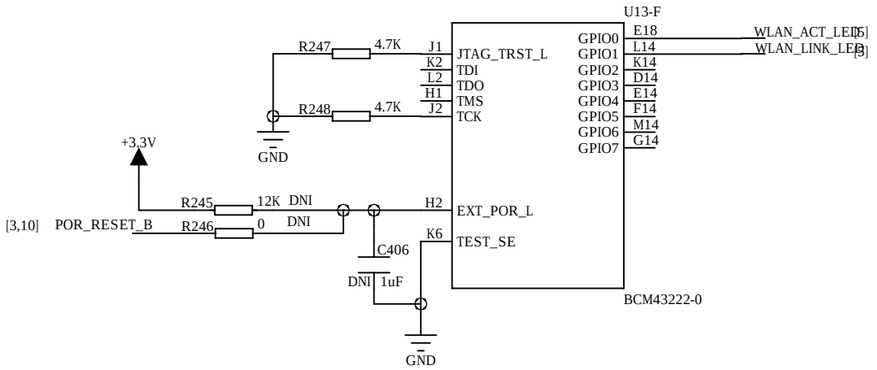
料号	名称		
批准	审核	设计	

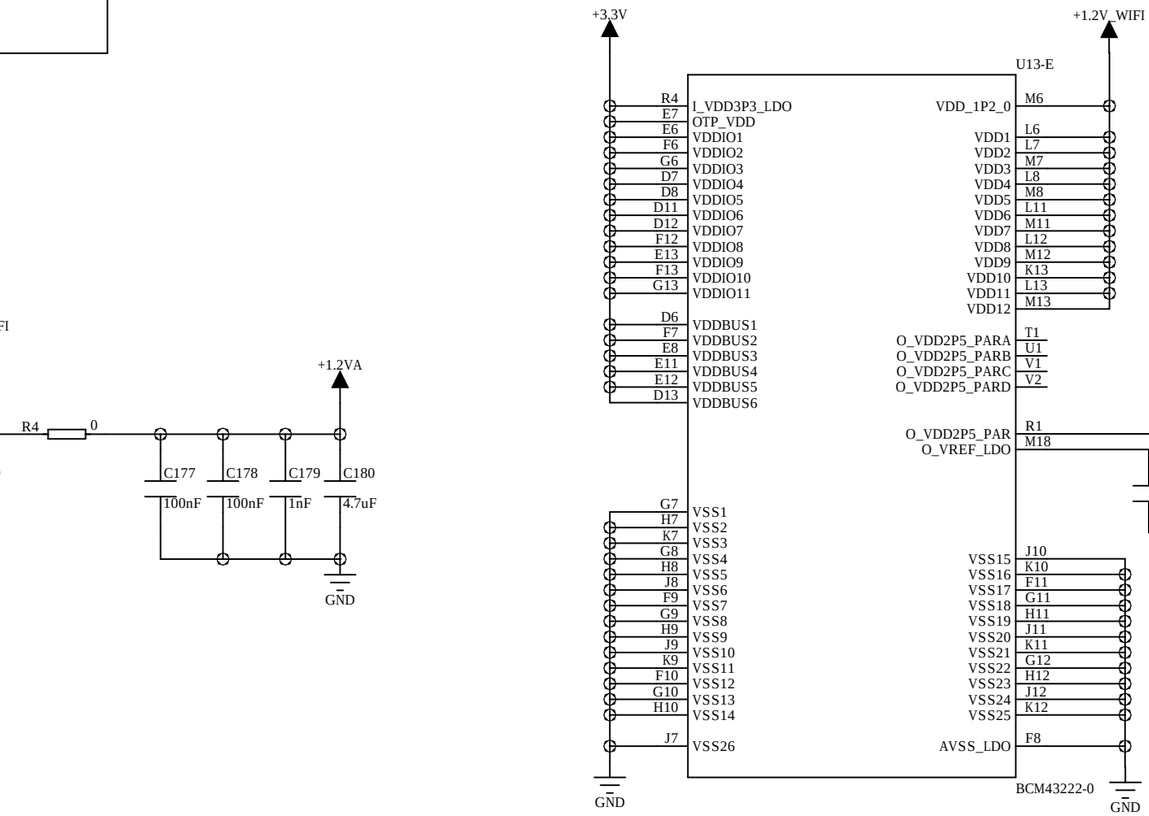

[12]
TXG_0
L38
0
C395
1.2pF
DNI
C396
1.2pF
DNI
GND
F1
2
IN
OUT
GND1
GND2
GND3
GND4
5
1
3
4
6
DEA1625000LT
GND
[12]
RXG_0
C391
5.6pF
C390
5.6pF
U22
RF1
VC1
GND
RFC
RF2
VC2
1
2
3
4
5
6
AS_179
GND
VRXA0_0
VTXA0_0
C392
5.6pF
C393
4.7pF
DNI
C394
4.7pF
DNI
GND
1
2
3
ANT0
ANTB
GND

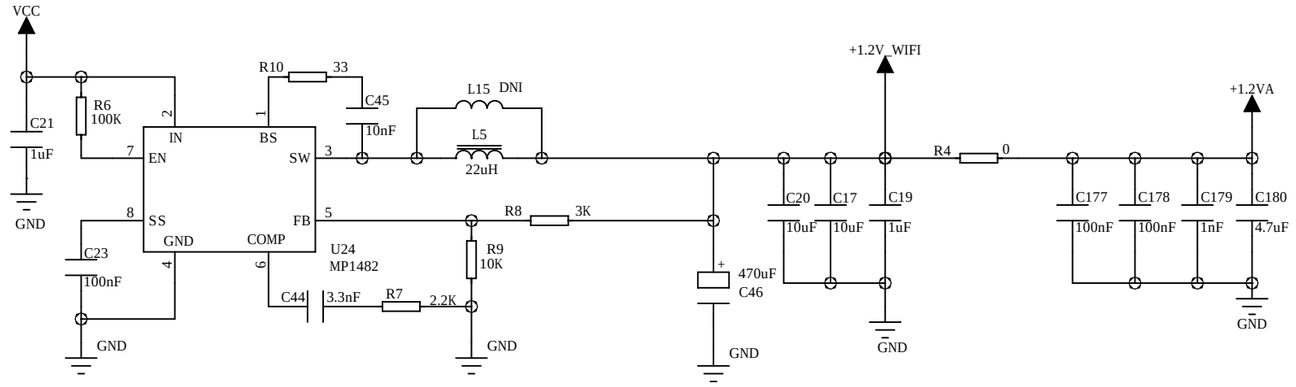

[12]
TXG_1
L39
0
C402
1.2pF
DNI
C403
1.2pF
DNI
GND
F2
2
IN
OUT
GND1
GND2
GND3
GND4
5
1
3
4
6
DEA1625000LT
GND
[12]
RXG_1
C398
5.6pF
C397
5.6pF
U23
RF1
VC1
GND
RFC
RF2
VC2
1
2
3
4
5
6
AS_179
GND
VRXA1_1
VTXA1_1
C399
5.6pF
C400
4.7pF
DNI
C401
4.7pF
DNI
GND
1
2
3
ANT3
ANTB
GND

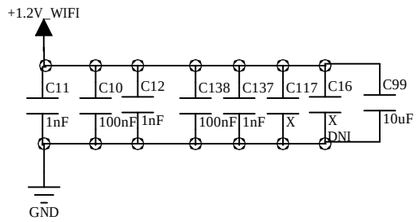
料号	名称		
批准	审核	设计	

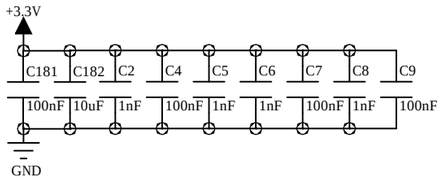

+3.3V
C81
C202
GND
U34
VP
VP
VP
EN
VCC
PFM
NC
SGND
FB
LX
LX
LX
NC
PGND
PGND
PGND
HS
17
AAT2158
R51
R52
C204
C203
R53
L41
R59
R58
C207
C205
C206
+1.2V_WIFI
R60
0
DNI
GND


U13-F
R247
4.7K
R248
4.7K
+3.3V
GND
JTAG_TRST_L
TDI
TDO
TMS
TCK
J1
K2
L2
H1
J2
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
E18
L14
K14
D14
E14
F14
M14
G14
WLAN_ACT_LED
WLAN_LINK_LED
[5]
[3]
R245
12K
DNI
R246
0
DNI
[3,10]
POR_RESET_B
H2
EXT_POR_L
K6
TEST_SE
C406
DNI
1uF
BCM43222-0


+3.3V
+1.2V_WIFI
U13-E
R4
E7
E6
F6
G6
D7
D8
D11
D12
F12
E13
F13
G13
D6
F7
E8
E11
E12
D13
G7
H7
K7
G8
H8
J8
F9
G9
H9
J9
K9
F10
G10
H10
J7
I_VDD3P3_LDO
OTP_VDD
VDDIO1
VDDIO2
VDDIO3
VDDIO4
VDDIO5
VDDIO6
VDDIO7
VDDIO8
VDDIO9
VDDIO10
VDDIO11
VDDBUS1
VDDBUS2
VDDBUS3
VDDBUS4
VDDBUS5
VDDBUS6
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS26
VDD_1P2_0
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDD10
VDD11
VDD12
O_VDD2P5_PARA
O_VDD2P5_PARB
O_VDD2P5_PARC
O_VDD2P5_PARD
O_VDD2P5_PAR
O_VREF_LDO
VSS15
VSS16
VSS17
VSS18
VSS19
VSS20
VSS21
VSS22
VSS23
VSS24
VSS25
AVSS_LDO
M6
L6
L7
M7
L8
M8
L11
M11
L12
M12
K13
L13
M13
T1
U1
V1
V2
R1
M18
J10
K10
F11
G11
H11
J11
K11
G12
H12
J12
K12
F8
C404
C405
10nF
1uF
BCM43222-0
GND


VCC
R6
100K
C21
1uF
GND
IN
EN
SS
GND
BS
SW
FB
COMP
U24
MP1482
R10
33
C45
10nF
L15
DNI
L5
22uH
R8
3K
R9
10K
C23
100nF
C44
3.3nF
R7
2.2K
470uF
C46
C20
C17
C19
10uF
10uF
1uF
R4
0
C177
C178
C179
C180
100nF
100nF
1nF
4.7uF
+1.2V_WIFI
+1.2VA


+1.2V_WIFI
C11
C10
C12
C138
C137
C117
C16
C99
1nF
100nF
1nF
100nF
1nF
X
X
DNI
10uF
GND


+3.3V
C181
C182
C2
C4
C5
C6
C7
C8
C9
100nF
10uF
1nF
100nF
1nF
1nF
100nF
1nF
100nF
GND

料号	名称		
批准	审核	设计	