PA module specification

MD7101_PA (DEMO)

General Description

The MD7101_PA module is designed for 2.4GHz ISM band wireless applications using AMIC A7101 FSK transceiver. This module features a fully programmable frequency synthesizer by SPI. The data rate is 57.6Kbps or 64Kbps.

Electrical specification

Item	Specification	Remark
Supply voltage	3.0 – 3.3 V	
Current consumption	6mA(typical) @sleep mode 8mA(typical) @stand-by mode 154mA(typical) @Tx mode, high power 36mA(typical) @Rx mode	MD7101_PA Tx/Rx switch[1:0]=00 for sleep and standby mode
Frequency	2416 – 2478 MHz	
Transmit output power	+4 ± 2 dBm @ high power, VIN = 3.3V	
Rx sensitivity	-86 dBm (typical)	BER≦1E-3
Modulation	FSK	
Transmission distance	15 meters (typical)	
Interface	15 pin 1.25mm header	
Dimension	47(L) x 25(W) x 1(H) mm^3	
Operating temperature	0 – 50 ℃	

Interface

Pin Number	Pin Name	Description	Note
1	Tx /Rx Switch	Switch[1:0]=10, Tx mode, PA enable	
2		Switch[1:0]=01, Rx mode, LNA enable	
3	VIN	Supply voltage.	
4	EN_REG	Voltage regulator enable pin. Signal is active high.	
5	SPI_LATCH	Latch for SPI interface	
6	SPI_CLOCK	Clock for SPI interface.	
7	SPI_DATA	Data for SPI interface.	
8	LVOUT	Battery-Low voltage indicator output. This pin is active low when LVIN is below BP_REG voltage level.	
9	LD	PLL locked detect indicator output, active high (open drain).	
10	TXDATAIN	Transmitter data input	
11	MUTE	Receiver mute control output pin.	
12	EN_AFC	AFC circuit control pin.	
13	XTALOUT	Buffered crystal oscillator output.	
14	RXDATA	Receiver data output.	
15	GND	Ground.	

Serial to Parallel Interface (SPI)

The SPI bus consists of three signals: SPI_DATA, SPI_CLOCK, and SPI_LATCH. This interface is used for external base-band controller to communicate with internal registers. The contents of the registers are shown in the following register description sections.

After setting SPI_LATCH signal to “Low” state, data on SPI_DATA is shifted into the internal shift register on the rising edge of SPI_CLOCK with MSB going in first. SPI_LATCH should be asserted at the end to latch the data packet into the register according to the address bits, bit 0 through bit 3, for each of the registers. All registers can only be written into except the Status Register which can only be read.

When the content of the Status Register need to be fetched by external controller, external baseband controller need to make sure that the address bits are pointing to address location 0x0 for proper read operation. After the address bits are shifted into the SPI interface and latched by asserting SPI_LATCH, the SPI interface will be in Read Mode and the content of the Status Register will be shifted out on SPI_DATA pin. When all 12 status bits have been shifted out, the SPI bus will be put back to Write Mode automatically.

A. Register Description

Note: Convention used:

1: Logic level “ONE”.
0: Logic level “ZERO”.
X: Don’t care.

Synthesizer Configuration Register I (Write only / Address 0xf)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
MB6	MB5	MB4	MB3	MB2	MB1	MB0	**MA4**	**MA3**	**MA2**	**MA1**	**MA0**	1	1	1	1

Synthesizer Configuration Register II (Write only / Address 0x7)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
X	MB9	MB8	MB7	**R7**	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**	0	1	1	1

Synthesizer Configuration Register I and Synthesizer Configuration Register II control synthesizer frequency settings where

MA[4:0]: A counter[4:0] . Valid range is from 0 to 31.
MB[9:0]: B counter[9:0] . Valid range is from 0 to 1023.
R[7:0]: R counter[7:0] . Valid range is from 2 to 255, for this module must be set to 0x78 at Rx mode and 0x18 at Tx mode.

The content of A, B and R registers are in unsigned binary format (i.e., $11111_2 = 31_{10}$).

The equation for setting the synthesizer frequency is:
$f_{vco} = f_{crystal} * (32*B + A) / R$, $(B > A)$.

For example :

For Rx mode
If f_{vco} = 2450MHz , f_{crysta} = 12MHz , $f_{reference}$ = 100KHz.
Then R = $f_{crysta} / f_{reference}$ = 120 = 01111000_2 , B = 765 = 1011111101_2 , A = 20 = 10100_2.

For Tx mode
If f_{vco} = 2450MHz , f_{crysta} = 12MHz , $f_{reference}$ = 500KHz.
Then R = $f_{crysta} / f_{reference}$ = 24 = 00011000_2 , B = 153 = 0010011001_2 , A = 4 = 00100_2.

Crystal Control Register (Write only / Address 0xb)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
0	DP	TXH2	TXH1	TXH0	TXL2	TXL1	TXL0	FX3	FX2	FX1	FX0	1	0	1	1

DP: Data Polarity. This control bit sets data output polarity.
0: Data is inverted.
1: Normal.

TXH[2:0]: Must be set to 0x0 for proper operation.
TXL[2:0]: Must be set to 0x0 for proper operation.
FX[3:0]: Must be set to 0x0 for proper operation.

VCO Control Register (Write only / Address 0x3)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
VTH2	VTH1	VTH0	T1	T0	HP0	CP2	CP1	CP0	VC2	VC1	VC0	0	0	1	1

VTH[2:0]: Set VCO tuning voltage range, for this module must be set to 0x6 for proper operation.

0x0 = 0.3 to VDD-0.3V , 0x1 = 0.4 to VDD-0.4V ,
0x2 = 0.5 to VDD-0.5V , 0x3 = 0.6 to VDD-0.6V ,
0x4 = 0.7 to VDD-0.7V , 0x5 = 0.8 to VDD-0.8V ,
0x6 = 0.9 to VDD-0.9V , 0x7 = 1.0 to VDD-1.0V ,

T[1:0]: Reserved. Must be set to 0x0 for proper operation.

HP0: RF output power level control.

0: Low power output (-16 dBm), for this module please set to low power mode when it operate on Tx mode..
1: High power output (-6 dBm).

CP[2]: Reserved. Must be set to 0x0 for proper operation.

CP[1:0]: Charge pump output current control, for this module must be set to 0x1(300uA) for proper operation.

0x0 = 100uA , 0x1 = 300uA ,
0x2 = 500uA , 0x3 = 700uA ,

VC[2:0]: Reserved. Must be set to 0x4 for proper operation.

RX Control Register (Write only / Address 0xd)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
T2	T1	T0	MT2	MT1	MT0	MTC	DM4	DM3	DM2	DMI	DM0	1	1	0	1

T[2:0]: Reserved. Must be set to 0x1 for proper operation.

MT[2:0]: Internal voltage threshold level for mute output (pin 37).

0x0 = 0.581*VDD , 0x1 = 0.516*VDD ,
0x2 = 0.452*VDD , 0x3 = 0.387*VDD ,
0x4 = 0.323*VDD , 0x5 = 0.258*VDD ,
0x6 = 0.194*VDD , 0x7 = 0.129*VDD ,

MTC: RXDATA mute function enable.

0: Disable mute function.
1: Enable mute function. When RSSI output voltage level is higher than the threshold set by MT[2:0], RXDATA becomes inactive and pull high.

DM[4:0]: Reference voltage level for demodulator tank center frequency tuning.
Valid range is from 0x1f to 0x6. The setting of DM varies with the voltage reference level such that when DM = 0x6 voltage reference = 0.9V and when DM = 0x1f voltage reference = 2.4V.

For this module must be set to 0x0 for proper operation.

Mode Select Register (Write only / Address 0x5)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
X	X	X	X	X	SC1	SC0	XOE	CM	EXTB	MD1	MD0	0	1	0	1

SC[1:0]: Status Register bit 6 control. Depends on the setting of SC[1:0], bit 6 of the Status Register can represent system error flag, Battery-low detect or PLL lock detect.

[1:0] = 10: System Error.
[1:0] = 11: Battery-low detect.
[1:0] = 0X: PLL lock detect.

XOE: Crystal oscillator buffer output enable.
0: Output enable.
1: Output disable. The output will be forced to low level at this setting.

CM: Reserved. Must be set to 1 for proper operation.

EXTB: Operating mode selection.
0: external mode. Operation mode is determined by external pin MODSEL0 and MODSEL1.
1: internal mode. Operation mode is determined by setting of MD[1:0].

MD[1:0]: Internal mode selection.
[1:0] = 00: Sleep mode. Transceiver circuit is turned off.
[1:0] = 01: Stand-by mode. X'TAL oscillator is turned on.
[1:0] = 10: Transmit mode.
[1:0] = 11: Receive mode.

Status Register (Read only / Address 0x0)

SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
X	X	X	X	X	X	X	X	X	S/B/P	X	X	0	0	0	0

S/B/P: Depends on the setting of SC[1:0] in Mode Select Register, this bit can be used to reflect the status of System Error, Battery-low detect .

System Error: 0: Normal; 1: Error.
Battery-low detect: 0: Battery supply voltage below threshold. 1: Normal.
PLL lock detect: 0: Unlock. 1: Lock.

SR[3:0]: Address bits.

B. SPI Timing Diagram

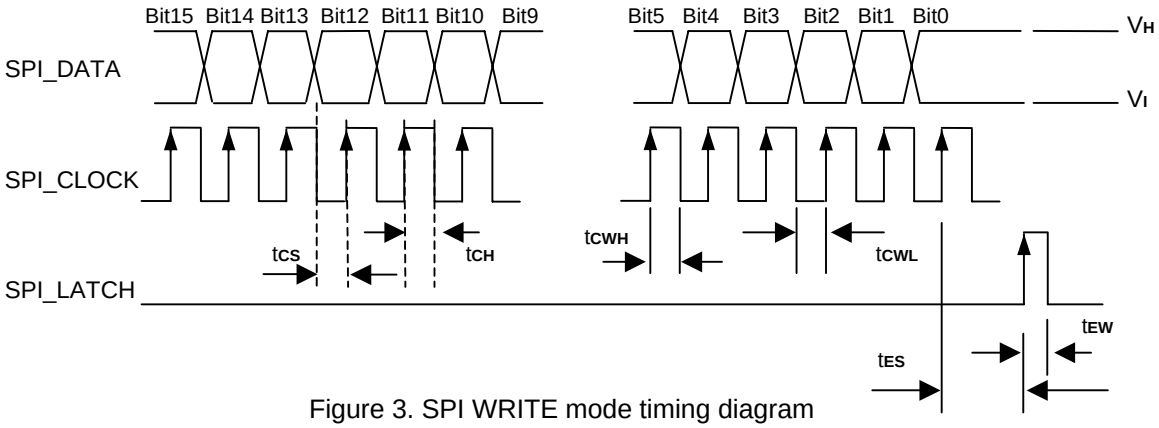


Figure 3. SPI WRITE mode timing diagram

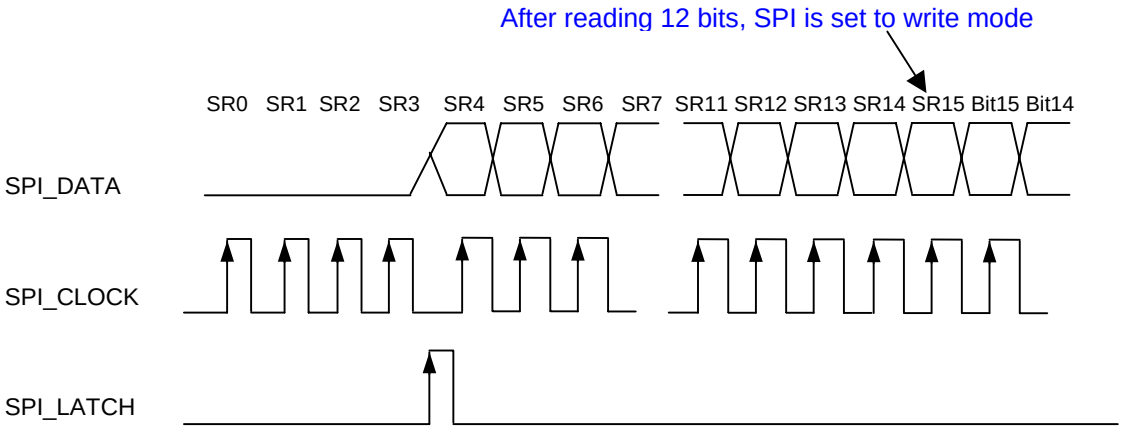


Figure 4. SPI READ mode timing diagram

C. SPI Timing Specification

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
V_H	The High level of voltage	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	VCC-0.4			V
V_I	The low level of voltage	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram			0.4	V
t_{CE}	SPI_DATA to SPI_CLOCK setup time	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{CH}	SPI_CLOCK to SPI_DATA hold time	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	10			ns
t_{CWH}	SPI_CLOCK pulse width high	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{CWL}	SPI_CLOCK pulse width low	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{ES}	SPI_CLOCK to SPI_LATCH setup time	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{EW}	SPI_LATCH pulse width	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns

Table 5.

Module setup procedure:

Step 1: Supply DC voltage to Pin 3, VIN.

Step 2: Reset IC by setting Pin 6, SPI_CLOCK and Pin 5, SPI _LATCH to logic high simultaneously for more than **1 us**.

Step 3: Setup IC's internal control registers by configuring the followings: Synthesizer Configuration Register I, Synthesizer Configuration Register II, Crystal Control Register, VCO Control Register, RX Control Register, and the Mode Select Register. All registers should be written to in the order specified above.

a. Synthesizer Configuration Register I and II: Set VCO center frequency.
b. VCO Control Register: Set VCO tuning range and charge pump output current.
c. RX Control Register: Set mute threshold level, RXDATA mute function and reference voltage for demodulator tank center frequency tuning. When **AFC** function is used, DM[4:0] must be set to **0x0** for proper operation.

Step 4: RX mode setting.

For Rx mode operation, set Mode Select Register to **0x05F5,** then set Pin 1, Tx to logic low and Pin 2, Rx to logic high.

TX mode setting.

For Tx mode operation, set Mode Select Register to **0x05E5**, then set Pin 1, Tx to logic high and Pin 2, Rx to logic low.

Whenever frequency is to be changed, or system error has been detected (by reading from the Status Register) the IC must be reset by repeating step **2, 3, 4-a,** and **5**.

Note: To fit FCC criteria, please set mode register to Rx mode before setting Tx mode .

SPI table for frequency setup:

Transmitter

Frequency (MHz)	Syn Reg I		Syn Reg. II.	
Tx	Hex	Binary	Hex	Binary
2416	4B8F	0100,1011,1000,1111	0067	0000,0000,0110,0111
2418	4B9F	0100,1011,1001,1111	0067	0000,0000,0110,0111
2420	4BAF	0100,1011,1010,1111	0067	0000,0000,0110,0111
2422	4BBF	0100,1011,1011,1111	0067	0000,0000,0110,0111
2424	4BCF	0100,1011,1100,1111	0067	0000,0000,0110,0111
2426	4BDF	0100,1011,1101,1111	0067	0000,0000,0110,0111
2428	4BEF	0100,1011,1110,1111	0067	0000,0000,0110,0111
2430	4BFF	0100,1011,1111,1111	0067	0000,0000,0110,0111
2432	4C0F	0100,1100,0000,1111	0067	0000,0000,0110,0111
2434	4C1F	0100,1100,0001,1111	0067	0000,0000,0110,0111
2436	4C2F	0100,1100,0010,1111	0067	0000,0000,0110,0111
2438	4C3F	0100,1100,1011,1111	0067	0000,0000,0110,0111
2440	4C4F	0100,1100,0100,1111	0067	0000,0000,0110,0111
2442	4C5F	0100,1100,0101,1111	0067	0000,0000,0110,0111
2444	4C6F	0100,1100,0110,1111	0067	0000,0000,0110,0111
2446	4C7F	0100,1100,0111,1111	0067	0000,0000,0110,0111
2448	4C8F	0100,1100,1000,1111	0067	0000,0000,0110,0111
2450	4C9F	0100,1100,1001,1111	0067	0000,0000,0110,0111
2452	4CAF	0100,1100,1010,1111	0067	0000,0000,0110,0111
2454	4CBF	0100,1100,1011,1111	0067	0000,0000,0110,0111
2456	4CCF	0100,1100,1100,1111	0067	0000,0000,0110,0111
2458	4CDF	0100,1100,1101,1111	0067	0000,0000,0110,0111
2460	4CEF	0100,1100,1110,1111	0067	0000,0000,0110,0111
2462	4CFF	0100,1100,1111,1111	0067	0000,0000,0110,0111
2464	4D0F	0100,1101,0000,1111	0067	0000,0000,0110,0111
2466	4D1F	0100,1101,0001,1111	0067	0000,0000,0110,0111
2468	4D2F	0100,1101,0010,1111	0067	0000,0000,0110,0111
2470	4D3F	0100,1101,0011,1111	0067	0000,0000,0110,0111
2472	4D4F	0100,1101,0100,1111	0067	0000,0000,0110,0111
2474	4D5F	0100,1101,0101,1111	0067	0000,0000,0110,0111
2476	4D6F	0100,1101,0110,1111	0067	0000,0000,0110,0111
2478	4D7F	0100,1101,0111,1111	0067	0000,0000,0110,0111

Table. 6

Receiver

Frequency (MHz)	Syn Reg I		Syn Reg. II.	
Rx	Hex	Binary	Hex	Binary
2405.4	DF6F	1101,1111,0110,1111	5787	0101,0111,1000,0111
2407.4	E0AF	1110,0000,1010,1111	5787	0101,0111,1000,0111
2409.4	E1EF	1110,0001,1111,1111	5787	0101,0111,1000,0111
2411.4	E32F	1110,0011,0010,1111	5787	0101,0111,1000,0111
2413.4	E46F	1110,0100,0110,1111	5787	0101,0111,1000,0111
2415.4	E5AF	1110,0101,1010,1111	5787	0101,0111,1000,0111
2417.4	E6EF	1110,0110,1111,1111	5787	0101,0111,1000,0111
2419.4	E82F	1110,1000,0010,1111	5787	0101,0111,1000,0111
2421.4	E96F	1110,1001,0110,1111	5787	0101,0111,1000,0111
2423.4	EAAF	1110,1010,1010,1111	5787	0101,0111,1000,0111
2425.4	EBEF	1110,1011,1111,1111	5787	0101,0111,1000,0111
2427.4	ED2F	1110,1101,0010,1111	5787	0101,0111,1000,0111
2429.4	EE6F	1110,1110,0110,1111	5787	0101,0111,1000,0111
2431.4	EFAF	1110,1111,1010,1111	5787	0101,0111,1000,0111
2433.4	F0EF	1111,0000,1111,1111	5787	0101,0111,1000,0111
2435.4	F22F	1111,0010,0010,1111	5787	0101,0111,1000,0111
2437.4	F36F	1111,0011,0110,1111	5787	0101,0111,1000,0111
2439.4	F4AF	0100,1100,1010,1111	5787	0101,0111,1000,0111
2441.4	F5EF	1111,0101,1111,1111	5787	0101,0111,1000,0111
2443.4	F72F	1111,0111,0010,1111	5787	0101,0111,1000,0111
2445.4	F86F	1111,1000,0110,1111	5787	0101,0111,1000,0111
2447.4	F9AF	1111,1001,1010,1111	5787	0101,0111,1000,0111
2449.4	FAEF	1111,1010,1111,1111	5787	0101,0111,1000,0111
2451.4	FC2F	1111,1100,0010,1111	5787	0101,0111,1000,0111
2453.4	FD6F	1111,1101,0110,1111	5787	0101,0111,1000,0111
2455.4	FEAF	1111,1110,1010,1111	5787	0101,0111,1000,0111
2457.4	FFEF	1111,1111,1111,1111	5787	0101,0111,1000,0111
2459.4	012F	0000,0001,0010,1111	6787	0110,0111,1000,0111
2461.4	026F	0000,0010,0110,1111	6787	0110,0111,1000,0111
2463.4	03AF	0000,0011,1010,1111	6787	0110,0111,1000,0111
2465.4	04EF	0000,0100,1111,1111	6787	0110,0111,1000,0111
2467.4	062F	0000,0110,0010,1111	6787	0110,0111,1000,0111

Table. 7

Example for SPI setup:

Tx Mode

Synthsizer configuration register I 324F Synthsizer configuration register II 1187	Osc Freq: 12 MHz F.D. Freq: 0.5 MHz VCO Frequency: 2450 MHz
Crystal control register 400B	Data: Normal
VCO control register C0C3	PA Power: Low Charge Pump: 300 uA VCO Vt Range: 0.9~1.6V VCO Band: Band 4
Rx control register 620D	Bit 13 must be '1'
Mode select register 05E5	Select Mode: Tx Oscillator Output: Off Status Mode: System Detect Calibration: Auto

Rx Mode

Synthsizer configuration register I F4AF Synthsizer configuration register II 5787	Osc Freq: 12 MHz F.D. Freq: 0.1 MHz VCO Frequency: 2439.4 MHz

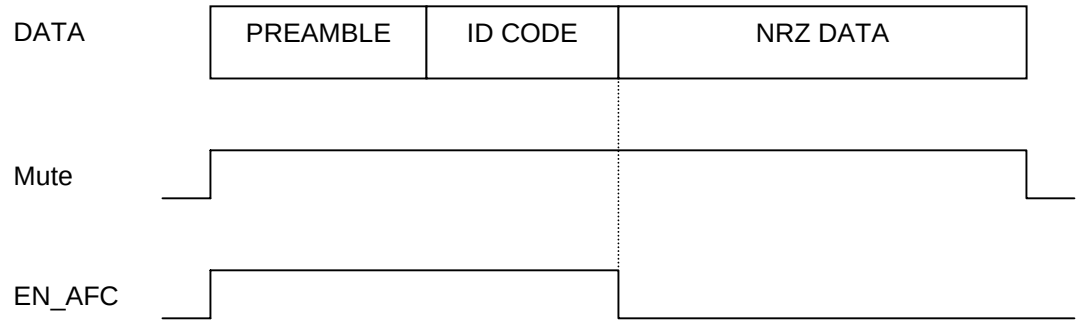
Crystal control register 400B	Data: Normal
VCO control register C4C3	PA Power: High Charge Pump: 300 uA VCO Vt Range: 0.9~1.6V VCO Band: Band 4
Rx control register 600D	Mute Threshold: 1.44V Data Mute Ctrl: Off Timing Ctrl: 256T
Mode select register 05F5	Select Mode: Rx Oscillator Output: Off Status Mode: System Detect Calibration: Auto
Rx control register 620D	Mute Threshold: 1.44V Data Mute Ctrl: ON Timing Ctrl: 256T
Rx control register 660D	Mute Threshold: 1.28V Data Mute Ctrl: ON Timing Ctrl: 256T
Rx control register 6A0D	Mute Threshold: 1.12V Data Mute Ctrl: ON Timing Ctrl: 256T

Note: You can optimize the performance of receiver by tuning mute threshold voltage.

Data format for data rate 57.6Kbps

1.) Preamble length: The length must larger than 32 bits and the format should be fit 101010….. or 010101….. .
2.) ID code: The times of '1' must be equal than '0' , and the continuous times of '1' and '0' should be less than 2 bits.
3.) About the architecture of NRZ data and Manchester data, please refer the timing diagram.

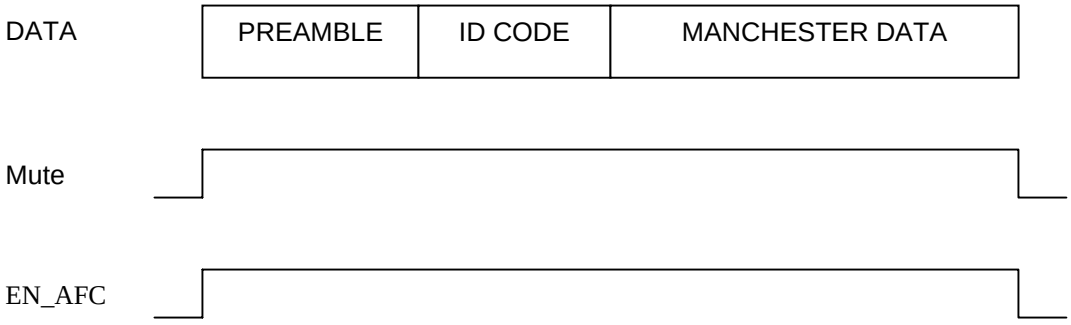
Timing Diagram for NRZ data



Note: EN_AFC be controlled by firmware when Mute from Lo to Hi, and disable EN_AFC (Lo level) after ID code has be received.

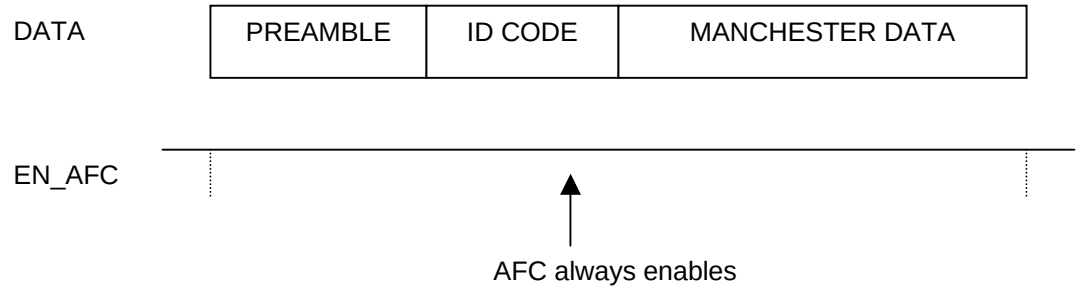
Timing Diagram for Manchester data

Method I:



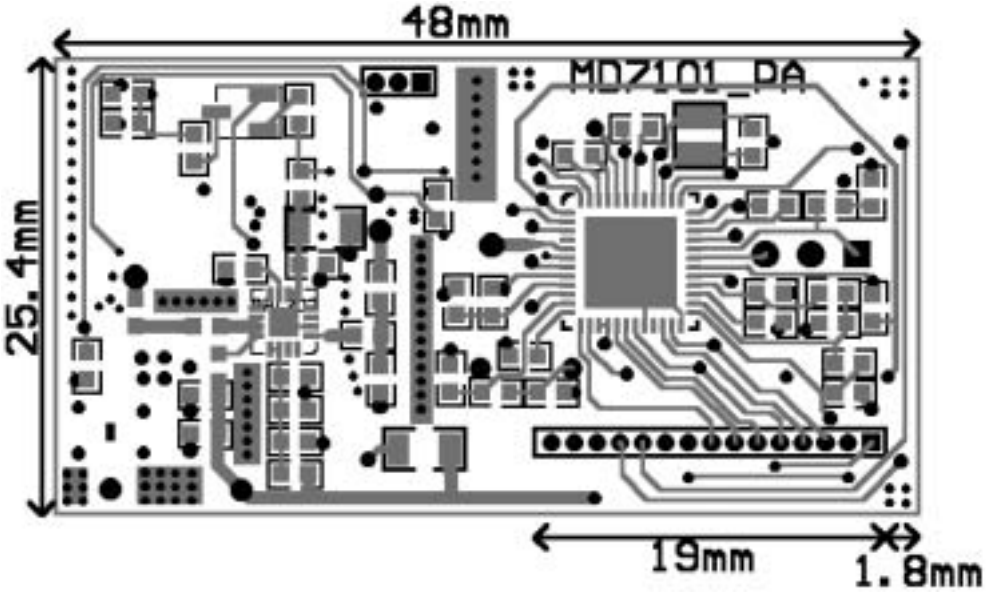
Note: EN_AFC(J2_pin2) could be controlled by firmware or Mute pin and please enable EN_AFC (Hi level) when Mute from Lo to Hi and then disable EN_AFC when Mute from Hi to Lo.

Method II:

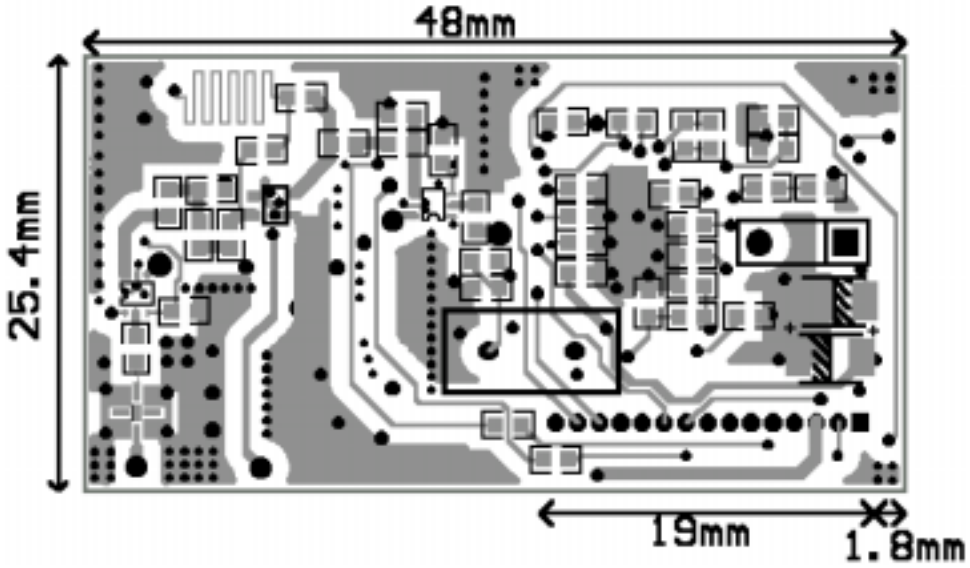


Note: EN_AFC always be enable(Hi level).

Module dimension and layout drawings



Top side layout



Bottom side layout