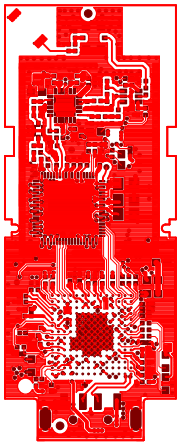
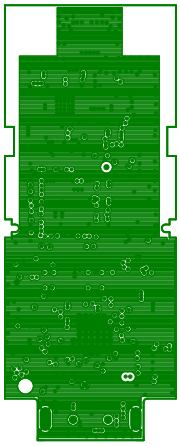
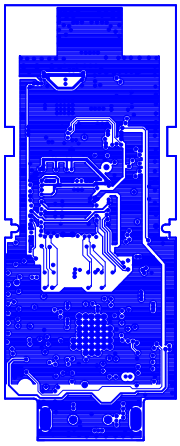


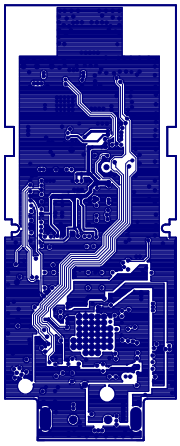
ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Top Route



ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Layer 2

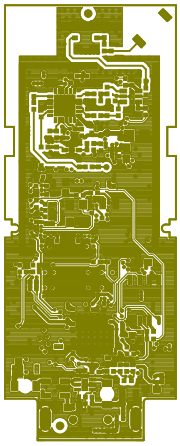


ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Layer 3



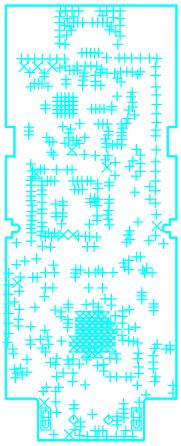
ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Layer 4

ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Layer 5

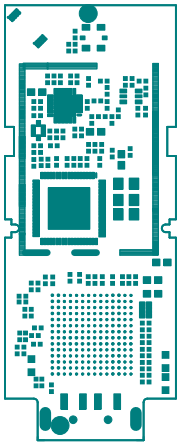


ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Bottom Route

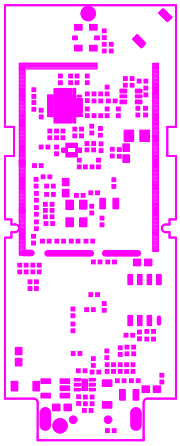
SIZE	QTY	SYM	PLTD	TOL
10	467	+	YES	+/-3
16	10	X	YES	+/-3
30 x 95	2	◳	YES	+/-3
43	2	◇	NO	+/-3
20	41	⧖	YES	+/-3



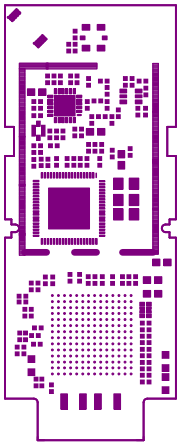
ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Drill Drawing
PCB P/N	8WUSN02..1B1G
PCB W/G	5/5
PCB Layer	6
PLD Engineer	Janis Huang
IDD Approved	Name
PLD Approved	Name
R&D Engineer	Jack Chen
R&D Approved	Name
LDS No.	LDS2006120094



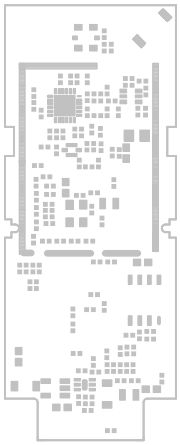
ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Solder Mask Top



ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Solder Mask Bottom

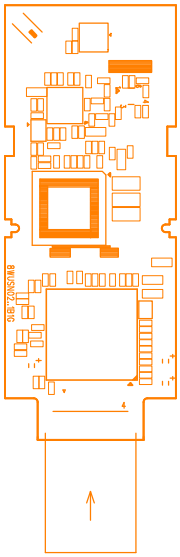


ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Paste Mask Top



ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Paste Mask Bottom

ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Silkscreen Bottom



ALPHA Networks Inc.	
PCB Name	WUS-N02
PCB Rev.	1B1G
Date	2007/01/03
Layer Name	Silkscreen Top