

WP1200 REFERENCE DESIGN

PCI Testing Board

(D02-RM-03A-10)

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REVISION HISTORY		
PREVIOUS VERSION: DB-1-R0-F-AC DB611823.DSN		
DATE	DESCRIPTION	REVISION
09/26/03	del C5 CONNECT C164.1 -> GND	V1.0 (LAYOUT)
09/29/03	ADD L7, L8	
10/16/03	DEL C182 Change DA3(LED) SMD--->DIP	V1.0+
10/24/03	Change U106 NC7SZ08P5X(AND Gate) -->NC7SZ86P5X(XOR Gate)	
10/30/03	L30 DNE	
11/10/03	C20, C21 P CASE--->B CASE	
11/13/03	change value C329, C330	

Note(I):

1. All resistors are 5% 0402 unless specified.
2. All chip capacitors are +/- 20% 0402 unless specified.
3. All chip inductors are 0402 unless specified.
3. All capacitors with polarity are SMD unless specified
4. "DNE" means "Do Not Equip"

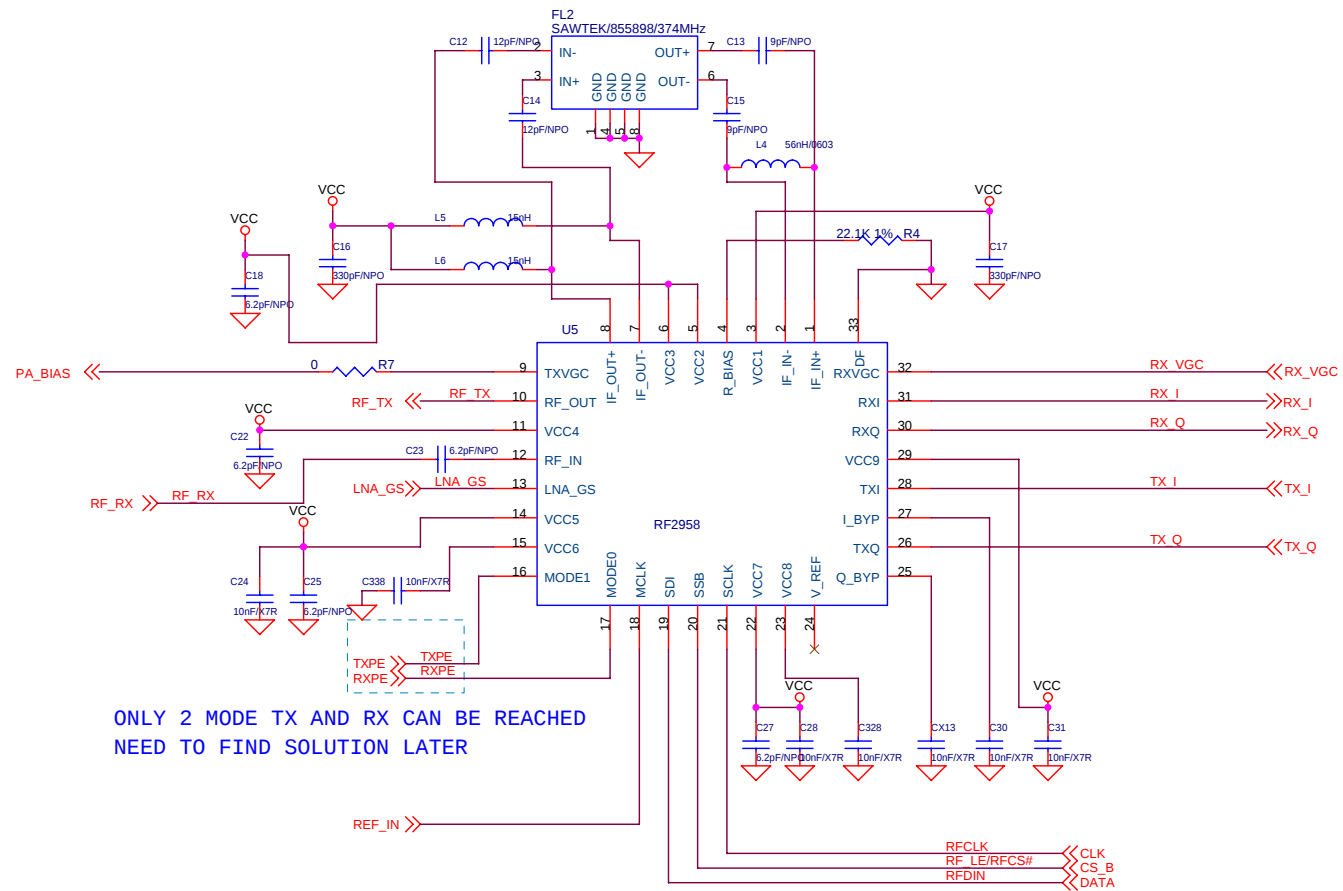
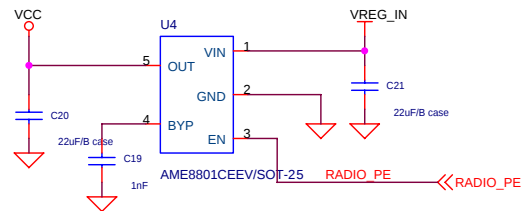
Note (II):

1. EEPROM should be programmed before loaded
2. Resistor arrays should be arranged for layout convinience.
3. Compnents loaded when assembling will follow BOM.

This reference design board is used to evaluate and demo the function of WP1200 Controller. Depending on customers' application, some components are optional. The information of this document is provide AS IS and WavePlus makes no representations or warranties whatsoever, whether express or implied, for the accuracy of the information provided herein. In no event shall WavePlus be liable for any consequences arising from the use of this information nor for any infringement of patents or other intellectual property rights of third parties which may result from the use. No license is granted by implication or otherwise under any intellectual property rights of WavePlus. All rights reserved. No part of this document may be reproduced in any form without the written permission of the copyright holder. The information in this document is subject to change without notice.

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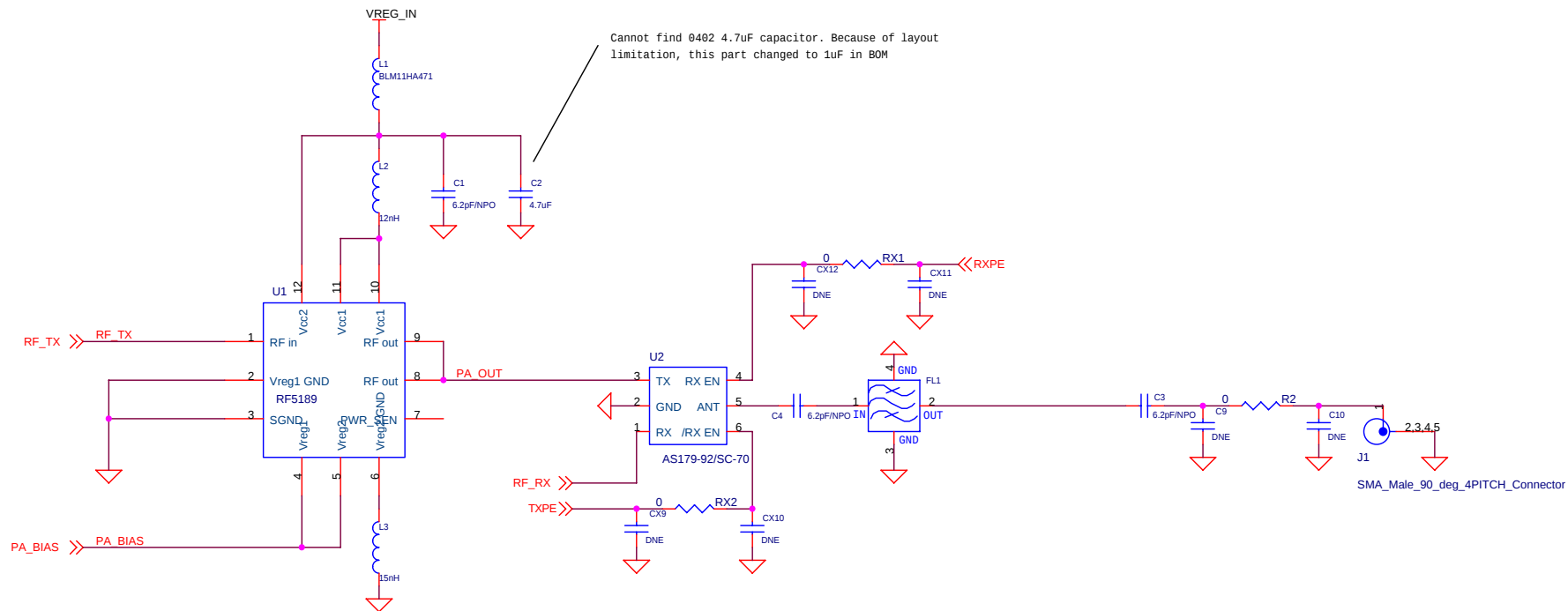
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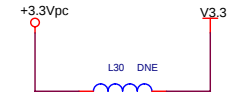
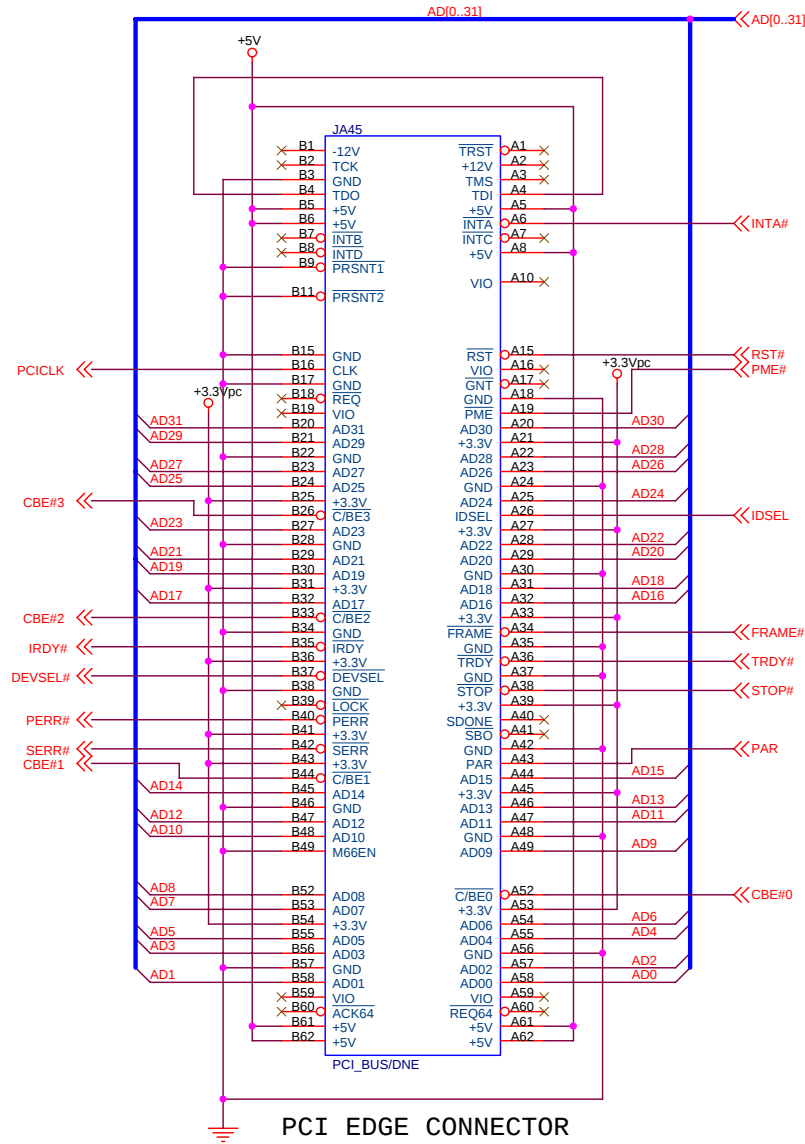
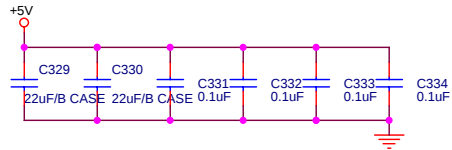
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		WP1200 PCI low profile Card RF5189	
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Clock trace
should be 2.5"
long



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