Confidential

# Operational Description

**SAILOR 6282 AIS Transponder** is a Class A AIS which normally is connected to the Display/Keyboard unit **SAILOR 6004 Control Panel** or an ECDIS to handle target list, settings etc.

**General Receiver principle.**
The receiver is a software defined radio. The antenna signal is routed to an ADC. The ADC sample clock is 122.880MHz. The ADC sample data is transferred to a FPGA. The FPGA have 3 parallel receive processes; 2 AIS channels and 1 DSC channel (156.525MHz).

All receivers are built in FPGA, the operating principle are the same. The difference is the receive frequency.

The FPGA down converts all 3 RF channels to zero frequency. The resulting 6 - I/Q Channels are further processed in a DSP.

List of IF frequencies:

| RX Freq. Mhz | 156.025Mhz | 156.525Mhz | 162.025Mhz |
|---|---|---|---|
| IF=Rx-122.88Mhz | 33.145Mhz | 33.645Mhz | 39.145Mhz |

**Switching Range:** The range is determined by the two SAW RF input filters.

The pass band is 156.025Mhz – 162.025Mhz and the stop band is 159Mhz +30Mhz -15Mhz.

The nominal IF frequency resulting from the subsampling of the input frequency is shown in the table above.

The normal sensitivity is -110dBm

**AIS Transmitter Exciter**
The exciter generates the TX signal by mixing a 100MHz VCXO with a LO from a PLL controlled VCO.

f(TX) = f(VCO) – f(VCXO)

The VCO covers the frequency range 256.025MHz to 262.025MHz in 25 kHz steps.
The VCXO is modulated by the baseband information generated by a DAC controlled by the DSP.

The antenna shift function is made by PIN diodes.

The final RF amplifying stage consists of a Power Amplifier module which is supplied with 8.5 VDC and delivers the 12.5 W RF output power to the antenna.
The output power is stabilized by a power regulator circuit which controls the PA.
The output power can be reduced to 1W

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