PMB 8753

BlueMoon UniCellular

BlueMoon Universal Platform

Never stop thinking.

Edition 2006-08-18

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany

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Revision History:	**2006-08-18**	T8753-XV10T10-7600
Previous Version:	2005-11-18	T8753-XV10T9-7600

Section	Subjects (major changes since last revision)
1	Added TST0-TST3 to pin list
2	Updated text in startup section. Added new section about reset behavior.
3	Added new section about GPIO and Logic Gate Interface. Removed TBD from WLAN coex section.
6	Non-manufacturer mode commands are not supported in manufacturer mode. Updated default values for BD_DATA parameters to comply with recommendations. Updated descriptions of BD_DATA parameters Osc_Settle and ULPM_Threshold. Updated description of Infineon_Enable_PCM_Loopback. Added BlueMoon Embedded to Infineon_Read_Version. Added HCI commands: - Infineon_Burst_Composer_Config - Infineon_Auto_Calibrate_Crystal - Infineon_Raw_Write_Ext_EEPROM - Infineon_Raw_Read_Ext_EEPROM
7	Added information about CLK32 pin resistance and capacitance. Corrected information about CLK32 pad supply. Updated ULPM current consumption with internal VDDPM regulator. Corrected throughput figures in Table 7-3. Updated spurious emission figures. Updated “output power fine steps” min. value. Updated “Max. tolerated ripple” figures for VDDSUP. Updated recommended crystal parameters.
8.1.2	Updated standoff and ball diameter
9	VCOCAP changed from 1.5nF to 1.0nF

Table of Contents

1 General Device Overview

1.1 Features

General

- True single chip Bluetooth 1.2, 2.0 and 2.0 + EDR solution
- Ultra low power design in 0.13 µm CMOS
- Temperature range from -40°C to 85°C
- Integrates ARM7TDMI, RAM and patchable ROM
- On-chip voltage regulators. External supply 1.8-3.6 V
- Reference clock from internal crystal oscillator or external 10-40 MHz clock
- Low power clock from internal oscillator or external low power clock (e.g. 32.768 kHz)
- Dynamic low power mode switching with request signal for clock and power supply

Interfaces

- 3.25 MBaud UART with transport layer detection (HCI UART, HCI Three-Wire UART)
- Two-channel PCM/I2S interface for digital audio
- WLAN coexistence interface
- I2C interface for optional external EEPROM (for device configuration data)
- External PA interface for 20 dBm class 1 operation.
- General purpose I/Os with interrupt capabilities. JTAG for boundary scan and debug
- Separate voltage domains for UART and PCM interfaces

RF

- Transmit power programmable from -45 dBm to 6 dBm
- Receiver sensitivity typ. -90 dBm at 2Mbit/s (DQPSK)
- Integrated antenna switch
- Integrated LNA with excellent blocking and intermodulation performance
- Low-IF receiver topology to eliminate external IF filters
- Digital demodulation for optimum sensitivity and co-/adjacent channel performance

Bluetooth

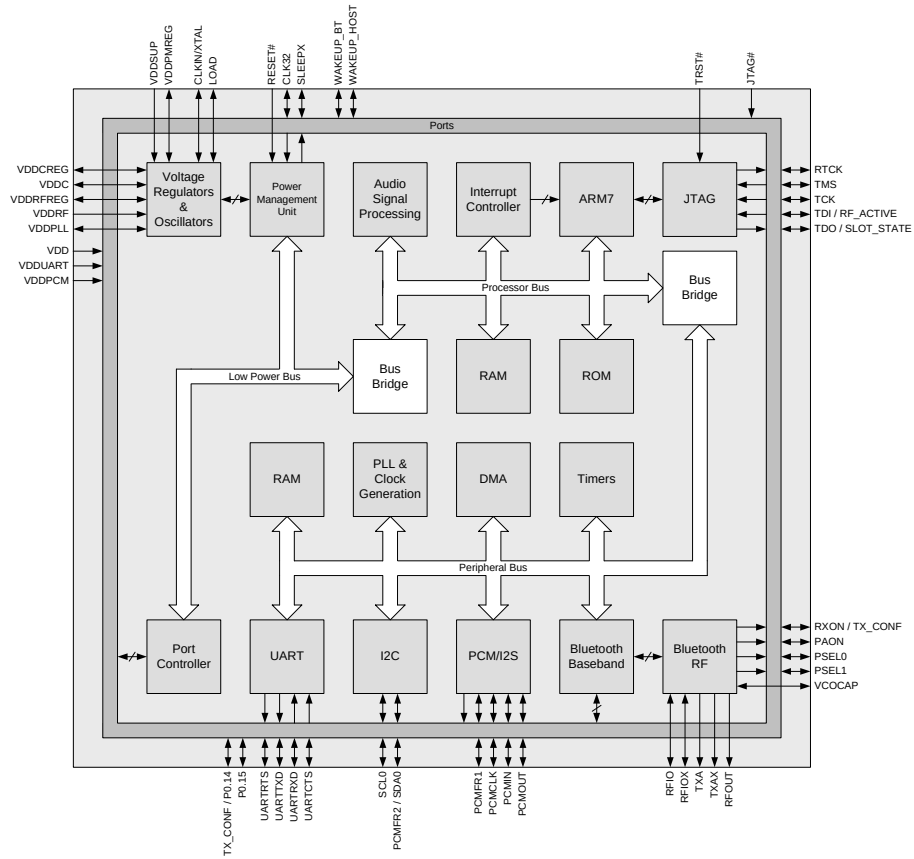
- Piconet with seven slaves. Scatternet with two slave roles while still being visible
- Two simultaneous SCO/eSCO links with hardware accelerated audio signal processing
- Audio error correction algorithm (PLC) improving speech quality
- Power control and RSSI. Hold, Park and Sniff.
- Adaptive Frequency Hopping, Quality of Service, Channel Quality Driven Data Rate
- Bluetooth security features: Authentication, Pairing and Encryption
- Bluetooth test mode and Infineon's active Bluetooth tester mode

Type	Package
PMB 8753	PG-WFSGA-65-1
PMB 8753	PG-VQFN-48-4 (for firmware evaluation)

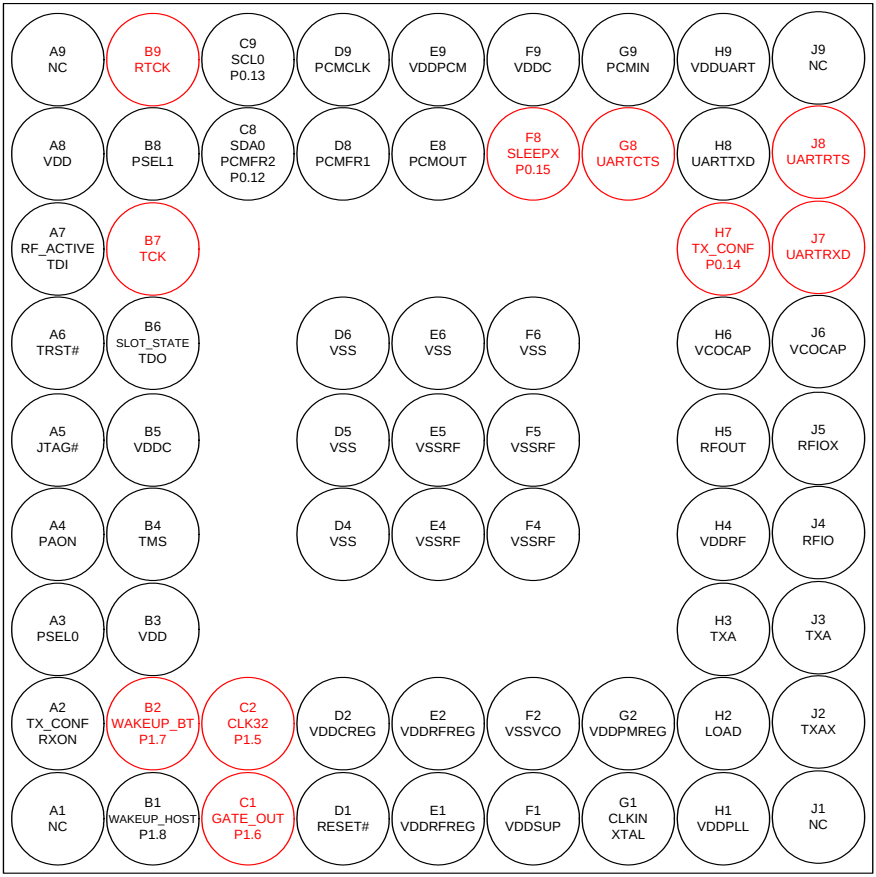
1.2 Product Variants

BlueMoon UniCellular is available in different variants and versions. Please check the corresponding errata and delta documents for the latest information.

1.3 Functional Block Diagram

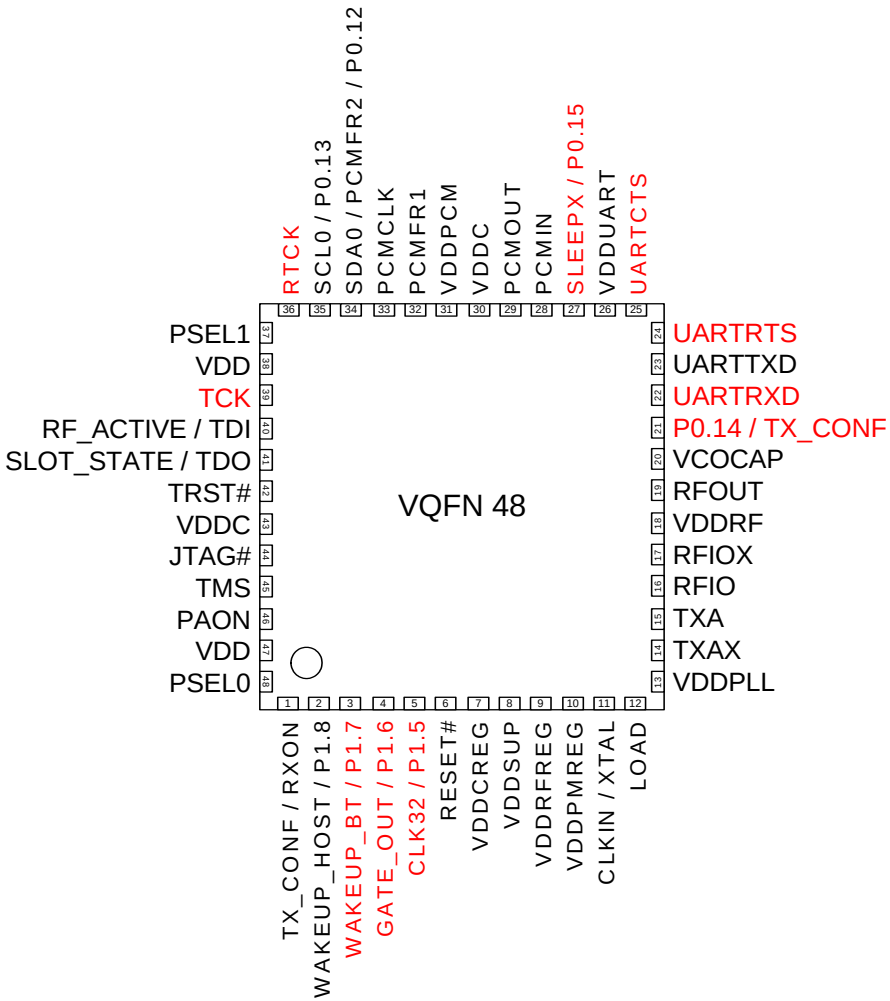


1.4 Pin Configuration PG-WFSGA-65-1



Red pins support wakeup functionality.

1.5 Pin Configuration PG-VQFN-48-4 (Firmware Evaluation Package)



Red pins support wakeup functionality.

1.6 Pin Description

Pin No. PG-VQFN-48-4/ PG-WFSGA-65-1	Symbol	Pin Type	Supply Voltage	During Reset	Function
32 / D8	P0.0/ PCMFR1	DIO-UD	VDDPCM	PD	Port 0.0 or PCM frame signal 1
33 / D9	P0.1/ PCMCLK	DIO-UD	VDDPCM	PD	Port 0.1 or PCM clock
28 / G9	P0.2/ PCMIN	DIO-UD	VDDPCM	Z	Port 0.2 or PCM data in
29 / E8	P0.3/ PCMOUT	DIO-UD	VDDPCM	Conf. PD def.	Port 0.3 or PCM data out
23 / H8	P0.4/ UARTTXD	DIO-UD	VDDUART	PU	Port 0.4 or UART transmit data
22 / J7	P0.5/ UARTRXD	DIO-UD	VDDUART	Z	Port 0.5 or UART receive data
24 / J8	P0.6/ UARTRTS	DIO-UD	VDDUART	PU	Port 0.6 or UART RTS flow control
25 / G8	P0.7/ UARTCTS	DIO-UD	VDDUART	Z	Port 0.7 or UART CTS flow control
46 / A4	P0.8/ PAON/ TST0	DIO-UD	VDD	PD	Port 0.8 or External PA control or Test output
48 / A3	P0.9/ PSEL0	DIO-UD	VDD	Z	Port 0.9 or External PA control
37 / B8	P0.10/ PSEL1/ TST1	DIO-UD	VDD	Z	Port 0.10 or External PA control or Test output
1 / A2	P0.11/ RXON/ TX_CONF/ TST2	DIO-UD	VDD	Z	Port 0.11or External PA control or WLAN coexistence interface or Test output
34 / C8	P0.12/ PCMFR2/ SDA0	DIO-U	VDD	PU	Port 0.12 or PCM frame signal 2 or I2C data signal
35 / C9	P0.13/ SCL0	DIO-U	VDD	PU	Port 0.13 or I2C clock signal
21 / H7	P0.14/ TX_CONF	DIO-UD	VDDUART	Z	Port 0.14 or WLAN coexistence interface
27 / F8	P0.15/ SLEEPX/ TST3	DIO-UD	VDDUART	PD	Port 0.15 or CLKIN & VDDSUP request or Test output
45 / B4	P1.0/ TMS	DIO-UD	VDD	PU[1)]	Port 1.0 or JTAG interface
39 / B7	P1.1/ TCK	DIO-UD	VDD	PU[1)]	Port 1.1 or JTAG interface

Pin No. PG-VQFN-48-4/ PG-WFSGA-65-1	Symbol	Pin Type	Supply Voltage	During Reset	Function
40 / A7	P1.2/ TDI/ RF_ACTIVE	DIO-UD	VDD	PU[1)]	Port 1.2 or JTAG interface or WLAN coexistence interface
41 / B6	P1.3/ TDO/ SLOT_STATE	DIO-UD	VDD	Z	Port 1.3 or JTAG interface or WLAN coexistence interface
36 / B9	P1.4/ RTCK	DIO-UD	VDD	Z	Port 1.4 or JTAG interface
5 / C2	P1.5/ CLK32	DIO-UD	VDDPM	Input	Port 1.5 or LPM clock input (e.g. 32.768kHz)
4 / C1	P1.6/ GATE_OUT	DIO-UD	VDDPM	Z	Port 1.6 or Logic gate output
3 / B2	P1.7/ WAKEUP_BT	DIO-UD	VDDPM	PD/ Input	Port 1.7 or Bluetooth wake-up signal
2 / B1	P1.8/ WAKEUP_HOST	DIO-UD	VDD	PD	Port 1.8 or Host wake-up signal
42 / A6	TRST#	DI	VDD	PD	JTAG interface
44 / A5	JTAG#	DI	VDD	PU	Mode selection Port 1: 0: JTAG 1: Port
6 / D1	RESET#	AI	VDDPM	Input	Hardware Reset
13 / H1	VDDPLL	SO	VDDPLL	-	PLL digital supply (generated internally)
20 / H6, J6	VCOCAP	AIO	VDDRF	inactive	VCO decoupling capacitor connection
16 / J4	RFIO	AIO	VDDRF	inactive	LNA input, driver output
17 / J5	RFIOX	AIO	VDDRF	inactive	LNA input inverted, driver output inverted
15 / H3, J3	TXA	AO	VDDRF	inactive	RF class 1 PA driver output
14 / J2	TXAX	AO	VDDRF	inactive	RF class 1 PA driver output (inv)
19 / H5	RFOUT	AIO	VDDRF	inactive	test pin for analog signals
12 / H2	LOAD	A	VDDPM		With external main clock: has to be connected to ground
11 / G1	CLKIN / XTAL	A	VDDPM	active	Main clock input
9 / E1, E2	VDDRFREG	SO			RF supply regulator output
18 / H4	VDDRF	SI			RF supply voltage
47 / B3	VDD	SI			Supply voltage I/Os
38 / A8	VDD	SI			Supply voltage I/Os
26 / H9	VDDUART	SI			Supply voltage UART interface pads
31 / E9	VDDPCM	SI			Supply voltage PCM interface pads
43 / B5	VDDC	SI			Digital core supply pad

Pin No. PG-VQFN-48-4/ PG-WFSGA-65-1	Symbol	Pin Type	Supply Voltage	During Reset	Function
30 / F9	VDDC	SI			Digital core supply pad
7 / D2	VDDCREG	SO			Digital core supply regulator output
8 / F1	VDDSUP	SI			Regulator supply input (VDDPM, VDDRF, VDDC)
10 / G2	VDDPMREG	SIO			Power Management supply Output on PMB8753 A Input on PMB8753 J
- / D4, D5, D6, E6, F6	VSS				Digital Ground
- / E4, E5, F4, F5	VSSRF				RF Ground
- / F2	VSSVCO				VCO Ground

[1] Fixed pull-up/pull-down if JTAG interface is selected, not affected by any chip reset. If JTAG interface is not selected the port is tristate.

Descriptions of acronyms used in the pin list:

Acronym	Description
I	Input
O	Output
DI	Digital input
DIO-UD	Digital input/output with support for open drain, pull-up and pull-down
DIO-U	Digital input/output with support for open drain and pull-up
Z	Tristate
PU	Pull-up
PD	Pull-down
A	Analog (e.g. AI means analog input)
S	Supply (e.g. SO means supply output)

1.7 System Integration

BlueMoon UniCellular is optimized for cellular phone applications. It has all the required interfaces and is designed to have a low bill of material (BOM) and a small PCB size. **Figure 1-1** shows a typical application example.

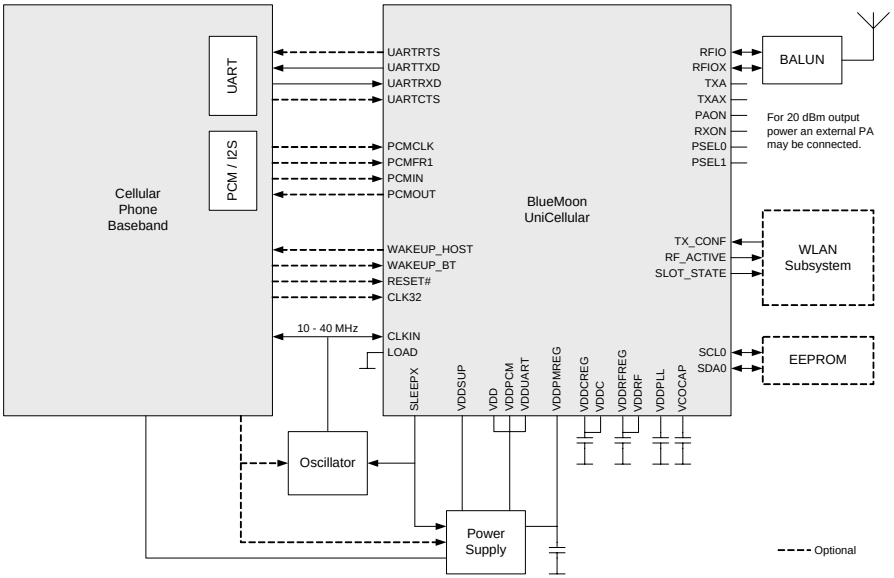


Figure 1-1 Example Cellular Phone Bluetooth System

The UART interface is used for Bluetooth HCI communication between the cellular baseband and BlueMoon UniCellular. When the HCI UART transport layer is used, four interface lines are needed: two for data (UARTTXD and UARTRXD) and two for hardware flow control (UARTRTS and UARTCTS). When the HCI Three-Wire UART transport layer is used the hardware flow control lines are optional. The UART interface has its own supply voltage (VDDUART) to ensure compatibility with the I/O voltages used by the cellular baseband. In addition to the standard Bluetooth HCI commands, BlueMoon UniCellular supports a set of Infineon specific commands called HCI+.

Digital audio can either be sent over the HCI interface or over the dedicated PCM/I2S interface. The PCM/I2S interface is highly configurable and handles up to two audio channels. The interface has a separate supply voltage (VDDPCM).

Low power mode control of BlueMoon UniCellular and the cellular baseband can be implemented in different ways, either using the dedicated WAKEUP_HOST and WAKEUP_BT signals or using signaling over the HCI interface. The host can reset

BlueMoon UniCellular via the RESET# signal or by grounding VDDPMREG and VDDSUP. Both methods will force BlueMoon UniCellular to enter its lowest power mode.

In a cellular system, BlueMoon UniCellular can make use of available oscillators and power supplies. A low power clock can be connected to CLK32 or generated internally by a low power oscillator. A 10 - 40 MHz reference clock can be connected to CLKIN or generated by the internal crystal oscillator with a crystal connected to CLKIN and LOAD. Power can be individually supplied to the different voltage domains or supplied to the single VDDSUP input from which internal regulators can generate all required voltages.

The SLEEPX signal indicates when CLKIN and VDDSUP are needed by BlueMoon UniCellular. This can be used to switch off the external oscillator and regulators when they are not needed. SLEEPX can be configured in several ways to coexist with the cellular baseband's clock and power request signals.

An optional EEPROM for storage of Bluetooth device data (BD_DATA) can be connected to the I2C interface. In a cellular system the device data is normally downloaded from the cellular baseband during startup and the EEPROM is not needed.

If a WLAN subsystem is collocated with BlueMoon UniCellular the WLAN coexistence interface should be used to enhance Bluetooth and WLAN performance. To coexist with external WLAN devices BlueMoon UniCellular supports adaptive frequency hopping.

The RF interface delivers enough output power for most use cases. If 20 dBm (maximum class 1 output power) is required, an external power amplifier can be connected.

2 Basic Operating Information

2.1 Power Supply

Figure 2-1 provides an overview of the power supply concept in BlueMoon UniCellular.

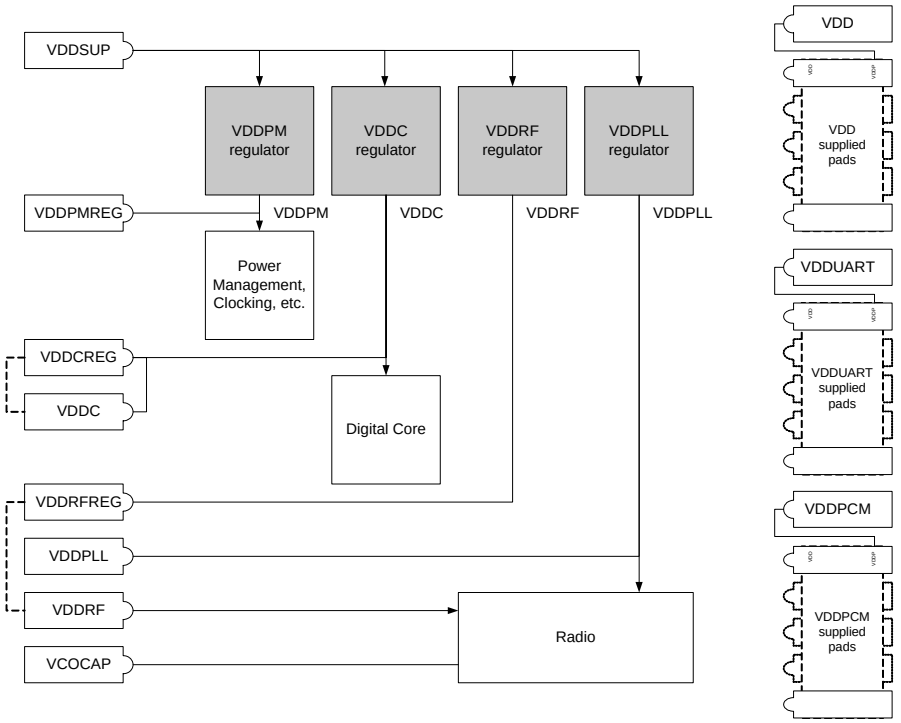


Figure 2-1 Power Supply Overview

VDDSUP is the main power supply for the device; it is possible to derive all other internal power supplies from this supply. Where a suitable external regulator exists, the VDDPM and/or the VDDRF supplies can be fed externally and the associated regulator disabled.

The low power supply VDDPM must always be present, which means that VDDSUP must always be supplied unless VDDPM is supplied externally. When VDDPM is supplied externally, the SLEEPX signal can be used to signal when the external VDDSUP supply can be switched off, and when it must be supplied. VDDPM must be supplied before or at the same time as any other supplies are applied. After VDDPM and

the I/O voltages (VDD, VDDUART and VDDPCM) has been supplied, VDDPM may be grounded and reapplied any number of times while the I/O voltages are present.

The main digital logic power supply, VDDC, is only present when in active mode. VDDC is derived from VDDSUP by the integrated VDDC regulator.

VDDRF is the main supply for the RF blocks in BlueMoon UniCellular. This is either generated from VDDSUP via the internal VDDRF regulator, or is supplied externally. The VDDRF regulator, when enabled, is switched on and off via internal control signals and is only on when required. VDDPLL, that is generated from VDDSUP by the VDDPLL regulator, supplies the digital parts of the PLL.

The regulator outputs should be decoupled externally. The outputs from VDDCREG and VDDRFREG should be connected to the other supply pads in the respective voltage domain (VDDC and VDDRF).

The PCM interface and the UART interface are supplied with dedicated, independent, reference levels via the VDDPCM and VDDUART pins. All other digital I/O pins are supplied by VDD. **Section 1.6** provides a mapping between pins and supply voltages.

The I/O power domains (VDDPCM, VDDUART and VDD) are completely separated from the other power domains and can stay present also in low power mode when VDDSUP, VDDC, VDDRF and VDDPLL are switched off.

2.2 Clocking

BlueMoon UniCellular requires two clocks: a reference clock and a low power clock. The reference clock is only needed when BlueMoon UniCellular is active (indicated by the SLEEPX signal) and is then used to generate clocks for main blocks like the CPU, the memories and the radio. The low power clock must always be present to keep the low power timers running and is also needed during startup. A part of the internal clock distribution is shown in **Figure 2-2**.

2.2.1 Reference Clock

The reference clock can either be generated by the built-in crystal oscillator or provided externally. When an external clock is used, the crystal oscillator may be switched off (by-passed) to save power. The Synthesizer Reference Input (SYRI) Divider is programmable to divide by 1 or 2 to create a suitable reference frequency for the PLLs. The configurations are done with the BD_DATA parameters *Clk_Conf* and *Input_Freq*.

If the crystal oscillator is used, a calibration value should be written to the BD_DATA parameter *Osc_Trim*. This value controls a built-in capacitance array with which it is possible to achieve a frequency accuracy of ±2 ppm.

Figure 2-3 shows how to connect a crystal or an external clock.

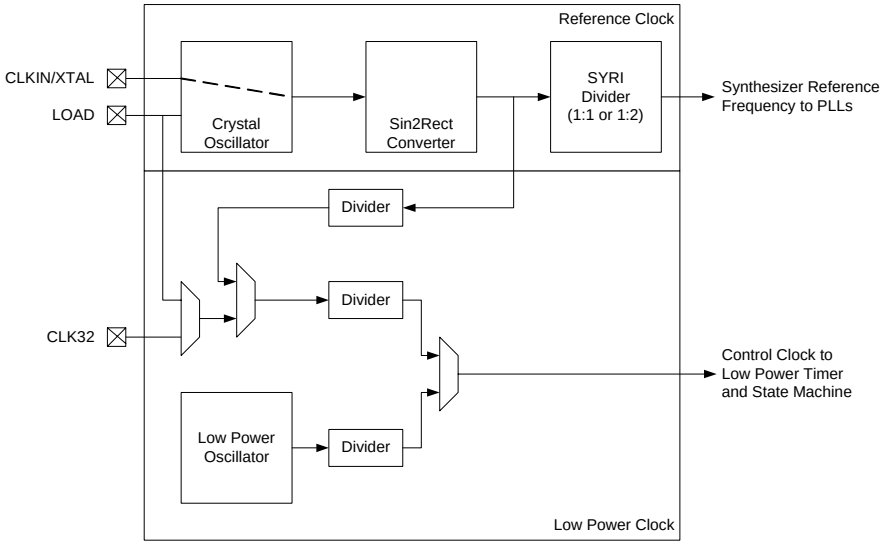


Figure 2-2 Internal Clock Distribution

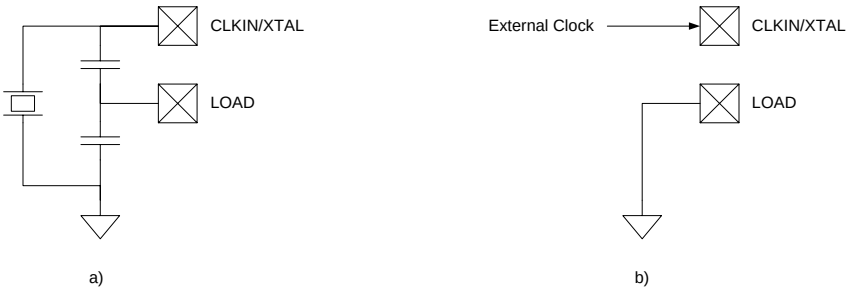


Figure 2-3 Connection of Crystal (a) or External Clock (b)

2.2.2 Low Power Clock

The low power clock can be generated internally by the crystal oscillator and/or the low power oscillator or provided externally. The clock path is selected with two bits in the BD_DATA parameter *Clk_Conf*. The following selections are possible:

External Clock at CLK32 (Figure 2-4)

This setting should be used when an external low power clock is available. The internal low power oscillator will be disabled to save power.

Internal Low Power Oscillator (Figure 2-5)

The internal low power oscillator is used to generate the low power clock. This setting could be used when no external clock is available.

Reference Clock and Low Power Oscillator (Figure 2-6)

This setting makes use of the reference clock when it is available and the low power oscillator otherwise. This gives a very accurate low power clock when the reference clock is available.

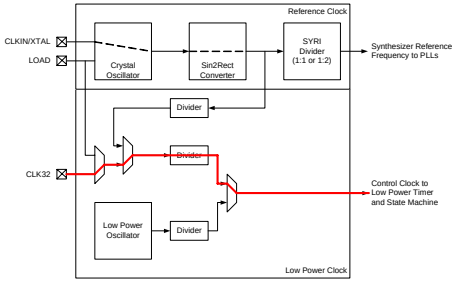


Figure 2-4 Low Power Clock Selection: External Clock at CLK32

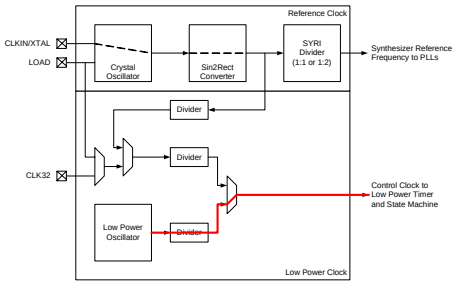


Figure 2-5 Low Power Clock Selection: Internal Low Power Oscillator

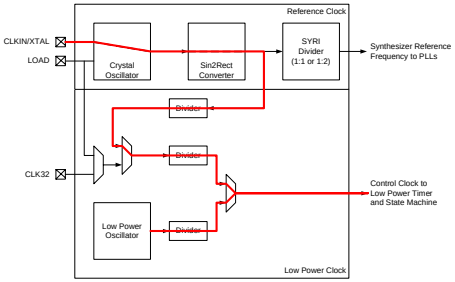


Figure 2-6 Low Power Clock Selection: Ref. Clock & Low Power Oscillator

2.2.3 Multiple Clock Detection

BlueMoon UniCellular can automatically detect the frequencies of external clocks for a number of scenarios. **Table 2-1** shows the combinations of CLKIN and CLK32 for which automatic detection is possible.

Table 2-1 Auto-detectable combinations of CLKIN and CLK32

CLKIN (MHz)	CLK32 (kHz)
12	32.768
13	32.768
14.4	32.768
16	32.768
19.2	32.768
26	32.768
26	96

If one of the scenarios in **Table 2-1** has been identified at startup, the UART baudrate is set to the default value 115.2 kBaud. If none of the scenarios has been identified, BlueMoon UniCellular uses the default value of the BD_DATA parameter *Input_Freq* and configures the baudrate to be 115.2 kBaud for a reference clock with that frequency. Multiple Clock Detection can be enabled/disabled with a bit in the parameter *Clk_Conf*.

2.3 Startup

Figure 2-7 shows a typical startup sequence with external VDDPM and CLK32.

All starts at time t_0 when the host switches on VDDPM and the low power clock (CLK32). Inside BlueMoon UniCellular, the availability of VDDPM will cause the low power

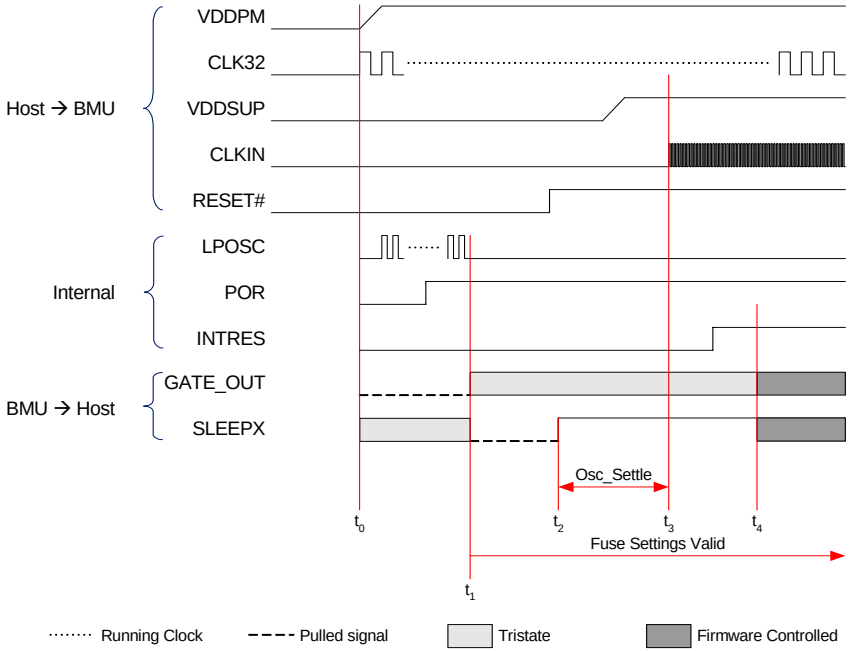


Figure 2-7 Typical Startup Sequence

oscillator (LPOSC) and the low power bandgap voltage reference to start. (If VDDSUP is available, the VDDPM regulator will also start.) When VDDPM and LPOSC are stable the internal power-on reset (POR) rises. This starts the power management state machine and initiates a read of BlueMoon UniCellular's configuration fuses.

At time t_1, the fuses have been read. Depending on their state the startup procedure will continue in different ways. In the example in **Figure 2-7** the fuses cause the internal VDDPM regulator, the low power bandgap and the low power oscillator to be switched off. Detailed information is available in **Section 2.3.1**.

At time t_1, the fuses have been read. Depending on their values, different things may happen. The internal VDDPM regulator, low power bandgap and low power oscillator may be switched off. (LPOSC is switched off in the figure.) The SLEEPX pad can be configured with different pulls and drivers. The RESET# pad can be configured with or without pull-up. The value of SLEEPX during reset may also be configured. Detailed information about the fuses is available in **Section 2.3.1**

The external reset signal (RESET#) is asynchronous. As long as RESET# is low, BlueMoon UniCellular is in its lowest power mode. When RESET# and POR are both

high and a low power clock is available (LPOSC or CLK32), the power management state machine sets SLEEPX high (at time t_2) to request the main power supply (VDDSUP) and the reference clock (CLKIN). The state machine then waits a time (Osc_Settle) for the external supply and clock to stabilize. When that is done, the internal reset (INTRES) to the rest of the chip rises and the firmware starts.

Note that RESET# may be tied high during startup. POR assures correct initialization.

Variations of the above startup sequence are possible. VDDPM and the low power clock may for example be generated internally in which case the host must supply VDDSUP to start the chip. If the host has the capability to switch off and ground VDDSUP and VDDPM, this can be used instead of external reset. RESET# can then be tied high.

When VDDSUP and VDDPM are grounded the outputs will be tristated. The I/O voltages VDD, VDDPCM and VDDUART may still be supplied.

2.3.1 Fuses

As mentioned in the previous section, BlueMoon UniCellular contains configuration fuses that define the behavior during and after reset. These fuses are programmed during chip production and cannot be changed later.

BlueMoon UniCellular is currently offered in two versions with different fuse settings. The behavior of each version is described in **Table 2-2**.

Table 2-2 Versions with Different Fuse Settings

Version	Description	Remark
PMB8753 A	Internal VDDPM regulator, low power oscillator and low power bandgap are enabled.	Can be disabled by firmware depending on BD_DATA settings. Note that the fuse setting still affects the behavior while RESET# is low.
PMB8753 J	Internal VDDPM regulator, low power oscillator and low power bandgap are disabled.	VDDPM must be supplied externally. An external low power clock must be connected to CLK32.

2.4 Reset

There are differerent ways to reset BlueMoon UniCellular with slightly different behavior. **Table 2-3** shows what happens to BD_DATA and patches for different types of reset.

Table 2-3 Different types of reset

	BD_DATA	Patches
Power-on reset	Set to default values	Disabled
External reset (RESET#)	Set to default values if *Save_RAM_BD_Data* = 0. Kept if *Save_RAM_BD_Data* = 1.	Disabled
HCI Reset	Kept	Kept
Leaving manufacturer mode with Reset = 0x01	Kept	Disabled
Leaving manufacturer mode with Reset = 0x02	Kept	Enabled

2.5 Low Power Modes

To minimize current consumption, BlueMoon UniCellular automatically switches between different low power modes. The major modes are described below.

2.5.1 Clock Disabling Mode

As soon as a part of BlueMoon UniCellular is inactive, the clocks to that part are disabled. This can be done very quickly and is done without host intervention.

2.5.2 Low Power Mode

In Low Power Mode (LPM) most parts of BlueMoon UniCellular are powered down. The reference clock is still running. Entering and leaving LPM cannot be done as quickly as disabling/enabling clocks since internal state must be saved and restored, but the power consumption is lower in LPM. The minimum time of inactivity that is required to enter LPM is configured with the BD_DATA parameter *LPM_Threshold*.

When BlueMoon UniCellular is in LPM, HCI communication is not possible; therefore it is necessary for the host to control when LPM is allowed. The control is done via the HCI transport layer. In addition to this dynamic control, low power modes must be globally enabled. This is usually done with the HCI+ command HCI_Infineon_Enable_LPM. The value *Default_LPM_Mode* in BD_DATA parameter *LPM_Conf* controls if low power modes are enabled or disabled after reset. The value *AutoDisable_LPM* in the same parameter controls if low power modes should be disabled after host initiated wakeup.

2.5.3 Ultra Low Power Mode

Ultra Low Power Mode (ULPM) is similar to LPM with the addition that the reference clock may be switched off. If VDDPM is externally supplied, the main supply voltage VDDSUP may also be switched off. Bluetooth state is updated using the low power clock. Leaving ULPM takes longer time than leaving LPM because the reference clock must be started. The minimum time of inactivity that is required to enter ULPM is configured with the BD_DATA parameter *ULPM_Threshold*. The accuracy of the low power clock is specified with the parameter *LPM_Drift*.

The signal SLEEPX is used to indicate when BlueMoon UniCellular enters ULPM. **Figure 2-8** shows an example with the default polarity of SLEEPX. When SLEEPX goes low the system is allowed to switch off VDDSUP and CLKIN. When BlueMoon UniCellular wants to leave ULPM it sets SLEEPX high again to request VDDSUP and CLKIN. The internal low power state machine waits for a time *Osc_Settle* for the power supply and clock to stabilize before starting the rest of the system. The parameter *Osc_Settle* is configurable in BD_DATA.

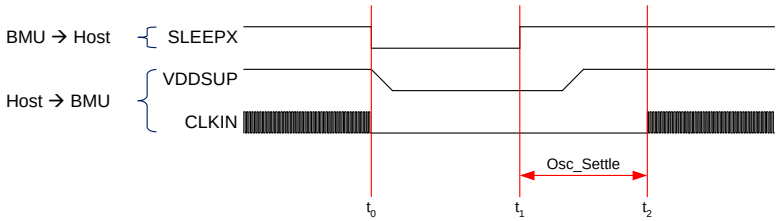


Figure 2-8 SLEEPX indicating Ultra Low Power Mode

ULPM is controlled and enabled in the same way as LPM.

2.5.4 Complete Power Down

If Bluetooth functionality is not needed at all, VDDSUP and VDDPM should be grounded to minimize power consumption. In this state there is no activity in BlueMoon UniCellular and the Bluetooth state (native clock, etc.) is not updated.

2.6 SLEEPX Configurations

The SLEEPX signal can be configured in different ways to fit the host system's clock and power supply requests. The behavior after firmware startup can be configured with HCI+ commands and BD_DATA parameters. The polarity of SLEEPX can be selected with a bit in the BD_DATA parameter *BB_Conf*. Some typical system configurations are shown below.

Separate Power Supply and Clock Request Signals

The simplest case is when BlueMoon UniCellular and the rest of the system has separate signals to request power and clocks. This is shown in **Figure 2-9**.

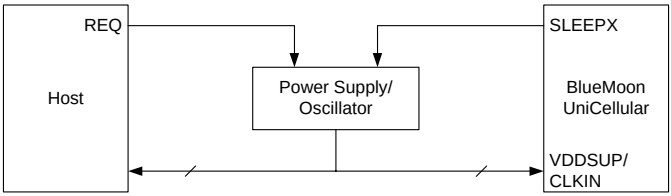


Figure 2-9 Separate Power Supply and Clock Request Signals

Shared Power Supply and Clock Request Signals

If the SLEEPX signal and the host's request signal are configured to pull in one direction and drive in the other, it is possible to wire the signals together. This is shown in **Figure 2-10**.

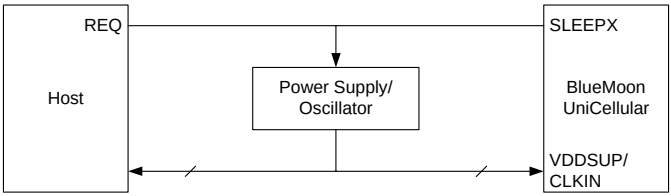


Figure 2-10 Shared Power Supply and Clock Request Signals

Gated Power Supply and Clock Request Signals

BlueMoon UniCellular contains a programmable logic gate that can be used to combine an external request signal with the internal SLEEPX signal. This configuration is shown in **Figure 2-11**.

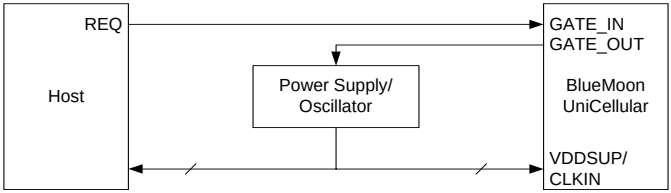


Figure 2-11 Gated Power Supply and Clock Request Signals

3 Interfaces

3.1 HCI / UART Interface

The HCI/UART interface is the main communication interface between the host and BlueMoon UniCellular. The standard HCI commands are supported together with an Infineon specific set of commands called HCI+. The HCI+ commands are described in detail in the HCI+ section.

The interface consists of four UART signals and two wake-up signals as shown in **Figure 3-1**. Depending on which HCI transport layer that is used, some or all of the signals are needed.

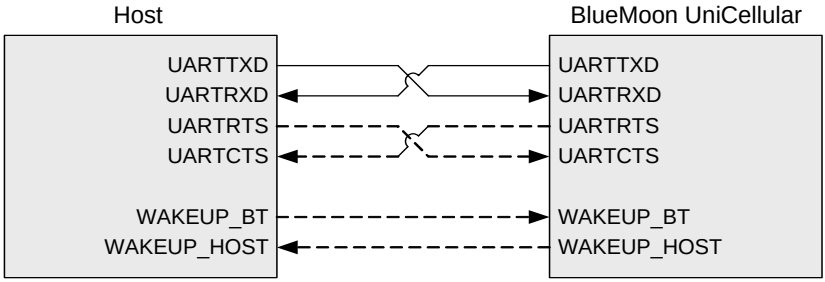


Figure 3-1 HCI/UART Interface

3.1.1 Supported Transport Layers

BlueMoon UniCellular supports the HCI Three-Wire UART transport layer and two derivatives of the HCI UART transport layer (HCI UART-4W and HCI-UART-6W) where the only difference is how low power modes are handled. BlueMoon UniCellular automatically detects which transport layer that is used by the host.

3.1.1.1 HCI Three-Wire UART

The HCI Three-Wire UART transport layer is specified by the Bluetooth SIG. It supports error detection and retransmissions and has built-in low power mode mechanisms. Hardware flow control with UARTRTS and UARTCTS is optional. The only required signals are UARTTXD and UARTRXD (the name “Three-Wire” includes the ground connection as well).

The BlueMoon UniCellular implementation has the following characteristics:

- BlueMoon UniCellular supports all features of the HCI Three-Wire UART transport layer except transmission of synchronous data packets as reliable packets.

- The time that BlueMoon UniCellular waits to receive an acknowledgement before resending a packet can be configured with the BD_DATA parameter *Three-Wire_ARQ_Timeout* (in multiples of T_{max}). The recommended value is 0x06 assuming that the host acknowledges packets within $2 \cdot T_{max}$ as recommended in the Bluetooth specification.
- T_{max} is defined as the time it takes to transfer 343 Bytes at the current Baud rate.

3.1.1.2 HCI UART-4W

This is an implementation of the HCI UART transport layer where control of low power modes has been added using BREAK signaling on the UART lines. The four UART lines (UARTTXD, UARTRXD, UARTRTS, UARTCTS) are required.

3.1.1.3 HCI UART-6W

This implementation of the HCI UART transport layer uses the two wake-up lines (WAKEUP_BT and WAKEUP_HOST) in combination with HCI+ commands and events to handle low power modes. All six HCI/UART lines are required.

3.1.2 Low Power Mode Protocols

Each HCI transport layer implements a specific low power mode protocol that can be configured in a number of ways. **Table 3-1** provides an overview of the BD_DATA parameters, the signals, and the HCI+ commands and events that are relevant for each transport layer. Detailed descriptions of the low power mode protocols are given below.

Table 3-1 Low Power Mode Configuration Overview

Name	Type	HCI UART-4W	HCI UART-6W	HCI Three-Wire UART
Host_LPM	BD_DATA	X	X	X
UART_Pulls (UARTTXD)	BD_DATA	X		
UART_Invert	BD_DATA	X	X	X
Wakup_Host	BD_DATA		X	
Wakeup_BT	BD_DATA		X	
AutoDisable_LPM	BD_DATA	X	X	X
Infineon_Enable_LPM	Command	X	X	X
Infineon_Host_LPM_Start	Command		X	
Infineon_Host_LPM_End	Command		X	
Infineon_LPM_Start	Event		X	

Table 3-1 Low Power Mode Configuration Overview

Name	Type	HCI UART-4W	HCI UART-6W	HCI Three-Wire UART
Infineon_LPM_End	Event		X	
WAKEUP_HOST	Signal		X	
WAKEUP_BT	Signal		X	
Hardware_Flow_Control	BD_DATA			X
Default_LPM_Mode	BD_DATA	X	X	X

3.1.2.1 HCI Three-Wire UART

The low power mode protocol for HCI Three-Wire UART is defined in the Bluetooth specification. Only UARTTXD and UARTRXD are required.

Configuration and Operation Details

The idle timeout (inactivity on the UART) before entering low power mode is 300 ms.

The BD_DATA parameter *UART_Pulls* has no effect when using the HCI Three-Wire UART LPM protocol. The *UART_Invert* parameter affects UARTTXD, UARTRXD (UARTRTS and UARTCTS if enabled (default) by the *Hardware_Flow_Control* bit in BD_DATA) while the controller is online[1)] and in LPM.

UARTRTS will stay asserted while the controller is in LPM. This makes it possible to send wake-up messages to the controller even if the host may consider the state of UARTRTS. UARTCTS will not be checked before a wake-up message is sent to the host from the controller. This makes it possible to wake up a host that cannot control its RTS to allow UART data while in for example “sleep mode”.

The Infineon_Host_LPM_Start and Infineon_Host_LPM_End commands are not used in the HCI Three-Wire UART LPM protocol. The commands are disallowed (results in a Command Complete event with Status = “Command Disallowed”). The events Infineon Low Power Mode Start and Infineon Low Power Mode End are not used.

The Infineon_Enable_LPM command enables the LPM feature of the controller so it is able to enter LPM. The controller will not be able to enter LPM if the Infineon_Enable_LPM command has not been sent to the controller.

The *AutoDisable_LPM* bit in BD_DATA controls if the controller shall disable the LPM feature or not after the host has woken the controller. When *AutoDisable_LPM* is enabled the controller will not enter LPM after being woken by the host until Infineon_Enable_LPM is sent and the host allows the controller to enter LPM. It is recommended to set *AutoDisable_LPM* to false when using HCI Three-Wire UART.

1) Online in this section means that the controller is active i.e not in LPM

The *Host_LPM* bit in the BD_DATA parameter *LPM_conf* affects the behavior of the signaling to the host during for example page scan. If activated there will be no signaling indicating autonomous wake-up of the controller (e.g. during page scan when LPM is allowed). If deactivated the controller will notify the host each time the controller wakes up autonomously.

3.1.2.2 HCI UART-4W

The low power mode protocol for HCI UART-4W is based on hardware signaling only. No HCI commands and events are required except Infineon_Enable_LPM.

The existing HCI UART signals (TXD, RXD, RTS and CTS) are used to tell the other device (host or controller) when it may enter low power mode, when it should wake up and when it cannot transmit because the first device is in low power mode.

Figure 3-2 shows the three basic signaling operations. To simplify the description it is assumed that the *UART_Invert* bits are zero

- To allow the other device to enter low power mode, TXD is set low long enough to generate a BREAK condition in the other device's UART receiver (long enough = longer than a complete character + stop bit).
- To request the other device to wake up, TXD is set high again. This operation is only allowed when the other device has been allowed to enter low power mode. It is not required that the other device has actually entered low power mode.
- When a device enters low power mode it has to signal "flow stop" to the other device by setting RTS high.

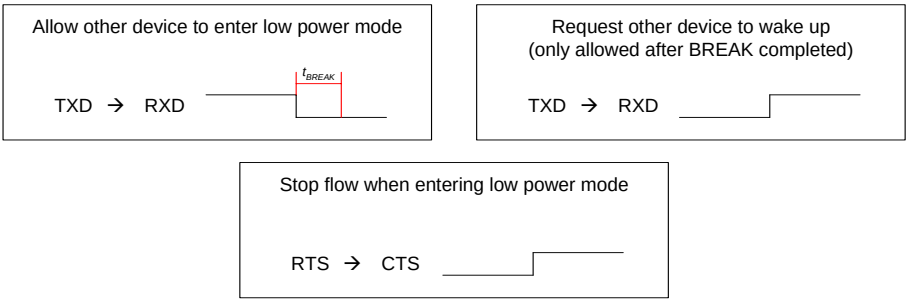


Figure 3-2 HCI UART-4W Basic Operations (*UART_Invert* = 0)

The BlueMoon UniCellular implementation of this protocol has the following behavior:

- BlueMoon UniCellular will only allow the host to enter low power mode while it is in low power mode itself.

- When requesting the host to wake up, BlueMoon UniCellular will set UARTRTS low in addition to setting UARTTXD high. This is to allow hosts that do not have interrupt capabilities on RXD to use the protocol.

Configuration and Operation Details

The BD_DATA parameter *UART_Pulls* sets the UARTTXD level while the controller is in LPM (UARTRXD, UARTRTS and UARTCTS are not affected by the *UART_Pulls* configuration). The level of UARTTXD during LPM, defined by the *UART_Pulls* parameter, is not affected by the *UART_Invert* configuration.

The *UART_Invert* parameter affects UARTTXD, UARTRXD, UARTRTS and UARTCTS while the controller is online. The *UART_Invert* parameter affects UARTRXD, UARTRTS and UARTCTS while the controller is in LPM.

The Infineon_Host_LPM_Start and Infineon_Host_LPM_End commands are not used in the HCI UART-4W transport layer. The commands are disallowed (results in a Command Complete event with Status = “Command Disallowed”). The events Infineon Low Power Mode Start and Infineon Low Power Mode End are not used by the controller.

The Infineon_Enable_LPM command enables the LPM feature of the controller so it is able to enter LPM. The controller will not be able to enter LPM if the Infineon_Enable_ LPM command has not been sent to the controller (even if the host tries to signal enter LPM to the controller via the LPM protocol).

The *AutoDisable_LPM* bit in BD_DATA controls if the controller shall disable LPM or not after it has been woken by the host. When *AutoDisable_LPM* is enabled the controller will not enter LPM after a host initiated wake-up until the Infineon_Enable_LPM command has been sent and the host allows the controller to enter LPM. It is recommended to set *AutoDisable_LPM* to false when using HCI UART-4W.

The *Host_LPM* bit in the BD_DATA parameter *LPM_conf* affects the behavior of the signaling to the host during for example page scan. If activated there will be no signaling indicating autonomous wake-up of the controller (e.g. during page scan when LPM is allowed). If deactivated the controller will notify the host each time the controller wakes up autonomously. If the *Host_LPM* bit is activated the controller assumes that the host may be asleep and will go through the wake-up procedure including checking UARTCTS before an event can be sent to the host. If deactivated the controller assumes that the host is always ready to receive an event (only UARTCTS will be checked).

Table 3-2 shows the signal levels on UARTTXD and UARTRTS in different modes for all combinations of *Host_LPM* and *UART_Pulls*. *UART_Invert* is zero in all cases.

Table 3-2 UARTTXD and UARTRTS Signal Levels

Host_LPM:	deactivated		deactivated		activated		activated	
UART_Pulls (UARTTXD):	pull-down		pull-up		pull-down		pull-up	
Mode	**UART TXD**	**UART RTS**	**UART TXD**	**UART RTS**	**UART TXD**	**UART RTS**	**UART TXD**	**UART RTS**
Online	High	Low	High	Low	High	Low	High	Low
LPM	Low	High	High	High	Low	High	High	High
Autonomous wake-up	High	Low	High	Low	Low	High	High	High

HCI UART-4W Examples

The following examples assume that the BD_DATA parameters have been set like this:

Host_LPM: 1 (activated)
UART_Pulls: 0b10 (UARTTXD pulled down during low power mode)
UART_Invert: 0 (not inverted)
AutoDisable_LPM: 0 (not activated)

Figure 3-3 shows a case where the host initiates low power mode entry and exit:

- The host allows BlueMoon UniCellular to enter low power mode (1).
- BlueMoon UniCellular enters low power mode (2) and allows the host to enter low power mode (3).
- The host may, if it can, enter low power mode.
- The host requests BlueMoon UniCellular to wake up (4).
- BlueMoon UniCellular wakes up (5).

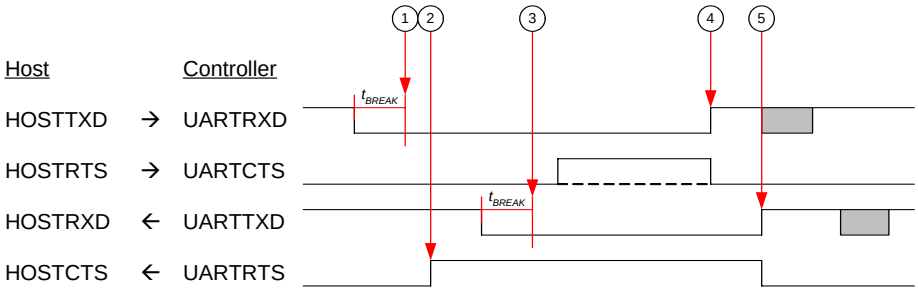


Figure 3-3 Host Initiates Low Power Mode Entry and Exit

Figure 3-4 shows a case where the controller wakes up the host:

- The host allows BlueMoon UniCellular to enter low power mode (1).
- BlueMoon UniCellular enters low power mode (2) and allows the host to enter low power mode (3).
- The host enters low power mode (4)
- BlueMoon UniCellular requests the host to wake up (5).
- The host wakes up (6).

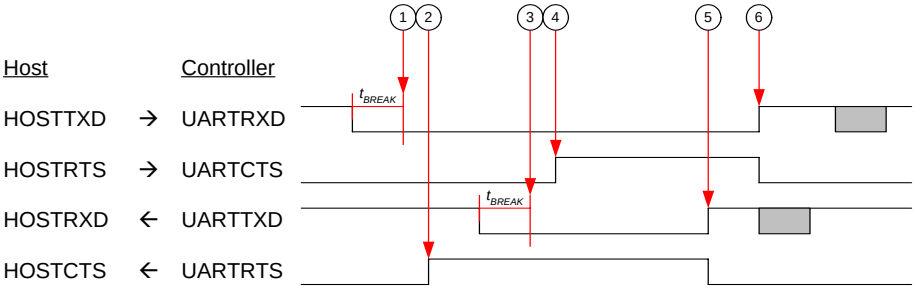


Figure 3-4 Host Initiates Low Power Mode Entry, Controller Initiates Exit

3.1.2.3 HCI UART-6W

The low power mode protocol for HCI UART-6W makes use of HCI+ commands and events as well as dedicated wake-up signals. Table 3-3 lists the commands and events that are used. Table 3-4 lists the dedicated wake-up signals.

Table 3-3 HCI+ Commands and Events used with HCI UART-6W

Name	Type	Description
Infineon_Enable_LPM	HCI+ command	Enables/disables use of low power modes
Infineon_Host_LPM_ Start	HCI+ command	Used by the host to indicate that it will enter low power mode
Infineon_Host_LPM_ End	HCI+ command	Used by the host to indicate that it has left low power mode
Infineon Low Power Mode Start Event	HCI+ event	Used by the controller to indicate that it will enter low power mode
Infineon Low Power Mode End Event	HCI+ event	Used by the controller to indicate that it has left low power mode

Table 3-4 Signals used with HCI UART-6W

Name	Type	Description
WAKEUP_BT	Signal	Signal to wake up BlueMoon UniCellular
WAKEUP_HOST	Signal	Signal to wake up the host

Configuration and Operation Details

There are several configurations that will affect the behavior of the HCI UART-6W LPM protocol. The following sections describe different configurations.

The BD_DATA parameter *UART_Pulls* has no effect when using the HCI UART-6W LPM protocol. The *UART_Invert* parameter will affect UARTTXD, UARTRXD, UARTRTS and UARTCTS while the controller is online and in LPM.

The Infineon_Host_LPM_Start and Infineon_Host_LPM_End commands are used by the host to notify the controller of which state it is about to enter. The events Infineon Low Power Mode Start and Infineon Low Power Mode End are used by the controller to notify the host of what mode the controller is about to enter.

The Infineon_Enable_LPM command enables the LPM feature of the controller so it is able to enter LPM. The controller will not be able to enter LPM if the Infineon_Enable_LPM command has not been sent to the controller.

The *AutoDisable_LPM* bit in BD_DATA controls if the controller shall disable LPM or not after it has been woken by the host. When *AutoDisable_LPM* is enabled the controller will not enter LPM after a host initiated wake-up until the Infineon_Enable_LPM command has been sent and the host allows the controller to enter LPM.

The *Host_LPM* bit in the BD_DATA parameter *LPM_conf* affects the behavior of the signaling to the host during for example page scan. If activated there will be no events indicating autonomous wake-up of the controller (e.g. during page scan when in LPM). If deactivated the controller will send an event to the host each time the controller wakes up autonomously. If *Host_LPM* is activated the controller assumes that the host may be asleep and will go through the wake-up procedure including checking UARTCTS before an event can be sent to the host. If deactivated the controller assumes that the host is always ready to receive an event (only UARTCTS will be checked).

The *Wakeup_Host* and *Wakeup_BT* bits in the BD_DATA parameter *BB_Conf* controls which level that defines active mode of the controller and the host.

Default_LPM_Mode should be set to false when using HCI UART-6W.

HCI UART-6W Examples

The basic configuration (if nothing else is mentioned) in the following examples are: *Host_LPM* bit = activated, *UART_Invert* bits = 0, *Wakeup_Host* and *Wakeup_BT* bits = 0, *AutoDisable_LPM* bit = 1.

EXAMPLE 1: The controller enters “unknown” mode

“Unknown” means that the host does not know the state of the controller. The controller will enter and leave LPM without notification, e.g. for Inquiry Scan.

- The controller informs the host before entering the “unknown” mode
- UART communication is disabled
- The controller and the host may wake up repeatedly and independently without notification, as long as no communication is needed on HCI

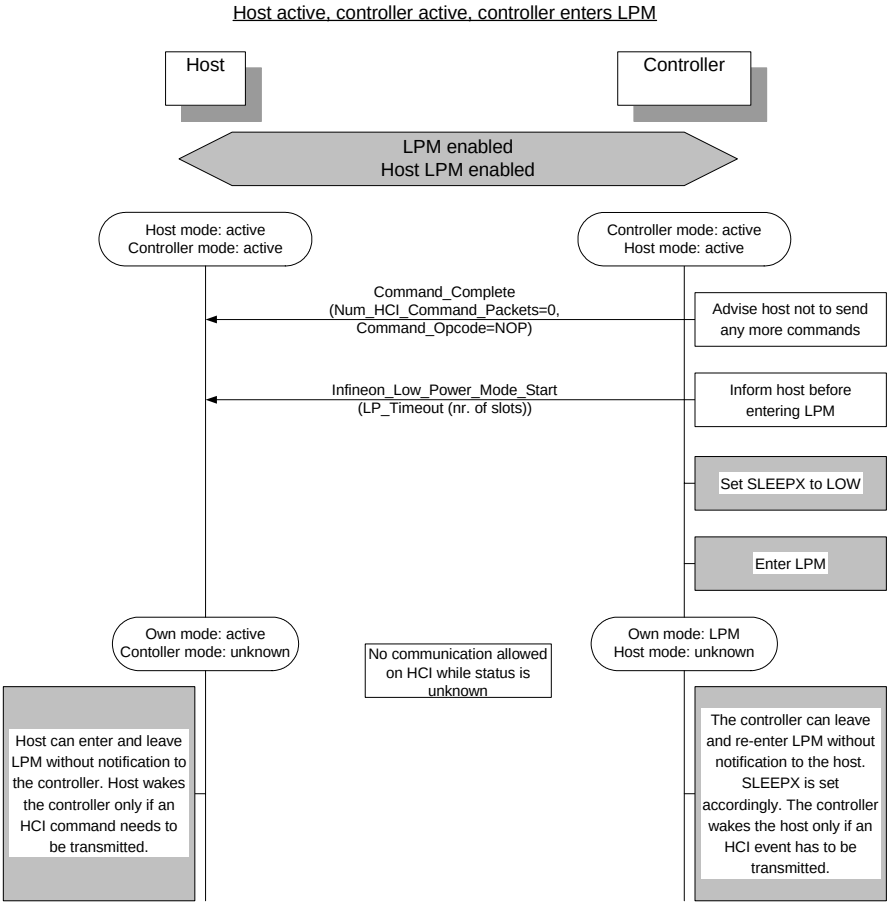


Figure 3-5 Host active, controller active, controller enters LPM

EXAMPLE 2: The host enters “unknown” mode

“Unknown” means that the controller will not know the state of the host. The host can enter and leave LPM without notification.

- Host informs the controller before entering the “unknown” mode.
- UART communication is disabled
- The host and the controller may wake up repeatedly and independently without notification, as long as no communication is needed on HCI.

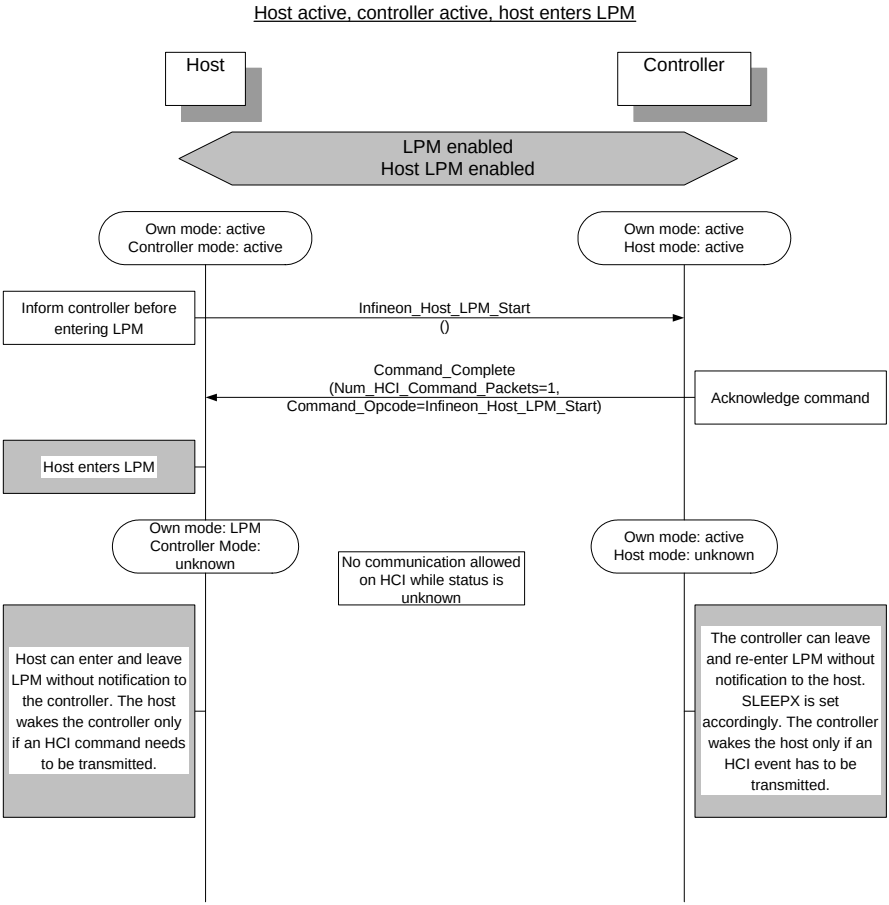


Figure 3-6 Host active, controller active, controller enters LPM

EXAMPLE 3: The controller wakes up the host

The controller has an event that it wants to send to the host via HCI.

- The controller generates a high pulse on WAKEUP_HOST to wake up the host.
- The host acknowledges via HCI.

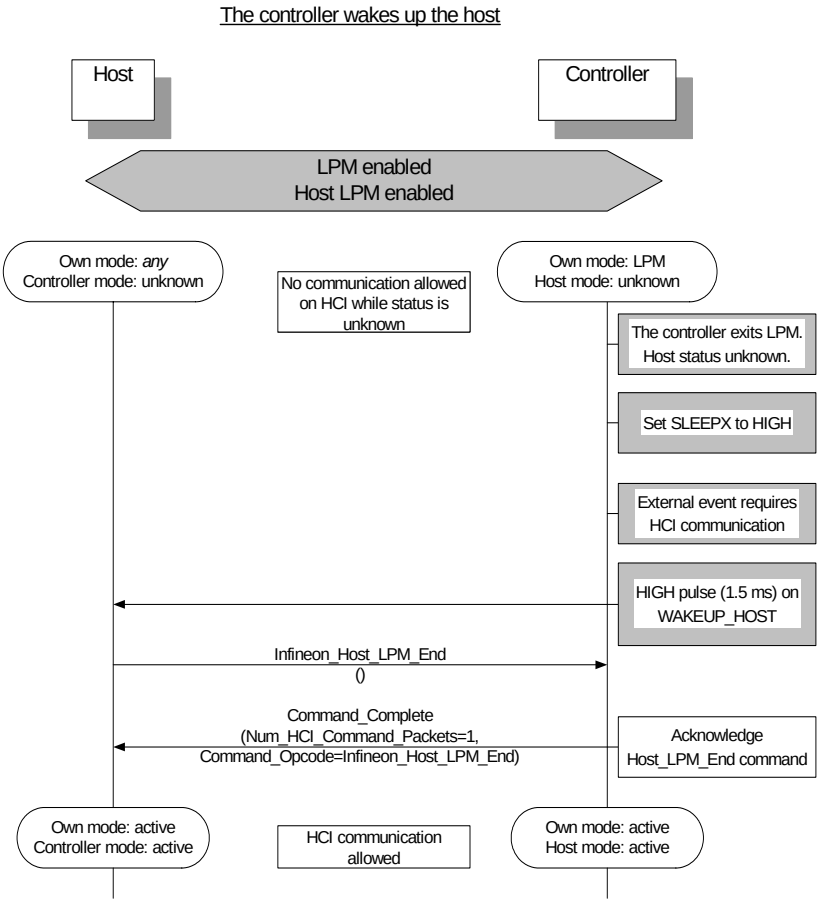


Figure 3-7 The controller wakes up the host

EXAMPLE 4: The host wakes up the controller

The host has a command that it wants to send to the controller via HCI.

- Host generates a high pulse on WAKEUP_BT to wake up the controller.
- The controller acknowledges via HCI.
- When the controller has seen the host pull the WAKEUP_BT line, it waits for further commands. The controller will not enter LPM again until the host enables it with the command Infineon_Enable_LPM.

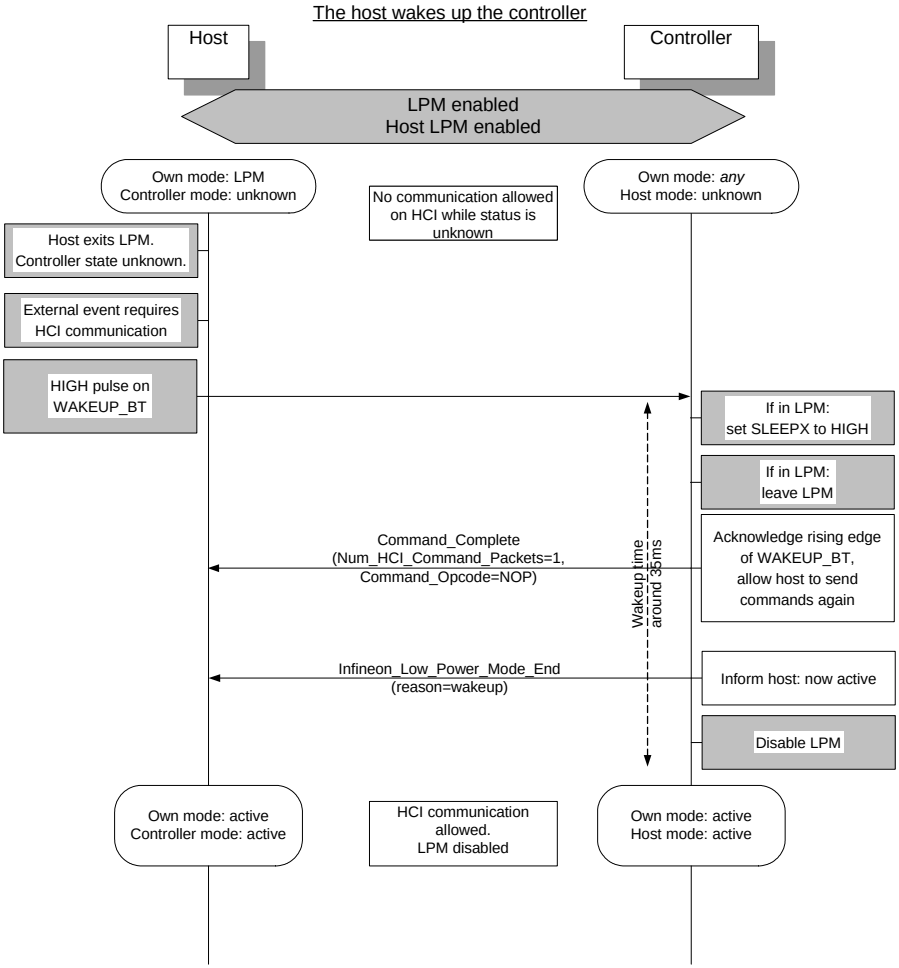


Figure 3-8 The host wakes up the controller

Exceptional Situations

Some exceptional situations may occur with the HCI UART-6W low power protocol. How to handle these is described below.

The controller enters the “unknown” mode while the host sends an HCI command

The wake-up protocol foresees that after having received a Command Complete event with Num_HCI_Packets = 0 and Command_Opcode = NOP from the controller, the host sends no more commands on HCI and enters the “unknown” mode.

It may exceptionally happen that the controller sends the Command Complete event at the same time as the host transmits an HCI command. In that case, the host is waiting for a Command Complete with Command_Opcode corresponding to the sent command. Instead it receives an Infineon Low Power Mode Start event.

In that exceptional case, the host must wake up the controller with the WAKEUP_BT line and re-send the HCI command when the controller has woken up again. The controller will not enter LPM again until the host enables it with the command Infineon_Enable_LPM.

An exception to the rule applies if the conflicting HCI command is an Infineon_Host_LPM_Start command. This exception is described in the following section.

The host and the controller enter the “unknown” mode simultaneously

It may exceptionally happen that the Command Complete event with Num_HCI_Packets = 0 and Command_Opcode = NOP is sent by the controller at the same time as the host sends an Infineon_Host_LPM_Start command.

In that exceptional case, the host must wait for the Infineon Low Power Mode Start event and then enter low power mode. The host must not expect a Command Complete event with Command_Opcode = Infineon_Host_LPM_Start in that case.

The host enters “unknown” mode while the controller sends an HCI event

The wake-up protocol foresees that after having received the Infineon_Host_LPM_Start command, the controller sends a Command Complete event and enters the “unknown” mode.

However it may exceptionally happen that the host sends the Infineon_Host_LPM_Start command at the same time as the controller sends an HCI event. In that case, it may happen that the controller is waiting for a response from the host, but receives an Infineon_Host_LPM_Start command instead. Example: The controller sends a Connection Request event and expects an Accept_Connection_Request command, but receives an Infineon_Host_LPM_Start command instead.

In such an exceptional case, the controller will answer the Infineon_Host_LPM_Start command with a Command Complete event with Status = “Command Disallowed” and will not enter the “unknown” mode. The host will also not enter the “unknown” mode

because Infineon_Host_LPM_Start is not acknowledged by a successful Command Complete event.

The host and the controller wakes up simultaneously

It may exceptionally happen that the host activates WAKEUP_BT at the same time as the controller activates WAKEUP_HOST. In that exceptional case, both wake-up procedures are executed.

The host wakes up and sends an Infineon_Host_LPM_End command to acknowledge the WAKEUP_HOST pulse.

The controller wakes up and sends a Command Complete event with Num_HCI_Packets = 1 followed by an Infineon_Low_Power_Mode_End event. The controller then acknowledges Infineon_Host_LPM_End with a Command Complete event.

3.1.3 UART

The on-chip UART (Universal Asynchronous Receiver and Transmitter) is compatible with standard UARTs and is optimized for Bluetooth communication. Hardware support for SLIP[1)] framing and 16-bit CRC calculation enhances performance with the HCI Three-Wire UART transport layer. A separate supply voltage, VDDUART, makes it easy to connect the UART interface to any system.

3.1.3.1 Baud Rates

The UART baud rate can be configured with the BD_DATA parameter *UART_Baudrate* or with the HCI+ command Infineon_Set_UART_Baudrate. The supported baud rates are listed in **Table 3-5** together with the small deviation error that results from the internal clock generation. The default baud rate is 115200 Baud.

1) See http://www.ietf.org/rfc/rfc1055.txt for information about SLIP.

Table 3-5 UART Baud Rates

Wanted Baud Rate	Real Baud Rate	Deviation Error (%)
9600	9615	0.16
19200	19230	0.16
38400	38461	0.16
57600	57522	-0.14
115200	115044	-0.14
230400	230088	-0.14
460800	464285	0.76
921600	928571	0.76
1843200	1857142	0.76
3250000	3250000	0

3.1.3.2 Detailed UART Behavior

After reset the UART interface is configured with one start bit, eight data bits, no parity bit and one stop bit. The least significant bit is transmitted first.

The polarity of the UART signals can be changed with the BD_DATA parameter *UART_Invert*. The default (non-inverted) behavior is shown in **Table 3-6**

Table 3-6 Default (non-inverted) behavior of UART signals

Signal	Level	Meaning
UARTTXD / UARTRXD	0	Start bit, ’0’ bit in character.
	1	Idle level, stop bit
UARTRTS / UARTCTS	0	Flow on
	1	Flow stopped

To prevent the system from floating signal lines while BlueMoon UniCellular is in low power mode it is possible to activate internal pull-up or pull-down resistors with the BD_DATA parameter *UART_Pulls*.

UARTCTS Response Time

Figure 3-9 shows the UARTCTS response time. Assuming non-inverted UART signals, the data flow stops within the “flow off response time” after UARTCTS has been set to high. If UARTCTS goes high during the transmission of a byte (phase 1 in the figure) this

byte will be completely transmitted. While UARTCTS is high, no data will be transmitted (phase 2). When UARTCTS goes low again, data transmission will continue (phase 3).

The maximum flow off response time is 10 UART bits (including start and stop bits). As an example, if the UART baud rate is 115200 Baud, the maximum flow off response time is 10 x 1/115200 s = 87 µs.

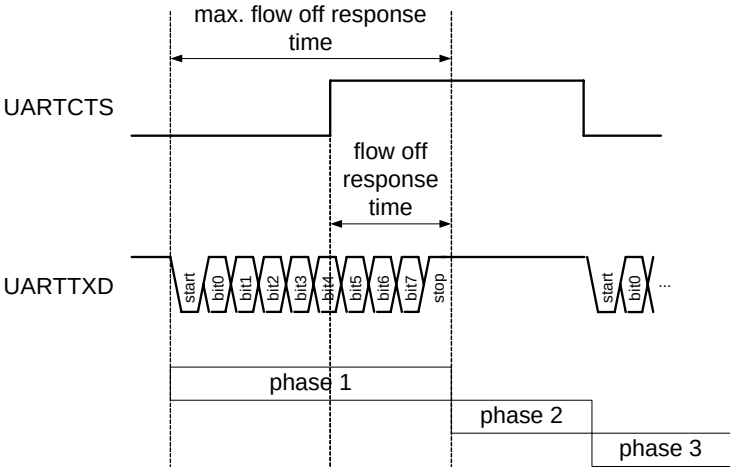


Figure 3-9 UARTCTS response time

3.2 PCM Interface

The PCM interface is used to exchange synchronous data (usually audio) between BlueMoon UniCellular and the host as well as to connect e.g. an external audio codec or an external DSP to BlueMoon UniCellular. It can be configured as an industry standard PCM interface supporting long and short frame synchronization, as an I2S interface[1)] or as an IOM-2 interface in terminal mode with reduced capabilities.

The main features of the PCM interface are:

- Two bidirectional PCM channels
- Separate supply voltage (VDDPCM) for easy interfacing to other systems
- Support for all sample types defined in the Bluetooth specification (Up to 16-bit linear samples and 8-bit A-law/μ-law compressed samples)[2)]
- 8x32-bit FIFOs for each channel
- Programmable frame length
- Programmable frame signal length
- Programmable channel start positions
- Programmable idle level on PCMOUT
- Programmable low-power/inactive levels on all PCM pins
- Data word LSB justified or MSB justified with respect to frame signal
- Clock master/slave mode
- Frame master/slave mode
- Fractional divider for PCM clock generation

1) Does not support variable word length. Hardware supports 16 or 24 bits. Current firmware supports 16 bits.
2) The hardware supports data word lengths of up to 24 bits.

3.2.1 Overview

The PCM interface consists of five signals as shown in **Figure 3-10** below

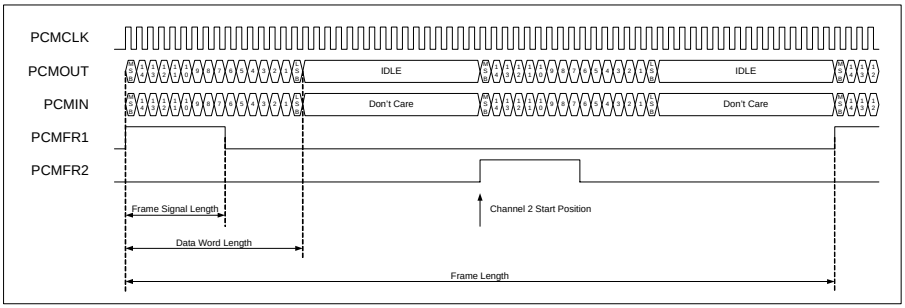


Figure 3-10 PCM Signals Overview

The clock signal PCMCLK is the timing base for the other signals in the PCM interface. In **clock master mode**, BlueMoon UniCellular generates PCMCLK from the internal system clock using a fractional divider. In **clock slave mode** PCMCLK is an input to BlueMoon UniCellular and has to be supplied by an external source. The maximum PCMCLK frequency (in both modes) is 1/8 of the internal system clock frequency.

The PCM interface supports up to two bidirectional channels. Data is transmitted on PCMOUT and received on PCMIN, always with the most significant bit first. The hardware supports a **Data Word Length** of 16 or 24 bits. The firmware always uses 16 bits since that is the maximum audio sample size (linear samples can be up to 16 bits, A-law or μ-law compressed samples are always 8 bits).

The samples are organized in frames such that each frame contains one sample in each direction of each active channel. The frame rate (i.e. sample rate) is controlled by the PCMCLK frequency and the programmable **Frame Length**. In the firmware the sample rate has been fixed to 8 kHz. This means that the PCMCLK frequency can be calculated from Frame Length and does not have to be specified.

Each channel has its own frame signal (PCMFR1/PCMFR2) that indicates where in the frame that channel starts. The **Frame Signal Length** is programmable. The start position of PCMFR2 in the frame is also programmable (Channel 2 Start Position). PCMFR1 always starts at the beginning of the frame.

In **frame master mode**, BlueMoon UniCellular generates PCMFR1 and PCMFR2. In **frame slave mode** the signal PCMFR1 is an input to BlueMoon UniCellular and has to be supplied externally (PCMFR2 is still generated by BlueMoon UniCellular). When only one channel is used PCMFR2 can be switched off with the HCI command Infineon_Write_PCM_Mode.

3.2.2 PCM Pin States

The PCM interface is only enabled when at least one (e)SCO connection is active and is routed through PCM or the interface is configured for PCM loopback. The signal levels when the interface is disabled or BlueMoon UniCellular is in low power mode are configurable with HCI_Infineon_Write_PCM_Mode. The pull-ups and pull-downs will only work correctly when VDDPCM is supplied.

Table 3-7 shows the possible states of the PCM pins in different operating modes. The column for PCMFR2 is only valid when two frame signals are used. When one frame signal is used the PCMFR2 pin is available for I2C.

Table 3-7 States of the PCM pins in various modes of operation

	PCMFR1 (P0.0)	PCMCLK (P0.1)	PCMIN (P0.2)	PCMOUT (P0.3)	PCMFR2[1] (P0.12)
During/after reset	Pull-down (PD)	Pull-down (PD)	Tristate (Z)	Pull-down (PD)[2]	Pull-up (PU)
Low power mode/ No (e)SCO connection	Conf.[3] Z/PU/PD	Conf.[3] Z/PU/PD	Conf.[3] Z/PU/PD	Conf.[3] Z/PU/PD	Conf.[3] Z/PU
Active (e)SCO connection PCM clock master PCM frame master	PCM output	PCM output	PCM input	PCM output	PCM output
Active (e)SCO connection PCM clock master PCM frame slave	PCM input	PCM output	PCM input	PCM output	PCM output
Active (e)SCO connection PCM clock slave PCM frame master	PCM output	PCM input	PCM input	PCM output	PCM output
Active (e)SCO connection PCM clock slave PCM frame slave	PCM input	PCM input	PCM input	PCM output	PCM output

1) If “Number of Used Frame Signals” has been set to 2 with the HCI+ command Infineon_Write_PCM_Mode.

2) Fusable to Z/PU/PD. Default PD

3) Configurable with the HCI+ command Infineon_Write_PCM_Mode

3.2.3 Sample Rate, Frame Length and PCMCLK Frequency

The sample rate is fixed by the firmware to 8 kHz. The *frame length* is programmable with HCI_Infineon_Write_PCM_Mode and is used internally by the firmware to calculate the frequency of PCMCLK. The calculation is done like this:

$$f_{PCMCLK} = Sample\_Rate * Frame\_Length$$

Some examples are shown in **Table 3-8**.

Table 3-8 Example Combinations of Frame Length and PCMCLK Frequency

Configuration	Frame Length (bits)	PCMCLK freq. (kHz)
1 channel with 16-bit samples	16	128
2 channels with 16-bit samples	32	256
1 or 2 channels, idle between data words	250	2000

The *frame length* supersedes all other configurable parameters like *frame signal length* and *data word length*, i.e. a new frame is started even if the current frame processing is not finished. Special care has to be taken when configuring the PCM interface or data may be lost.

3.2.4 Channel Start Positions

The position of a channel within a frame is determined by the *channel start position*. At the configured bit position the transmit and receive operation of the corresponding channel starts. For channel 2 the *channel start position* also sets the start of the frame signal (for channel 1 the frame signal always starts at the beginning of the frame).

Figure 3-11 shows an example where channel 1 start position = 2 and channel 2 start position = 20. Note that PCMFR1 still starts at position 0.

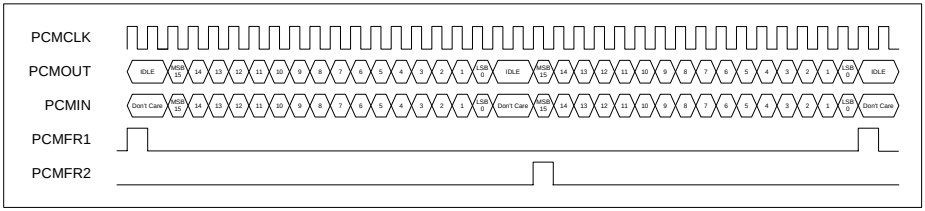


Figure 3-11 Channel Start Positions

The *data word length* supersedes the *channel start position*, i.e. the earliest possible start of channel n is directly after channel n-1. For example, if 16 bit data words are selected the earliest possible start of channel 2 is at bit position 16 since channel 1 blocks bit positions 0 to 15.

3.2.5 Frame Signal Length and Justification Mode

The *frame signal length* is programmable with HCI_Infineon_Write_PCM_Mode. The programmed value is valid for all channels. When *frame signal length* is larger than *data*

word length, the data word can be aligned either to the beginning or the end of the frame signal[1)].

In **MSB justified mode** the data word is aligned to the beginning of the frame signal as shown in **Figure 3-12**. When LSB of the data word has been transmitted, PCMOUT is set to zero.

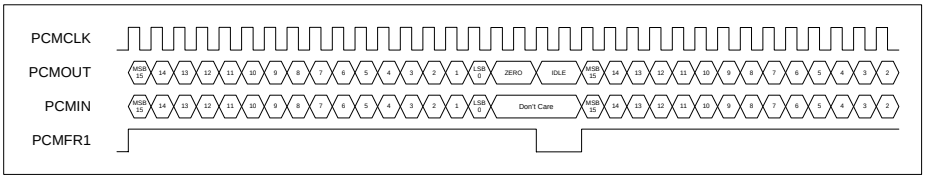


Figure 3-12 MSB Justified Mode

In **LSB justified mode** the data word is aligned to the end of the frame signal as shown in **Figure 3-13**. PCMOUT is set to MSB until the data word starts to be transmitted.

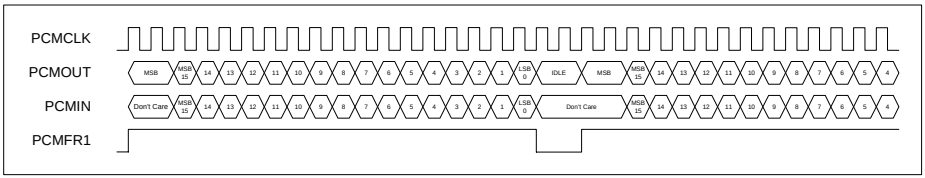


Figure 3-13 LSB Justified Mode

The justification mode is configured with HCI_Infineon_Write_PCM_Mode.

3.2.6 Idle Level

When the PCM interface is enabled but no channel is currently active, PCMOUT is set to the idle level. This level is programmable to high, low or tristate with HCI_Infineon_Write_PCM_Mode.

3.2.7 Early Frame Signal Mode

In **early frame signal mode** the data on PCMIN and PCMOUT is delayed by one clock cycle as shown in **Figure 3-14**.

1) If the channel start position for channel 1 is non-zero the data for channel 1 will be aligned as if the frame signal had started at the channel start position.

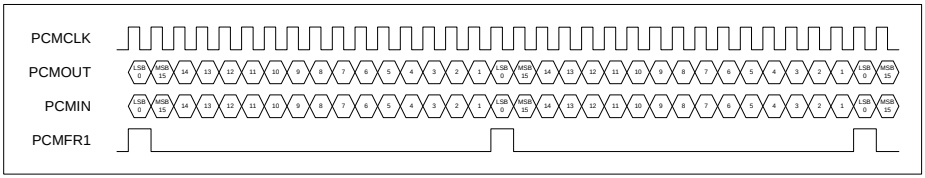


Figure 3-14 Early Frame Signal Mode

3.2.8 Double Clock Mode

In **double clock mode** two PCMCLK cycles are used for each data bit. The incoming data is sampled on the second falling edge. When BlueMoon UniCellular generates the frame signals (frame master mode) the frame signal length will always be a multiple of two PCMCLK cycles. In frame slave mode the length of PCMFR1 shall be at least one PCMCLK cycle.

3.2.9 Inverting PCMCLK, PCMFR1 and PCMFR2

Data is normally shifted with the rising edge of PCMCLK and sampled with the falling edge. The frame signals (PCMFR1 and PCMFR2) are normally active high. If an application needs reverse polarity on any of these signals the PCM interface can be configured to invert the signal. This configuration is done with HCI_Infineon_Write_PCM_Mode.

3.2.10 Enabling/Disabling Channels

The PCM channels are normally all enabled but can be enabled/disabled individually. When a channel is disabled, no data is received for that channel and the PCMOUT signal is set to the idle level during the active time for that channel. The behavior of the frame signals is the same irrespective of whether the channels are enabled or not.

3.2.11 Timing in Frame Slave Mode

BlueMoon UniCellular is said to be in frame slave mode when it is configured to use an externally supplied frame signal for channel 1 (PCMFR1). A new frame begins with every rising edge of PCMFR1. If the start of a new frame is detected while frame processing is still ongoing for another frame the currently processed frame will be aborted. For the input direction, if a data word is not completely received it will be sign extended with MSB. It is important to notice that the channels are handled separately. If reception/transmission is interrupted while channel 1 is active, the prepared data for channel 2 will be sent in the next frame.

Figure 3-15 shows the timing relations between PCMFR1 and PCMCLK. If the frame signal becomes active in the low phase of PCMCLK the new frame starts at the next rising edge of PCMCLK. If the frame signal becomes active in the high phase of PCMCLK the new frame starts immediately

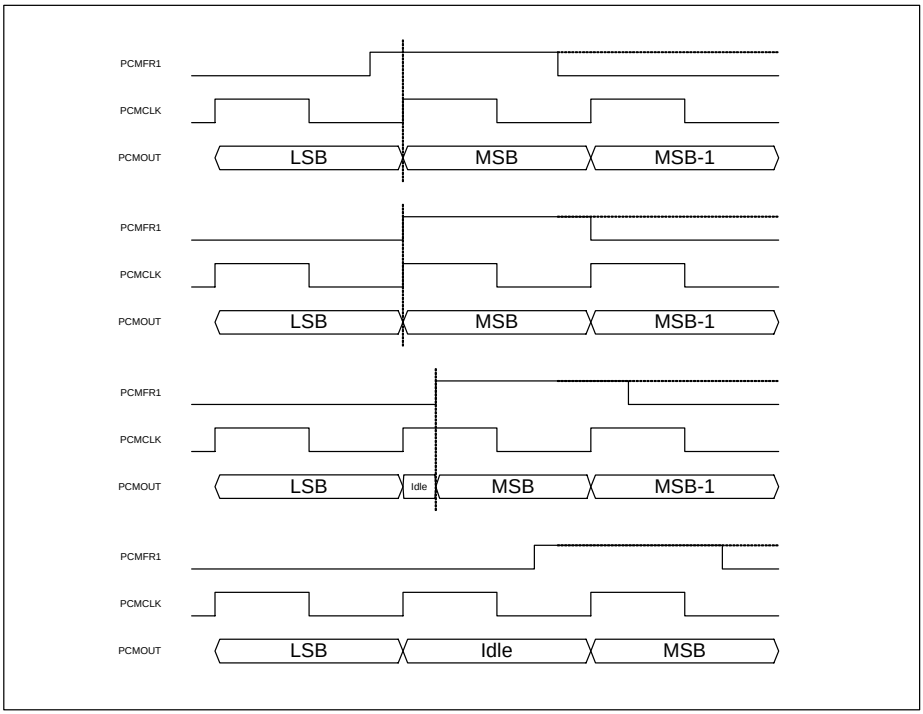


Figure 3-15 Timing Relations between PCMFR1 and PCMCLK

3.2.12 Start and Stop of Frame Processing

In the following two sections first frame means the first processed data frame after enabling the PCM interface and last frame means the last processed data frame after disabling the PCM interface.

3.2.12.1 Clock Master Mode

The logical timings for the first frame and the last frame in frame master mode are shown in Figure 3-16 a) for the normal frame signal mode and b) for the early frame signal mode. The first rising clock edge occurs with the rising clock edge of the frame signal.

The logical timings for the first frame and the last frame in frame slave mode are shown in **Figure 3-16** c) for the normal frame signal mode and d) for the early frame signal mode. The clock signal on PCMCLK is activated when the PCM interface is enabled. The frame processing starts with the first rising edge of the frame signal PCMFR1.

The last rising clock edge on the PCMCLK output occurs with the shift of the idle level on PCMOUT.

3.2.12.2 Clock Slave Mode

The logical timings for the first frame and the last frame are shown in **Figure 3-16** e) for the normal frame signal mode and f) for the early frame signal mode. The frame processing starts with the first rising edge on the frame signal PCMFR1. For driving the idle level on the output PCMOUT it is required that a rising clock edge on PCMCLK occurs after the transmission of the last bit (LSB) of the last enabled channel of this last data frame as shown in the figures. If this clock edge does not occur, e.g. the last rising clock edge is the clock edge that shifts out the LSB on PCMOUT, the LSB will remain on the output signal PCMOUT.

3.2.13 PCM Loopback

For test purposes the PCM interface can be put into different loopback modes. This is done with the HCI+ command HCI_Infineon_Enable_PCM_Loopback. Details about the different loopback modes are provided in the HCI+ specification.

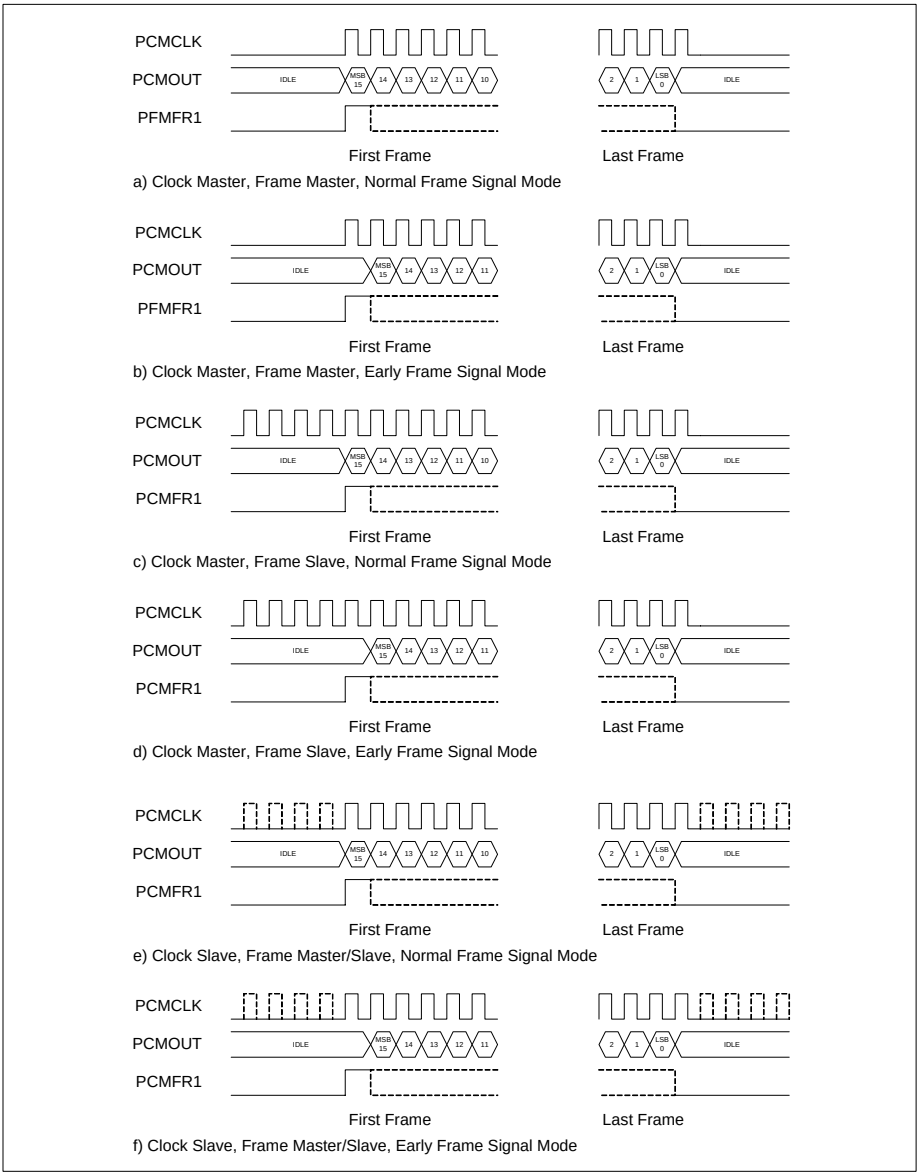


Figure 3-16 Start and Stop of Frame Processing

3.2.14 Examples for PCM Modes

3.2.14.1 Single Channel Modes

In these modes, only channel 1 of the PCM interface is used.

Long Frame Mode

Long frame modes are defined by a *frame signal length* larger than one.

If the *frame signal length* is equal to the *data word length*, the *frame length* needs to be at least the *data word length* plus one as shown in **Figure 3-17**.

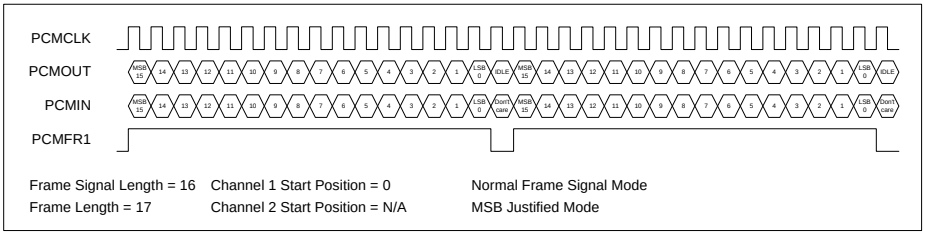


Figure 3-17 One Channel, Frame Signal Length = Data Word Length

If the *frame signal length* is smaller than the *data word length* the *frame length* must be larger than or equal to the *data word length* as shown in **Figure 3-18**.

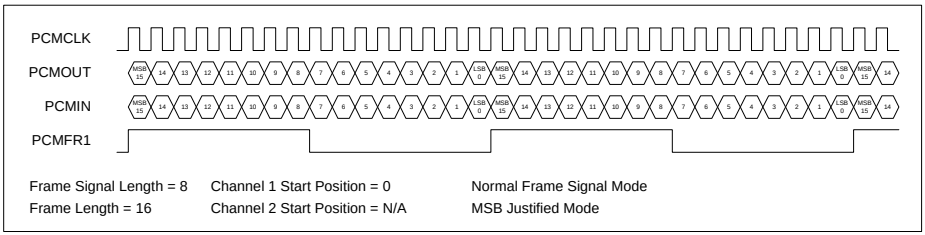


Figure 3-18 One Channel, Frame Signal Length < Data Word Length

If the *frame signal length* is larger than the *data word length* the *frame length* must be larger than the *frame signal length* and the data can be MSB justified as shown in **Figure 3-19** or LSB justified as shown in **Figure 3-20**.

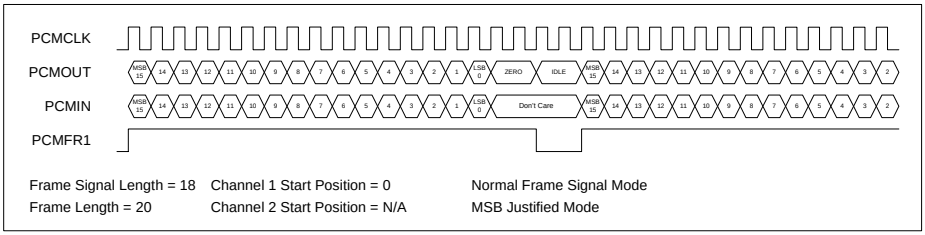


Figure 3-19 One Channel, Frame Signal Length > Data Word Length, MSB Justified

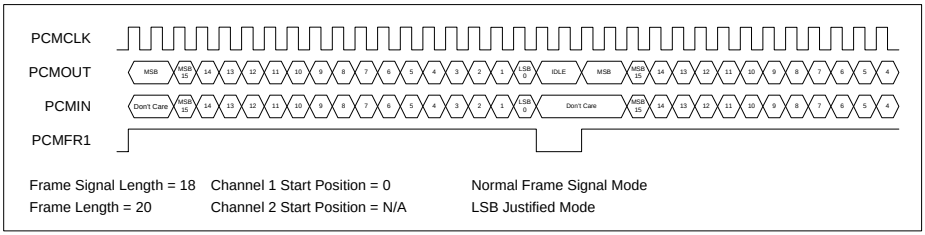


Figure 3-20 One Channel, Frame Signal Length > Data Word Length, LSB Justified

Short Frame Mode

Short frame modes are defined by a *frame signal length* equal to one.

In short frame mode the *frame length* can be equal to the *data word length* as shown in **Figure 3-21** for normal frame signal mode and in **Figure 3-22** for early frame signal mode.

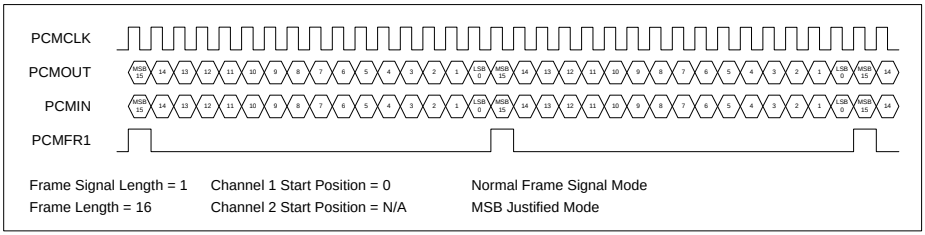


Figure 3-21 One Channel, Short Frame Signal, Frame Length = Data Word Length, Normal Frame Signal Mode

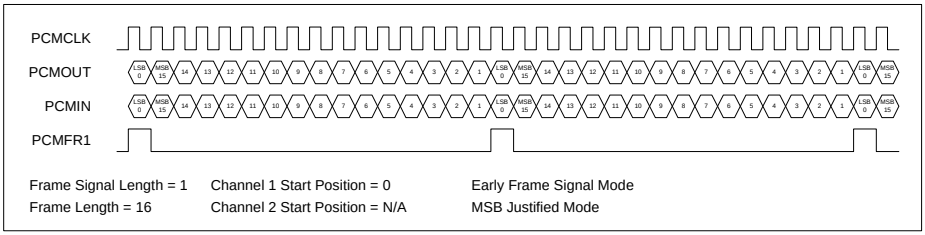


Figure 3-22 One Channel, Short Frame Signal, Frame Length = Data Word Length, Early Frame Signal Mode

If the *frame length* is larger than the *data word length* the idle value is output on PCMOUT as shown in **Figure 3-23** for normal frame signal mode and in **Figure 3-24** and **Figure 3-25** for early frame signal mode.

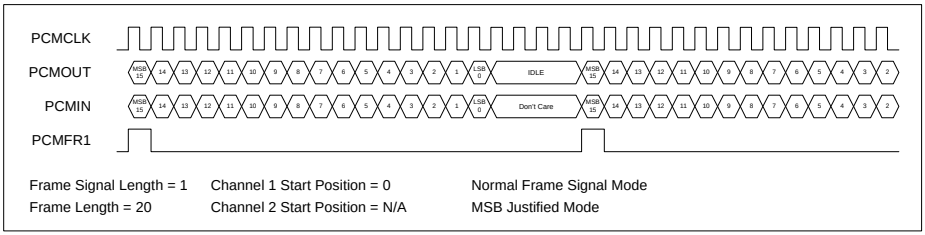


Figure 3-23 One Channel, Short Frame Signal, Frame Length > Data Word Length, Normal Frame Signal Mode

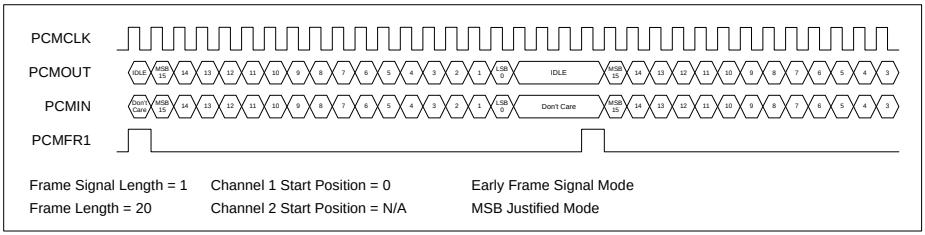


Figure 3-24 One Channel, Short Frame Signal, Frame Length > Data Word Length, Early Frame Signal Mode

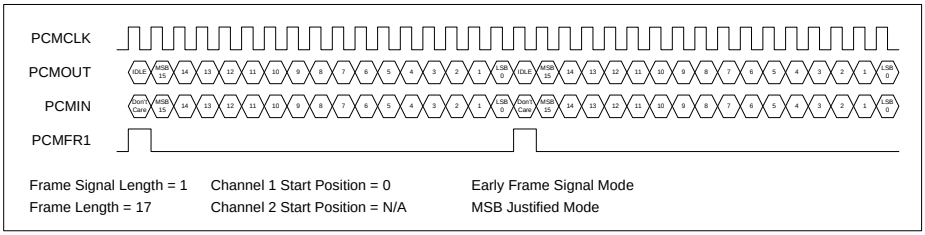


Figure 3-25 One Channel, Short Frame Signal, Frame Length > Data Word Length, Early Frame Signal Mode

3.2.14.2 Dual Channel Modes

In these modes, both channels of the PCM interface are used.

Long Frame Mode

If the *frame signal length* is equal to the *data word length* an I2S like behavior is achieved as shown in **Figure 3-26** for the normal frame signal mode and in **Figure 3-27** for the early frame signal mode.

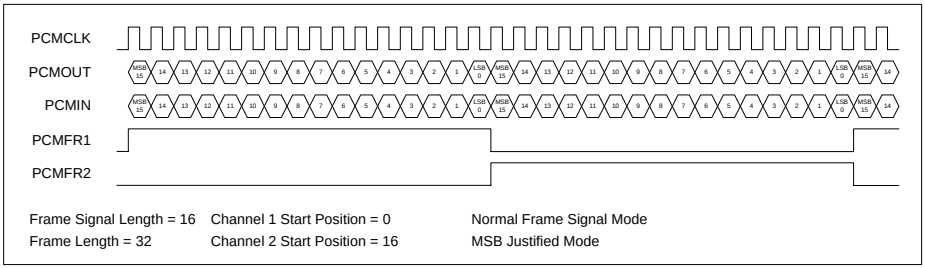


Figure 3-26 Two Channels, Frame Signal Length = Data Word Length, Normal Frame Signal Mode

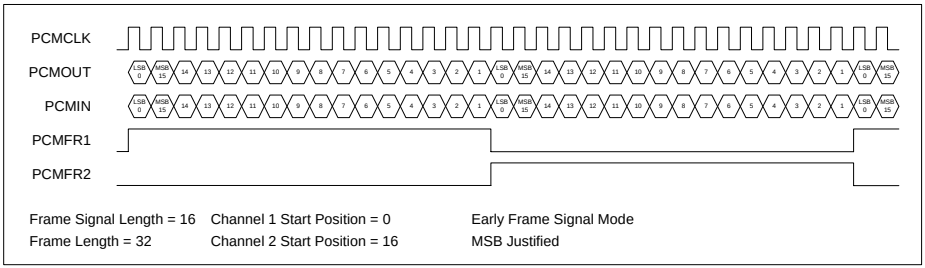


Figure 3-27 Two Channels, Frame Signal Length = Data Word Length, Early Frame Signal Mode

If the *frame signal length* is smaller than the *data word length*, the *frame length* must be larger than or equal to twice the *data word length* as shown in **Figure 3-28**.

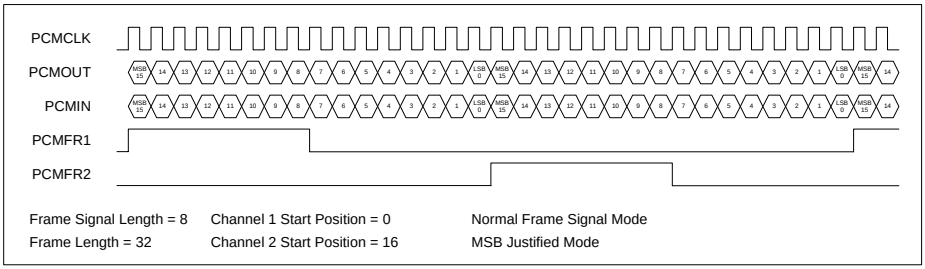


Figure 3-28 Two Channels, Frame Signal Length < Data Word Length

If the *frame signal length* is larger than the *data word length*, the data can be MSB justified as shown in **Figure 3-29** or LSB justified as shown in **Figure 3-30**.

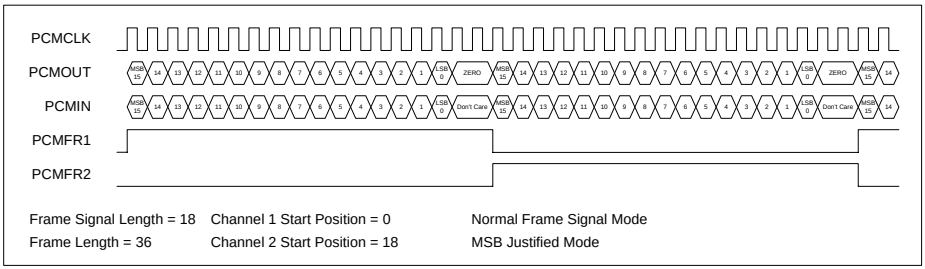


Figure 3-29 Two Channels, Frame Signal Length > Data Word Length, MSB justified

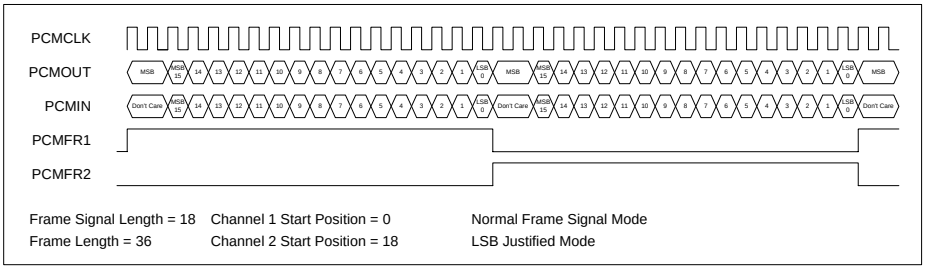


Figure 3-30 Two Channels, Frame Signal Length > Data Word Length, LSB Justified

Short Frame Mode

Examples of two channels in short frame mode are shown in **Figure 3-31** for normal frame signal mode and in **Figure 3-32** for early frame signal mode.

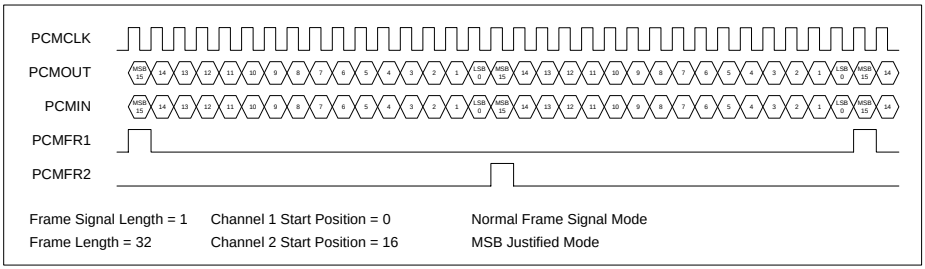


Figure 3-31 Two Channels, Short Frame Signal, Normal Frame Signal Mode

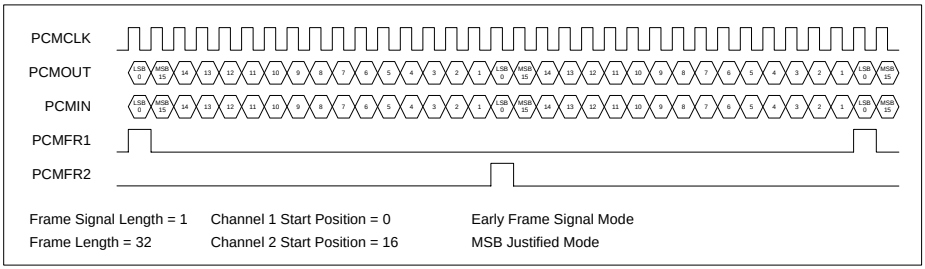


Figure 3-32 Two Channels, Short Frame Signal, Early Frame Signal Mode

Free alignment of data channels within the frame

The available channels can be freely aligned within the frame as long as the channel sequence is not changed. **Figure 3-33** shows an example with two 16-bit channels where the first channel starts at position 0 and the second channel starts at position 32.

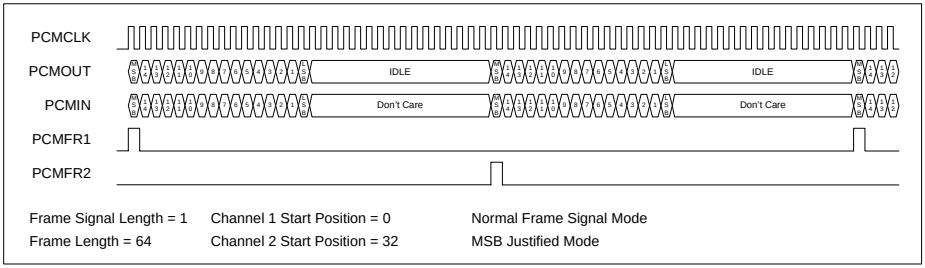


Figure 3-33 Two Channels, Short Frame Signal, Idle Bits between the Channels

Double Clock Mode

An example of the *double clock mode* is shown in **Figure 3-34**. In this case the PCM interface generates the frame signal.

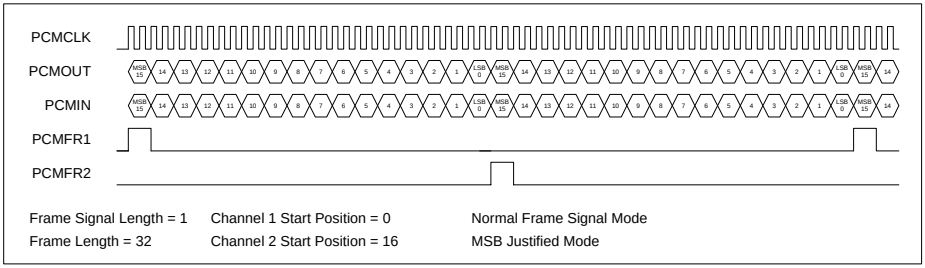


Figure 3-34 Two Channels, Short Frame Signal, Double Clock Mode

3.3 WLAN Coexistence Interface

BlueMoon UniCellular has a WLAN coexistence interface that is based on the IEEE 802.15.2 Packet Traffic Arbitration (PTA) scheme[1]. The interface prevents interference between collocated WLAN and Bluetooth devices by not letting the two devices transmit and/or receive at the same time. WLAN packets and Bluetooth packets are assigned priorities, and a control unit decides on a per-packet basis which of the devices that should be allowed to operate.

The interface uses three wires as shown in **Figure 3-35**.

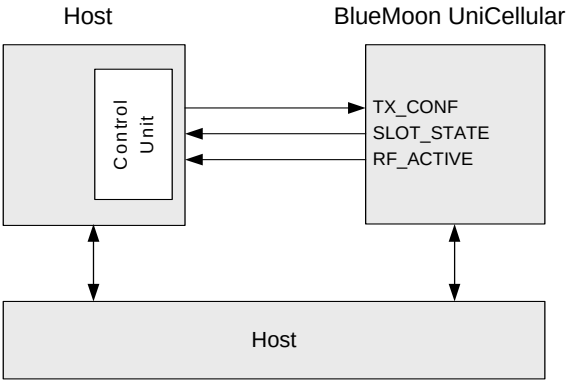


Figure 3-35 WLAN Coexistence Interface

3.3.1 Signals

The signals in the three-wire interface are listed in **Table 3-9**. The signal polarities are selected so that both systems work independently if all signals are pulled down. This allows operation of either system if the other one is powered down.

Table 3-9 Coexistence signals between Bluetooth and WLAN

Signal	Direction	Description
TX_Conf	From WLAN	Transaction confirmation
Slot_State	To WLAN	Signals priority, data type and RX/TX state, using time multiplexing
RF_Active	To WLAN	Bluetooth activity indication

[1] "802.15.2: Coexistence of Wireless Personal Area Networks with other Wireless Devices Operating in Unlicensed Frequency Bands", IEEE, 28 August 2003

BlueMoon UniCellular requests permission to send or receive using the RF_Active signal, and transfers information about the requested operation via the Slot_State signal. The control unit located in the WLAN device uses this information, together with available information about the current WLAN activity, to decide whether Bluetooth should be allowed to operate or not. The control unit uses the TX_Conf signal to grant or deny Bluetooth operation.

3.3.1.1 RF_Active

The RF_Active signal indicates the activity of the Bluetooth device during the next slot(s). The polarity of RF_Active is defined as:

- Logic low => no Bluetooth activity
- Logic high => Bluetooth is active

In general, the duration between rising and falling edge of RF_Active frames a transaction, which is defined as one or more polling slots and immediately following response slot(s). RF_Active is used as a request signal to the control unit located in the WLAN device and is therefore raised before data is actually sent or received, giving the control unit time to decide whether Bluetooth should be allowed to operate or not. The signal is deasserted between back-to-back transactions. The signal is deasserted as soon as possible when Bluetooth is no longer active, e.g. after expiry of the RX search window.

RF_Active synchronizes the control unit to the Bluetooth slot for the duration of each transaction.

3.3.1.2 Slot_State

The Slot_State signal is used for transferring information about priority, data type, and RX/TX status.

After RF_Active has been raised, the Slot_State signal first indicates the priority of the requested transaction:

- Logic low => low priority
- Logic high => high priority

After the priority signaling, Slot_State is used for indicating the type of data that is to be sent or received in the requested Bluetooth transaction:

- Logic low => ACL data transactions, which have low priority by default but can be given high priority with the HCI+ command Infineon_Coexistence_Set_Link_Prio.
- Logic high => Transactions that have a fixed high priority.

After the data type signaling, Slot_State is used for indicating the RX/TX status of the Bluetooth radio:

- Logic low => receive
- Logic high => transmit

The data type signaling and RX/TX signaling are not present in all modes of operation.

3.3.1.3 TX_Conf

TX_Conf is used by the control unit in the WLAN device to grant or refuse Bluetooth permission to perform the requested transaction. The polarity of TX_Conf is:

- Logic low => transaction granted
- Logic high => transaction denied

BlueMoon UniCellular will not start a transaction if TX_Conf is high. TX_Conf may change during an ongoing Bluetooth transaction, in which case the transaction will be aborted immediately.

3.3.2 Pins

The pins SLOT_STATE and RF_ACTIVE are supplied in the VDD domain and shared with the JTAG interface. To select the coexistence interface the JTAG# pin must be set high. The pins are tristate during reset. External pull-down resistors may be needed so that WLAN can operate undisturbed during this time.

The pin placement for TX_CONF is configurable. If no external PA is used, the RXON pin in the VDD domain can be used. If external PA is used, the pin P0.14 in the VDDUART domain must be used instead. The selection is done with the BD_DATA parameter *RF_Conf*.

3.3.3 Modes of Operation

There are three different modes of the three-wire interface to choose between:

- Simplified three-wire
- Standard three-wire
- Standard three-wire with data type signaling

The choice of mode is done with the HCI+ command Infineon_Coexistence_Enable.

3.3.3.1 Simplified three-wire

In the simplified three-wire mode, the Slot_State signal is used only for priority information. No information about data type or RX/TX status is transferred. Slot_State is kept at the same level for the duration of the transaction. Assertion of the Slot_State signal follows the timing of RF_Active.

3.3.3.2 Standard three-wire

In the standard three-wire mode, the Slot_State signal is used for priority information and RX/TX information. **Figure 3-36** shows the signaling in standard three-wire mode for a transaction starting with TX.

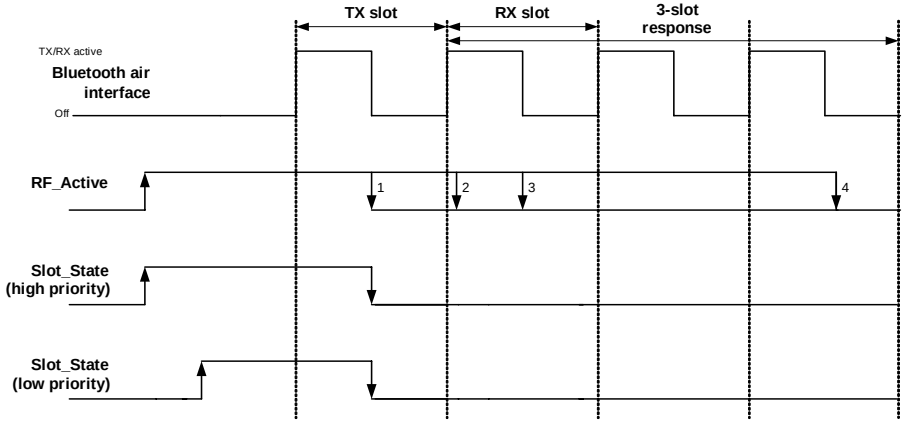


Figure 3-36 Signaling in standard three-wire mode, TX at first slot

The signal RF_Active is raised before the transmit slot begins. RF_Active remains active for the expected duration of the slave response. The cases shown are:

- 1: No response expected
- 2: Response expected, but search window expired
- 3: One-slot response
- 4: Three-slot response. Five-slot response follows the same pattern

In the case of a high priority transaction, the Slot_State signal is raised after the rising edge of RF_Active. For low priority transactions, Slot_State remains low until TX mode is signalled.

TX mode is signalled by setting Slot_State to high after the priority signaling. The switch to RX mode is indicated by setting the Slot_State signal to low before the start of the RX slot. Slot_State may be deasserted as early as the start of the first TX frame.

Figure 3-37 shows the signaling in standard three-wire mode for a transaction starting with RX.

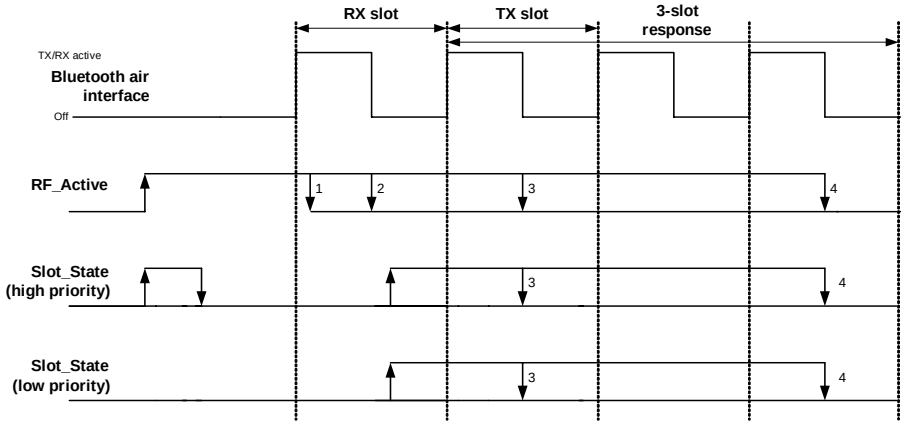


Figure 3-37 Signaling in standard three-wire mode, RX at first slot

The signal RF_Active is raised before the receive slot begins. RF_Active remains active until any response transmission has finished. The cases shown are:

- 1: Search window expired
- 2: No data to transmit
- 3: One-slot response
- 4: Three-slot response. Five-slot response follows the same pattern

In the case of a high priority transaction, the Slot_State signal is raised after the rising edge of RF_Active. For low priority transactions, Slot_State remains low until TX mode is signaled.

RX mode is signaled by setting Slot_State to low after the priority signaling. The switch to TX mode is indicated by setting the Slot_State signal to high before the start of the TX slot. Slot_State may be asserted as early as the start of the first RX frame.

3.3.3.3 Standard three-wire with data type signaling

When data type signaling is enabled, the Slot_State signal is used for priority information, data type information, and RX/TX information. This is done by dividing the time which would be used only for priority signaling in the standard three-wire mode into two parts: one for priority signaling and one for data type signaling.

Figure 3-38 shows the signaling in standard three-wire mode with data type signaling enabled, for a transaction starting with TX.

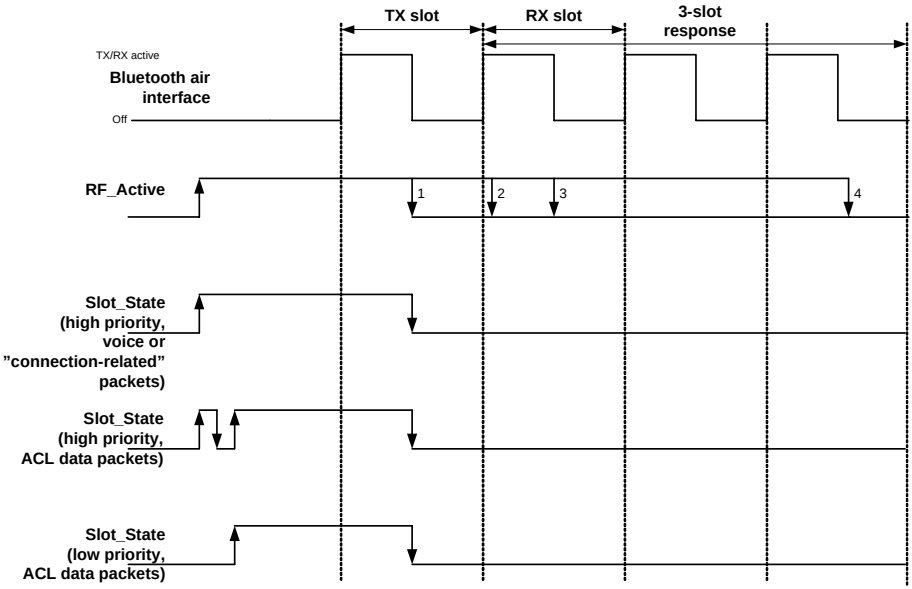


Figure 3-38 Standard three-wire mode with data type signaling, TX at first slot

The RF_Active signal is raised before the transmit slot begins. RF_Active remains active for the expected duration of the slave response. The cases 1-4 shown in **Figure 3-38** are the same as in **Figure 3-36**.

In the case of a high priority transaction, the Slot_State signal is raised after the rising edge of RF_Active. For low priority transactions, Slot_State remains low until the data type is signalled.

The data type is signalled by setting Slot_State to high or low immediately after the priority signaling.

TX mode is signalled by setting Slot_State to high after the data type signaling. The switch to RX mode is indicated by setting the Slot_State signal to low before the start of the RX slot. Slot_State may be set to low as early as the start of the first TX frame.

Figure 3-39 shows the signaling in standard three-wire mode with data type signaling enabled, for a transaction starting with an RX slot.

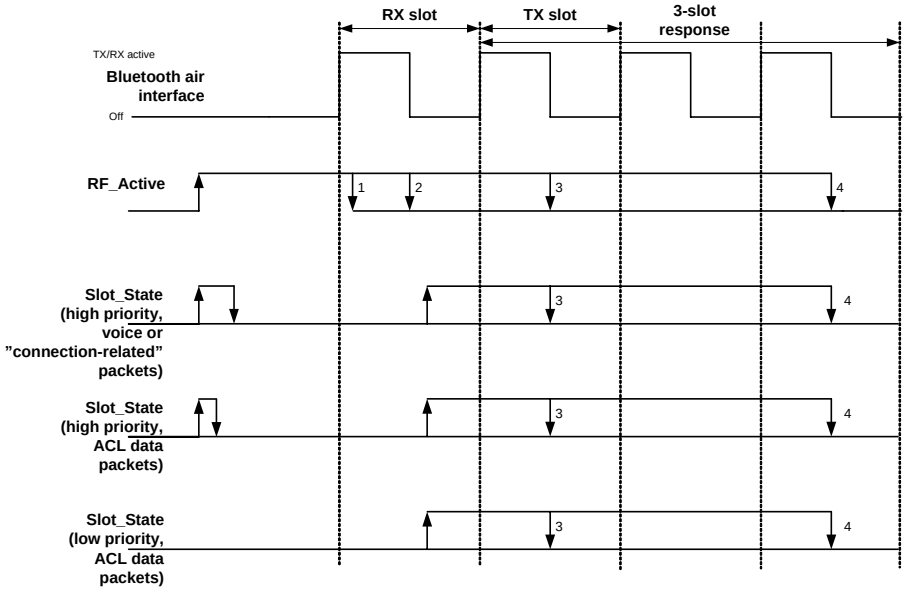


Figure 3-39 Standard three-wire mode with data type signaling, RX at first slot

The RF_Active signal is raised before the receive slot begins. RF_Active remains active until any response transmission has finished. The cases 1-4 shown in **Figure 3-39** are the same as in **Figure 3-37**.

In the case of a high priority transaction, the Slot_State signal is raised after the rising edge of RF_Active. For low priority transactions, Slot_State remains low until the data type is signalled.

The data type is signalled by setting Slot_State to high or low immediately after the priority signaling.

RX mode is signalled by setting Slot_State to low after the data type signaling. The switch to TX mode is indicated by setting the Slot_State signal to high before the start of the TX slot. Slot_State may be set to high as early as the start of the first RX frame.

3.3.4 Packet Prioritization

Packets belonging to the following types of Bluetooth transactions are given high priority:

- Inquiry, inquiry scan, and inquiry response
- Page, page scan, and page response

- LMP PDU transactions, when Bluetooth master
- SCO/eSCO transactions
- Poll transactions, when Bluetooth master
- Transactions at sniff anchor point and during sniff attempt
- First transaction when waking up from hold. Priority is kept at a high level until a packet has been successfully received. Priority is then returned to the default level.
- Master/slave role switch
- Park beacons and park access windows
- If no packet has been received on a link within the poll interval, the priority of all packets on that link is set to high. When a packet has been successfully received, priority is returned to the default level.

ACL data transactions are given high priority if that has been requested with the HCI+ command Infineon_Coexistence_Set_Link_Prio. Otherwise they have low priority.

All other transactions will have low priority.

3.3.5 Timing Diagrams

Timing diagrams for various scenarios can be found in the following figures. Timing values are given in **Table 3-10**.

RF_Active is asserted t_1 before the start of a transaction. RF_Active is deasserted within t_7 after the last RX or TX activity of the transaction has ended.

If data type signaling is enabled, Slot_State indicates the priority of a transaction during t_9. Data type is signalled during t_{10}. If data type signaling is not enabled, Slot_State indicates the priority of a transaction for the duration of $[t_3 – t_2]$ after RF_Active is raised.

After the priority or data type indication window, the Slot_State signal indicates the RX/TX mode of the first slot. For subsequent slots, the Slot_State signal is set to reflect the RX/TX mode for the next slot N no later than t_4 from the start of slot N-1.

TX_Conf shall respond at least t_6 before start of the slot, giving the control logic the maximum of t_5 to process the information. TX_Conf shall not change during t_6, but may change outside of t_6. If TX_Conf is changed during an already started transaction, the transaction will be aborted within t_{11}.

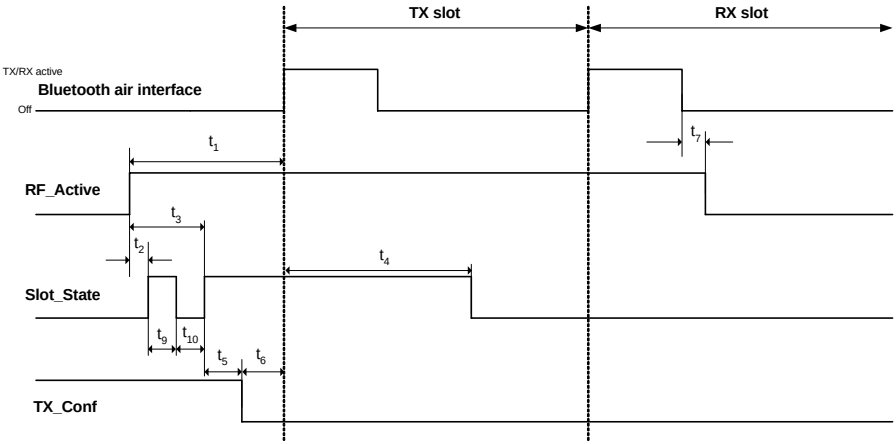


Figure 3-40 High priority transaction, starting with TX Data type = ACL data

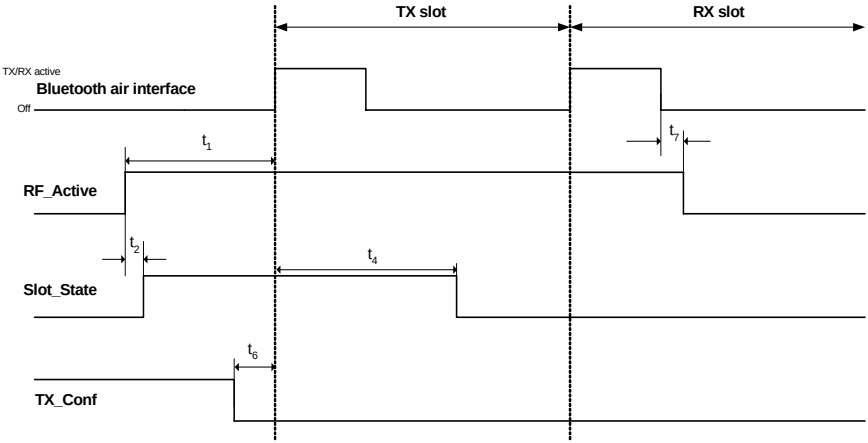


Figure 3-41 High priority transaction, starting with TX Data type = voice or “connection-related” (poll, sniff etc.) or Data type signaling not enabled

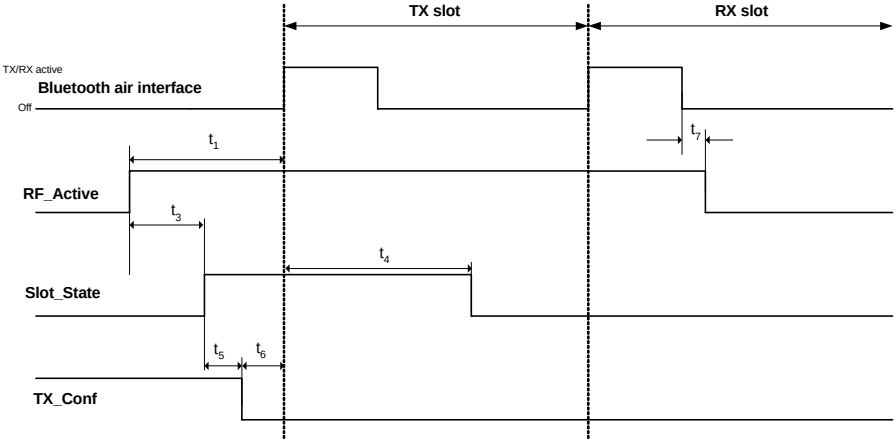


Figure 3-42 Low priority transaction, starting with TX
Data type = ACL data
or
Data type signaling not enabled

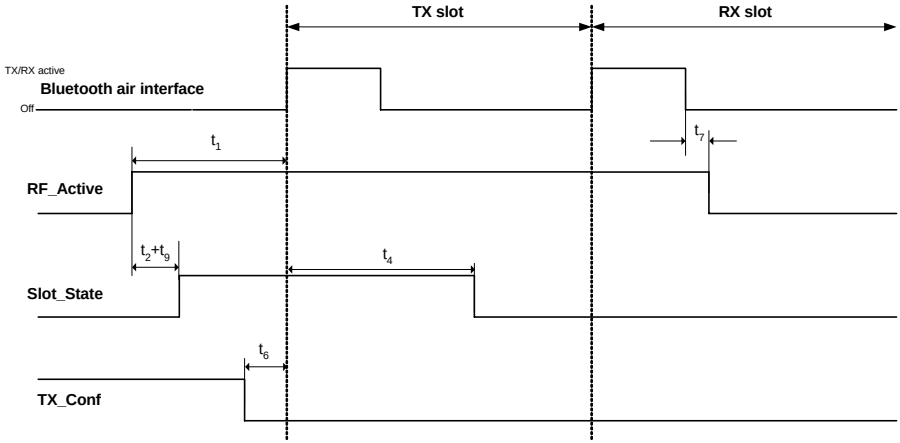


Figure 3-43 Low priority transaction, starting with TX
Data type = voice or “connection-related” (poll, sniff etc.)

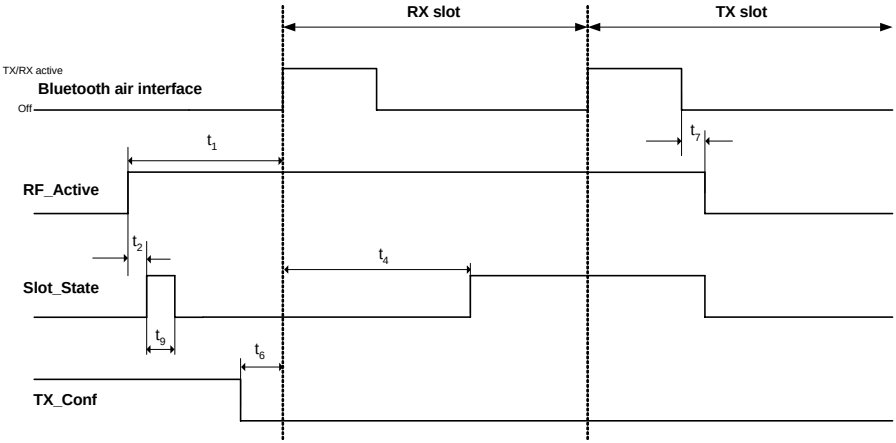


Figure 3-44 High priority transaction, starting with RX
Data type = ACL data

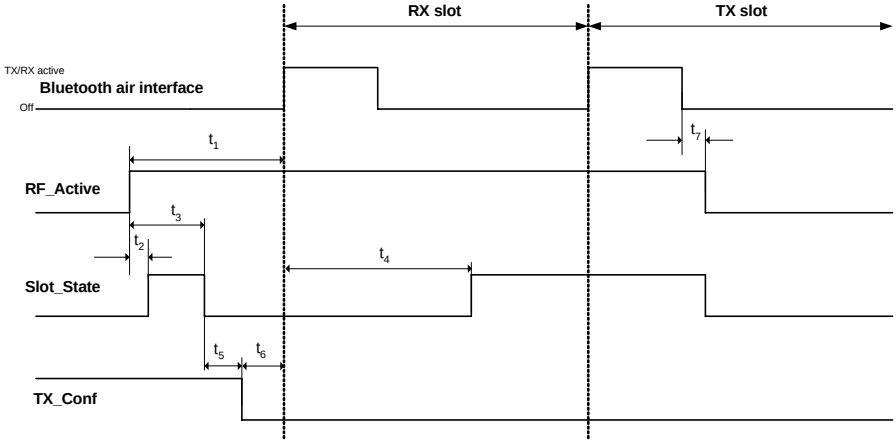


Figure 3-45 High priority transaction, starting with RX
Data type = voice or “connection-related” (poll, sniff etc.)
or
Data type signaling not enabled

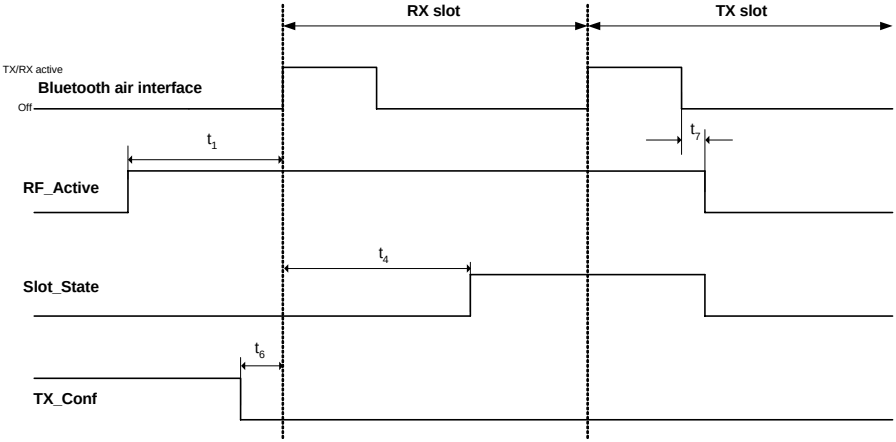


Figure 3-46 Low priority transaction, starting with RX
Data type = ACL data
or
Data type signaling not enabled

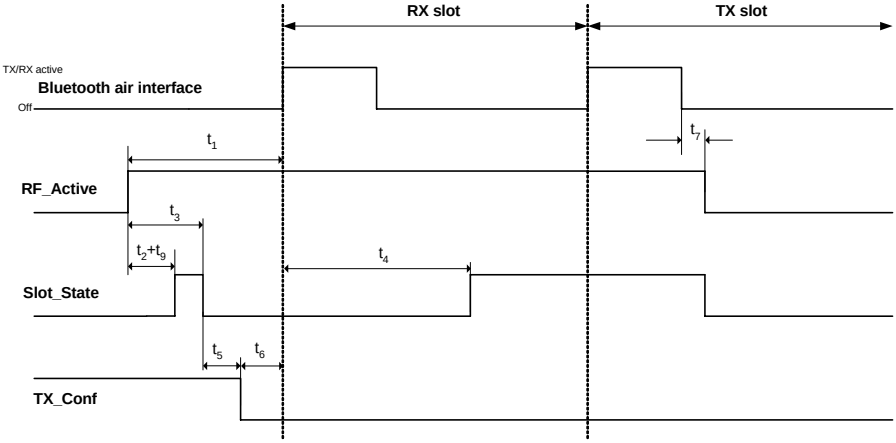


Figure 3-47 Low priority transaction, starting with RX
Data type = voice or “connection-related” (poll, sniff etc.)

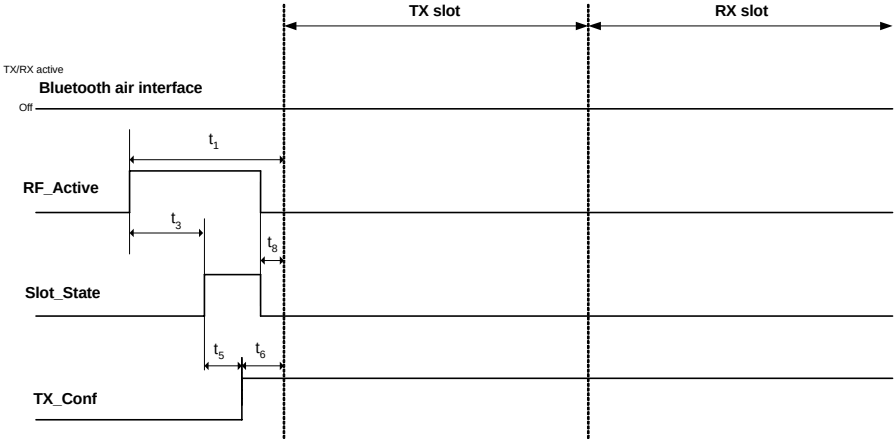


Figure 3-48 Transaction inhibited by TX_Conf before it started

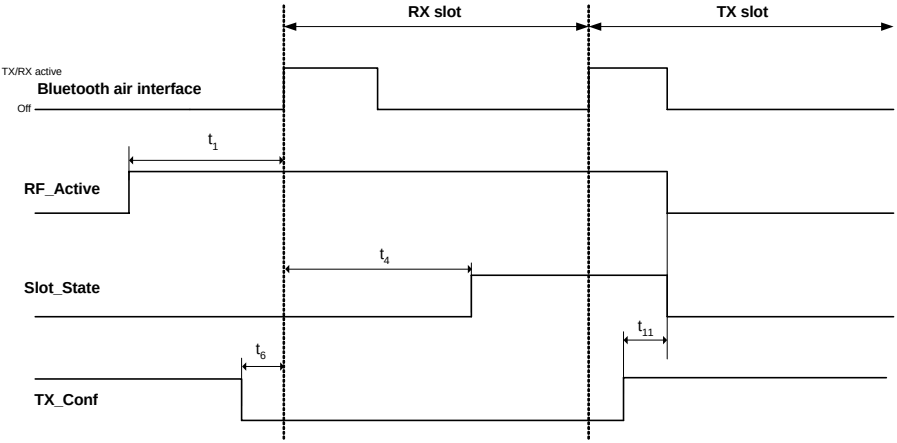


Figure 3-49 Ongoing transaction interrupted by TX_Conf

Table 3-10 WLAN Coexistence Interface Timing

Parameter	Min	Max	Unit
t_1	150	165	µs
t_2	0	2	µs
t_3	15	20	µs
t_4	0	495	µs
t_5	0	80[1)]	µs
t_6	70	-	µs
t_7	0	25	µs
t_8	25	35	µs
t_9	8	10	µs
t_{10}	8	10	µs
t_{11}	0	20	µs
$t_{Rise/Fall}$	0	0.3	µs

1) For reference only, must meet t_6.

3.4 GPIO and Logic Gate Interface

3.4.1 General Purpose I/Os

Most digital pins on BlueMoon UniCellular can be used as general purpose I/Os (GPIOs). The GPIO pins are grouped into two ports: P0 and P1. P0 has 16 pins (P0.0 - P0.15) and P1 has nine pins (P1.0 - P1.8). Information about each pin's placement and capabilities can be found in the pin description in **Section 1.6**.

The host controls and monitors the GPIOs with the following HCI+ commands:

- Infineon_Write_Ports
- Infineon_Read_Ports
- Infineon_Set_Port_Bit
- Infineon_Clear_Port_Bit

It is the responsibility of the host to assure that pins needed for other functionality (e.g. UART and PCM pins) are not configured as GPIOs by mistake. The above commands perform the requested operation without checking pin usage.

Each port is controlled and monitored through a number of hardware registers where each bit corresponds to a port pin (bit 0 corresponds to Px.0, bit 1 to Px.1, etc.). The registers are described in **Table 3-11**.

Table 3-11 GPIO Hardware Registers

Register	Description
Px	Px output. Writes to port pins configured as outputs
PxIN	Px input. Reads from port pins
PxD	Px direction. Sets directions of port pins (0 = input, 1 = output)
PxODC	Px open drain control. Selects normal or open drain operation for port pins (0 = normal, 1 = open drain)
PxIEN	Px input enable. Enables/disables input drivers for port pins (0 = disabled, 1 = enabled)
PxUDEN	Px pull enable. Enables/disables pull resistors for port pins (0 = disabled, 1 = enabled)
PxUDSEL	Px pull select. Selects pull-up or pull-down for port pins (0 = pull-down, 1 = pull-up)
PxALTSEL0	Px alternate output select 0. Selects between GPIO and other output.
PxALTSEL1	Px alternate output select 1. Selects between GPIO and other output.

The ALTSEL registers configure pins for GPIO output or other functionality. To use a port pin as a GPIO both ALTSEL registers must have a zero in the corresponding bit position.

Figure 3-50 shows schematically how a single port pin is affected by the registers. The figure shows a pin with all capabilities. Some pins have limited capabilities as specified in the pin description in **Section 1.6**.

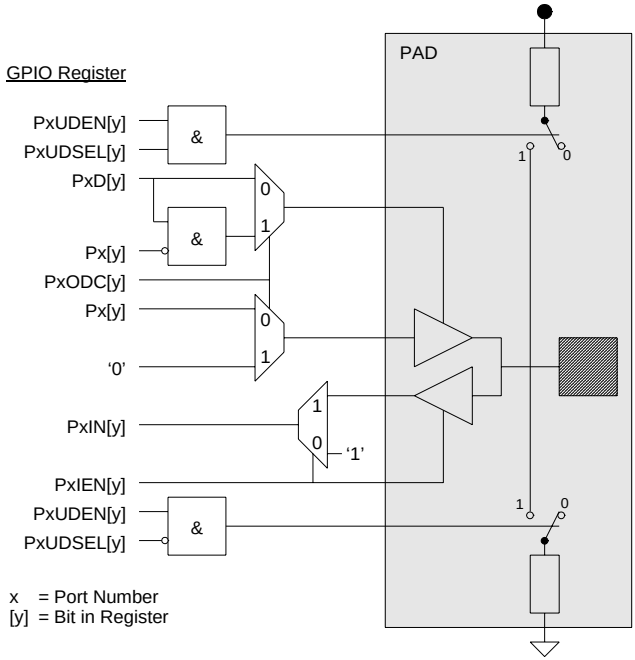


Figure 3-50 Mapping between GPIO Registers and Pad Behaviour for PX.Y

3.4.2 Programmable Logic Gate

BlueMoon UniCellular contains a programmable logic gate that can be used to combine external and internal signals. The gate can perform all possible logic functions with two inputs and is supplied by VDDPM to work even when VDDSUP is not available. The selection of input signals and logic function is done with the following HCI+ commands:

- Infineon_Set_Logic_Gate
- Infineon_Read_Logic_Gate

The possible gate inputs are shown in **Figure 3-51**.

The gate output can be connected to the GATE_OUT pin by setting P1ALTSEL1 bit 6 = 0 and P1ALTSEL0 bit 6 = 1.

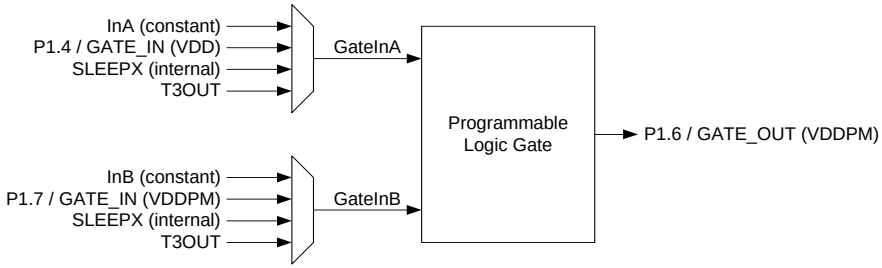


Figure 3-51 Programmable Logic Gate - Input Combinations

3.5 External Power Amplifier Interface

BlueMoon UniCellular has an interface for an optional Class 1 external power amplifier consisting of the following pins:

RFIO/RFIOX

These signals are differential analog RF input/output signals. They might be converted into a single ended signal by using a balun before coming from/fed to the antenna filter or antenna.

RXON

This signal is required to switch the antenna-switch to RX-mode if an optional Class 1 external power amplifier is used. The signal for TX-mode is delivered from the external power amplifier.

PAON

This signal activates the power amplifier if an optional Class1 external power amplifier is used.

PSEL0 and PSEL1

These signals determine the output power if an optional Class1 external power amplifier is used.

TXA/TXAX

These signals are the differential RF output signals. They can be converted into a single ended signal by using a balun before fed into the antenna switch. These signals are required if an optional Class1 external power amplifier is used.

3.6 External EEPROM / I2C Interface

BlueMoon UniCellular supports storage of non-volatile information in an external EEPROM connected to the I2C interface. The EEPROM is divided into two storage areas:

Bluetooth Device Data (BD_DATA) Storage

This area contains information that is vital for the operation of BlueMoon UniCellular. The storage area is accessible in manufacturer mode with the following HCI+ commands:

- Infineon_Write_BD_Data
- Infineon_Write_Ext_EEPROM_Data
- Infineon_Read_Ext_EEPROM_Data

The data is protected by a checksum.

Class Of Device will be stored in non-volatile memory as well. It can be written and read with the following HCI commands:

- HCI_Write_Class_Of_Device
- HCI_Read_Class_Of_Device

Controller Data Storage

This area contains data that is important but not crucial for operation. The link manager can store information here directly but the area can also be accessed with the following HCI commands:

- HCI_Write_Stored_Link_Keys
- HCI_Read_Stored_Link_Keys
- HCI_Delete_Stored_Link_Keys
- HCI_Change_Local_Name

The data in this area is also protected by a checksum.

3.6.1 I2C Hardware

The I2C hardware is compatible with standard I2C interfaces. It supports data rates of up to 400 kbit/s and features both 7-bit and 10-bit addressing. The interface can operate in master mode, slave mode and multi-master mode[1)].

1) Current HCI firmware support is limited to master mode.

4 General Device Capabilities

4.1 HCI+ and Bluetooth Device Data (BD_DATA)

In addition to the standard Bluetooth HCI commands and events, BlueMoon UniCellular supports a set of Infineon specific commands and events called HCI+. All Infineon specific features are accessed using HCI+. The HCI+ commands and events are described in detail in the HCI+ section.

All configuration information that is critical for correct operation of BlueMoon UniCellular is called Bluetooth Device Data (BD_DATA). This data is stored in BlueMoon UniCellular's internal RAM or in non-volatile memory if that is available. BD_DATA can be read and written with the HCI+ commands Infineon_Read_BD_Data and Infineon_Write_BD_Data.

4.2 Manufacturer Mode

HCI+ commands that modify critical information are not available during normal operation. To access these commands the host must first tell BlueMoon UniCellular to enter manufacturer mode with the Infineon_Manufacturer_Mode command.

Commands that are only available in manufacturer mode are marked with (M) in the HCI+ section.

Operations that are only allowed in manufacturer mode are for example:

- Changing the Baud rate with Infineon_Set_UART_Baudrate.
- Switching to the built-in boot loader with Infineon_Switch_To_Loader. The loader is primarily used for firmware evaluation and is not described in this document.
- Accessing Bluetooth Device Data (BD_DATA) with any of the following commands: Infineon_Write_BD_Data, Infineon_Read_BD_Data, Infineon_Write_Ext_EEPROM_Data, Infineon_Read_Ext_EEPROM_Data.
- Accessing internal memory and registers with Infineon_Memory_Write and Infineon_Memory_Read.

It is necessary to leave manufacturer mode before start of normal operation. Leaving manufacturer mode is done with the Infineon_Manufacturer_Mode command.

4.3 Firmware ROM Patching

4.3.1 Patch Support

BlueMoon UniCellular contains dedicated hardware that makes it possible to apply patches to any code and data in the firmware ROM. The hardware is capable of replacing up to 32 blocks of 16 bytes each with new content. In addition to this, an 8 kByte area of

the firmware RAM has been reserved for patches. This area can be filled with any combination of code and data.

Figure 4-1 shows an example where two blocks in firmware ROM have been replaced. The dashed arrow shows that the second block makes use of code and/or data in the dedicated patch RAM area.

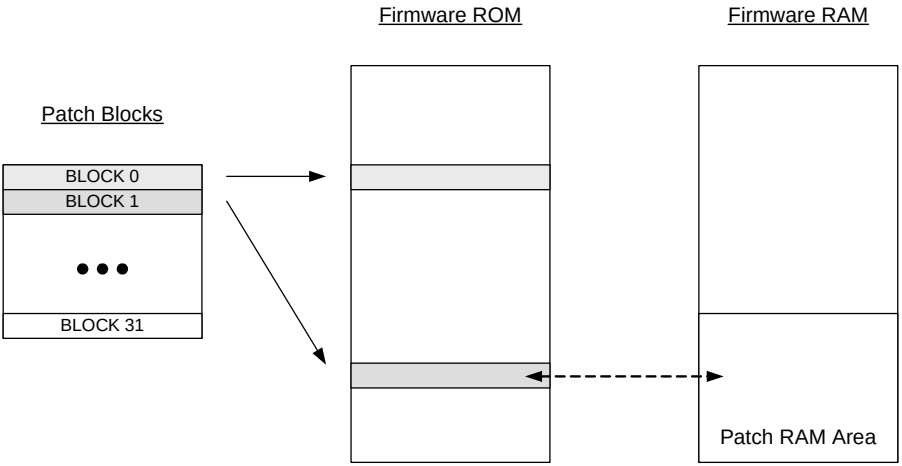


Figure 4-1 Patch Hardware

4.3.2 Downloading Patches

To activate patches on BlueMoon UniCellular, the patch hardware must be configured and code and data must be written to RAM. This can be done in two different ways: via HCI or via the boot loader.

4.3.2.1 Patching via HCI

Patches are downloaded to BlueMoon UniCellular using normal HCI commands. Any supported HCI transport layer may be used. The procedure consists of three steps:

1. Enabling Manufacturer Mode

To get access to the RAM and the patch hardware it is necessary to enable Manufacturer Mode. This is done with the HCI command Infineon_Manufacturer_Mode.

2. Writing to RAM and Patch Hardware

Infineon_Memory_Write is used to initialize the RAM and the patch hardware. Patches should not be enabled/disabled in this step since that may cause unwanted things to

happen, for example if patches modify code or data that is currently in use. Instead, patches should be enabled/disabled as an atomic operation in the next step.

3. Disabling Manufacturer Mode, Enabling/Disabling Patches

Infineon_Manufacturer_Mode is used again to disable manufacturer mode and enable/disable patches. There are three ways to leave manufacturer mode:

Without reset:	Should generally not be used for patching.
With reset, disabling patches:	Should be used to disable patches.
With reset, enabling patches:	Should be used to enable patches.

For safety reasons all patches contain a version ID. This version ID is checked by BlueMoon UniCellular, and must match the version ID in the firmware ROM, before any patches are enabled. If there is a version ID mismatch, the Infineon_Manufacturer_Mode command will fail with the Bluetooth error code “Command Disallowed” (0x0C) and BlueMoon UniCellular will still be in manufacturer mode.

4.3.2.2 Patching via the Loader

If there is a severe error in the firmware that prevents HCI from starting, patches can be downloaded to BlueMoon UniCellular using the built-in boot loader. This is an “emergency mode” and should not be used when HCI is working; therefore it is not described in this document.

4.3.3 Patching from the Host Perspective

Patches are delivered in a binary file that should be downloaded by the host when BlueMoon UniCellular has been powered up. The following sections describe the data format of the patch file and shows with a C code example how the host can download patches and enable them.

4.3.3.1 Data Format

The patch file consists of data blocks that are built up of 32-bit fields. The fields are stored in the file with little-endian byte order (i.e. least significant byte first). The first field in each block, “START ADDRESS”, defines where in the BlueMoon UniCellular memory space the data in that block shall be written. The second field, “SIZE IN BYTES”, specifies how many bytes of data that shall be written. This field shall always specify a multiple of four bytes. The remaining fields contain the data. The last data block contains a single field with the special value 0xFFFFFFFF which means “END OF DATA”. The format is shown in **Figure 4-2**

.

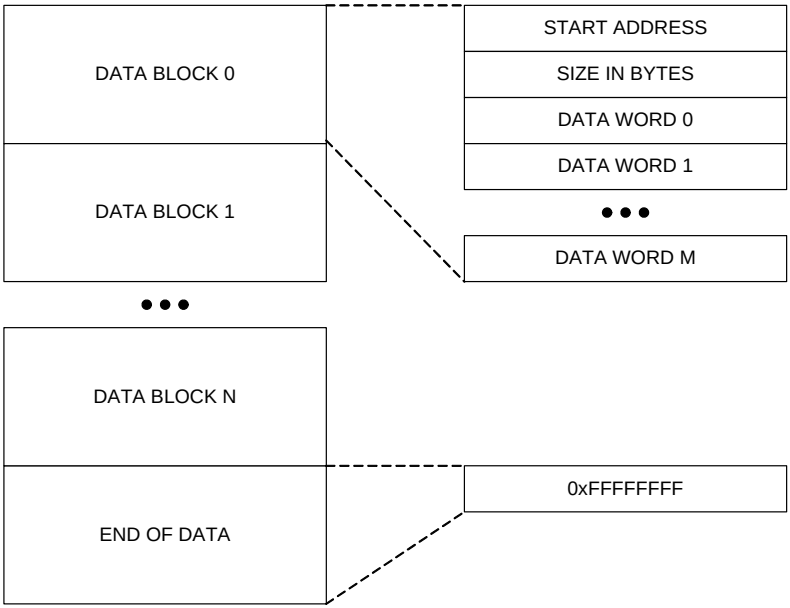


Figure 4-2 Patch File Format

4.3.3.2 Example Host Code

The following C code shows a function that the host can use to write patches to BlueMoon UniCellular, enable them and restart the firmware. The patch file is assumed to be in the format described above.

```
void write_patches()
{
  #define MAX_LEN 244         // Maximum length of HCI data in bytes
  unsigned char buf[MAX_LEN]; // HCI data buffer
  unsigned int addr;          // Start address of current data
  unsigned int len;           // Remaining length of current block
  unsigned int hci_len;       // Length of data in current HCI command
  FILE *f;                    // File handle for patch file

  // Open patch file for binary read
  f = fopen("patch.bin", "rb");

  // Enter manufacturer mode
```

```
  HCI_Infineon_Manufacturer_Mode(MM_ENABLE, MM_NO_RESET);

  // Write patch file to BlueMoon UniCellular
  while ((addr = READ_UINT32(f)) != 0xFFFFFFFF) {
    len = READ_UINT32(f);

    do {
      hci_len = MIN(len, MAX_LEN);
      fread(buf, 1, hci_len, f);

      HCI_Infineon_Memory_Write(addr, MW_WORD, hci_len, buf);

      len  -= hci_len;
      addr += hci_len;
    } while (len);
  };

  // Leave manufacturer mode with reset and enabling of patches
  HCI_Infineon_Manufacturer_Mode(MM_DISABLE, MM_RESET_ENABLE_PATCHES);

  // Close the patch file
  fclose(f);
}
```

4.4 Hardware and Software Version Information

The host can get detailed information about the hardware and software versions of BlueMoon UniCellular using the following HCI+ commands:

Infineon_Read_HW_Version

Infineon_Read_Version

4.5 Advanced Error Reporting

BlueMoon UniCellular has the capability to detect and report various error conditions. The following types of errors can be distinguished:

Fatal Exception: A fatal error has been detected and BlueMoon UniCellular cannot continue normal operation. The device performs a reset and reports the error with an Infineon Fatal Exception event.

Debug Exception: An error has been detected but BlueMoon UniCellular can continue normal operation. The exception is reported with an Infineon Debug Exception event.

Hardware Error: Hardware error conditions are reported with the Hardware Error event that is defined in the Bluetooth specification.

Watchdog Reset: A watchdog timer guarantees that BlueMoon UniCellular is restarted if the firmware stops working for some reason. The condition is reported with a Hardware Error event.

After reception of an Infineon Fatal Exception event or an Infineon Debug Exception event, the exception should be cleared with the Infineon_Clear_Exception_Info command or hardware reset.

The Infineon_Stimulate_Exception command can be used to trigger a fatal exception or a debug exception for test purposes.

5 Bluetooth Capabilities

5.1 Supported Features

BlueMoon UniCellular supports all features in the Bluetooth 2.0 + EDR specification, including:

- Enhanced Data Rate up to 3 Mbit/s
- Adaptive Frequency Hopping (AFH)
- All packet types
- All LMP features
- Authentication, Pairing and Encryption
- Quality of Service
- Channel Quality Driven Data Rate change
- Sniff, Hold and Park
- Role Switch
- RSSI and Power Control
- Power class 1, 2 and 3
- 7 point-to-multipoint connections
- Scatternet with two slave roles while still being visible
- 2 synchronous links (SCO/eSCO)
- A-law, μ-law, CVSD and transparent synchronous data
- Dual SCO/eSCO channels in scatternet

5.2 BlueMoon UniCellular Specifics and Extensions

5.2.1 Configurable LMP Features

BlueMoon UniCellular supports all feature bits that are defined in the Bluetooth 2.0 + EDR specification. The host can disable unwanted LMP features with the BD_DATA parameter *LMP_Features*. The following rules apply:

- A feature is fully supported if the corresponding feature bit is set.
- If a feature bit is not set, the link manager behaves as if the feature was not supported. If the feature is requested by the local host or the remote link manager the request will be denied.
- Depending on the feature bits, BlueMoon UniCellular behaves as a Bluetooth 1.1, 1.2 or 2.0+EDR device. If at least one of the feature bits corresponding to Bluetooth 1.2 (e.g. AFH) is set, BlueMoon UniCellular behaves as a Bluetooth 1.2 device. If at least one of the feature bits corresponding to Bluetooth 2.0+EDR (e.g. 3-slot EDR packets) is set, BlueMoon UniCellular behaves as a Bluetooth 2.0+EDR device.

Some of the feature bits do not follow the general rules:

- **Flow Control Lag:** The flow control lag is a characteristic of the firmware and cannot be configured. The *Flow Control Lag* bits should be set to zero.

- **Enhanced Inquiry Scan:** Enhanced Inquiry Scan is always used whether or not the feature bit is set.

A list of all features can be found in section 3.3 in the Bluetooth 2.0 + EDR specification.

5.2.2 Local Device

5.2.2.1 HCI Command Flow Control

BlueMoon UniCellular is able to buffer two HCI command packets and starts performing the commands in the order in which they are received. Execution of a command can be started before the previous command has been completed. Commands that involve the page procedure (i.e. HCI_Create_Connection and HCI_Remote_Name_Request) cannot be performed at the same time since two page procedures cannot be performed simultaneously; the second command will be delayed until the first has completed.

5.2.2.2 HCI Buffers

BlueMoon UniCellular supports the following number of HCI buffers and buffer sizes (as returned by the HCI_Read_Buffer_Size command):

Type	Number of Buffers	Size of each Buffer
ACL	11	339
SCO/eSCO	14	93

5.2.2.3 Event Filtering

Up to 15 event filters are supported with the HCI command Set_Event_Filter.

5.2.2.4 Local Name

BlueMoon UniCellular can store a local name with a length of 100 bytes (excluding the 0x00 termination character). The local name can be stored in RAM or in non-volatile memory if that is available. The place of storage is configured with the *Local_Name* field in the BD_DATA parameter *BB_Conf*.

5.2.3 Discovery and Connection Establishment

5.2.3.1 Multiple Inquiry Access Codes

BlueMoon UniCellular can scan for up to five inquiry access codes (IACs) during inquiry scan. The number can be read with HCI_Read_Number_Of_Supported_IAC. The IACs

can be read and written with HCI_Read_Current_IAC_LAP and HCI_Write_Current_IAC_LAP.

The IACs will be used cyclically in consecutive scan windows. The number of IACs has no influence on the scan window and scan interval settings. Consequently, the overall scan time for each IAC is proportionally reduced. If interlaced scan is enabled, the same IAC is used for both interlaced scan windows. The IACs provided by the host may be identical to allow prioritization of one IAC over the others.

Figure 5-1 shows the use of multiple IACs.

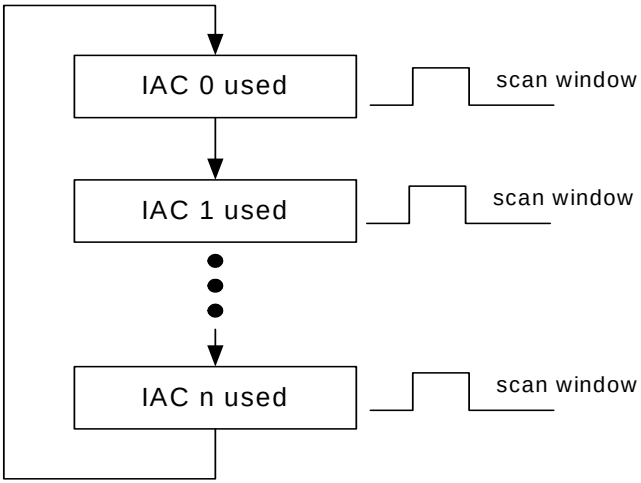


Figure 5-1 Use of Multiple IACs

5.2.3.2 Page and Page Scan

BlueMoon UniCellular supports the mandatory paging scheme, paging modes P0, P1 and P2 and scan repetition modes R0, R1 and R2. The default page scan repetition mode is R1.

5.2.4 During Connection

5.2.4.1 Scatternet and Piconet Capabilities

BlueMoon UniCellular supports point-to-multipoint and scatternet scenarios:

- Up to 7 links
- Up to 2 simultaneous slave roles
- Always capable of responding to inquiry and remote name request

- Always capable of Inquiry

5.2.4.2 Role Switch

Only one role switch can be performed at a time. If a role switch request is pending, other role switch requests on the same or other links are rejected. If a role switch fails, BlueMoon UniCellular will automatically try again a maximum of three times. Encryption (if present) is stopped in the old piconet before a role switch is performed and re-enabled when the role switch has succeeded or failed. If the physical link is in Sniff Mode, Hold Mode or Park State, or has any synchronous logical transports, a role switch will not be performed.

5.2.4.3 Dynamic Polling Strategy

In addition to the regular polling scheme, BlueMoon UniCellular dynamically assigns unused slots to links where data is exchanged. This adapts very well to bursty traffic and improves throughput and latency on the links.

5.2.4.4 Adaptive Frequency Hopping (AFH)

BlueMoon UniCellular supports adaptive frequency hopping according to the Bluetooth 2.0 + EDR specification. AFH switch and channel classification are supported both as master and slave. Channel classification from the host is also supported.

A number of HCI+ commands and events are available to provide information about AFH operation. The commands Infineon_Enable_AFH_Info_Sending and Infineon_Disable_AFH_Info_Sending turn on and off the Infineon AFH Info events that provide detailed information about channel classification, channel maps, interferers, etc.

If enabled by the Infineon_Enable_Infineon_Events command, the Infineon AFH Extraordinary RSSI event informs the host whenever extraordinary RSSI measurements in unused slots have been started. This is done when the number of known good channels has decreased below a critical limit and periodically after a defined time.

The Infineon_Set_AFH_Measurement_Period command can be used to configure the duration of the AFH measurement period.

5.2.4.5 Channel Quality Driven Data Rate Change (CQDDR)

BlueMoon UniCellular supports channel quality driven data rate change according to the Bluetooth 2.0 + EDR specification. A device that receives an LMP_preferred_rate message is not required to follow all recommendations. BlueMoon UniCellular normally at least follows the recommendation whether to use forward error correction (FEC) or not. If possible, recommendations about packet size and modulation scheme will be taken into account. When BlueMoon UniCellular sends an LMP_preferred_rate to another device the proposal always includes preferences for all parameters.

The HCI+ commands Infineon_Enable_CQDDR_Info_Sending and Infineon_Disable_CQDDR_Info_Sending turn on and off sending of the Infineon CQDDR Info event. This event provides information to the host every time a new CQDDR proposal is sent to a remote device.

5.2.4.6 Quality of Service (QoS)

BlueMoon UniCellular supports quality of service according to the Bluetooth 2.0 + EDR specification. It is recommended to use the HCI_Flow_Specification command to set the QoS parameters for both outgoing and incoming traffic. The old HCI_QoS_Setup command can be used to set the QoS parameters for outgoing traffic.

The outgoing QoS parameters Access_Latency/Latency and Token_Rate are used to set the poll interval. The incoming QoS parameter Access_Latency is used to define the maximum reassembly time. (To optimize throughput, BlueMoon UniCellular tries to fill internal buffers before sending received data to the host. If a buffer has not been filled “maximum reassembly time” after a packet has been received, the buffer will be sent to the host anyway.) The default maximum reassembly time is the same as the default poll interval (40 slots).

If both QoS and EDR are enabled in BlueMoon UniCellular and supported by the remote device, BlueMoon UniCellular automatically tries to switch to EDR if the QoS bandwidth requirements are too high to be supported by basic rate. For power saving reasons, the QoS algorithm makes use of EDR packets whenever the RF quality is high enough.

In order to make the QoS algorithm work efficiently the host should always allow all packet types. It may disallow the use of 5-slot packets or restrict the packet types to 1-slot packets completely but should not use other combinations.

5.2.5 Security

5.2.5.1 Authentication

Authentication can be performed at connection creation or during connection.

The repeated attempts algorithm described in section 5.1 in the Bluetooth 2.0 + EDR specification is implemented with the following parameters:

The first waiting interval is 5 seconds. After each subsequent authentication failure the waiting interval is doubled. Every 30 seconds the waiting interval falls back one step. The maximum waiting interval is 40 seconds.

5.2.5.2 Link Key Management

Up to five link keys can be stored with HCI_Write_Stored_Link_Key. The link keys are stored in RAM or non-volatile memory if available.

5.2.5.3 Encryption

Encryption can be enabled at connection creation or during connection if an authentication has been performed. Both point-to-point and broadcast encryption are supported.

When BlueMoon UniCellular is connected to several other devices as master and broadcast encryption is requested, a common encryption key length will be chosen to maximize the number of devices that can be included in the broadcast encryption group. Devices that cannot accept the settings will be disconnected.

The minimum and maximum encryption key sizes accepted by BlueMoon UniCellular can be set and read with the HCI+ commands Infineon_Set_Encryption_Key_Size and Infineon_Read_Encryption_Key_Size.

5.2.5.4 Pairing

The HCI+ command Infineon_Write_Pairing_Mode can be used to set BlueMoon UniCellular in pairable or non-pairable mode.

5.2.6 Synchronous Links

BlueMoon UniCellular supports up to two simultaneous synchronous links (SCO/eSCO).

5.2.6.1 Interface

The interface for synchronous data is either the HCI transport layer or the dedicated PCM/I2S interface. The choice of interface for a synchronous connection is done with the HCI+ command Infineon_Config_Synchronous_Interface and must be done before the connection is established. The default interface is configurable via the bit *Default_SCO_interface* in the BD_DATA parameter *BB_Conf*.

All details about the PCM/I2S interface are described in **Section 3.2**.

5.2.6.2 Voice Coding

Table 5-1 shows the supported values of the Bluetooth parameter Voice_Settings.

Table 5-1 Supported Voice Settings

Parameter	Supported Values
Input Coding	Linear (PCM/I2S only), μ-law, A-law
Input Data Format	2's complement
Input Sample Size	16-bit (only relevant for linear input coding)
Air Coding Format	CVSD, μ-law, A-law, Transparent Data

BlueMoon UniCellular supports transcoding between any combination of linear, μ-law and A-law. If the air coding format is “Transparent Data” and the synchronous interface is the transport layer, the input coding is ignored. If transparent data is sent through the PCM/I2S interface, the input coding determines if 8-bit or 16-bit samples are used. Transparent Data is the only setting for which data rates other than 64 kbit/s can be used.

5.2.6.3 eSCO

Table 5-2 shows the supported parameter ranges for eSCO.

Table 5-2 Supported Parameter Ranges for eSCO

Parameter	Range		
	EV3, 2-EV3, 3-EV3	**EV4**	**EV5, 2-EV5, 3-EV5**
T_{eSCO} (in slots)	2-12 (even)	6-48 (even)	6-72 (even)
D_{eSCO} (in slots)	2-10	2-46	2-70
W_{eSCO} (in slots)	0-10 (even)	0-42 (even)	0-66 (even)
Length of eSCO payload (in bytes)	10-30	30-120	30-180

The maximum data rate that is supported for eSCO is 384 kbit/s.

5.2.6.4 Packet Loss Concealment (PLC)

Packet Loss Concealment can be used to improve voice quality by replacing lost or incorrectly received SCO/eSCO packets. The algorithm creates natural-sounding replacement samples using information from previously received packets in a way that maintains pitch and amplitude variation.

The PLC algorithm can be enabled or disabled for individual voice links with the HCI+ command Infineon_Signal_Proc_Config. For eSCO links it is possible to configure if packets with bit errors shall be treated as lost and replaced or used as is.

The bit *Default_PLC_Mode* in the BD_DATA parameter *BB_Conf* controls if the PLC algorithm is enabled or disabled when a new voice connection is created.

5.2.6.5 Digital Gain Stages

BlueMoon UniCellular can amplify and attenuate the signal in the SCO/eSCO path, both in the air-to-audio and in the audio-to-air direction. Configuration of the digital gain stages are done with the HCI+ command Infineon_Gain_Setting. The gain stages are enabled with the Infineon_Signal_Proc_Config command.

5.2.6.6 Clock Drift Compensation

To smooth the effects of clock drift between the air side and the PCM/I2S or HCI interface, BlueMoon UniCellular has a built-in clock drift compensation algorithm. Samples are inserted and removed in a way that keeps the good voice quality. The algorithm is turned on and off with the HCI+ command Infineon_Signal_Proc_Config.

5.2.7 RSSI and Output Power Control

5.2.7.1 Received Signal Strength Indication (RSSI)

BlueMoon UniCellular supports received signal strength measurements and uses LMP signaling to keep the output power of a remote device within the golden receive power range. The range is set with the BD_DATA parameters *RSSI_Min* and *RSSI_Max*.

5.2.7.2 Output Power Control

BlueMoon UniCellular supports power control according to the Bluetooth 2.0 + EDR specification.

- The output power can be controlled in 4 steps when an external power amplifier is present.
- The output power can be controlled in 3 or 4 steps (configurable) with internal power settings. In this case no power amplifier is present; therefore BlueMoon UniCellular can work as a class 1, 2 or 3 device depending on the settings.
- Fine tuning can be used on the power steps.

The following BD_DATA parameters are used for configuration:
RF_Psel_D, RF_Psel_Conf, RF_Conf, TX_Power_Ref#.

5.2.7.3 Ultra Low Transmit Power

For high security devices the output power can be reduced to a value that reduces the communication range to a few inches. This mode is enabled with the HCI+ command Infineon_TX_Power_Config.

5.2.8 Test Modes

5.2.8.1 Active Tester Mode

BlueMoon UniCellular can act as a Bluetooth RF tester running the Bluetooth test mode. All defined test mode scenarios can be configured and initiated with the HCI+ command Infineon_Active_Tester. Detailed information about the active tester mode is available in the HCI+ specification.

5.2.8.2 RF Test Modes

RF transmitter and receiver measurements can be done in the following test modes:

- TX burst mode
- RX burst mode
- RX burst mode with data transparently sent to host
- RX bit & packet error rate measurement mode

The modes are configured with the HCI+ command Infineon_Test_Mode. Detailed information about the modes is available in the HCI+ specification.

5.2.8.3 EDR Packet Test Command

The HCI+ command Infineon_Test_EDR_Packets can be used to force BlueMoon UniCellular to use enhanced data rate or basic rate. This will be done without LMP negotiation and should only be used for testing.

5.2.9 Debugging

5.2.9.1 LMP Tracing and Sending

An LMP trace mode makes it possible to trace the LMP traffic between BlueMoon UniCellular and other devices without an external protocol analyzer. The LMP PDUs that are sent and received are sent to the host with the Infineon LMP PDU Trace event. The trace events are activated with the Infineon_Activate_Deactivate_Traces command.

It is also possible to send an LMP PDU to another device. This is done with the HCI+ command Infineon_Send_LMP.

5.2.9.2 Error Events

The following Infineon specific error events exist:

Event	Description
Infineon Invalid ACL_BC_PB Flag	Indicates that BlueMoon UniCellular has received an HCI packet with invalid BC or PB flag from the host.
Infineon Invalid ACL_CNC_Handle	Indicates that BlueMoon UniCellular has received an ACL HCI packet with invalid connection handle from the host.
Infineon Invalid SCO_CNC_Handle	Indicates that BlueMoon UniCellular has received a SCO/eSCO HCI packet with invalid connection handle from the host.

5.2.9.3 Information Events

With the HCI+ command Infineon_Enable_Infineon_Events it is possible to enable and disable the following information events:

Event	Description
Infineon SCO Rejected Via LMP	Indicates that the link manager has rejected a request for a SCO/eSCO link
Infineon PTT Switch Notification	Indicates that the packet type table (PTT) has been switched.
Infineon Scan Status	Indicates that the link manager has temporarily changed the scan settings provided by the host.
Infineon Debug Exception	Indicates an internal problem in BlueMoon UniCellular.

6 Infineon-specific HCI Extensions (HCI+)

This chapter lists the Infineon-specific HCI commands and events.

A command that is marked with (M) can be used in manufacturer mode only.

6.1 Infineon-specific HCI Commands

The OGF of all Infineon-specific HCI commands is 0x3F. The structure is shown in **Figure 6-1**.

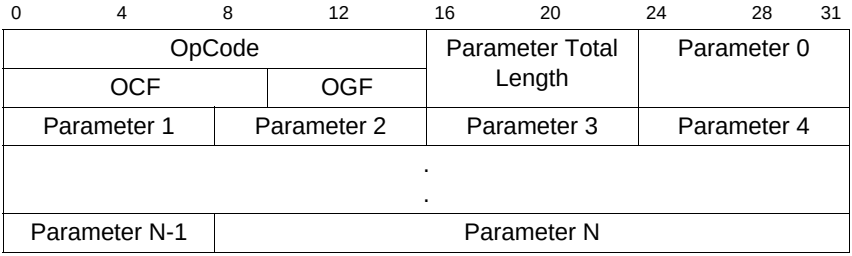


Figure 6-1 Structure of Infineon-specific HCI Commands

The Infineon-specific commands are ordered based on their functionality (interface configuration, system management, extended Bluetooth features and testing). Some commands are only accepted by the Bluetooth controller if the Infineon Manufacturer Mode is switched on. These commands are marked as Manufacturer Mode commands (M). The Manufacturer Mode is a protected mode (see **Section 6.1.3.6** for details).

6.1.1 Table of Infineon-specific Commands

Table 6-1 gives an overview of the Infineon-specific HCI commands described in **Section 6.1.2** - **Section 6.1.5**.

Table 6-1 Infineon-specific HCI Commands

OCF	Command
0x0001	**“Infineon_Switch_To_Loader (M)” on Page 135**
0x0003	**“Infineon_Read_PCM_Mode” on Page 106**
0x0004	**“Infineon_Write_PCM_Mode” on Page 103**
0x0005	**“Infineon_Read_Version” on Page 116**
0x0006	**“Infineon_Set_UART_Baudrate (M)” on Page 123**
0x0007	**“Infineon_Enable_LPM” on Page 118**

OCF	Command
0x000B	“Infineon_Host_LPM_Start” on Page 119
0x000C	“Infineon_Host_LPM_End” on Page 120
0x0011	“Infineon_Manufacturer_Mode” on Page 121
0x0012	“Infineon_Read_Link_Quality” on Page 122
0x0013	“Infineon_Write_Ports” on Page 107
0x0014	“Infineon_Read_Ports” on Page 109
0x0015	“Infineon_Set_Port_Bit” on Page 110
0x0016	“Infineon_Clear_Port_Bit” on Page 111
0x0017	“Infineon_Read_Encryption_Key_Size” on Page 140
0x0019	“Infineon_Set_Encryption_Key_Size (M)” on Page 139
0x001A	“Infineon_Test_Mode (M)” on Page 169
0x001B	“Infineon_Enable_Infineon_Events (M)” on Page 141
0x001C	“Infineon_Enable_PCM_Loopback” on Page 178
0x0022	“Infineon_Get_Exception_Info (M)” on Page 151
0x0024	“Infineon_Clear_Exception_Info (M)” on Page 152
0x0025	“Infineon_Send_LMP (M)” on Page 181
0x0029	“Infineon_Set_Logic_Gate” on Page 153
0x002A	“Infineon_Read_Logic_Gate” on Page 155
0x002C	“Infineon_Signal_Proc_Config” on Page 145
0x002E	“Infineon_Gain_Setting” on Page 148
0x002F	“Infineon_Write_BD_Data (M)” on Page 125
0x0030	“Infineon_Read_BD_Data (M)” on Page 134
0x0035	“Infineon_TX_Power_Config” on Page 160
0x0039	“Infineon_Config_Synchronous_Interface” on Page 101
0x003A	“Infineon_Coexistence_Enable” on Page 113
0x003D	“Infineon_Coexistence_Set_Link_Prio” on Page 114
0x0043	“Infineon_Activate_Deactivate_Traces (M)” on Page 173
0x0044	“Infineon_Burstcomposer_Config” on Page 167
0x0045	“Infineon_Active_Tester (M)” on Page 175
0x0046	“Infineon_Enable_AFH_Info_Sending” on Page 161
0x0047	“Infineon_Disable_AFH_Info_Sending” on Page 163

OCF	Command
0x0048	“Infineon_Enable_CQDDR_Info_Sending” on Page 165
0x0049	“Infineon_Disable_CQDDR_Info_Sending” on Page 166
0x004A	“Infineon_Set_AFH_Measurement_Period (M)” on Page 164
0x004C	“Infineon_Write_Pairing_Mode” on Page 166
0x004D	“Infineon_Stimulate_Exception (M)” on Page 182
0x0050	“Infineon_Read_HW_Version” on Page 115
0x0089	“Infineon_Write_Ext_EEPROM_Data (M)” on Page 136
0x008A	“Infineon_Read_Ext_EEPROM_Data (M)” on Page 137
0x008D	“Infineon_Memory_Read (M)” on Page 142
0x008E	“Infineon_Memory_Write (M)” on Page 144
0x008F	“Infineon_Raw_Write_Ext_EEPROM (M)” on Page 156
0x0090	“Infineon_Raw_Read_Ext_EEPROM (M)” on Page 157
0x0091	“Infineon_Auto_Calibrate_Crystal (M)” on Page 158

6.1.2 HCI+ Interface Configuration Commands

6.1.2.1 Infineon_Config_Synchronous_Interface

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Config_Synchronous_Interface	0x3F	0x0039	Connection_Handle, Synchronous_Interface	Status

Description:

Infineon_Config_Synchronous_Interface is used to select the interface for the next synchronous connection. The default synchronous interface is the either the transport layer (UART) or the PCM interface depending on the value of the bit Default_SCO_interface in the BD_Data parameter BB_Conf.

The synchronous interface can be changed prior to establishing an eSCO/SCO link. The **Infineon_Config_Synchronous_Interface** command can be sent either before the synchronous setup procedure begins or after a connection request for an eSCO/SCO link has been sent to the host. The selected interface is only valid for the next eSCO/

SCO connection and is set to default afterwards (even in case the connection establishment failed).

Note: It is not possible to change the interface for a running eSCO/SCO connection.

Command Parameters:

Connection_Handle: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0x0EFF	ACL Connection handle

Synchronous_Interface: *Size: 1 Octet*

Value	Parameter Description
0x00	Reserved
0x01	Synchronous interface for the connection is PCM channel 1
0x02	Synchronous interface for the connection is PCM channel 2
0x04	Synchronous interface for the connection is HCI Transport

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Config_Synchronous_Interface command succeeded
0x01 - 0xFF	Infineon_Config_Synchronous_Interface command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Config_Synchronous_Interface command has completed execution, a Command Complete event will be generated.

6.1.2.2 Infineon_Write_PCM_Mode

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Write_PCM_Mode	0x3F	0x0004	PCM_Mode, Frame_Length, Frame_Signal_Length, Channel_Pos, LPM_Level	Status

Description:

This command will set the modes of the PCM Interface. The sample rate of the PCM Interface is fixed to 8 kHz where different numbers of bits per frame can be programmed in the parameter *PCM_Mode*.

The data word length is determined from the parameter *Voice_Setting* in the HCI_Write_Voice_Setting, the HCI_Setup_Synchronous_Connection or the HCI_Accept_Synchronous_Connection command.

Note: This command is not allowed while an eSCO/SCO connection, configured to use the PCM interface, is present.

Command Parameters:

PCM_Mode: *Size: 2 Octets*

Value (bits)	Parameter Description
XXXXXXXX XXXXXXX0 MSB LSB	Clock master mode (PCMCLK generated by the controller) (default)
XXXXXXXX XXXXXXX1	Clock slave mode (PCMCLK supplied externally)
XXXXXXXX XXXXXX0X	Frame master mode (PCMFR1 generated by the controller) (default)
XXXXXXXX XXXXXX1X	Frame slave mode (PCMFR1 supplied externally)
XXXXXXXX XXXXX0XX	Frame Signal is MSB justified (default)
XXXXXXXX XXXXX1XX	Frame Signal is LSB justified
XXXXXXXX XXX0XXXX	PCMCLK is not inverted (default)
XXXXXXXX XXX1XXXX	PCMCLK is inverted
XXXXXXXX XX1X0XXX	Idle level on PCMOUT is high
XXXXXXXX XX0X0XXX	Idle level on PCMOUT is low (default)
XXXXXXXX XX1X1XXX	Idle level on PCMOUT is tristate

Value (bits)	Parameter Description
XXXXXXXX XX0X1XXX	Idle level on PCMOUT is tristate
XXXXXXXX X0XXXXXX	Single clock mode enabled (default)
XXXXXXXX X1XXXXXX	Double clock mode enabled (two clock cycles per data bit)
XXXXXXXX 0XXXXXXX	Reserved
XXXXXXXX 1XXXXXXX	Reserved
XXXXXX00 XXXXXXXX	Normal frame signal mode (default)
XXXXXX01 XXXXXXXX	Early frame signal mode
XXXXXX10 XXXXXXXX	Reserved
XXXXXX11 XXXXXXXX	Reserved
XXXXX0XX XXXXXXXX	PCMFR1 is not inverted (default)
XXXXX1XX XXXXXXXX	PCMFR1 is inverted
XXXX0XXX XXXXXXXX	PCMFR2 is not inverted (default)
XXXX1XXX XXXXXXXX	PCMFR2 is inverted
XX00XXXX XXXXXXXX	Reserved
XX01XXXX XXXXXXXX	Number of used frame signals = 1 (default)
XX10XXXX XXXXXXXX	Number of used frame signals = 2
XX11XXXX XXXXXXXX	Reserved

Frame_Length: *Size: 1 Octet*

Value	Parameter Description
0x10-0xFF	Formula: $\text{Framelength} = \frac{\text{PCMCLK}}{8}$ Where frame length is in bits and PCMCLK in kHz. Examples for different PCM clocks are shown below.
0x10	Frame length is 16 bits => PCMCLK = 128kHz Number of PCM channels: 1
0x20	Frame length is 32 bits (I2S Mode) => PCMCLK = 256kHz Number of active PCM channels: 1 or 2
0xFA	Frame length is 250 bits => PCMCLK = 2MHz Number of PCM channels: 1 or 2

Frame_Signal_Length: *Size: 1 Octet*

Value (bits)	Parameter Description
0x01 - *Frame_ Length (max 0x3F)*	Length of PCMFRx in clock cycles (in multiples of two clock cycles if double clock mode is used)

Channel_Pos: *Size: 3 Octets*

Value	Parameter Description
Octet 1: 0x00 - 0xFF	Channel start position for channel 1
Octet 2: 0x00 - 0xFF	Channel start position for channel 2
Octet 3: 0x00 - 0xFF	Reserved

LPM_Level: *Size: 2 Octets*

Value (bits)	Parameter Description
XXXXXXXX XXXXXX00 MSB LSB	PCMOUT is pulled low when in LPM (default)
XXXXXXXX XXXXXX01	PCMOUT is pulled high when in LPM
XXXXXXXX XXXXXX10	PCMOUT is tristate when in LPM
XXXXXXXX XXXX00XX	PCMIN is pulled low when in LPM
XXXXXXXX XXXX01XX	PCMIN is pulled high when in LPM
XXXXXXXX XXXX10XX	PCMIN is tristate when in LPM (default)
XXXXXXXX XX00XXXX	PCMCLK is pulled low when in LPM (default)
XXXXXXXX XX01XXXX	PCMCLK is pulled high when in LPM
XXXXXXXX XX10XXXX	PCMCLK is tristate when in LPM
XXXXXXXX 00XXXXXX	PCMFR1 is pulled low when in LPM (default)
XXXXXXXX 01XXXXXX	PCMFR1 is pulled high when in LPM
XXXXXXXX 10XXXXXX	PCMFR1 is tristate when in LPM
XXXXXX00 XXXXXXXX	Reserved
XXXXXX01 XXXXXXXX	PCMFR2 is pulled high when in LPM (default)
XXXXXX10 XXXXXXXX	PCMFR2 is tristate when in LPM

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Write_PCM_Mode command succeeded
0x01 - 0xFF	Infineon_Write_PCM_Mode command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Write_PCM_Mode command has completed execution, a Command Complete event will be generated

6.1.2.3 Infineon_Read_PCM_Mode

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Read_PCM_Mode	0x3F	0x0003		Status, PCM_Mode, Frame_Length, Frame_Signal_Length, Channel_Pos, LPM_Level

Description:

This command will read the modes of the PCM Interface.

Command Parameters:

None.

Return Parameters:

Status: *Size:1 Octet*

Value	Parameter Description
0x00	Read_PCM_Mode command succeeded
0x01 - 0xFF	Read_PCM_Mode command failed. See list of error codes in Bluetooth specification

PCM_Mode: *Size: 2 Octets*

Value	Parameter Description
	see **“Infineon_Write_PCM_Mode” on Page 103**

Frame_Length: *Size: 1 Octet*

Value	Parameter Description
	see **“Infineon_Write_PCM_Mode” on Page 103**

Frame_Signal_Length: *Size: 1 Octet*

Value	Parameter Description
	see **“Infineon_Write_PCM_Mode” on Page 103**

Channel_Pos: *Size: 3 Octets*

Value	Parameter Description
	see **“Infineon_Write_PCM_Mode” on Page 103**

LPM_Level: *Size: 2 Octets*

Value	Parameter Description
	see **“Infineon_Write_PCM_Mode” on Page 103**

Event(s) generated (unless masked away):

When the HCI_Infineon_Read_PCM_Mode command has completed execution, a Command Complete event will be generated.

6.1.2.4 Infineon_Write_Ports

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Write_Ports	0x3F	0x0013	Port, Register, Register_Value	Status

Description:

This command writes to a GPIO port register. The parameter *Port* corresponds to the port number and the parameter *Register* corresponds to a register of the port. *Register_Value* is the 32-bit value that will be written to the register.

Note: Infineon_Write_Ports can be used to reconfigure ports already being used by the system. Therefore it is of utmost importance to understand how the device is affected when using this command. If not used carefully the device can be rendered useless and will need a hardware reset to return to normal operation.

Command Parameters:

Port: *Size: 1 Octet*

Value	Parameter Description
0x00	P0
0x01	P1
0x02-0xFF	Reserved

Register: *Size: 1 Octet*

Value	Parameter Description
0x00	Px output. Writes to port pins configured as outputs.
0x01	Px input. Reads from port pins. (Cannot be written.)
0x02	Px direction. Sets the directions of the port pins. (0 = input, 1 = output)
0x03	Px open drain control. Selects normal or open drain operation. (0 = normal, 1 = open drain)
0x04	Px input enable. Enables/disables input drivers for specified pins. (0 = disabled, 1 = enabled)
0x05	Px pull enable. Enables/disables pull resistors for specified pins. (0 = disabled, 1 = enabled)
0x06	Px pull select. Selects pull-up or pull-down. (0 = pull-down, 1 = pull-up)
0x07	Px alternate output select 0. Selects between GPIO and other output. Set to 0 for GPIO.
0x08	Px alternate output select 1. Selects between GPIO and other output. Set to 0 for GPIO.
0x09 - 0xFF	Reserved

Register_Value: *Size: 4 Octets*

Value	Parameter Description
0xXXXXXXXX	Value that will be written into register *Register* of port *Port.*

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Write_Ports command succeeded
0x01 - 0xFF	Infineon_Write_Ports command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Write_Ports command has completed execution, a Command Complete event will be generated.

6.1.2.5 Infineon_Read_Ports

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Read_Ports	0x3F	0x0014	Port, Register	Status, Register_Value

Description:

This command reads from a GPIO port register. The parameter *Port* corresponds to the port number and the parameter *Register* corresponds to a register of the port. *Register_Value* is the 32-bit content that will be read from the register.

Command Parameters:

Port: *Size: 1 Octet*

Value	Parameter Description
0x00	P0
0x01	P1
0x02-0xFF	Reserved

Register: *Size: 1 Octet*

Value	Parameter Description
0xXX	See **“Infineon_Set_Logic_Gate” on Page 153**.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Read_Ports command succeeded.
0x01 - 0xFF	Infineon_Read_Ports command failed. See list of error codes in Bluetooth specification

Register_Value: *Size: 4 Octets*

Value	Parameter Description
0xXXXXXXXX	Content of register *Register* of port *Port.*

Event(s) generated (unless masked away):

When the HCI_Infineon_Read_Ports command has completed execution, a Command Complete event will be generated.

6.1.2.6 Infineon_Set_Port_Bit

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Set_Port_Bit	0x3F	0x0015	Port, Register, Bit_Mask	Status

Description:

This command sets individual bits of a GPIO port register. The parameter *Port* corresponds to the port number. The parameter *Register* corresponds to a register of the port. Desired bits are selected with *Bit_Mask*.

Command Parameters:

Port: *Size: 1 Octet*

Value	Parameter Description
0x00	P0
0x01	P1
0x02-0xFF	Reserved

Register: *Size: 1 Octet*

Value	Parameter Description
0xXX	See **"Infineon_Set_Logic_Gate" on Page 153**.

Bit_Mask: *Size: 4 Octets*

Value	Parameter Description
XX..0..XX (32 bits)	Bit x of register *Register* of port *Port* is not set.
XX..1..XX (32 bits)	Bit x of register *Register* of port *Port* is set.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Set_Port_Bit command succeeded
0x01 - 0xFF	Infineon_Set_Port_Bit command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Set_Port_Bit command has completed execution, a Command Complete event will be generated.

6.1.2.7 Infineon_Clear_Port_Bit

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Clear_Port_Bit	0x3F	0x0016	Port, Register, Bit_Mask	Status

Description:

This command clears individual bits of a GPIO port register. The parameter *Port* corresponds to the port number. The parameter *Register* corresponds to a register of the port. Desired bits are selected with *Bit_Mask*.

Command Parameters:

Port: *Size: 1 Octet*

Value	Parameter Description
0x00	P0
0x01	P1
0x02-0xFF	Reserved

Register: *Size: 1 Octet*

Value	Parameter Description
0xXX	See **“Infineon_Set_Logic_Gate” on Page 153**.

Bit_Mask: *Size: 4 Octets*

Value	Parameter Description
XX..0..XX (32 bits)	Bit x of register *Register* of port *Port* is not cleared
XX..1..XX (32 bits)	Bit x of register *Register* of port *Port* is cleared

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Clear_Port_Bit command succeeded
0x01 - 0xFF	Infineon_Clear_Port_Bit command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Clear_Port_Bit command has completed execution, a Command Complete event will be generated.

6.1.2.8 Infineon_Coexistence_Enable

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Coexistence_Enable	0x3F	0x003A	Coex_Mode	Status

Description:

This command shall be used by the host to enable or disable WLAN coexistence functions in the controller. When enabling coexistence functions, the host shall also indicate which mode of operation that is to be enabled.
This command can be issued at any time.

Command Parameters:

Coex_Mode: *Size: 1 Octet*

Value	Parameter Description
0x00	Coexistence is disabled (default)
0x11	Simplified three-wire coexistence interface enabled
0x12	Standard three-wire coexistence interface enabled
0x13	Standard three-wire coexistence interface with data type signaling enabled

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Coexistence_Enable command succeeded
0x01 - 0xFF	Infineon_Coexistence_Enable command failed. See list of error codes in Bluetooth specification

Events generated (unless masked):

When the HCI_Infineon_Coexistence_Enable command has completed execution, a Command Complete event will be generated.

6.1.2.9 Infineon_Coexistence_Set_Link_Prio

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Coexistence_ Set_Link_Prio	0x3F	0x003D	Connection_ Handle, Coex_ Prio	Status

Description:

This command can be used by the host to configure the coexistence priority of data packets on an ACL link. Packets which have a fixed high priority are not affected by this command.
The link priority is kept over a master / slave role switch, and it is also kept if the link is put into park.
The command can not be used on a link that is in the park state.
The command can be issued at any time when the coexistence interface is enabled.

Command Parameters:

Connection_Handle: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0x0EFF	Connection Handle identifies the connection for which the coexistence priority is set. The connection handle must be a connection handle for an ACL connection.

Coex_Prio: *Size: 1 Octet*

Value	Parameter Description
0x00	Normal priority (default) Data packets on the link have low priority
0x01	High priority Data packets on the link have high priority

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Coexistence_Set_Link_Prio command succeeded
0x01 - 0xFF	Infineon_Coexistence_Set_Link_Prio command failed. See list of error codes in Bluetooth specification

Events generated (unless masked):

When the HCI_Infineon_Coexistence_Set_Link_Prio command has completed execution, a Command Complete event will be generated.

If the command is used on a link that is in park state, “Command Disallowed” will be returned.

6.1.3 HCI+ System Management Commands

6.1.3.1 Infineon_Read_HW_Version

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Read_HW_Version	0x3F	0x0050		HW-Variant, HW-Revision,

Description:

This command will read the hardware version the controller.

Command Parameters:

None.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Read_HW_Version command succeeded
0x01 - 0xFF	Infineon_Read_HW_Version command failed. See list of error codes in Bluetooth specification

HW-Variant: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Hardware Variant 0x03: BlueMoon UniCellular

HW-Revision: *Size: 1 Octet*

Value	Parameter Description
0x01 - 0xFF	Hardware Revision. This parameter keeps the hardware revision number. The first revision is 0x01.

Event(s) generated (unless masked away):

When the HCI_Infineon_Read_HW_Version command has completed execution, a Command Complete event will be generated reporting the versions.

6.1.3.2 Infineon_Read_Version

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Read_Version	0x3F	0x0005		Status, HW-Platform, HW-Variant, HW-Revision, FW-Variant, FW-Revision, FW-Build FW-Patch

Description:

This command will read both the hardware and firmware versions of the controller.

Command Parameters:

None.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Read_Version command succeeded
0x01 - 0xFF	Infineon_Read_Version command failed. See list of error codes in Bluetooth specification

HW-Platform: *Size: 1 Octet*

Value	Parameter Description
0x37	Hardware Platform Number. This value is fixed to 0x37.

HW-Variant: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Hardware Variant 0x03: BlueMoon UniCellular

HW-Revision: *Size: 1 Octet*

Value	Parameter Description
0x01 - 0xXY	Hardware Revision. This parameter keeps the hardware revision number. X: Revision Number Y: Subrevision Number

FW-Variant: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Firmware Variant: 0x01: BlueMoon UniCellular 0x02-0x0F: Reserved 0x10: BlueMoon Embedded HID/RFCOMM 0x11-0x1F: Reserved

FW-Revision: *Size: 1 Octet*

Value	Parameter Description
0x01 - 0xXY	Firmware Revision. This parameter keeps the firmware revision number. X: Revision Number Y: Subrevision Number

FW-Build: *Size: 3 Octets*

Value	Parameter Description
0xYMDDNN	Firmware Build Number Y: Year (0x0 = 2000, ..., 0xF = 2015) M: Month (0x0 = Jan, ..., 0xC = Dec) DD: Day NN: Build number of date YM-DD

FW-Patch: *Size: 1 Octet*

Value	Parameter Description
0xPP	Firmware Patch Number PP: Patch number

Event(s) generated (unless masked away):

When the HCI_Infineon_Read_Version command has completed execution, a Command Complete event will be generated reporting the versions.

6.1.3.3 Infineon_Enable_LPM

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Enable_LPM	0x3F	0x0007	OnOff	Status

Description:

This command is used to enable and disable autonomous use of low power modes. If low power modes are enabled, the controller will enter low power mode (LPM) or ultra low power mode (ULPM) during long periods of inactivity. The BD_Data parameters LPM_Threshold and ULPM_Threshold specify the length of inactivity that is required to enter LPM and ULPM respectively.

If the Auto_Disable_LPM bit is set in the BD_Data parameter LPM_Conf, low power modes are automatically disabled after a host initiated wake-up and must be re-enabled with this command.

BD_Data parameters are set with **Infineon_Write_BD_Data (M)**.

Command Parameters:

OnOff: *Size: 1 Octet*

Value	Parameter Description
0x00	Low-Power Mode (LPM) is disabled (default)
0x01	Low-Power Mode (LPM) is enabled

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Enable_LPM command succeeded
0x01 - 0xFF	Infineon_Enable_LPM command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Enable_LPM command has completed execution, a Command Complete event will be generated.

6.1.3.4 Infineon_Host_LPM_Start

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Host_LPM_Start	0x3F	0x000B		Status

Description:

This command is only allowed when the HCI UART-6W transport layer is used and the Host_LPM bit in the BD_Data parameter LPM_Conf is activated. The command is used by the host to tell the controller that it will enter the “unknown” state.

Command Parameters:

None.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Host_LPM_Start command succeeded
0x01 - 0xFF	Infineon_Host_LPM_Start command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Host_LPM_Start command has completed execution, a Command Complete event will be generated.

6.1.3.5 Infineon_Host_LPM_End

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Host_LPM_End	0x3F	0x000C		Status

Description:

This command is only allowed when the HCI UART-6W transport layer is used and the Host_LPM bit in the BD_Data parameter LPM_Conf is activated. The command is used by the host to tell the controller that it has woken up from low power mode.

Command Parameters:

None.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Host_LPM_End command succeeded
0x01 - 0xFF	Infineon_Host_LPM_End command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Host_LPM_End LPM command has completed execution, a Command Complete event will be generated.

6.1.3.6 Infineon_Manufacturer_Mode

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Manufacturer_ Mode	0x3F	0x0011	Mode_Switch, Reset	Status

Description:

This command enables or disables Infineon manufacturer mode.

When manufacturer mode is disabled (default), commands that modify device critical parameters are disabled to prevent unintentional changes. These commands are marked with (M) in this specification.

When manufacturer mode is enabled all commands marked wih (M) are enabled. Most other commands are disabled.

In Manufacturer Mode, best possible performance of the controller cannot be guaranteed.

Command Parameters:

Mode_Switch: *Size: 1 Octet*

Value	Parameter Description
0x00	Manufacturer mode is disabled
0x01	Manufacturer mode is enabled

Reset: *Size: 1 Octet*

Value	Parameter Description
0x00	No reset is done when leaving Manufacturer Mode (only valid if Mode_Switch = 0x00)
0x01	A reset is done when leaving Manufacturer Mode and available firmware patches (if any) are erased (only valid if Mode_Switch = 0x00)
0x02	A reset is done when leaving Manufacturer Mode and available firmware patches are applied and activated (only valid if Mode_ Switch = 0x00).

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Manufacturer_Mode command succeeded
0x01 - 0xFF	Infineon_Manufacturer_Mode command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Manufacturer_Mode command has completed execution, a Command Complete event will be generated.

6.1.3.7 Infineon_Read_Link_Quality

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Read_Link_Quality	0x3F	0x0012	Connection_Handle	Status, Connection_Handle, Link_Quality

Description:

The Link_Quality value can be read per connection handle with this command.

Command Parameters:

Connection_Handle: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0x0EFF	Connection Handle identifies the connection for which the Link_Quality value is read. The connection handle must be a connection handle for an ACL connection.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Link_Quality value successfully read.
0x01 - 0xFF	Link_Quality measurement failed. See list of error codes in Bluetooth specification

Connection_Handle: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0x0EFF	Connection Handle identifies the connection for which the Link_ Quality value was read.

Link_Quality: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Link Quality (signal in relation to noise) in dB (signed integer)

Event(s) generated (unless masked away):

When the HCI_Infineon_Read_Link_Quality command has completed execution, a Command Complete event will be generated.

6.1.3.8 Infineon_Set_UART_Baudrate (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Set_UART_ Baudrate	0x3F	0x0006	Baudrate	Status

Description:

This command is only accepted in Manufacturer Mode (M).

The command changes the UART baudrate and updates the BD_Data parameter UART_Baudrate. When the baudrate is changed, a command status event will be sent at the current baudrate followed by an **Infineon Set UART Baudrate Complete Event** at the new baudrate.

Note: The host must not send commands or data to the controller after the host has issued the Infineon_Set_UART_Baudrate command until the host has received the Infineon_Set_UART_Baudrate_Complete event. The host must also not expect any data from the controller during the same period i.e. no active links and no page/inquiry scanning should be enabled.

Command Parameters:

Baudrate: *Size: 1 Octet*

Value	Parameter Description
0x00	9600 Baud
0x01	19200 Baud
0x02	38400 Baud
0x03	57600 Baud
0x04	115200 Baud (default)
0x05	230400 Baud
0x06	460800 Baud
0x07	921600 Baud
0x08	1843200 Baud
0x09	3250000 Baud
0x0A - 0xFF	Reserved

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Set_UART_Baudrate command succeeded
0x01 - 0xFF	Set_UART_Baudrate command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

The controller sends the Command Status event to the host when it has received the HCI_Infineon_Set_UART_Baudrate command at the current baudrate. The controller waits for a fixed amount of time (200 slots = 0.125 s) to let the host change its baudrate. The Infineon Set UART Baudrate Complete event will occur when the UART baudrate has been changed. This event will be sent at the new baudrate.

*Note: No Command Complete event will be sent by the controller to indicate that this command has been completed. Instead the **Infineon Set UART Baudrate Complete Event** will indicate that this command has been completed.*

6.1.3.9 Infineon_Write_BD_Data (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Write_BD_Data	0x3F	0x002F	BD_ADDR, Channel_ Word_Offset, Clk_ Conf, EEPROM_Size, Input_Freq, LMP_ Features, LPM_Conf, LPM_Drift, LPM_ Threshold, ULPM_ Threshold, PMU_ Config, RF_Psel_D, RF_Psel_Conf, RSSI_ Min, RSSI_Max, DDC_ TL_Conf, UART_ Baudrate, UART_ Invert, UART_Pulls, Osc_Settle, BB_Conf, RF_Conf, TX_Power_Ref0,..., TX_Power_Ref3, Osc_ Trim, Three-Wire_ARQ_ Timeout, Reserved	Status

Description:

This command is only accepted in Manufacturer Mode.

The command is used to set operation critical parameters, including oscillator frequency, RF parameters, Bluetooth device address, HCI transport layer parameters and low power mode parameters.

If BD_Data is not available after power-up, all parameters will be set to default values. These values are marked with (default) in the following tables.

BD_Data is stored in internal RAM or non-volatile memory if available. The settings will become valid after a reset. The reset can either be generated when leaving manufacturer mode or by sending an HCI_Reset command to the controller.

Note: If BD_Data is stored in internal RAM and the bit Save_RAM_BD_Data in BB_Conf is not set, BD_Data will be replaced by default values after hardware reset.

Note: Wrong parameters (especially concerning the transport layer) in the BD_Data may cause malfunction of the device.

Command Parameters:

BD_ADDR: *Size: 6 Octets*

Value	Parameter Description
0xXXXXXXXXXXXX	Bluetooth device address (least significant byte first) (default: 0x0003199E8B00)

Channel_Word_Offset: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0xFFFF	Channel word offset for RF PLL (default: 0x0000)

Clk_Conf: *Size: 1 Octet*

Value (bits)	Parameter Description
XXXXXXX0	*Multiple_Clock_Detection*: Enabled (default)
XXXXXXX1	*Multiple_Clock_Detection*: Disabled
XXXXX00X	*Low_Power_Clock_Selection*: External clock at CLK32 (default)
XXXXX01X	*Low_Power_Clock_Selection*: Internal low power oscillator
XXXXX10X	*Low_Power_Clock_Selection*: Reference clock & low power oscillator
XXXXX11X	*Low_Power_Clock_Selection*: Reserved
XXXX0XXX	*Reference_Clock_Selection*: External clock at CLKIN (default)
XXXX1XXX	*Reference_Clock_Selection*: Internal crystal oscillator
XXX0XXXX	Reserved (shall be set to 0)
XX0XXXXX	*SYRI_Divider*: Synthesizer reference input is not divided (shall be used if the nominal input frequency is below 27 MHz). (default)
XX1XXXXX	*SYRI_Divider*: Synthesizer reference input is divided by two (shall be used if the nominal input frequency is greater than or equal to 27MHz).
X0XXXXXX	Reserved (shall be set to 0)
1XXXXXXX	Reserved (shall be set to 1)

EEPROM_Size: *Size: 1 Octet*

Value	Parameter Description
0x00	EEPROM not present or size unknown (default)
0x01 - 0xFF	Number of memory pages (256 bytes each) of the external EEPROM

Input_Freq: *Size: 4 Octets*

Value	Parameter Description
0x00989680 - 0x02625A00	Specifies the frequency of the reference clock in Hertz. The value is used if multiple clock detection is disabled or the controller was unable to detect the frequency. Range: 10MHz - 40MHz (default: 26MHz (0x018CBA80))

LMP_Features: *Size: 8 Octets*

Value	Parameter Description
0xXXXXXXXXXXXXXXXX	LMP features bit mask

LPM_Conf: *Size: 1 Octet*

Value (bits)	Parameter Description
XXXX0000	Reserved (shall be set to 0b0000)
XXX0XXXX	*Auto_Disable_LPM*: Autonomous use of low power modes is not disabled after a host initiated wake-up. (default)
XXX1XXXX	*Auto_Disable_LPM*: Autonomous use of low power modes is automatically disabled after a host initiated wake-up.
XX0XXXXX	*Host_LPM*: Not activated (default)
XX1XXXXX	*Host_LPM*: Activated
X0XXXXXX	*Default_LPM_Mode*: The controller is not allowed to enter any low power mode without an explicit reception of the **Infineon_Enable_LPM** command. (default)
X1XXXXXX	*Default_LPM_Mode*: The controller is allowed to enter low power modes without explicit reception of the **Infineon_Enable_LPM** command. This setting shall not be used when *Auto_Disable_LPM* = 1 or the HCI UART-6W transport layer is used.
0XXXXXXX	Reserved (shall be set to 0)

LPM_Drift: *Size: 1 Octet*

Value	Parameter Description
0x00-0xFA	Low power clock drift in ppm. A value for the internal low power oscillator is provided by Infineon. (default: 250ppm (0xFA))
0xFB - 0xFF	Reserved

LPM_Threshold: *Size: 1 Octet*

Value	Parameter Description
0x00	Reserved
0x01 - 0xFF	Idle time threshold for entering low power mode (LPM) in slots. The optimal value is provided by Infineon.

ULPM_Threshold: *Size: 1 Octet*

Value	Parameter Description
0x00	Ultra low power mode (ULPM) is disabled.
0x01 - 0xFF	Idle time threshold for entering ultra low power mode (ULPM) in slots. The value has to fulfill one of the following conditions. With internal LPO: ULPM_Threshold ≥ ((Osc_Settle + 18) · 125.0 + 5000)/625 With external CLK32: ULPM_Threshold ≥ ((Osc_Settle + 18) · 122.1 + 5000)/625 The optimal value is provided by Infineon.

PMU_Config: *Size: 2 Octets*

Value (bits)	Parameter Description
XXXXXXXX XXXXX000 MSB LSB	Reserved (shall be set to 0b000)
XXXXXXXX XXXX0XXX	*ResetCtrl*: Pull up disabled (default)
XXXXXXXX XXXX1XXX	*ResetCtrl*: Pull up enabled
XXXXXXXX XXX0XXXX	*RFREGOFF*: RF regulator on (default)
XXXXXXXX XXX1XXXX	*RFREGOFF*: RF regulator off
XXXXXXXX X00XXXXX	*VDDPM*: VDDPM uses low power bandgap. (default)
XXXXXXXX X01XXXXX	*VDDPM*: VDDPM uses high precision bandgap.
XXXXXXXX X10XXXXX	*VDDPM*: VDDPM regulator is switched off.
XXXXXXXX X11XXXXX	Reserved

Value (bits)	Parameter Description
XXXXXXXX 1XXXXXXX	Reserved (shall be set to 1)
XXXXXXX0 XXXXXXXX	Reserved (shall be set to 0)
XXXXXX0X XXXXXXXX	Reserved (shall be set to 0)

RF_Psel_D *Size: 4 Octets*

Value (bits)	Parameter Description
0x00 - 0x0F (each Byte)	Configuration of power steps for digital control of an external power amplifier and for control of internal power steps, when no external power amplifier is present. With the first octet the lowest power step is configured. The fourth octet is used to configure the highest power step. Default: 0x03, 0x04, 0x05, 0x06

RF_Psel_Conf: *Size: 1 Octet*

Value (bits)	Parameter Description
0xXY X: 0x0 - 0x4 Y: 0x0 - 0x4	Configuration of the default and the maximum power step used for power control. Default setting is 0x44. X: Default power step. This power setting is used during Inquiry, Page and after Connection Setup for a new connection until the remote device requests a change. Y: Maximum power step. This configuration is used to restrict the number of power steps, which is useful when the controller shall work as a Class 3 device.

RSSI_Min, RSSI_Max: *Size: 1 Octet each*

Value	Parameter Description
0x00 - 0xFF	RSSI_Min and RSSI_Max represent the lower and the upper limit of the Golden Receive Power Range (see Bluetooth Radio specification). The automatic power control on the controller tries to keep the RSSI value within this range. On reception of an HCI_Read_RSSI command the controller calculates the deviation from this range and reports it. (Default: RSSI_Min = 0x0C, RSSI_Max = 0x10)

DDC_TL_Conf: *Size: 1 Octet*

Value (bits)	Parameter Description
XXXXXXX0	Reserved (shall be set to 0)
XXXXXX0X	*HCI_UART*: HCI UART transport layer disabled
XXXXXX1X	*HCI_UART*: HCI UART transport layer enabled (default)
XXXXX0XX	*HCI_TW_UART*: HCI Three-Wire UART transport layer disabled
XXXXX1XX	*HCI_TW_UART*: HCI Three-Wire UART transport layer enabled (default)
XXXX0XXX	*CRC_Mirroring*: HCI Three-Wire UART CRC mirroring disabled (default)
XXXX1XXX	*CRC_Mirroring*: HCI Three-Wire UART CRC mirroring enabled
X000XXXX	*LPM_Protocol*: HCI UART-4W (default)
X001XXXX	*LPM_Protocol*: HCI UART-6W
X010XXXX - X111XXXX	*LPM_Protocol*: Reserved
0XXXXXXX	*HW_Flow*: UART hardware flow control enabled (default)
1XXXXXXX	*HW_Flow*: UART hardware flow control disabled

UART_Baudrate: *Size: 1 Octet*

Value	Parameter Description
0x00	9600 Baud
0x01	19200 Baud
0x02	38400 Baud
0x03	57600 Baud
0x04	115200 Baud (default)
0x05	230400 Baud
0x06	460800 Baud
0x07	921600 Baud
0x08	1843200 Baud
0x09	3250000 Baud
0x0A - 0xFF	Reserved

UART_Invert: *Size: 1 Octet*

Value (bits)	Parameter Description
XXXXXXX0	*Inv_TXD*: UARTXD not inverted (default)
XXXXXXX1	*Inv_TXD*: UARTXD inverted
XXXXXX0X	*Inv_RXD*: UARTRXD not inverted (default)
XXXXXX1X	*Inv_RXD*: UARTRXD inverted
XXXXX0XX	*Inv_RTS*: UARTRTS not inverted (default)
XXXXX1XX	*Inv_RTS*: UARTRTS inverted
XXXX0XXX	*Inv_CTS*: UARTCTS not inverted (default)
XXXX1XXX	*Inv_CTS*: UARTCTS inverted

UART_Pulls: *Size: 1 Octet*

Value (bits)	Parameter Description
XXXXXX00	*Pull_TXD*: Reserved
XXXXXX01	*Pull_TXD*: UARTTXD is pulled up during low power modes if HCI UART-4W is used. (default)
XXXXXX10	*Pull_TXD*: UARTTXD is pulled down during low power modes if HCI UART-4W is used.
XXXXXX11	*Pull_TXD*: Reserved
XXXX00XX	Reserved (shall be set to 00)
XX00XXXX	Reserved (shall be set to 00)
00XXXXXX	Reserved (shall be set to 00)

Osc_Settle: *Size: 1 Octet*

Value	Parameter Description
0x02-0xFF	Specifies the time required for the reference clock and the external power supply to stabilize after they have been requested by SLEEPX. The delay corresponding to a specific Osc_Settle value can be calculated with one of the following formulas. With internal LPO: Delay = Osc_Settle·125.0µs. With external CLK32: Delay = Osc_Settle·122.1µs. Typical delays when the internal crystal oscillator is used are in the range 1-10ms (depending on crystal). The reset value of Osc_Trim is 0x7F.

BB_Conf: *Size: 1 Octet*

Value (bits)	Parameter Description
XXXXXXX0	*Wakeup_Host*: WAKEUP_HOST high to wake host (default)
XXXXXXX1	*Wakeup_Host*: WAKEUP_HOST low to wake host
XXXXXX0X	*Wakeup_BT*: WAKEUP_BT high to wake controller (default)
XXXXXX1X	*Wakeup_BT*: WAKEUP_BT low to wake controller
XXXXX0XX	*Default_SCO_interface*: Default (e)SCO interface is UART
XXXXX1XX	*Default_SCO_interface*: Default (e)SCO interface is PCM (default)
XXXX0XXX	Default_PLC_mode: PLC is by default off
XXXX1XXX	Default_PLC_mode: PLC is by default on (default)
XX0XXXXX	*Local_Name*: stored in non-volatile memory, if available (default)
XX1XXXXX	*Local_Name*: not stored in non-volatile memory
X0XXXXXX	*Save_RAM_BD_Data*: BD_Data in RAM is cleared on HW reset. BD_Data in non-volatile memory is not cleared.
X1XXXXXX	*Save_RAM_BD_Data*: BD_Data in RAM is saved on HW reset (default)
0XXXXXXX	*Inv_SLEEPX*: SLEEPX not inverted (default)
1XXXXXXX	*Inv_SLEEPX*: SLEEPX inverted

RF_Conf: *Size: 1 Octet*

Value (bits)	Parameter Description
XXXXXX00	*PA_Conf*: Internal power amplifier is used and parameter RF_PSEL_D refers to internal power settings (default). P0.14 is used as input pin for PTA interface.
XXXXXX01	*PA_Conf*: External power amplifier is used and parameter RF_PSEL_D refers to external power amplifier settings. P0.14 is used as input pin for PTA interface.
XXXXXX10	*PA_Conf*: Internal power amplifier is used and parameter RF_PSEL_D refers to internal power settings. P0.11 is used as input pin for PTA interface.
XXXXXX11	*PA_Conf*: Reserved
XXXX00XX	*PA_Fine_Tuning*: Fine tuning of TX power: -4dB
XXXX01XX	*PA_Fine_Tuning*: Fine tuning of TX-Power: -2dB
XXXX10XX	*PA_Fine_Tuning*: Fine tuning of TX-Power: nominal

Value (bits)	Parameter Description
XXXX11XX	*PA_Fine_Tuning*: Fine tuning of TX-Power: +2dB
XXX0XXXX	*RF_Mode*: RF active (default)
XXX1XXXX	*RF_Mode*: RF inactive.
XX0XXXXX	*Ext_PA_control:* Shall be set to 0
X0XXXXXX	*Lowppfgain*: Shall be set to 0
0XXXXXXX	*LNAgain*: Shall be set to 0

TX_Power_Ref0... TX_Power_Ref3: *Size: 4 Octets*

Value	Parameter Description
0x00 - 0xFF (each Octet)	Transmit power level reference value: the controller (with or without external power amplifier) supports 4 power settings. When issuing the HCI_Read_Transmit_Power_Level command the reference value of the current power level is returned. TX_Power_Ref0 (first octet) contains the lowest power value. TX_Power_Ref3 (last octet) contains the highest power value..

Osc_Trim: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0xFFFF	Oscillator trim value. Bits 5-0 switch binary weighted capacitances from 32*LSB to 1*LSB. Bits 9-6 switch capacitances with value 64*LSB. LSB ≈ 40fF.

Three-Wire_ARQ_Timeout: *Size: 1 Octet*

Value	Parameter Description
0x03 - 0xFF	This parameter sets the Three-Wire UART ARQ time in multiples of Tmax, where Tmax is the transmission time for the largest supported HCI packet in the currently used baud rate. (default: 0x06)

Reserved: *Size: 9 Octets*

Value	Parameter Description
0x00 - 0xFF (each octet)	Reserved (shall be set to 0x00 00 00 00 00 00 00 00 00)

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Write_BD_Data command succeeded
0x01 - 0xFF	Infineon_Write_BD_Data command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the controller receives the HCI_Infineon_Write_BD_Data command, the controller sends the Command Status event to the host.

*Note: No Command Complete event will be sent by the controller to indicate that this command has been completed. Instead, the **Infineon Write BD Data Complete Event** will indicate that this command has been completed.*

6.1.3.10 Infineon_Read_BD_Data (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Read_BD_Data	0x3F	0x0030		Status, See parameters of **Infineon_ Write_BD_ Data (M)**

Description:

This command is only accepted in Manufacturer Mode.

This command may be used to read values for the Bluetooth device data.

Command Parameters:

None.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Read_BD_Data command succeeded
0x01 - 0xFF	Infineon_Read_BD_Data command failed. See list of error codes in Bluetooth specification

For all other return parameters, see command parameters for **Infineon_Write_BD_Data (M)**.

Event(s) generated (unless masked away):

When the HCI_Infineon_Read_BD_Data command has completed execution, a Command Complete event will be generated.

6.1.3.11 Infineon_Switch_To_Loader (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Switch_To_Loader	0x3F	0x0001		Status

Description:

This command is only accepted in Manufacturer Mode (M).

With the Infineon_Switch_To_Loader command, the device gives program control to the loader located in internal ROM of the controller. The loader is used for writing the program code (sent by the host) into the RAM. Right before switching to the loader, the device returns a Command Complete event with parameter *Status* to the host.

Command Parameters:

None.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Switching to Loader
0x01 - 0xFF	Infineon_Switch_To_Loader command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

A Command Complete event will be generated right before switching to the Loader.

6.1.3.12 Infineon_Write_Ext_EEPROM_Data (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Write_Ext_ EEPROM_Data	0x3F	0x0089	ADL, ADH, Data	Status, ADL, ADH, Data

Description:

This command is only accepted in Manufacturer Mode (M).

The Link Manager's internal data (DDC) stored in external EEPROM (clock information, Bluetooth device data, etc.) can be altered with this command.

Note: If no EEPROM is connected, only the current settings stored in RAM will be affected. It is not possible to access addresses outside the DDC data area with this command.

Command Parameters:

ADL, ADH: *Size: 1+1 Octets*

Value	Parameter Description
0x00 - 0xFF	Low and high byte of address

Data: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Data to be written to defined address

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Write_Ext_EEPROM_Data command succeeded
0x01 - 0xFF	Infineon_Write_Ext_EEPROM_Data command failed. See list of error codes in Bluetooth specification

ADL, ADH: *Size: 1+1 Octets*

Value	Parameter Description
0x00 - 0xFF	Low and high byte of address

Data: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Data written to defined address

Event(s) generated (unless masked away):

When the HCI_Infineon_Write_Ext_EEPROM_Data command has completed execution, a Command Complete event will be generated.

6.1.3.13 Infineon_Read_Ext_EEPROM_Data (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Read_Ext_EEPROM_Data	0x3F	0x008A	ADL, ADH, Data	Status, ADL, ADH, Data

Description:

This command is only accepted in Manufacturer Mode (M).

The Link Manager's internal data stored in external EEPROM (clock information, Bluetooth device data, etc.) can be read with this command.

Command Parameters:

ADL, ADH: *Size: 1+1 Octets*

Value	Parameter Description
0x00 - 0xFF	Low and high Byte of the address

Data: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	This is a dummy parameter, set to 0

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Read_Ext_EEPROM_Data command succeeded
0x01 - 0xFF	Infineon_Read_Ext_EEPROM_Data command failed. See list of error codes in Bluetooth specification

ADL, ADH: *Size: 1+1 Octets*

Value	Parameter Description
0x00 - 0xFF	Low and high byte of address

Data: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Data read from the defined address

Event(s) generated (unless masked away):

When the HCI_Infineon_Read_Ext_EEPROM_Data command has completed execution, a Command Complete event will be generated.

6.1.3.14 Infineon_Set_Encryption_Key_Size (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Set_Encryption_Key_Size	0x3F	0x0019	Enc_Key_Size_Min, Enc_Key_Size_Max	Status

Description:

This command is only accepted in Manufacturer Mode (M).

The minimum and maximum encryption key sizes are configured with the HCI_Infineon_Set_Encryption_Key_Size command. The default settings are:

Enc_Key_Size_Min = 0x01

Enc_Key_Size_Max = 0x10

They will be overwritten when sending this command.

Command Parameters:

Enc_Key_Size_Min: *Size: 1 Octet*

Value	Parameter Description
0x01 - 0x10	Minimum size of encryption key in Bytes.

Enc_Key_Size_Max: *Size: 1 Octet*

Value	Parameter Description
0x01 - 0x10	Maximum size of encryption key in Bytes.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Set_Encryption_Key_Size command succeeded
0x01 - 0xFF	Infineon_Set_Encryption_Key_Size command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Set_Encryption_Key_Size command has completed execution, a Command Complete event will be generated.

6.1.3.15 Infineon_Read_Encryption_Key_Size

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Read_Encryption_Key_Size	0x3F	0x0017	Connection_Handle	Status, Connection_Handle, Enc_Key_Size

Description:

The size of the encryption key that is currently in use on a link (described by *Connection_handle* parameter) can be read with this command. The information helps the host to judge on the security level of a link and decide what action to take, if the level of security is not sufficient.

Command Parameters:

Connection_Handle: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0x0EFF	Connection Handle identifies the connection for which the encryption key size is read.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Read_Encryption_Key_Size command succeeded
0x01 - 0xFF	Infineon_Read_Encryption_Key_Size command failed. See list of error codes in Bluetooth specification

Connection_Handle: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0x0EFF	Connection Handle identifies the connection for which the encryption key size was read.

Enc_Key_Size: *Size: 1 Octet*

Value	Parameter Description
0x01 - 0x10	Size of encryption key in Bytes.

Event(s) generated (unless masked away):

When the HCI_Infineon_Read_Encryption_Key_Size command has completed, a Command Complete event will be generated.

6.1.3.16 Infineon_Enable_Infineon_Events (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Enable_Infineon_Events	0x3F	0x001B	Event_Switch	Status

Description:

This command is only accepted in Manufacturer Mode (M).

Some Infineon specific events are only for debugging purposes (e.g. they will not be sent as a response to a command). Sending these events to the host can be enabled and disabled via the Infineon_Enable_Infineon_Events command.

When sending this command the following events will be masked:

- **Infineon Debug Exception Event**
- **Infineon SCO Rejected Via LMP Event**
- **Infineon Scan Status Event**
- **Infineon PTT Switch Notification Event**
- **Infineon AFH Extraordinary RSSI Event**

Command Parameters:

Event_Switch: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon debugging events are switched off (default)
0x01	Infineon debugging events are switched on

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Enable_Infineon_Events command succeeded
0x01 - 0xFF	Infineon_Enable_Infineon_Events command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Enable_Infineon_Events command has completed execution, a Command Complete event will be generated.

6.1.3.17 Infineon_Memory_Read (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Memory_Read	0x3F	0x008D	Address, Mode, Length	Status, Address, Data

Description:

This command is only accepted in Manufacturer Mode (M).

This command is for direct reading of controllers internal registers. Starting at the given address, the next n Bytes are read, where n= *Length*.

Note: The parameter Length must be set corresponding to the Mode parameter, e.g. if the Mode is 0x01 (Half Word Access), the Length must be a multiple of 2 Bytes.

Command Parameters:

Address: *Size: 4 Octets*

Value	Parameter Description
0xXXXXXXXX	Start address for read access. The start address has to be aligned according to the access mode.

Mode: *Size: 1 Octet*

Value	Parameter Description
0xXX	Read access is performed as 00: Byte access 01: Half word access 02: Word access

Length: *Size: 1 Octet*

Value	Parameter Description
0x01 - 0xF7	Number of bytes to read from RAM *Note: Parameter Length must correspond to the Mode Parameter:* *Mode = 00: Length = Multiple of 1 Byte* *Mode = 01: Length = Multiple of 2 Bytes* *Mode = 10: Length = Multiple of 4 Bytes*

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Memory_Read command succeeded
0x01 - 0xFF:	Infineon_Memory_Read command failed. See list of error codes in Bluetooth specification

Address: *Size: 4 Octets*

Value	Parameter Description
0xXXXXXXXX	Address of memory location to read from

Data: *Size: Length Octets*

Value	Parameter Description
0x00 - 0xFF each Octet	Data read from the register

Event(s) generated (unless masked away):

When the HCI_Infineon_Memory_Read command has completed execution, a Command Complete event will be generated.

6.1.3.18 Infineon_Memory_Write (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Memory_Write	0x3F	0x008E	Address, Mode, Length, Data	Status

Description:

This command is only accepted in Manufacturer Mode (M).

This command is for direct writing to controllers internal registers. Starting from the address defined in Address the next n Bytes are written, where n= *Length*.

Note: This command should not be used unauthorized, since improper usage may cause unexpected results, permanent malfunction, or damage to the circuit.

Note: The data shall be delivered in little endian format.

Command Parameters:

Address: *Size: 4 Octets*

Value	Parameter Description
0xXXXXXXXX	Address of memory location to write to

Mode: *Size: 1 Octet*

Value	Parameter Description
0xXX	Write access is performed as 00: Byte access 01: Half word access 02: Word access

Length: *Size: 1 Octet*

Value	Parameter Description
0x01 - 0xF7	Number of bytes to write to RAM *Note: Parameter Length must correspond to the Mode Parameter:* *Mode = 00: Length = Multiple of 1 Byte* *Mode = 01: Length = Multiple of 2 Bytes* *Mode = 10: Length = Multiple of 4 Bytes*

Data: *Size: Length Octets*

Value	Parameter Description
0x00 - 0xFF each Octet	Data to be written to the defined memory location *Note: Data Length must correspond to the Mode Parameter:* *Mode = 00: Length = Multiple of 1 Byte* *Mode = 01: Length = Multiple of 2 Bytes* *Mode = 10: Length = Multiple of 4 Bytes*

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x0	Infineon_Memory_Write command succeeded
0x01 - 0xFF:	Infineon_Memory_Write command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Memory_Write command has completed execution, a Command Complete event will be generated.

6.1.3.19 Infineon_Signal_Proc_Config

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Signal_Proc_Config	0x3F	0x002C	Connection, Handle, ConfigBits_AIR2AUDIO, ConfigBits_AUDIO2AIR	Status

Description:

Each of the eSCO/SCO connections goes through a signal processing path. There are some algorithms in the signal processing path. Each of these algorithms has its own bit to switch it on and off. The signal processing algorithms can be switched on and off by this HCI command. The configuration can be done separately for the air-to-audio and the audio-to-air paths.

The configuration of the signal processing path can be done in two ways:

Pre-eSCO/SCO-Connection Setup mode: Configuration of the signal processing path is done before setting up a synchronous connection but after having established an ACL connection. The parameters denote the settings used for the next synchronous connection that will be set up on the ACL connection with the corresponding ACL connection handle *Connection_Handle*.

Post-eSCO/SCO-Connection Setup mode: The signal processing path will be configured after eSCO/SCO connection establishment by choosing the corresponding eSCO/SCO Connection_Handle parameter. The signal processing settings can be changed during an existing eSCO/SCO connection by choosing the corresponding eSCO/SCO connection handle.

Note: The controller will automatically distinguish between the two modes by examining the given Connection Handle (whether it is an ACL or an eSCO/SCO connection handle).

Command Parameters:

Connection Handle: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0x0EFF	Connection handle: – ACL connection handle in case a Pre-eSCO/SCO-Connection configuration should be performed (Pre-eSCO/SCO-Connection Setup mode) – eSCO/SCO connection handle in case a Post-eSCO/SCO-Connection configuration should be performed (Post-eSCO/SCO-Connection Setup mode)
0xFFFF	pseudo eSCO/SCO connection handle: must be used if PCM Signal Processing Loopback mode is active (only possible after PCM_Loopback is enabled via **Infineon_Enable_PCM_Loopback**)

ConfigBits_AIR2AUDIO: *Size: 2 Octets*

Value (bits)	Parameter Description
bit 0	Reserved (shall be set to 0)
bit 1	Reserved (shall be set to 0)
bit 2	Reserved (shall be set to 0)
bit 3	Enable bit for gain stage: 1: the gain stage is switched on 0: the gain stage is switched off (default)
bit 4	Reserved (shall be set to 0)

Value (bits)	Parameter Description
bit 5	Reserved (shall be set to 0)
bit 6	Reserved (shall be set to 0)
bit 7	Reserved (shall be set to 0)
bit 8	Reserved (shall be set to 0)
bit 9	Reserved (shall be set to 0)
bit 10	Enable bit for PLC algorithm: 1: the PLC algorithm is switched on 0: the PLC algorithm is switched off (default)
bit 11	Usage of PLC on packets with CRC errors (eSCO only): 1: packets with CRC errors are replaced by PLC 0: packets with CRC errors are used as is (default)
bit 12	Clock drift compensation bit: 1: clock drift compensation task on (default) 0: clock drift compensation task off
bit 13	Reserved (shall be set to 0)
bit 14	Reserved (shall be set to 0)
bit 15	Reserved (shall be set to 0)

ConfigBits_AUDIO2AIR: *Size: 2 Octets*

Value (bits)	Parameter Description
bit 0	Reserved (shall be set to 0)
bit 1	Reserved (shall be set to 0)
bit 2	Reserved (shall be set to 0)
bit 3	Enable bit for gain stage: 1: the gain stage is switched on 0: the gain stage is switched off (default)
bit 4	Reserved (shall be set to 0)
bit 5	Reserved (shall be set to 0)
bit 6	Reserved (shall be set to 0)
bit 7	Reserved (shall be set to 0)
bit 8	Reserved (shall be set to 0)
bit 9	Reserved (shall be set to 0)
bit 10	Reserved (shall be set to 0)

Value (bits)	Parameter Description
bit 11	Reserved (shall be set to 0)
bit 12	Clock drift compensation bit: 1: clock drift compensation task on (default setting) 0: clock drift compensation task off
bit 13	Reserved (shall be set to 0)
bit 14	Reserved (shall be set to 0)
bit 15	Reserved (shall be set to 0)

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Signal_Proc_Config command succeeded
0x01 - 0xFF	Infineon_Signal_Proc_Config command failed

Event(s) generated (unless masked away):

When the HCI_Infineon_Signal_Proc_Config command has completed execution, a Command Complete event will be generated.

6.1.3.20 Infineon_Gain_Setting

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Gain_Setting	0x3F	0x002E	Connection_Handle, Datadir, Gain	Status

Description:

The controller can amplify and attenuate the signal in the eSCO/SCO path, both in air-to-audio and in audio-to-air directions. Consider that this command only is for the gain stage configuration, not for switching the gain stage on and off (see **Infineon_Signal_Proc_Config**).

The configuration of the gain settings can be done in two ways:

Pre-eSCO/SCO-Connection Setup mode: Configuration of the gain setting is done before setting up a synchronous connection but after having established an ACL connection. The parameters denote the settings used for the next synchronous

connection that will be set up on the ACL connection with the corresponding ACL connection handle *Connection_Handle*.

Post-eSCO/SCO-Connection Setup mode: The gain settings will be configured after eSCO/SCO connection establishment by choosing the corresponding eSCO/SCO Connection_Handle parameter. The gain settings can be changed during an existing eSCO/SCO connection by choosing the corresponding eSCO/SCO connection handle.

Note: The controller will automatically distinguish between the two modes by examining the given Connection Handle (whether it is an ACL or an eSCO/SCO connection handle).

Command Parameters:

Connection_Handle: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0x0EFF	Connection handle: – ACL connection handle in case a Pre-eSCO/SCO-Connection configuration should be performed (Pre-eSCO/SCO-Connection Setup mode) – eSCO/SCO connection handle in case a Post-eSCO/SCO-Connection configuration should be performed (Post-eSCO/SCO-Connection Setup mode)
0xFFFF	Pseudo eSCO/SCO connection handle: must be used if PCM Signal Processing Loopback mode is active (only possible after PCM_Loopback is enabled via **Infineon_Enable_PCM_Loopback**)

Datadir: *Size: 1 Octet*

Value	Parameter Description
0x00	Air-to-audio path
0x01	Audio-to-air path
0x02-0xFF	Invalid

Gain: *Size: 2 Octets*

Value	Parameter Description

0x0000-0x0079	SCO/eSCO audio gain is controlled by three parameters (n, s and m) according to the following formula:
	$$PCM_{out} = \frac{2^m - 2s + 1}{2^n \times 2^m} \times PCM_{in}$$
	The Gain parameter defines n, s and m:
	`n = Gain[bits 6-4]`
	`s = Gain[bit 3]`
	`m = Gain[bits 2-0]`
	The remaining bits of the Gain parameter are ignored.
	Examples:
	`Value  Gain in dB`
	`0x0000  +6.0 dB`
	`0x0010  0.0 dB`
	`0x0020  -6.0 dB`
	`0x0030  -12.0 dB`
	`0x0037  -18.0 dB`
	`0x0047  -24.0 dB`
	`0x0057  -30.0 dB`
	`0x0066  -36.0 dB`
	`0x0076  -42.0 dB`
	`0x0079  -48.2 dB`
	"Gain in dB" is calculated like this:
	$$Gain_{dB} = 20 \times \log\left(\frac{PCM_{out}}{PCM_{in}}\right)$$
	Note: Some combinations of n, s and m will mute PCM_{out}.

0x007A-0xFFFF	Invalid

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Gain_Setting command succeeded
0x01 - 0xFF	Infineon_Gain_Setting command failed

Event(s) generated (unless masked away):

When the HCI_Infineon_Gain_Setting command has completed execution, a Command Complete event will be generated.

6.1.3.21 Infineon_Get_Exception_Info (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Get_ Exception_Info	0x3F	0x0022	Type	Status, Exception

Description:

This command is only accepted in Manufacturer Mode (M).

This command will read exception information from the controller.

*Note: The Exception parameter is a string parameter and is therefore not sent LSB first as are other parameters.The first byte of the parameter Exception is received first. The exception is cleared with the **Infineon_Clear_Exception_Info (M)**.*

Command Parameters:

Type: *Size: 1 Octet*

Value	Parameter Description
0x00	Fatal Exception
0x01 - 0xFF	Reserved for future use

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Get_Exception_Info command succeeded
0x01 - 0xFF	Infineon_Get_Exception_Info command failed. See list of error codes in Bluetooth specification

Exception: *Size: 12 Octets*

Value	Parameter Description
LxxxxPxxRxx 0x00	UTF-8 encoded Exception Information The Exception Information is terminated by 0x00. Thus it contains 11 valid exception information Bytes. See the next table for possible fatal exceptions.

Possible fatal exceptions: *Size: 12 Octets*

Value	Parameter Description
P[02]R[71]	H_EXC_UNKNOWN_PACKET_TYPE Unknown HCI PacketType received. Occurs, if an invalid HciPacketType is used.
P[02]R[72]	H_EXC_PACKET_IS_TOO_LARGE HCIPacketSize too large. Occurs, if the HCIPacketLen parameter doesn't fit to the Packetsize itself.
P[02]R[87]	H_EXC_FIFO_OVERFLOW Unexpected Fifo overflow detected.
P[03]R[01]	C_EXC_ARM_RESET Unexpected ARM reset error detected.
P[03]R[00]	C_EXC_TESTMODE_EXIT Occurs, if Tester tries to exit Bluetooth test mode.

Event(s) generated (unless masked away):

When the HCI_Infineon_Get_Exception_Info command has completed execution, a Command Complete event will be generated.

6.1.3.22 Infineon_Clear_Exception_Info (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Clear_Exception_Info	0x3F	0x0024		Status

Description:

This command is only accepted in manufacturer mode (M).

This command will clear all exception information.

Command Parameters:

None.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Clear_Exception_Info command succeeded.
0x01 - 0xFF	Infineon_Clear_Exception_Info command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Clear_Exception_Info command has completed execution, a Command Complete event will be generated.

6.1.3.23 Infineon_Set_Logic_Gate

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Set_Logic_Gate	0x3F	0x0029	Logic_Gate_Settings	Status

Description:

This command selects the inputs and the function of the programmable logic gate.

GATE_OUT has to be enabled by setting P1ALTSEL1 bit 6 = 0 and P1ALTSEL0 bit 6 = 1 with Infineon_Write_Ports or Infineon_Set_Port_Bit/Infineon_Clear_Port_Bit. Port pins used as inputs must have their input drivers enabled.

Command Parameters:

Logic_Gate_Settings: *Size: 4 Octets*

Value	Parameter Description
bit 15	InB. Can be selected as gate input B.
bit 14	InA. Can be selected as gate input A.

Value	Parameter Description
bits 7-6	Selects gate input B: 00: InB (bit 15) 01: P1.7/GATE_IN (VDDPM) 10: SLEEPX (internal) 11: T3OUT (internal)
bits 5-4	Selects gate input A: 00: InA (bit 14) 01: P1.4/GATE_IN (VDD) 10: SLEEPX (internal) 11: T3OUT (internal)
bits 3-0	Logic function: 0x0 - 0xF according to **Table 6-2**.

Table 6-2 Selection of function for programmable logic gate

Gate Input A	Gate Input B	Low	NOR	$\overline{AB}$	A	$\overline{AB}$	B	XOR	NAND	AND	XNOR	B	$\overline{NOT(AB)}$	A	$\overline{NOT(AB)}$	OR	High
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Set_Logic_Gate command succeeded
0x01 - 0xFF	Infineon_Set_Logic_Gate command failed. See list of error codes in Bluetooth specification

Events generated (unless masked away):

When the HCI_Infineon_Set_Logic_Gate command has completed execution, a Command Complete event will be generated.

6.1.3.24 Infineon_Read_Logic_Gate

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Read_Logic_Gate	0x3F	0x002A		Status, Logic_Gate_Settings

Description:

This command reads the logic gate settings written with Infineon_Set_Logic_Gate.

Command Parameters:

None.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Read_Logic_Gate command succeeded
0x01 - 0xFF	Infineon_Read_Logic_Gate command failed. See list of error codes in Bluetooth specification

Logic_Gate_Settings: *Size: 4 Octets*

Value	Parameter Description
0xXXXXXXXX	See **“Infineon_Set_Logic_Gate” on Page 153**

Events generated (unless masked away):

When the HCI_Infineon_Read_Logic_Gate command has completed execution, a Command Complete event will be generated.

6.1.3.25 Infineon_Raw_Write_Ext_EEPROM (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Raw_Write_Ext_EEPROM	0x3F	0x008F	EEPROM_Clock_Speed, EEPROM_Write_Page_Size, Address, Length, Data	Status

Description:

This command is only accepted in Manufacturer Mode (M).

This command writes to an external EEPROM. The command writes to actual addresses in the EEPROM and has nothing to do with the DDC area as the Infineon_Write_Ext_EEPROM_Data command.

Command Parameters:

EEPROM_Clock_Speed: *Size: 2 Octets*

Value	Parameter Description
0x0064 (100)	100 kHz
0x0190 (400)	400 kHz

EEPROM_Write_Page_Size: *Size: 1 Octets*

Value	Parameter Description
0x01-0xFF	EEPROM write page size in bytes

Address: *Size: 4 Octets*

Value	Parameter Description
0xXXXXXXXX	Start address in EEPROM

Length: *Size: 1 Octets*

Value	Parameter Description
0x01-0xF8 (247)	Number of bytes to write (size of Data parameter)

Data: *Size: Length Octets*

Value	Parameter Description
0xXX...XX	Data to write to the EEPROM in little endian byte order (first byte written to lowest address)

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Raw_Write_Ext_EEPROM command succeeded
0x01 - 0xFF	Infineon_Raw_Write_Ext_EEPROM command failed. See list of error codes in Bluetooth specification

Events generated (unless masked away):

When the HCI_Infineon_Raw_Write_Ext_EEPROM command has completed execution, a Command Complete event will be generated.

6.1.3.26 Infineon_Raw_Read_Ext_EEPROM (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Raw_Read_Ext_EEPROM	0x3F	0x0090	EEPROM_Clock_Speed, Address, Length	Status, Data

Description:

This command is only accepted in Manufacturer Mode (M).

This command reads from an external EEPROM. The command reads from actual addresses in the EEPROM and has nothing to do with the DDC area as the Infineon_Read_Ext_EEPROM_Data command.

Command Parameters:

EEPROM_Clock_Speed: *Size: 2 Octets*

Value	Parameter Description
0x0064 (100)	100 kHz
0x0190 (400)	400 kHz

Address: *Size: 4 Octets*

Value	Parameter Description
0xXXXXXXXX	Start address in EEPROM

Length: *Size: 1 Octets*

Value	Parameter Description
0x01-0xFB (251)	Number of bytes to read

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Raw_Read_Ext_EEPROM command succeeded
0x01 - 0xFF	Infineon_Raw_Read_Ext_EEPROM command failed. See list of error codes in Bluetooth specification

Data: *Size: Length Octets*

Value	Parameter Description
0xXX...XX	Data read from the EEPROM in little endian byte order (first byte read from lowest address)

Events generated (unless masked away):

When the HCI_Infineon_Raw_Read_Ext_EEPROM command has completed execution, a Command Complete event will be generated.

6.1.3.27 Infineon_Auto_Calibrate_Crystal (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Auto_Calibrate_Crystal	0x3F	0x0091	Crystal_Freq, Reference_Freq, Reference_Pulse_Count	Status, Osc_Trim

Description:

This command is only accepted in Manufacturer Mode (M).

The frequency of BlueMoon UniCellular's crystal oscillator can be calibrated with a built-in capacitance array that is configured by the BD_DATA value Osc_Trim. This command obtains the optimal value of Osc_Trim by comparing the crystal oscillator frequency to a reference signal with known frequency. The reference signal shall be applied to the CLK32 pin.

Command Parameters:

Crystal_Freq: *Size: 4 Octets*

Value	Parameter Description
0xXXXXXXXX	Wanted frequency in Hz

Reference_Freq: *Size: 4 Octets*

Value	Parameter Description
0xXXXXXXXX	Reference frequency in Hz

Reference_Pulse_Count: *Size: 4 Octets*

Value	Parameter Description
0xXXXXXXXX	Number of reference pulses in measurement

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Auto_Calibrate_Crystal command succeeded
0x01 - 0xFF	Infineon_Auto_Calibrate_Crystal command failed. See list of error codes in Bluetooth specification

Osc_Trim: *Size: 2 Octets*

Value	Parameter Description
0x0000-0xFFFF	Optimal Osc_Trim value

Events generated (unless masked away):

When the HCI_Infineon_Auto_Calibrate_Crystal command has completed execution, a Command Complete event will be generated.

6.1.4 HCI+ Extended Bluetooth Functionality Commands

6.1.4.1 Infineon_TX_Power_Config

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_TX_Power_Config	0x3F	0x0035	Connection_Handle, Power_Setting, TX_Power_Ref	Status

Description:

The TX output power can be switched between normal setting for a class 2 or class 1 device, and ultra-low output power mode with this command.

The TX power settings can be configured independently for each link.

Note: The ultra-low output power mode cannot be used, if the controller is configured to use an external power amplifier.

Command Parameters:

Connection_Handle: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0x0EFF	Connection handle

Power_Setting: *Size: 1 Octet*

Value	Parameter Description
0x00	Nominal output power is used. Link Manager Power Control is used if enabled.
0x01	Output Power is reduced to -45dBm
0x02 - 0xFF	Reserved

TX_Power_Ref: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Transmit power level reference value for ultra-low transmit power mode. When issuing the HCI_Read_Transmit_Power_Level command the reference value of the current power level is returned. *Note: If Power_Setting is "nominal output power" this value is ignored.*

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_TX_Power_Config command succeeded.
0x01 - 0xFF	Infineon_TX_Power_Config command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_TX_Power_Config command has completed execution, a Command Complete event will be generated.

6.1.4.2 Infineon_Enable_AFH_Info_Sending

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Enable_AFH_Info_Sending	0x3F	0x0046	Number_Of_Info_IDs, List_Of_Info_IDs	Status

Description:

This command is used to send information concerning Adaptive Frequency Hopping (AFH). Once enabled, the **Infineon AFH Info Events** A - H will be sent asynchronously with updated information to the host every time a new channel map is generated. The number and kind of data that will be sent by the AFH Info Events is specified by the parameters *Number_Of_Info_IDs* and *List_Of_Info_IDs*.

*Note: The possible Info_IDs can be found in the table on **Page 196**.*

Note: The number of Info_IDs that can be enabled is limited to a maximum total size. The total size must be less or equal to 680 bytes otherwise the command is rejected.

Command Parameters:

Number_Of_Info_IDs: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Number of Info IDs

List_Of_Info_IDs: *Size: Number_Of_Info_IDs Octets*

Value	Parameter Description
Info_IDs (see table below for possible values)	List of Info ID Bytes indicates which information shall be updated each time the AFH Info is sent (Each Info ID = 1 Byte)

Info_IDs: *Size: 1 Octet*

Value	Parameter Description
0x01	Info_ID A, Connection Handle
0x02	Info_ID A, Channel Classification
0x03	Info_ID A, Channel Map
0x04	Info_ID A, Interferer Identification
0x05	Info_ID B, RSSI values (sum of RSSI values of one measuring period)
0x06	Info_ID C, RSSI counter (number of measured RSSI values)
0x07	Info_ID D, BER values (sum of BER values of one measuring period)
0x08	Info_ID E, BER counter (number of measured BER values)
0x09	Info_ID F, Number Received Packets
0x0A	Info_ID G, Number Total Bytes
0x0B	Info_ID H, Number CRC errors

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Enable_AFH_Info_Sending command succeeded.
0x01 - 0xFF	Infineon_Enable_AFH_Info_Sending command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Enable_AFH_Info_Sending command has completed execution, a Command Complete event will be generated.

6.1.4.3 Infineon_Disable_AFH_Info_Sending

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Disable_AFH_Info_Sending	0x3F	0x0047		Status

Description:

This command is used to deactivate the sending of **Infineon AFH Info Events**.

Command Parameters:

None.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Disable_AFH_Info_Sending command succeeded.
0x01 - 0xFF	Infineon_Disable_AFH_Info_Sending command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Disable_AFH_Info_Sending command has completed execution, a Command Complete event will be generated.

6.1.4.4 Infineon_Set_AFH_Measurement_Period (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Set_AFH_ Measurement_ Period	0x3F	0x004A	Duration	Status

Description:

This command is only accepted in Manufacturer Mode (M).

This command is used to set the duration of the next AFH measurement period.

Command Parameters:

Duration: *Size: 2 Octets*

Value	Parameter Description
0x0640 - 0xBB80	Duration of AFH measurement interval in slots. Range: 1600 - 48000 slots (1 - 30 seconds) Default value is 8000 slots (5 seconds)

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Set_AFH_Measurement_Period command succeeded.
0x01 - 0xFF	Infineon_Set_AFH_Measurement_Period command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Set_AFH_Measurement_Period command has completed execution, a Command Complete event will be generated.

6.1.4.5 Infineon_Enable_CQDDR_Info_Sending

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Enable_ CQDDR_Info_ Sending	0x3F	0x0048		Status

Description:

This command is used to activate the sending of information concerning Channel Quality Driven Data Rate change (CQDDR). Once enabled, the CQDDR Info Event will be sent asynchronously with updated information to the host every time a measurement interval is finished. The CQDDR information always include the number of received DM packets, the number of received Bytes (for DM packets), the number of corrected bit errors (for DM packets), the number of received DM packets, and the number or received packets with CRC error (for DH packets) (see **Infineon CQDDR Info Event** description for details).**Command Parameters:**

None.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Enable_CQDDR_Info_Sending command succeeded.
0x01 - 0xFF	Infineon_Enable_CQDDR_Info_Sending command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Enable_CQDDR_Info_Sending command has completed execution, a Command Complete event will be generated.

6.1.4.6 Infineon_Disable_CQDDR_Info_Sending

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Disable_ CQDDR_Info_ Sending	0x3F	0x0049		Status

Description:

This command is used to deactivate the sending of the CQDDR Info Event.

Command Parameters:

None.

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Disable_CQDDR_Info_Sending command succeeded.
0x01 - 0xFF	Infineon_Disable_CQDDR_Info_Sending command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Disable_CQDDR_Info_Sending command has completed execution, a Command Complete event will be generated.

6.1.4.7 Infineon_Write_Pairing_Mode

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Write_Pairing_ Mode	0x3F	0x004C	Pairing_Mode	Status

Description:

This command is used to set the pairing mode of the controller. The controller can either be in pairable mode or non-pairable mode. In non-pairable mode pairing requests from the remote device are automatically rejected. If the host does no set the pairing mode, the controller will be in pairable mode.

Command Parameters:

Pairing_Mode: *Size: 1 Octet*

Value	Parameter Description
0x00	Non-Pairable Mode
0x01	Pairable Mode (default)

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Write_Pairing_Mode command succeeded
0x01 - 0xFF	Infineon_Write_Pairing_Mode command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Write_Pairing_Mode command has completed execution, a Command Complete event will be generated.

6.1.4.8 Infineon_Burstcomposer_Config

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Burstcomposer_Config	0x3F	0x0044	Hopping_Mode RX_Single_frequency, TX_Single_frequency, Scrambler_Mode	Status

Description:

With this command both the Hopping Mode and the Scrambling Mode can be switched on and off. In case the Hopping Mode is switched off the Single_frequency for receive and transmit can be specified. Otherwise the parameters will be ignored.

This command is for debugging only.

Command Parameters:

Hopping_Mode: *Size: 1 Octet*

Value	Parameter Description
0x00	Hopping switched off
0x01	Hopping switched on (default)
0x02 - 0xFF	Reserved

RX_Single_frequency: *Size:1 Octet*

Value	Parameter Description
0<= k <= 93	RX Single_frequency = [2402+k]MHz to receive on a fixed channel. (default = 0, i.e. 2.402 GHz) *Note: this parameter will be ignored if the Hopping_Mode is switched on.*

TX_Single_frequency: *Size: 1 Octet*

Value	Parameter Description
0<= k <= 93	RX Single_frequency = [2402+k]MHz to transmit on a fixed channel. (default = 0, i.e. 2.402 GHz) *Note: this parameter will be ignored if the Hopping_Mode is switched on.*

Scrambler_Mode: *Size: 1 Octet*

Value	Parameter Description
0x00	Scrambler switched off
0x01	Scrambler switched on (default)
0x02 - 0xFF	Reserved

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	HCI_Infineon_Burstcomposer_Config command succeeded
0x01 - 0xFF	IHCI_Infineon_Burstcomposer_Config command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Burstcomposer_Config command has completed execution, a Command Complete event will be generated.

6.1.5 HCI+ Test Mode Commands

6.1.5.1 Infineon_Test_Mode (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Test_Mode	0x3F	0x001A	Test Scenario, Packet_type, Bit_pattern, Single_frequency, TX_Burst_period, Scrambler_Mode, Power_Level, Packet_size	Status

Description:

This command is only accepted in Manufacturer Mode (M).

Four different test modes can be activated with the HCI_Infineon_Test_Mode command:

- TX Burst Mode
- RX Burst Mode
- RX Burst Mode with data transparently sent to host
- RX Bit & Packet Error Rate measurement mode
-

For all four modes frequency hopping is switched off and the frequency defined with the parameter *Single_frequency* is used.

When already in Test mode this command can be sent again to just change the parameters.

When in Test mode the controller uses the Access Code etc. derived from the local BD_ADDR.

The test scenarios provide the following functionality:

TX Burst Mode

In TX Burst Mode, the controller sends ACL data packets (DH1, DH3, DH5, 2-DH1, 2-DH3, 2-DH5, 3-DH1, 3-DH3 or 3-DH5) of length *Packet_size* and repeats those packets in a configured interval (*Tx_Burst_period*). Thus, it behaves like a master in point-to-point connection in active mode whose supervision time out has been switched off, and that tries to transmit a packet to a non-existent slave. Via the parameter *Scrambler_Mode* the scrambler is switched off (default) or on. No connection setup procedure needs to be performed to get into the TX burst mode.

The TST0 pin is active during transmission of the data packet.

Note: The packets are transmitted on the channel that is specified by the parameter Single_frequency and the interval between packets is defined by the parameter TX_Burst_period.

RX Burst Mode

Performance measurements (sensitivity, co-channel interference, adjacent channel interference, blocking, etc.) can be made with the RX Burst Mode receiver. In RX Burst Mode, the offset-compensated, synchronized received data is made available at the external pins TST0,TST1 and TST2 (receive signal after sliding correlator).

The TST3 pin is active during reception of the burst.

Note: In RX-Burst Mode, the parameter TX_Burst_period is ignored. The packets are received on the channel that is specified by the parameter Single_frequency.

RX Burst Mode with data transparently sent to host

The RX Burst Mode with data transparently sent to host allows the host system to evaluate the received data. The CRC is ignored so that all received packets are sent transparently to the host including the CRC.

Note: The parameter TX_Burst_period is ignored. The packets are received on the channel that is specified by the parameter Single_frequency.

RX BER/PER Measurement Mode

The result of the BER and PER measurements is reported to the host after every 1000 possible occasions when a packet is received or could be received (but is missing). The result is sent to the host via the **Infineon Active Tester Result Event**.

Note: The parameter TX_Burst_period is ignored. The chosen packet to be received is specified by the Packet_size parameter. The packets are received on the channel that is specified by the parameter Single_frequency. Only DH packet types are allowed in BER/PER measurement mode. The PER result is only valid when the transmitter sends a packet in every receive slot, i.e. TX_Burst_period of the transmitter is set to the smallest possible value.

*Note: See formulas in **Infineon Active Tester Result Event** on how to calculate the PER and BER.*

Command Parameters:

Test_Scenario: *Size: 1 Octet*

Value	Parameter Description
0x00	The Infineon Testmode is switched off.
0x01	The TX Burst Mode is switched on.
0x02	The RX Burst Mode is switched on.
0x03	The RX Burst Mode with data transparently sent to host switched on.
0x04	The RX Burst Mode with Bit Error Rate & Packet Error Rate Measurement mode is switched on. The result is reported through the **Infineon Active Tester Result Event**.

Packet_Type: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Packet Type used during the Test. Bits 3-0 Numbering as in TYPE field in the packet header (See Bluetooth Baseband specification) Bits 7-4 0: ACL/SCO 1: eSCO 2: Enhanced Data Rate ACL 3: Enhanced Data Rate eSCO 4-15: Reserved Other values are reserved.

Bit_pattern: *Size: 1 Octet*

Value	Parameter Description
0x01	All zero pattern (00...0)
0x02	All one pattern (11...1)
0x03	One bit alternating pattern (1010...10)
0x04	PRBS-9 sequence
0x09	Four bit alternating pattern (11110000...11110000)
0x0A	Two bit alternating pattern (11001100...1100)

Single_frequency: *Size: 1 Octet*

Value	Parameter Description
0<= k <= 93	Single_frequency = [2402+k] MHz to send/receive on a fixed channel. (default = 0, i.e. 2.402 GHz)

TX_Burst_period: *Size: 1 Octet*

Value	Parameter Description
0x02 - 0xFE	Interval between the beginning of the packets in TX burst mode in frames. *Note: This parameter is only valid for TX burst mode (in other modes the parameter will be ignored).*

Scrambler_Mode: *Size: 1 Octet*

Value	Parameter Description
0x00	Scrambler switched off (default)
0x01	Scrambler switched on
0x02 - 0xFF	Reserved

Power_Level: *Size: 1 Octet*

Value	Parameter Description
0x01-0x04	Power Level used for transmitting packets. 0x01 refers to the lowest power level, 0x04 the highest
0x00, 0x05 - 0xFF	Reserved

Packet_size: *Size: 2 Octets*

Value	Parameter Description
0x0000-0x03FD	Number of bytes to be sent in each packet to be sent or received
0x03FE-FFFF	Reserved

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Test_Mode command succeeded
0x01 - 0xFF	Infineon_Test_Mode command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the Infineon_Test_Mode command has completed execution, a Command Complete event will be generated.

Note: When the RX Burst Mode with Bit Error Rate and Packet Error Rate Measurement mode is switched on. The result is reported through the Infineon Active Tester Result Event.

6.1.5.2 Infineon_Activate_Deactivate_Traces (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Activate_ Deactivate_ Traces	0x3F	0x0043	Transmit_ Trace_ Activation, Transmit_ ARQ_Trace_ Activation Receive_ Trace_ Activation	

Description:

This command is only accepted in Manufacturer Mode (M).

This command is used to activate or deactivate traces of Link Manager traffic (LMP-PDUs) for the host. Hence the host can be informed about all received and transmitted

LMP messages. For the transmitted PDU a trace can also show, when the PDU was actually transmitted over the air, i.e. an ARQ for the LMP has been received.

Command Parameters:

Transmit_Trace_Activation: *Size: 1 Octet*

Value	Parameter Description
0x00	Deactivation of traces corresponding to a transmitted LMP PDU
0x01	Activation of traces corresponding to a transmitted LMP PDU

Transmit_ARQ_Trace_Activation: *Size: 1 Octet*

Value	Parameter Description
0x00	Deactivation of ARQ traces corresponding to a transmitted LMP PDU
0x01	Activation of ARQ traces corresponding to a transmitted LMP PDU

Receive_Trace_Activation: *Size: 1 Octet*

Value	Parameter Description
0x00	Deactivation of traces corresponding to a received LMP PDU
0x01	Activation of traces corresponding to a received LMP PDU

Return Parameters:

None.

Event(s) generated (unless masked away):

When the controller receives the HCI_Infineon_Activate_Deactivate_Traces command, the controller sends the Command Status event to the host.

As soon as one of the Activation commands succeeds, an **Infineon LMP PDU Trace Event** is sent whenever the corresponding LMP PDUs between Link Managers are transmitted or received, respectively.

*Note: No Command Complete event will be sent by the controller to indicate that this command has been completed. Instead, the **Infineon Activate Deactivate Traces Complete Event** will indicate that this command has been completed.*

6.1.5.3 Infineon_Active_Tester (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Active_Tester	0x3F	0x0045	Test_Scenario, Hopping_ Mode, TX_Frequency, RX_Frequency, Power_ control_mode, Poll_period, Packet_Type	

Description:

This command is only accepted in Manufacturer Mode (M).

The controller can act as a Bluetooth RF tester, running the Bluetooth test mode. In active tester mode, the controller can initiate all the test mode scenarios that are defined for the Bluetooth Test Mode:

- Pause Test Mode
- Transmitter test – 0 pattern
- Transmitter test – 1 pattern
- Transmitter test – 1010 pattern
- Pseudorandom bit sequence
- Closed Loop Back – ACL packets
- Closed Loop Back – (e)SCO packets
- ACL Packets without whitening
- (e)SCO Packets without whitening
- Transmitter test – 1111 0000 pattern
- Exit Test Mode

The controller must be the master in a point-to-point connection to go into Active Tester Mode. Substates are disabled automatically when entering active tester mode.

The controller runs BER and PER measurements on the test pattern. In the transmitter test scenarios, the received data packets are compared to the corresponding reference pattern. In the loopback test scenarios, the received data packets are compared to the corresponding packets that the controller has sent to the DUT.

The BER and PER results are sent to the host via the **Infineon Active Tester Result Event**. The result of the BER and PER measurements is reported to the host after every 1000 possible occasions when a packet is received or could be received (but is missing). After the measurement is completed the controller will automatically continue the current test until the test is stopped via the Infineon Active tester command.

The BER measurement is based only on the payload (full packets) and the packets with wrong CRC or HEC are ignored. For the transmitter test mode, only packets without FEC should be used; i.e. HV3, EV3, EV5, DH1, DH3, DH5, 2-EV3, 2-EV5, 3-EV3, 3-EV5, 2-DH1, 2-DH3, 2-DH5, 3-DH1, 3-DH3, 3-DH5 and AUX1 packets.

The BER measurement is based on the correctly received packets and packets with CRC errors only. Packets that fails on the HEC check, have invalid payload length and packets that were expected but not received are ignored.

The PER measurement is based on packets that fails on the HEC check, have invalid payload length and packets that were expected but not received. Correct packets and packets with CRC errors are ignored.

For EDR packet tests, the synchronization sequence is checked and packets that fails the check will be added to the PER measurement.

*Note: See formulas in **Infineon Active Tester Result Event** on how to calculate the PER and BER.*

Command Parameters:

Test_Scenario: *Size: 1 Octet*

Value	Parameter Description
0x00	Pause Test Mode
0x01	Transmitter test – 0 pattern
0x02	Transmitter test – 1 pattern
0x03	Transmitter test – 1010 pattern
0x04	Transmitter test – Pseudorandom bit sequence
0x05	Closed Loop Back – ACL packets
0x06	Closed Loop Back – (e)SCO packets
0x07	Closed Loop Back – ACL Packets without whitening
0x08	Closed Loop Back – (e)SCO Packets without whitening
0x09	Transmitter test – 1111 0000 pattern
0x0A - 0xFE	Reserved
0xFF	Exit Test Mode

Hopping_mode: *Size: 1 Octet*

Value	Parameter Description
0x00	RX/TX on single frequency

Value	Parameter Description
0x01	Normal hopping
0x02 - 0xFF	Reserved

TX_frequency: *Size: 1 Octet*

Value	Parameter Description
0<= k <= 93	tx_frequency = [2402+k]MHz in case of fixed channel mode

RX_frequency: *Size: 1 Octet*

Value	Parameter Description
0<= k <= 93	rx_frequency = [2402+k]MHz in case of fixed channel mode

Power_Control_mode: *Size: 1 Octet*

Value	Parameter Description
0x00	Fixed TX output power
0x01	Adaptive power control
0x02 - 0xFF	Reserved

Poll_Period: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Poll period in TDD frames (n * 1.25 ms) *Note: The recommended poll period should be at least twice as long as the packet size used. E.g. for DH5 packets the poll period should be five frames.*

Packet_Type: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Packet Type used during the Test. Bits 3-0 Numbering as in TYPE field in the packet header (See Bluetooth Baseband specification) Bits 7-4 0: ACL/SCO 1: eSCO 2: Enhanced Data Rate ACL 3: Enhanced Data Rate eSCO 4-15: Reserved Other values are reserved.

Return Parameters:

None.

Event(s) generated (unless masked away):

When the controller receives the HCI_Infineon_Active_Tester command, the controller sends the Command Status event to the host. No Command Complete event will be sent by the controller to indicate that this command has been completed. Instead, the **Infineon Active Tester Complete Event** will indicate that this command has been completed.

*Note: The **Infineon Active Tester Result Event** will periodically report PER and BER measurement data to the host.*

6.1.5.4 Infineon_Enable_PCM_Loopback

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Enable_PCM_Loopback	0x3F	0x001C	PCM_Loopback	Status

Description:

This command enables and disables PCM loopback modes as described below.

Internal PCM loopback

When internal PCM loopback is enabled, data is looped back at the “internal side” of the PCM interface as shown in **Figure 6-2**. This type of loopback can only be used when an eSCO/SCO link has been established.

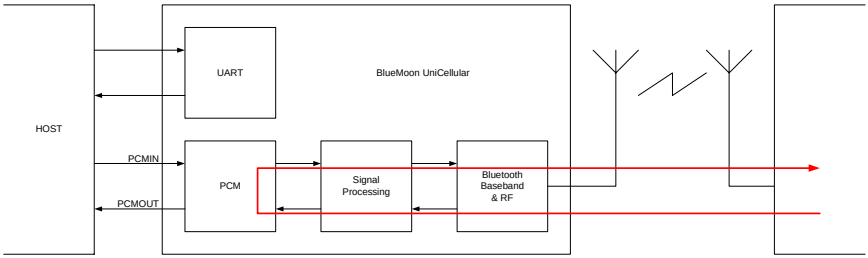


Figure 6-2 Internal PCM Loopback

External PCM loopback

When external PCM loopback is enabled, data is looped back at the “external side” of the PCM interface as shown in **Figure 6-3**. This type of loopback does not require that an eSCO/SCO link exists.

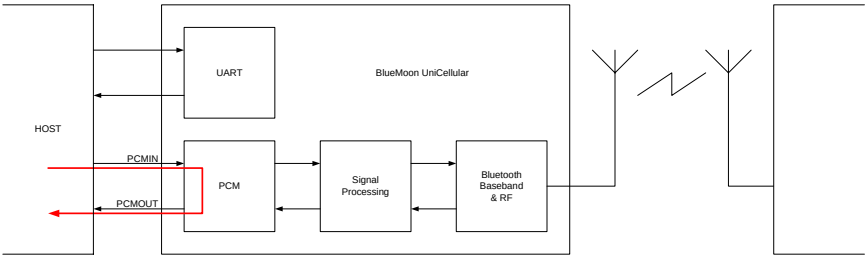


Figure 6-3 External PCM Loopback

Signal processing PCM loopback

Signal processing PCM loopback is a variant of external PCM loopback. Instead of being looped back in the PCM interface, the data is first passed through the signal processing path as shown in **Figure 6-4**.

Configuration of the signal processing path is done with **Infineon_Gain_Setting** and **Infineon_Signal_Proc_Config** using the special connection handle 0xFFFF.

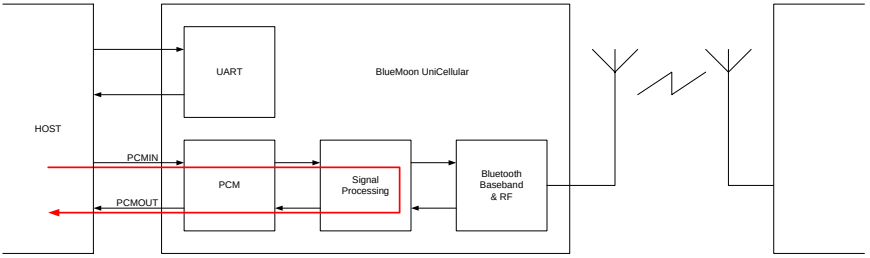


Figure 6-4 Signal Processing PCM Loopback

Command Parameters:

PCM_Loopback: *Size: 1 Octet*

Value (bits)	Parameter Description
XXXX0000	PCM loopback disabled (default)
XXXX0001	Internal PCM loopback enabled on channels 1 and 2
XXXX0010	External PCM loopback enabled on channels 1 and 2
XXXX0100	Signal processing PCM loopback enabled on channel 1
XXXX1000	Signal processing PCM loopback enabled on channel 2

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Enable_PCM_Loopback command succeeded
0x01 - 0xFF	Infineon_Enable_PCM_Loopback command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Enable_PCM_Loopback command has completed execution, a Command Complete event will be generated.

6.1.5.5 Infineon_Send_LMP (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_ Send_LMP	0x3F	0x0025	Connection_ Handle, LMP_ ACK, Data[i]	Status

Description:

This command is only accepted in Manufacturer Mode (M).

This command orders the controller to send an LMP PDU contained in the parameter Data[i] to the remote device on the stated connection handle. The LMP_ACK parameter specifies whether or not the packet shall be acknowledged at LMP level.

Command Parameters:

Connection_Handle: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0x0EFF	Connection handle

LMP_ACK: *Size: 1 Octet*

Value (bits)	Parameter Description
0x00-0x01	0x00 no ACK requested 0x01 ACK requested

Data[i]: *Size: i Octets*

Value (bits)	Parameter Description
0x00 - 0xFF (each byte)	LMP PDU to be send to the remote device

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Send_LMP command succeeded
0x01 - 0xFF	Infineon_Send_LMP command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

When the HCI_Infineon_Send_LMP command has completed execution, a Command Complete event will be generated

6.1.5.6 Infineon_Stimulate_Exception (M)

Command	OGF	OCF	Command Parameters	Return Parameters
HCI_Infineon_Stimulate_Exception	0x3F	0x004D	Exception_Type	Status

Description:

This command is only accepted in Manufacturer Mode (M).

This command is used to test the sending of a fatal exception and a debug exception.

Command Parameters:

Exception_Type: *Size: 1 Octet*

Value	Parameter Description
0x00	Fatal Exception
0x01	Debug Exception

Return Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Stimulate_Exception command succeeded
0x01 - 0xFF	Infineon_Stimulate_Exception command failed. See list of error codes in Bluetooth specification

Event(s) generated (unless masked away):

The response from this command depends on the parameter Exception_Type.

If Exception_Type is “Fatal Exception”, the controller will be reset and an Infineon Fatal Exception event will be generated. The fatal exception can be read with HCI_Infineon_Get_Exception_Info and cleared with HCI_Infineon_Clear_Exception_Info.

If Exception_Type is “Debug Exception”, a Command Complete event will be generated. If Infineon events are enabled, an Infineon Debug Exception event will be generated before the Command Complete event.

6.2 Infineon-specific HCI Events

The Event Code for all Infineon-specific events is 0xFF. The structure is shown in **Figure 6-5**.

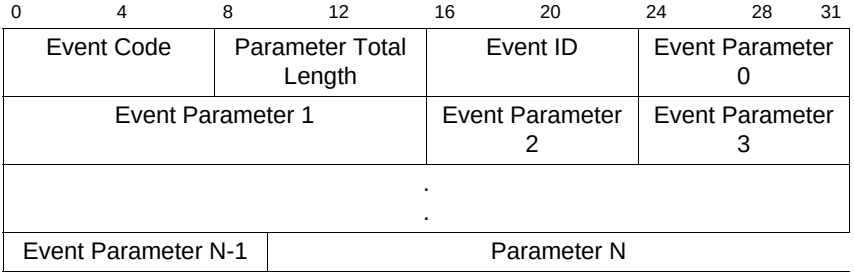


Figure 6-5 Structure of Infineon-specific HCI Events

6.2.1 Table of Infineon-specific Events

Table 6-3 gives an overview of the Infineon-specific events described in **Section 6.2.2**.

Table 6-3 Infineon-specific HCI Events

Event ID	Event
0x00	**"Infineon Startup Event" on Page 184**
0x01	**"Infineon Fatal Exception Event" on Page 201**
0x05	**"Infineon Default BD Data Event" on Page 185**
0x08	**"Infineon Debug Exception Event" on Page 200**
0x09	**"Infineon Invalid ACL_BC_PB_Flag Event" on Page 187**
0x0A	**"Infineon Invalid ACL_CNC_Handle Event" on Page 187**
0x0B	**"Infineon Invalid SCO_CNC_Handle Event" on Page 187**
0x0C	**"Infineon Low Power Mode Start Event" on Page 188**
0x0D	**"Infineon Low Power Mode End Event" on Page 188**
0x0E	**"Infineon LM Data Invalid Event" on Page 188**
0x11	**"Infineon Scan Status Event" on Page 189**
0x12	**"Infineon Set UART Baudrate Complete Event" on Page 189**
0x16	**"Infineon Activate Deactivate Traces Complete Event" on Page 190**

Event ID	Event
0x17	**“Infineon LMP PDU Trace Event” on Page 190**
0x10	**“Infineon Active Tester Result Event” on Page 192**
0x19	**“Infineon Write BD Data Complete Event” on Page 193**
0x1A	**“Infineon AFH Info Events” on Page 193**
0x1B	**“Infineon AFH Info Events” on Page 193**
0x1C	**“Infineon AFH Info Events” on Page 193**
0x1E	**“Infineon CQDDR Info Event” on Page 199**
0x1F	**“Infineon AFH Extraordinary RSSI Event” on Page 198**
0x20	**“Infineon AFH Info Events” on Page 193**
0x21	**“Infineon AFH Info Events” on Page 193**
0x22	**“Infineon AFH Info Events” on Page 193**
0x23	**“Infineon AFH Info Events” on Page 193**
0x24	**“Infineon AFH Info Events” on Page 193**
0x25	**“Infineon SCO Rejected Via LMP Event” on Page 185**
0x26	**“Infineon PTT Switch Notification Event” on Page 186**
0x27	**“Infineon Active Tester Complete Event” on Page 186**

6.2.2 Regular Events

6.2.2.1 Infineon Startup Event

Event	Event ID	Event Parameters
Infineon Startup Event	0x00	

Description:

After startup of the controller, the device searches for a valid set of Bluetooth device data in non-volatile memory and internal RAM. This data consists of the clock information, BD_ADDR, and other configurations. If valid BD_Data is found in the external EEPROM or internal RAM, the Infineon Startup event is generated.

Event Parameters:

None.

6.2.2.2 Infineon Default BD Data Event

Event	Event ID	Event Parameters
Infineon Default BD Data	0x05	Memory Status

Description:

After startup of the controller, the device searches for valid BD_Data in the non-volatile memory and internal RAM. If valid data is not found in the external EEPROM or internal RAM, the default BD_Data is loaded and the Infineon Default BD Data event is generated.

Note: This event cannot be masked.

Event Parameters:

Memory Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Reserved for future use
0x01	External EEPROM is available. Manufacturing data in EEPROM and RAM is invalid or does not exist. Default BD_Data is used.
0x02	No external EEPROM available. Manufacturing data in RAM is invalid or does not exist. Default BD_Data used.

6.2.2.3 Infineon SCO Rejected Via LMP Event

Event	Event ID	Event Parameters
Infineon SCO Rejected via LMP	0x25	BD_ADDR, Reason

Description:

If enabled with **Infineon_Enable_Infineon_Events (M)**, this event occurs when the link manager rejects an LMP_SCO_link_req (in which case the host wouldn't usually be informed). The Bluetooth Device Address of the rejected device and reason for rejecting the request is given in the parameters *BD_ADDR* and *Reason*.

Event Parameters:

BD_ADDR: *Size: 6 Octets*

Value	Parameter Description
0xXXXXXXXXXXXX	Bluetooth device address of the device from which the eSCO/ SCO connection request was rejected.

Reason: *Size: 1 Octet*

Value	Parameter Description
0x01 - 0xFF	Reason for rejection of eSCO/SCO request. See list of error codes in Bluetooth specification.

6.2.2.4 Infineon PTT Switch Notification Event

Event	Event ID	Event Parameters
Infineon PTT_switch_notification	0x26	Connection_Handle, PTT

Description:

If enabled with **Infineon_Enable_Infineon_Events (M)**, this event notifies the host when the Packet Type Table has been switched.

Connection_Handle: *Size: 2 Octets*

Value	Parameter Description
0xXXXX	The Connection handle for which the PTT has been switched

PTT: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0x01	PTT=0x00 means basic rate (1 Mbps). PTT=0x01 means enhanced data rate (2 or 3 Mbps)

6.2.2.5 Infineon Active Tester Complete Event

Event	Event ID	Event Parameters
Infineon Active Tester Complete Event	0x27	Status

Description:

This event is the response to the **Infineon_Active_Tester (M)** command.

Event Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Command Succeeded
0x01-0xFF	Command Failed

6.2.2.6 Infineon Invalid ACL_BC_PB_Flag Event

Event	Event ID	Event Parameters
Infineon Invalid ACL_BC_PB_Flag	0x09	

Description:

This event reports an invalid BC or PB flag in the packet header of an HCI packet.

Event Parameters:

None.

6.2.2.7 Infineon Invalid ACL_CNC_Handle Event

Event	Event ID	Event Parameters
Infineon Invalid ACL_CNC_Handle	0x0A	

Description:

This event reports an ACL packet with an unexpected connection handle.

Event Parameters:

None.

6.2.2.8 Infineon Invalid SCO_CNC_Handle Event

Event	Event ID	Event Parameters
Infineon Invalid SCO_CNC_Handle	0x0B	

Description:

This event reports a synchronous data packet (eSCO/SCO) with an unexpected connection handle.

Event Parameters:

None.

6.2.2.9 Infineon Low Power Mode Start Event

Event	Event ID	Event Parameters
Infineon Low Power Mode Start Event	0x0C	

Description:

This event is only used with the HCI UART-6W transport layer. The event indicates that the controller will enter low power mode. It is only sent when the controller knows that the host is in the “active” state.

Event Parameters:

None.

6.2.2.10 Infineon Low Power Mode End Event

Event	Event ID	Event Parameters
Infineon Low Power Mode End	0x0D	

Description:

This event is only used with the HCI UART-6W transport layer. The event indicates that the controller will leave low power mode. It is only sent when the controller knows that the host is in the “active” state.

Event Parameters:

None.

6.2.2.11 Infineon LM Data Invalid Event

Event	Event ID	Event Parameters
Infineon LM Data Invalid	0x0E	

Description:

The Infineon LM Data Invalid event is generated at startup if the consistency check on the controller data storage area of the external EEPROM fails. If this occurs, all data in this storage area will be reset to their default values, e.g. link keys will be deleted, the device's name will be reset to "IFX BlueMoon Universal Platform".

6.2.2.12 Infineon Scan Status Event

Event	Event ID	Event Parameters
Infineon Scan Status	0x11	Scan_Enable

Description:

If enabled with **Infineon_Enable_Infineon_Events (M)**, this event is sent to the host to indicate that the scan settings (set by the host with HCI_Write_Scan_Enable) have been temporarily changed. This is necessary in e.g. scatternet scenarios. When the limiting scenario is no longer present, the original host setting is restored and another Infineon Scan Status event is sent.

The current scan status is given in the parameter Scan_Enable. This parameter also indicates whether the interlaced scan mode is currently active.

Event Parameters:

Scan_Enable: *Size: 1 Octet*

Value	Parameter Description
XXXXXXX0	Inquiry Scan is disabled
XXXXXXX1	Inquiry Scan is enabled
XXXXXX0X	Page Scan is disabled
XXXXXX1X	Page Scan is enabled
XXXXX0XX	Interlaced Scan Mode for Inquiry Scan is disabled
XXXXX1XX	Interlaced Scan Mode for Inquiry Scan is enabled
XXXX0XXX	Interlaced Scan Mode for Page Scan is disabled
XXXX1XXX	Interlaced Scan Mode for Page Scan is enabled

6.2.2.13 Infineon Set UART Baudrate Complete Event

Event	Event ID	Event Parameters
Infineon Set UART Baudrate Complete	0x12	Status

Description:

The Infineon Set UART Baudrate Complete Event is used to indicate that the UART baudrate has been modified.

Event Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Infineon_Set_UART_Baudrate command succeeded
0x01 - 0xFF	Infineon_Set_UART_Baudrate command failed. See list of error codes in Bluetooth specification

6.2.2.14 Infineon Activate Deactivate Traces Complete Event

Event	Event ID	Event Parameters
Infineon Activate Deactivate Traces Complete	0x16	Status

Description:

This event is the response to the **Infineon_Activate_Deactivate_Traces (M)** command.

Event Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	Succeed

6.2.2.15 Infineon LMP PDU Trace Event

Event	Event ID	Embedded Messages
Infineon LMP PDU Trace	0x17	Trace_Event_Type, Connection_Handle, Content

Description:

The Infineon LMP PDU Trace event serves as a Link Manager tracer, i.e. all LMP PDUs that are received or transmitted by the LM can be traced in the host. The event will be sent only in case a preceding **Infineon_Activate_Deactivate_Traces (M)** command with the corresponding parameters (Activation of Receive/Transmit Traces) succeeds.

*Note: There is no corresponding command for this event because once the **Infineon_Activate_Deactivate_Traces (M)** command succeeds, the event will be sent whenever a PDU is received or transmitted, respectively. The length of the event*

message (i.e. the length of the parameter 'Content') depends on the Trace_ Event_Type.

Embedded Messages:

Trace_Event_Type: *Size: 1 Octet*

Value	Embedded Message Description
0x00	Trace of received LMP-PDU (RX LMP)
0x01	Trace of transmitted LMP-PDU (TX LMP)
0x02	Trace of received ACK for transmitted LMP-PDU (ACK LMP)

Connection_Handle: *Size: 2 Octets*

Value	Embedded Message Description
0x0000 - 0x0EFF	Connection handle

Content:

Trace_ Event_Type	Value	Content Description	Size in Octet
RX LMP	0x00 - 0xFF	Transaction_ID and PDU OP Code (see Bluetooth specification)	1
	0x00 - 0xFF (each Byte)	PDU parameter data (n=XXXXX-1)	n
	0xXX...XX	CLK: Bluetooth Piconet Clock of the link with the above connection handle	4
TX LMP	0x00 - 0xFF	Transaction_ID and PDU OP Code (see Bluetooth specification)	1
	0x00 - 0xFF (each Byte)	PDU parameter data (n=XXXXX-1)	n
	0xXX...XX	CLK: Bluetooth Piconet Clock of the link with the above connection handle	4
	0x00 - 0xFF	LMP ID: this value uniquely identifies the transmitted LMP	1
ACK LMP	0xXX...XX	CLK: Bluetooth Piconet Clock of the link with the above connection handle	4
	0x00 - 0xFF	LMP ID: this value uniquely identifies the transmitted LMP	1

6.2.2.16 Infineon Active Tester Result Event

Event	Event ID	Event Parameters
Infineon Active Tester Result	0x18	Status, Num_Bit_Errors, Num_ Packet_Errors

Description:

This event is generated when running PER/BER measurements initialized by the **Infineon_Active_Tester (M)** or **Infineon_Test_Mode (M)** commands.

Event Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	BER/PER test that was performed successfully.
0x01-0xFF	BER/PER test failed. See list of error codes in Bluetooth specification.

Number_of_Bit_Errors: *Size: 4 Octets*

Value	Parameter Description
0x00000000- 0xFFFFFFFF	The accumulated number of bit errors

Number_of_Packet_Errors: *Size: 2 Octets*

Value	Parameter Description
0x0000- 0xFFFF	The accumulated number of packet errors

Formulas to calculate the error rate:

$$PER = \frac{A}{B}$$

Where A = *Number_of_Packet_Errors* and B = 1000.

$$BER = \frac{X}{8 \times Y \times Packetsize}$$

Where X = *Number_of_Bit_Errors* and Y = 1000-*Number_of_Packet_Errors*.

Note: The packet size (in bytes) is dependent on size of the packet used in the current test.

6.2.2.17 Infineon Write BD Data Complete Event

Event	Event ID	Event Parameters
Infineon Write BD Data Complete	0x19	Status

Description:

This event is generated when the **Infineon_Write_BD_Data (M)** command has been completed.

Event Parameters:

Status: *Size: 1 Octet*

Value	Parameter Description
0x00	**Infineon_Write_BD_Data (M)** command succeeded
0x01 - 0xFF	**Infineon_Write_BD_Data (M)** command failed. See list of error codes in Bluetooth specification

6.2.2.18 Infineon AFH Info Events

Event	Event ID	Event Parameters
Infineon AFH Info A Event	0x1A	Number_Of_Subblocks, Info_ID[x], Subblock_Length[x], Info_Data[x]
Infineon AFH Info B Event	0x1B	Number_Of_Subblocks, Info_ID[x], Subblock_Length[x], Info_Data[x]
Infineon AFH Info C Event	0x1C	Number_Of_Subblocks, Info_ID[x], Subblock_Length[x], Info_Data[x]
Infineon AFH Info D Event	0x20	Number_Of_Subblocks, Info_ID[x], Subblock_Length[x], Info_Data[x]

Event	Event ID	Event Parameters
Infineon AFH Info E Event	0x21	Number_Of_Subblocks, Info_ID[x], Subblock_Length[x], Info_Data[x]
Infineon AFH Info F Event	0x22	Number_Of_Subblocks, Info_ID[x], Subblock_Length[x], Info_Data[x]
Infineon AFH Info G Event	0x23	Number_Of_Subblocks, Info_ID[x], Subblock_Length[x], Info_Data[x]
Infineon AFH Info H Event	0x24	Number_Of_Subblocks, Info_ID[x], Subblock_Length[x], Info_Data[x]

Note: x = 1...y (Number_Of_Subblocks)

Description:

The AFH Info Events gives information about the AFH. Once enabled with the **Infineon_Enable_AFH_Info_Sending** command, AFH Info Events A - H will be sent with updated information every time a new channel map is generated.

An AFH Info Event consists of a header (includes the *Number_Of_Subblocks* y) and of y information data subblocks. The subblocks contain the *Info_ID*, the *Subblock_Length* and the *Info_Data*. The format of the AFH Info Event is always the same and is shown below.

Note: If the device is in sleep mode, enabling an AFH Info Event increases power consumption because the device must wake up.

Note: The number of Info_IDs that can be enabled is limited to a maximum total size. The total size must be less or equal to 680 bytes otherwise the command is rejected.

Header	Number_Of_ Subblocks y

Info data subblock 1	Info_ID 1
	Subblock_ Length 1
	Info_Data 1
Info data subblock y	Info_ID y
	Subblock_ Length y
	Info_Data y

Event Parameters:

Number_Of_Subblocks: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Number of Info data subblocks

Info_ID: *Size: 1 Octet*

Value	Parameter Description
0x01 - 0xFF	Info ID for Subblock x (see **Page 196** for possible info IDs; they are different for all AFH Info Events)
0x00	In case an info ID is required but is unknown or not available for the Bluetooth device

Subblock_Length: *Size: 1 Octet*

Value	Parameter Description
0x04 - 0xFC	Length of Subblock x

Info_Data: *Size: 0-n Octets*

Value	Parameter Description
Info_Data_Values (each Byte 0x00 - 0xFF) (see table on **Page 196** for possible values)	Info data for Subblock x

Info_Data_Values:

	Value	Info Data Description	Info_ID	Size in Octet
AFH Info A	0x0000 - 0x0EFF	Connection Handle *Note: The connection handle will be reported anyway (even if it is not triggered by the HCI_Infineon_Enable_AFH_Info_Sending command)*	0x01	2
	0xXXXX...XX	Channel Classification: First Byte contains the channel classification for channels 0-3, second Byte for channels 4-7 and so on. The two bit field per channel is interpreted as follows: 00: channel is unknown 01: channel is good 10: reserved 11: channel is bad	0x02	20
	0xXXXXX...X	Channel Map: The structure of this field is identical to the parameter AFH_Channel_Map in the LMP_set_AFH message The nth (numbering from 0) field (in the range 0 to 78) contains the value for channel n. Bit 79 is reserved. The 1-bit field is interpreted as follows: 0: channel n is unused 1: channel n is used	0x03	10
	0x00 - 0xFF	Interferer Identification 0x00 Unknown 0x01 Wireless LAN Band I 0x02 Wireless LAN Band II 0x04 Wireless LAN Band III 0x08 GSM 850 0x10 Microwave 0x20 Reserved for future use 0x40 Reserved for future use 0x80 Reserved for future use	0x04	1

	Value	Info Data Description	Info_ID	Size in Octet
AFH Info B	0xXXXX...XX	RSSI values: Gives the sum of all RSSI values that have been measured within one measuring period. The nth (numbering from 0) Byte (in the range 0 to 78) contains the value for channel n.	0x05	158
AFH Info C	0xXXXX...XX	RSSI counter: Gives the number of RSSI measurements that have been made on the specific channel during one measuring period. The nth (numbering from 0) Byte (in the range 0 to 78) contains the value for channel n.	0x06	79
AFH Info D	0xXXXX...XX	BER values: Gives the sum of bit error values that have been counted within one measuring period. The nth (numbering from 0) Byte (in the range 0 to 78) contains the value for channel n.	0x07	79
AFH Info E	0xXXXX...XX	BER counter: Gives the number of bit error measurements that have been made on the specific channel during one measuring period. The nth (numbering from 0) Byte (in the range 0 to 78) contains the value for channel n.	0x08	79
AFH Info F	0xXXXX...XX	Number Received Packets: Gives the total number of received packets during one measurement period. This includes both those packets with valid CRC and packets with invalid CRC. Packets where the HEC is corrupt are not counted. The nth (numbering from 0) two Bytes (n in the range 0 to 78) contain the value for channel 0, 1, 2, 3,..	0x09	158

	Value	Info Data Description	Info_ID	Size in Octet
AFH Info G	0xXXXX...XX	Number Total Bytes: Gives the total number of received Bytes during one measurement period. The nth (numbering from 0) two Bytes (n in the range 0 to 78) contain the value for channel 0, 1, 2, 3,..	0x0A	158
AFH Info H	0xXXXX...XX	Number CRC errors: Gives the number of received DH packets with an invalid CRC. The nth (numbering from 0) two Bytes (n in the range 0 to 78) contain the value for channel 0, 1, 2,..	0x0B	158

6.2.2.19 Infineon AFH Extraordinary RSSI Event

Event	Event ID	Event Parameters
Infineon AFH Extraordinary RSSI	0x1F	Extra_RSSI_active

Description:

If enabled with **Infineon_Enable_Infineon_Events (M)**, this event informs the host when the device starts extraordinary RSSI measurements in unused frames. Extraordinary RSSI measurements are performed in unused frames if the number of used channels decreases below a limit value ($N_{used} < N_{THRS}$), and periodically after a defined time. Whenever this is the case, the event will be generated with *Extra_RSSI_active*=1. This event indicates that there is a lot of interference in the surroundings, and that power consumption will increase during the next measurement interval. When extraordinary RSSI measurements are no longer necessary, the event parameter *Extra_RSSI_active* is set to 0.

Event Parameters:

Extra_RSSI_active: *Size: 1 Octet*

Value	Parameter Description
0x01	Extraordinary RSSI measurements for AFH are performed in unused frames during the next measurement interval.
0x00	No extraordinary RSSI measurements for AFH are performed during the next measurement interval.

6.2.2.20 Infineon CQDDR Info Event

Event	Event ID	Event Parameters
Infineon CQDDR Info	0x1E	N_RX_DM, N_RX_Bytes_DM, N_RX_FEC_DM, N_RX_DH, N_RX_CRC_DH

Description:

The CQDDR Info Event gives information about CQDDR. Once enabled with the **Infineon_Enable_CQDDR_Info_Sending** command, the CQDDR Info Event will be sent with updated information every time a new packet type proposal is sent to the remote device.

Event Parameters:

N_RX_DM: *Size: 7*2 Octets*

Value	Parameter Description
0xXXXXX...XXX	Number of received DM packets N_RX_DM during one measurement interval. This includes packets with either valid or invalid CRC. Packets where the HEC is corrupt are not counted. The nth pair of bytes (n in the range 1 to 7) contain the value for link n.

N_RX_Bytes_DM: *Size: 7*2 Octets*

Value	Parameter Description
0xXXXXX...XXX	Number of received Bytes N_RX_Bytes_DM in both DM packets during one measurement interval. This includes packets with either valid or invalid CRC. Packets where the HEC is corrupt are not counted. The nth pair of bytes (n in the range 1 to 7) contain the value for link n.

N_RX_FEC_DM: *Size: 7*2 Octets*

Value	Parameter Description
0xXXXXX...XXX	0xXXXXX...XXX Number of bits N_RX_FEC_DM that have been corrected by the hardware in received DM packets. The nth two Bytes (n in the range 1 to 7) contain the value for link n.

N_RX_DH: *Size: 14 Octets*

Value	Parameter Description
0xXXXXX...XXX	Number of received DH packets N_RX_DH during one measurement interval. This includes packets with either valid or invalid CRC. Packets where the HEC is corrupt are not counted. The nth two Bytes (n in the range 1 to 7) contain the value for link n.

N_RX_CRC_DH: *Size: 14 Octets*

Value	Parameter Description
0xXXXXX...XXX	Number or received DH packets with CRC error NRX_CRC. The nth two Bytes (n in the range 1 to 7) contain the value for link n.

6.2.2.21 Infineon Debug Exception Event

Event	Event ID	Event Parameters
Infineon Debug Exception	0x08	Line, Module, Reason

Description:

This event reports debug exceptions in the controller.

Event Parameters:

Line: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0xFFFF	Source line number where the exception occurred

Module: *Size: 1 Octet*

Value	Parameter Description
0x00	Reserved
0x01	BC
0x02	HCI
0x03	LLC
0x04	OS
0x05	LM
0x06	SC

Value	Parameter Description
0x07	SP
0x08	OSAL
0x09	LC
0x0A	Reserved
0x0B	TLD
0x0C - 0xEF	Reserved
0xF0	Debug
0xF1 - 0xFF	Reserved

Reason: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Module specific exception reason

6.2.2.22 Infineon Fatal Exception Event

Event	Event ID	Event Parameters
Infineon Fatal Exception	0x01	Line, Module, Reason

Description:

This event reports fatal exceptions in the controller.

In the unlikely event that the host receives an Infineon Fatal Exception event, the device has just been reset due to an internal fatal error. The host should then read the exeption code with HCI_Infineon_Get_Exception_Info and clear it with HCI_Infineon_Clear_Exception_Info.

Note: The controller performs a reset before this event is sent.

Event Parameters:

Line: *Size: 2 Octets*

Value	Parameter Description
0x0000 - 0xFFFF	Source line number where the exception occurred

Module: *Size: 1 Octet*

Value	Parameter Description
0x00	Reserved
0x01	BC
0x02	HCI
0x03	LLC
0x04	OS
0x05	LM
0x06	SC
0x07	SP
0x08	OSAL
0x09	LC
0x0A	App
0x0B	TLD
0x0C - 0xEF	Reserved
0xF0	Debug
0xF1 - 0xFF	Reserved

Reason: *Size: 1 Octet*

Value	Parameter Description
0x00 - 0xFF	Module specific exception reason

6.3 Infineon-specific Hardware Error Event Codes

The Hardware Error event is an HCI event specified in the HCI part of the Bluetooth specification. It is used to indicate some type of hardware failure for the controller and to notify the host that a specific (declared by the Hardware_Code parameter) hardware problem has occurred.

The structure of the Hardware Error event is specified in the Bluetooth specification.

Event Parameters:

Hardware_Code: *Size: 1 Octet*

Value	Parameter Description
0x00	Reserved
0x01	HW_ERR_EVENT_UNKNOWN

Value	Parameter Description
0x02	Reserved
0x03	Reserved
0x04	HW_ERR_EVENT_INVALID_PACKET_LEN: An invalid length in the payload header of a received data packet has been detected.
0x05	Reserved
0x06	HW_ERR_EVENT_AUTOCALIB_FAILED
0x07	HW_ERR_EVENT_INVALID_PACKET_TYPE: An HCI packet with an invalid packet type has been received. This indicates that the start of packets from the host are not detected, and there are synchronization problems on the UART.
0x08	HW_ERR_EVENT_WDOG_RESET: The controller recognizes that a Hardware Watchdog Reset has occurred. This situation should never occur in normal operation of the device, and indicates that the LM has run into a deadlock situation.
0x09	Reserved
0x0A	Reserved
0x0B	RF_INIT_FAILURE: If the VCO adjustment during startup fails this event will be sent from the controller.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Storage temperature	-55	150	°C	
VDD supply voltage	-0.9	4.0	V	
VDDUART supply voltage	-0.9	4.0	V	
VDDPCM supply voltage	-0.9	4.0	V	
VDDPM supply voltage	-0.3	1.7	V	
VDDRF supply voltage	-0.3	1.9	V	
Pad input voltage	-0.9	4.0	V	
RFIO/RFIOX voltage	-0.9	VDDRF+1.5	V	
TXA/TXAX voltage	-0.9	VDDRF+1.5	V	
TXA/TXAX current		9	mA	

Note: Stresses above those listed here are likely to cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.
Maximum ratings are not operating conditions.

7.2 Operating Conditions

Table 7-2 Operating Conditions

Parameter	Min	Max	Unit	Notes
Operating temperature	-40	85	°C	
VDD supply voltage	1.35	3.63	V	
VDDUART supply voltage	1.35	3.63	V	
VDDPCM supply voltage	1.35	3.63	V	
VDDPM supply voltage	1.35	1.65	V	

Table 7-2 Operating Conditions

Parameter	Min	Max	Unit	Notes
VDDPM supply voltage (reduced leakage current)	1.43	1.57	V	
VDDSUP supply voltage (internal VDDRF regulator used)	2.1	3.6	V	
VDDSUP supply voltage (VDDRF supplied externally)	1.8	3.6	V	

7.3 Power Consumption

Table 7-3 Current Consumption in Different Operating Modes

This table shows the VDDSUP current consumption in different operating modes. VDD, VDDUART and VDDPCM are not included as they mainly depend on external loads.

T=25°C, VDDSUP=3V, CLKIN=26MHz, CLK32=32.768kHz, Output Power=0dBm,

Parameters	Min	Typ	Max	Unit	Comment
Ultra Low Power Mode		11		µA	VDDPM supplied externally
		31		µA	VDDPM from internal regulator
Page & Inquiry Scan (1.28s)		0.89		mA	
Sniff (1.28s)		0.20		mA	
ACL (Transmit DH1)		38		mA	Basic Rate, 172.8 kb/s[1)]
ACL (Receive DH1)		35		mA	Basic Rate, 172.8 kb/s[1)]
ACL (Transmit 2-DH1)		40		mA	Enhanced Data Rate, 345.6 kb/s[1)]
ACL (Receive 2-DH1)		37		mA	Enhanced Data Rate, 345.6 kb/s[1)]
ACL (Transmit 3-DH1)		40		mA	Enhanced Data Rate, 531.2 kb/s[1)]
ACL (Receive 3-DH1)		37		mA	Enhanced Data Rate, 531.2 kb/s[1)]
SCO (HV3)		19		mA	
eSCO (Symmetric 64 kb/s, EV3)		20		mA	
eSCO (Symmetric 64 kb/s, 2-EV3)		13		mA	Enhanced Data Rate
eSCO (Symmetric 64 kb/s, 3-EV3)		11		mA	Enhanced Data Rate
eSCO (Symmetric 64 kb/s, EV5)		14		mA	
eSCO (Symmetric 64 kb/s, 2-EV5)		10		mA	Enhanced Data Rate
eSCO (Symmetric 64 kb/s, 3-EV5)		8.7		mA	Enhanced Data Rate

1) Figure indicates maximum possible data rate with this packet type

7.4 Supplies and Voltage Regulators

7.4.1 VDDSUP

Table 7-5 VDDSUP Characteristics (Internal VDDRF Regulator Used)

Parameters	Min	Typ	Max	Unit	Conditions
VDDSUP voltage	2.1		3.6	V	
Load			100	mA	Peak current
Max. tolerated ripple	100			mVpp	@ 1 MHz, 25°C
	25			mVpp	@ 100 kHz, 25°C
	100			mVpp	@ 10 kHz, 25°C

7.4.2 VDDPM

Table 7-6 VDDPM Characteristics[1)]

Parameters	Min	Typ	Max	Unit	Conditions
VDDPM voltage	1.35		1.65	V	
	1.43		1.57	V	Reduced leakage current
Load			1.5	mA	Peak current

1) Externally supplied VDDPM is not needed on PMB8753 A.

7.4.3 Integrated VDDPM Regulator

Table 7-7 VDDPM Regulator Characteristics

Parameters	Min	Typ	Max	Unit	Conditions
Supply current		10		µA	Idle
Dropout voltage		0.3		V	
Output Voltage (VDDPMREG)	1.35	1.5	1.65	V	Output current = 2mA
Load regulation			25	mV	Input voltage = 1.8V Output current ≤ 2mA
Line regulation		>40		dB	Input voltage = 2.5V - 3.6V Output current = 1mA

Table 7-7 VDDPM Regulator Characteristics

Parameters	Min	Typ	Max	Unit	Conditions
Output load[1)]			8	mA	
Output load[1)]			3	mA	Idle mode
Output load capacitance		100		nF	

1) Maximum load as design parameter only, not subject to test

7.4.4 Integrated VDDRF Regulator

Table 7-8 VDDRF Regulator Characteristics

Parameters	Min	Typ	Max	Unit	Conditions
Supply current		0.5		mA	Regulator on, no load connected
Dropout voltage			0.2	V	No line regulation if VDDSUP ≤ VDDRFREG + drop
Output voltage (VDDRFREG)	1.7	1.8	1.9	V	Output current = 50mA
Load regulation		50	150	mV	Input voltage = 2.1V Output current ≤ 50mA
Line regulation		>40		dB	Input voltage = 2.2V - 3.6V Output current = 50mA
Output load			50	mA	
Output load capacitance		100		nF	

7.5 Pads

7.5.1 Pad Driver and Input Stages

Table 7-9 VDD Supplied Pads (Except I2C Pads)

Parameter	Conditions	Min	Typ	Max	Unit
Input low voltage		-0.3		0.2·VDD	V

Table 7-9 VDD Supplied Pads (Except I2C Pads)

Parameter	Conditions	Min	Typ	Max	Unit
Input high voltage	P0.10/PSEL1	0.7·VDD		VDD	V
	JTAG#	0.7·VDD		VDD	V
	Other pads	0.7·VDD		3.63	V
Output low voltage	I_{OL} = 5mA, VDD = 2.5V			0.25	V
Output low voltage	I_{OL}=2mA, VDD = 2.5V			0.15	V
Output high voltage	I_{OH} = -5mA, VDD = 2.5V	VDD-0.25			V
Output high voltage	I_{OH} = -2mA, VDD = 2.5V	VDD-0.15			V
Continuous load[1)]				5	mA
Pin capacitance				10	pF
Pin leakage	Input and output drivers disabled		0.01	1	µA

1) The total continuous load for all pads shall not exceed 35mA.

Table 7-10 I2C Pads

Parameter	Conditions	Min	Typ	Max	Unit
Input low voltage		-0.3		0.2·VDD	V
Input high voltage		0.7·VDD		VDD	V
Output low voltage	I_{OL} = 3mA, VDD = 2.5V			0.1·VDD	V
Continuous load				3	mA
Pin capacitance				12	pF
Pin leakage	Input and output drivers disabled		0.01	1	µA

Table 7-11 VDDPCM Supplied Pads

Parameter	Conditions	Min	Typ	Max	Unit
Input low voltage		-0.3		0.2·VDDPCM	V
Input high voltage		0.7·VDDPCM		3.63	V
Output low voltage	I_{OL} = 5mA, VDDPCM = 2.5V			0.25	V
Output low voltage	I_{OL}=2mA, VDDPCM = 2.5V			0.15	V
Output high voltage	I_{OH} = -5mA, VDDPCM = 2.5V	VDDPCM-0.25			V
Output high voltage	I_{OH} = -2mA, VDDPCM = 2.5V	VDDPCM-0.15			V
Continuous load[1)]				5	mA
Pin capacitance				10	pF
Pin leakage	Input and output drivers disabled		0.01	1	µA

1) The total continuous load for all pads shall not exceed 35mA.

Table 7-12 VDDUART Supplied Pads

Parameter	Conditions	Min	Typ	Max	Unit
Input low voltage		-0.3		0.2·VDDUART	V
Input high voltage	P0.5/UARTRXD	0.7·VDDUART		VDDUART	V
	Other pads	0.7·VDDUART		3.63	V
Output low voltage	I_{OL} = 5mA, VDDUART = 2.5V			0.25	V
Output low voltage	I_{OL}=2mA, VDDUART= 2.5V			0.15	V
Output high voltage	I_{OH} = -5mA, VDDUART = 2.5V	VDDUART-0.25			V
Output high voltage	I_{OH} = -2mA, VDDUART = 2.5V	VDDUART-0.15			V
Continuous load[1)]				5	mA

Table 7-12 VDDUART Supplied Pads

Parameter	Conditions	Min	Typ	Max	Unit
Pin capacitance				10	pF
Pin leakage	Input and output drivers disabled		0.01	1	µA

1) The total continuous load for all pads shall not exceed 35mA.

Table 7-13 VDDPM Supplied Pads

Parameter	Conditions	Min	Typ	Max	Unit
Input low voltage		-0.3		0.2·VDDPM	V
Input high voltage		0.7·VDDPM		3.63	V
Output low voltage	I_{OL} = 1mA, VDDPM = 1.5V			0.25	V
Output high voltage	I_{OH} = -1mA, VDDPM = 1.5V	VDDPM-0.25			V
Continuous load[1)]	Internal VDDPM			1	mA
	External VDDPM			5	mA
Pin capacitance				10	pF
Pin leakage	Input and output drivers disabled		0.01	1	µA

1) The total continuous load for all VDDPM supplied pads shall not exceed 2mA when the internal VDDPM regulator is used.

7.5.2 Pull-ups and Pull-downs

Table 7-14 Pull-up and Pull-down Currents

Pin	Pull Up Current			Pull Down Current			Unit	Conditions
	Min	Typ	Max	Min	Typ	Max		
P0.12/SDA0, P0.13/SCL0	260	740	1300	N/A	N/A	N/A	µA	Pull-up current measured with pin voltage = 0V Pull-down current measured with pin voltage = supply voltage Min measured at 125°C with supply = 1.35V Typ measured at 27°C with supply = 2.5V Max measured at -40°C with supply = 3.63V
TRST#, JTAG#, P0.0/PCMFR1, P0.1/PCMCLK, P0.2/PCMIN, P0.3/PCMOUT	22	130	350	23	150	380	µA	
P0.4/UARTTXD, P0.5/UARTRXD, P0.6/UARTRTS, P0.7/UARTCTS, P0.10/PSEL1, P0.8/PAON, P0.9/PSEL0, P0.11/RXON, P0.14/TX_CONF, P0.15/SLEEPX	4.2	24	68	3.0	20	55	µA	
P1.0/TMS, P1.1/TCK, P1.2/TDI, P1.3/TDO, P1.4/RTCK, P1.5/CLK32, P1.6, P1.7/WAKEUP_BT, P1.8/WAKEUP_HOST,	1.1	6.0	17	0.75	5.0	14	µA	

7.5.3 Protection Circuits

All pads have an inverse protection diode against VSS.

RFOUT and VCOCAP have an inverse protection diode against VDDRF.
CLKIN/XTAL and LOAD have an inverse protection diode against VDDPM.
P0.10/PSEL1 has an inverse diode against VDD.
P0.5/UARTRXD has an inverse diode against VDDUART.
All other pads have no diode against their supply.

7.6 Clock Inputs and Crystal Oscillator

7.6.1 Reference Clock Input (CLKIN)

Table 7-15 Reference Clock Characteristics

Parameter	Min	Typ	Max	Unit	Conditions
Waveform		Sine or Square			
Frequency		26		MHz	Note: Hardware supports 10-40 MHz
Accuracy	-20		20	ppm	
Input voltage	-0.3		VDDPM+0.3	V	
Amplitude peak-to-peak	350		1800	mV	
Phase noise			-131	dBc/ Hz	Input frequency 13MHz. Measured at 10kHz
			-125	dBc/ Hz	Input Frequency 26MHz. Measured at 10kHz
Pin capacitance		3		pF	Internal oscillator disabled
		2.5		pF	Internal oscillator enabled
Pin resistance		10		kΩ	Internal oscillator disabled
		6		kΩ	Internal oscillator enabled

7.6.2 Crystal Oscillator

Table 7-16 Crystal Oscillator Characteristics[1)]

Parameter	Min	Typ	Max	Unit	Conditions
Nominal frequency		26		MHz	
Start up time		1	10	ms	Depends on crystal
Allowed resistance increase (**D**rive **L**evel **D**ependence - DLD effect of crystal) at low drive levels			100	Ω	
Voltage at crystal after settling	300	800		mV	
Crystal current		0.5	2	mA	Depends on crystal
Current consumption		100	200	µA	@ 1.5V, 25 °C

Table 7-16 Crystal Oscillator Characteristics[1)]

Parameter	Min	Typ	Max	Unit	Conditions
Frequency stability vs. supply voltage		0.5		ppm/V	
Frequency stability vs. temperature	-2		2	ppm	@ 1.5V, -40°C - 85°C
Frequency adjustment accuracy	-2		2	ppm	

1) valid only for crystal according the recommended specification (**Chapter 7.6.3 on Page 213**)

7.6.3 Recommended Crystal Specification

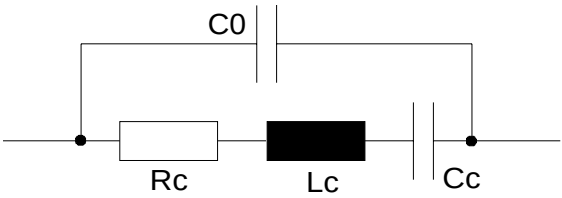


Figure 7-1 Electrical Equivalent Circuit for a Crystal, Composed of a Motional Series Resonant Linear Circuit

The following crystal specifications are recommended for the crystal oscillator. Correct system design ensures great reliability and low failure rates during production. Please note that system aspects as e.g. oscillation start up, temperature tolerances and phase noise are in the responsibility of the system engineer. The PCB layout has a great influence on system behavior. Therefore this crystal specification should only be treated as a recommendation. Because of packaging and internal circuitry an additive capacitance between XTAL and VSS of approximate 2 pF should be considered in addition to the static capacitance.

Table 7-17 Recommended Specification of 26.000MHz Crystal

Parameter	Min	Typ	Max	Unit	Conditions
Frequency		26.000		MHz	
Frequency tolerance	-15		+15	ppm	
Drive Level		0.1	2	mW	
Load capacitance C_L		12		pF	
Dynamic capacitance Cc		10		fF	

Table 7-17 Recommended Specification of 26.000MHz Crystal

Parameter	Min	Typ	Max	Unit	Conditions
Resonance resistance Rc		12	35	Ω	
Static capacitance C_0		3	2	pF	

7.6.4 Low Power Clock Input (CLK32)

Table 7-18 CLK32 Characteristics

Parameter	Min	Typ	Max	Unit	Conditions
Waveform		Square			
Frequency		32.768		kHz	
Accuracy	-250		250	ppm	
Jitter	-10		10	µs	
Rise time			10	µs	
Fall time			10	µs	
Duty cycle	10		90	%	
Pin capacitance		6		pF	
Pin resistance		5		MΩ	

Note: The CLK32 input is a VDDPM supplied digital pad. Voltage levels and other characteristics can be found in previous sections.

7.7 Interface Timing

Supply voltage is defined individually for each interface.

Timing measurements are made at 50% of the supply voltage for rising edge (logic 0 to 1) and falling edge (logic 1 to 0).

The AC testing input/output waveform are shown in **Figure 7-2**.

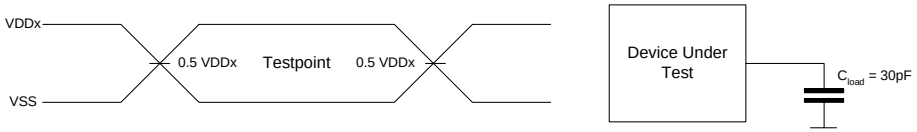


Figure 7-2 Input/Output Waveform for AC Tests

7.7.1 PCM Interface

The figures show the timing characteristics for default polarity settings of the PCM signals. When the interface is configured to generate both PCMCLK and PCMFR1 (clock master mode and frame master mode) the edges are generated at the same time. Differences in delay time might occur only because of different pin loads. During time t_{d1} the signal PCMOUT is undefined.

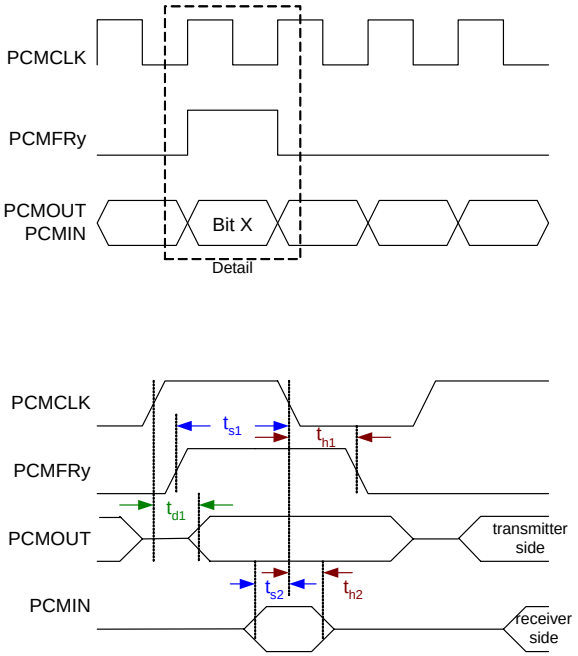


Figure 7-3 PCM Timing Characteristics for Single Clock Mode

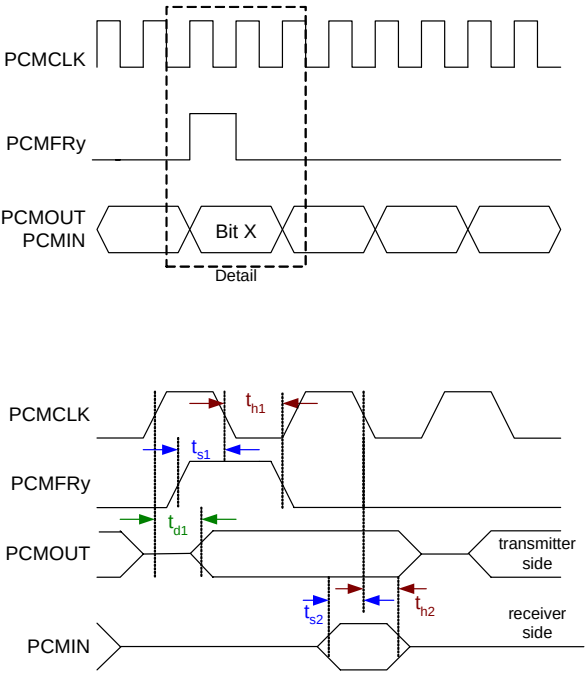


Figure 7-4 PCM Timing Characteristics for Double Clock Mode

Table 7-19 Timing Characteristics of PCM Interface

Symbol	Parameters	Min	Typ	Max	Unit
t_{d1}	PCMOUT delay from rising clock edge			100	ns
t_{s1}	PCMFRy setup time to falling clock edge	100[1)]			ns
t_{h1}	PCMFRy hold time from falling clock edge	100[1)]			ns
t_{s2}	PCMIN setup time to falling clock edge	50			ns
t_{h2}	PCMIN hold time from falling clock edge	50			ns

1) in frame slave mode

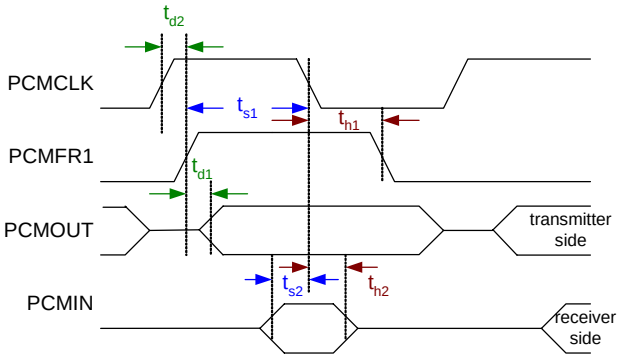


Figure 7-5 Characteristics for the First Output Bit in Frame Slave Mode

For the first bit the timing definition is slightly different in frame slave mode. Here the PCMFR1 timing defines the timing of the first output bit (PCMOUT) if the delay t_{d2} is positive. If the delay t_{d2} is negative the output timing is defined by the PCMCLK as for all other data bits.

Table 7-20 Timing Characteristics of PCM Interface for the First Bit

Symbol	Parameters	Min	Typ	Max	Unit
t_{d1}	PCMOUT delay from PCMCLK or PCMFR1			100	ns
t_{d2}	PCMFR1 delay from PCMCLK	-0.25T[1)]		+0.25T	ns

1) T is the PCMCLK period time

7.7.2 I2C Interface

The I2C interface provides the interface to an optional external EEPROM. The data transfer is accomplished according to the I2C bus protocol.

In the following figure, the timing of the I2C interface is given.

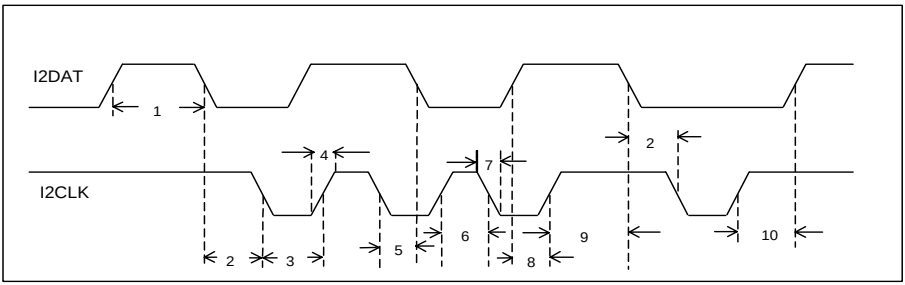


Figure 3-6: I2C Bus Timing

Table 7-21 I2C Bus Characteristics

Symbol	No.	Parameter	Limit Values			Unit
			Min	Typ	Max	
F_{I2CLK}		I2CLK- clock-frequency	99.7		104	kHz
T_{buf}	1	unused time before new data transfer	4.7			µs
T_{HSTA}	2	hold-time after start-generation	4.0			µs
T_{low}	3	low-period-width I2CLK	4.7			µs
T_{high}	6	high-period-width I2CLK	4.0			µs
T_{suSTA}	9	set up time for start-generation	4.7			µs
T_{HDAT}	5	hold time for data	0			µs
T_{suDAT}	8	set up time data	250			ns
T_r	4	rise-time I2CLK, I2DAT			1	µs
T_f	7	fall-time I2CLK, I2DAT			300	ns
T_{suSTO}	10	set up time for stop-generation	4.7			µs

7.8 RF Part

7.8.1 Operating Range RF Part

Table 7-22 Operating Range RF Part

Parameter	Limit Values		Unit	Notes
	Min	Max		
Supply voltage	1.7	1.9	V	Supply voltage of RF part
RFIO/X input/output		8	dBm	
RFIO/X input/output frequency	2402	2480	MHz	
TXA/X output		8	dBm	
TXA/X output frequency	2402	2480	MHz	
Ambient temperature	-40	85	°C	

7.8.2 AC / DC Characteristics RF Part

The AC/DC characteristics involve the spread of values to be within the specific supply voltage and temperature range. Typical characteristics are the median of the production.

All specified values are verified and valid on Infineon Golden Board using the BD_DATA setting PA_Fine_Tuning = -2 dB.

7.8.2.1 Bluetooth Related Specifications

Table 7-23 BDR - Transmitter Part

Parameters	Min	Typ	Max	Unit	Conditions
Output power (nominal setting)	2	4	6	dBm	BD_DATA setting PA_Fine_Tuning = -2 dB
Output power (high setting)		6		dBm	BD_DATA setting PA_Fine_Tuning = 0 dB
Power control step size	4	6	8	dB	
Frequency range fL	2400	2401.3		MHz	
Frequency range fH		2480.7	2483.5	MHz	
20dB bandwidth		0.930	1	MHz	
2nd adjacent channel power		-50	-40	dBc	

Table 7-23 BDR - Transmitter Part

Parameters	Min	Typ	Max	Unit	Conditions
3rd adjacent channel power		-62	-60	dBc	
>3rd adjacent channel power		-66	-60	dBc	Max. 2 of 3 exceptions @ 52 MHz offset might be used
Average modulation deviation for 00001111 sequence	140	156	175	kHz	
Minimum modulation deviation for 01010101 sequence	115	145		kHz	
Ratio Deviation 01010101 / Deviation 00001111	0.8	1			
Initial carrier frequency tolerance |foffset|		5	75	kHz	Typ. value is valid if the reference frequency has no frequency offset.
Carrier frequency drift (one slot) |fdrift|		10	25	kHz	
Carrier frequency drift (three slots) |fdrift|		10	40	kHz	
Carrier frequency drift (five slots) |fdrift|		10	40	kHz	
Carrier frequency driftrate (one slot) |fdriftrate|		5	20	kHz/ 50µs	
Carrier frequency driftrate (three slots) |fdriftrate|		5	20	kHz/ 50µs	
Carrier frequency driftrate (five slots) |fdriftrate|		5	20	kHz/ 50µs	

Table 7-24 BDR - Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
Sensitivity		-88	-83	dBm	Ideal wanted signal
Sensitivity		-86	-70	dBm	Wanted signal with frequency offset and drift, acc. to BT-spec

Table 7-24 BDR - Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
C/I-performance: -4th adjacent channel		-51	-40	dB	
C/I-performance: -3rd adjacent channel (1st adj. of image)		-46	-20	dB	
C/I-performance: -2nd adjacent channel (image)		-35	-9	dB	
C/I-performance: -1st adjacent channel		-4	0	dB	
C/I-performance: co. channel		9	11	dB	
C/I-performance: +1st adjacent channel		-4	0	dB	
C/I-performance: +2nd adjacent channel		-40	-30	dB	
C/I-performance: +3rd adjacent channel		-50	-40	dB	
Blocking performance 30MHz-2GHz	-10			dBm	Some spurious responses, but according to BT-specification
Blocking performance 2GHz-2.4GHz	-27			dBm	
Blocking performance 2.5GHz-3GHz	-27			dBm	
Blocking performance 3GHz-12.75GHz	-10			dBm	Some spurious responses, but according to BT-specification
Intermodulation performance	-39	-34		dBm	Valid for all intermodulation tests
Maximum input level	-20			dBm	

Table 7-25 EDR - Transmitter Part

Parameters	Min	Typ	Max	Unit	Conditions
Output power (nominal setting)	-1	1	3	dBm	BD_DATA setting PA_Fine_Tuning = -2 dB
Output power (high setting)		3		dBm	BD_DATA setting PA_Fine_Tuning = 0 dB
Relative transmit power: PxPSK - PGFSK	-4	-0.6	1	dB	
Carrier frequency stability |ωi|			75	kHz	
Carrier frequency stability |ωi+ω0|			75	kHz	
Carrier frequency stability |ω0|		2	10	kHz	
DQPSK - RMS DEVM		10	20	%	
8DPSK - RMS DEVM		10	13	%	
DQPSK - Peak DEVM		20	35	%	
8DPSK - Peak DEVM		20	25	%	
DQPSK - 99% DEVM			30	%	
8DPSK - 99% DEVM			20	%	
Differential phase encoding	99	100		%	
1st adjacent channel power		-40	-26	dBc	
2nd adjacent channel power			-40	dBc	Carrier power measured at basic rate.
≥3rd adjacent channel power			-60	dBc	Carrier power measured at basic rate. Exceptions at the 3rd adjacent channel are used for class 1 devices.

Table 7-26 EDR - Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
DQPSK-Sensitivity		-90	-85	dBm	Ideal wanted signal
DQPSK-Sensitivity		-88	-70	dBm	Wanted signal with frequency offset and drift, acc. to BT-spec
8DPSK-Sensitivity		-85.	-80	dBm	Ideal wanted signal
8DPSK-Sensitivity		-81	-70	dBm	Wanted signal with frequency offset and drift, acc. to BT-spec
DQPSK - BER Floor Sensitivity		-86	-60	dBm	
8DPSK - BER Floor Sensitivity		-81	-60	dBm	
DQPSK - C/I-performance: -4th adjacent channel		-53	-40	dB	
DQPSK - C/I-performance: -3rd adjacent channel (1st adj. of image)		-47	-20	dB	
DQPSK - C/I-performance: -2nd adjacent channel (image)		-31	-7	dB	
DQPSK - C/I-performance: -1st adjacent channel		-7	0	dB	
DQPSK - C/I-performance: co. channel		11	13	dB	
DQPSK - C/I-performance: +1st adjacent channel		-9	0	dB	
DQPSK - C/I-performance: +2nd adjacent channel		-44	-30	dB	
DQPSK - C/I-performance: +3rd adjacent channel		-50	-40	dB	
8DPSK - C/I-performance: -4th adjacent channel		-48	-33	dB	

Table 7-26 EDR - Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
8DPSK - C/I-performance: -3rd adjacent channel (1st adj. of image)		-44	-13	dB	
8DPSK - C/I-performance: -2nd adjacent channel (image)		-25	0	dB	
8DPSK - C/I-performance: -1st adjacent channel		-5	5	dB	
8DPSK - C/I-performance: co. channel		17	21	dB	
8DPSK - C/I-performance: +1st adjacent channel		-5	5	dB	
8DPSK - C/I-performance: +2nd adjacent channel		-36	-25	dB	
8DPSK - C/I-performance: +3rd adjacent channel		-46	-33	dB	
Maximum input level	-20			dBm	

7.8.2.2 Customer Related Specifications

Table 7-27 Customer Related Specifications: Transmitter Part

Parameters	Min	Typ	Max	Unit	Conditions
Output power fine steps	0.8	2	4	dB	
Output power (lowest gain)		-45		dBm	
Output power (noise) in dedicated bands		-147	-142	dBc/Hz	869MHz<f_{out}<894 MHz [1)]
		-147	-142	dBc/Hz	925MHz<f_{out}<960 MHz [1)]
		-143	-138	dBc/Hz	1805MHz<f_{out}<1880 MHz [1)]
		-143	-138	dBc/Hz	1930MHz<f_{out}<1990 MHz [1)]
		-145	-140	dBc/Hz	1565MHz<f_{out}<1585 MHz [1)]
		-142	-139	dBc/Hz	2110MHz<f_{out}<2170 MHz [1)]

Table 7-27 Customer Related Specifications: Transmitter Part

Parameters	Min	Typ	Max	Unit	Conditions
Output power (spurious) in dedicated bands		-88	-70	dBc	869 MHz<f_{out}<894 MHz [2]
		-83	-74	dBc	925 MHz<f_{out}<960 MHz [2]
		-84	-78	dBc	1805 MHz<f_{out}<1880 MHz [2]
		-85	-80	dBc	1930 MHz<f_{out}<1990 MHz [2]
				dBc	1565 MHz<f_{out}<1585 MHz [2]
		-80	-76	dBc	2110 MHz<f_{out}<2170 MHz [2]
Out of band spurious emissions, 2*f_{out}			-30	dBc	Measured at nominal output power
Out of band spurious emissions, 3*f_{out}			-35	dBc	Measured at nominal output power
Spurious emissions			-30	dBm	2300 MHz<f_{out}<2600 MHz
Spurious emissions			-47	dBm	30 MHz<f_{out}<6 GHz, exceptions cf. above

[1] Spectrum analyzer settings: Detector RMS, Trace Maxhold, RBW: 100kHz, VBW: 1MHz, Sweeptime: 20ms for all spans, Sweepcount: 100. Testmode: IFX-TX-burstmode (DH1, PRBS, 6dBm output power)

[2] Spectrum analyzer settings: Detector peak, Trace Maxhold, RBW: 100kHz, VBW: 100kHz, Sweeptime: 20ms/ 1MHz span, Sweepcount: 10. Testmode: IFX-TX-burstmode (DH1, PRBS, 6dBm output power)

Table 7-28 Customer Related Specification: Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
Blocking performance (noise) with reduced wanted signal in dedicated bands for GFSK mode	-22	-20		dBm	824MHz<f_{in}<849 MHz 1/3*(f_{wanted}-1MHz) ±660kHz for GFSK mode [1]
	-21	-19		dBm	880MHz<f_{in}<915 MHz 3/8*(f_{wanted}-1MHz) ±250kHz for GFSK mode [1]
	-18	-16		dBm	1710MHz<f_{in}<1785 MHz 5/7*(f_{wanted}-1MHz) ±300kHz for GFSK mode [1]
	-21	-19		dBm	1850MHz<f_{in}<1910 MHz 3/4*(f_{wanted}-1MHz) ±500kHz for GFSK mode [1]
	-22	-20		dBm	1920MHz<f_{in}<1980 MHz 4/5*(f_{wanted}-1MHz) ±400kHz for GFSK mode [1]

Table 7-28 Customer Related Specification: Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
Spurious responses with reduced wanted signal in dedicated bands for GFSK mode	-58	-53		dBm	824MHz<f_{in}<849 MHz 1/3*(f_{wanted}-1MHz) ±660kHz for GFSK mode [1)]
	-25	-20		dBm	880MHz<f_{in}<915 MHz 3/8*(f_{wanted}-1MHz) ±250kHz for GFSK mode [1)]
	-26	-21		dBm	1710MHz<f_{in}<1785 MHz 5/7*(f_{wanted}-1MHz) ±300kHz for GFSK mode [1)]
	-31	-26		dBm	1850MHz<f_{in}<1910 MHz 3/4*(f_{wanted}-1MHz) ±500kHz for GFSK mode [1)]
	-29	-27		dBm	1920MHz<f_{in}<1980 MHz 4/5*(f_{wanted}-1MHz) ±400kHz for GFSK mode [1)]
Blocking performance (noise) with reduced wanted signal in dedicated bands for DQPSK mode	-19	-14		dBm	824MHz<f_{in}<849 MHz 1/3*(f_{wanted}-1MHz) ±660kHz for DQPSK mode [1)]
	-15	-12		dBm	880MHz<f_{in}<915 MHz 3/8*(f_{wanted}-1MHz) ±250kHz for DQPSK mode [1)]
	-13	-11		dBm	1710MHz<f_{in}<1785 MHz 5/7*(f_{wanted}-1MHz) ±300kHz for DQPSK mode [1)]
	-12	-10		dBm	1850MHz<f_{in}<1910 MHz 3/4*(f_{wanted}-1MHz) ±500kHz for DQPSK mode [1)]
	-16	-14		dBm	1920MHz<f_{in}<1980 MHz 4/5*(f_{wanted}-1MHz) ±400kHz for DQPSK mode [1)]

Table 7-28 Customer Related Specification: Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
Spurious responses with reduced wanted signal in dedicated bands for DQPSK mode	-48	-46		dBm	824MHz<f_{in}<849 MHz 1/3*(f_{wanted}-1MHz) ±660kHz for DQPSK mode [1)]
	-22	-18		dBm	880MHz<f_{in}<915 MHz 3/8*(f_{wanted}-1MHz) ±250kHz for DQPSK mode [1)]
	-23	-20		dBm	1710MHz<f_{in}<1785 MHz 5/7*(f_{wanted}-1MHz) ±300kHz for DQPSK mode [1)]
	-27	-23		dBm	1850MHz<f_{in}<1910 MHz 3/4*(f_{wanted}-1MHz) ±500kHz for DQPSK mode [1)]
	-17	-15		dBm	1920MHz<f_{in}<1980 MHz 4/5*(f_{wanted}-1MHz) ±400kHz for DQPSK mode [1)]
Blocking performance (noise) with reduced wanted signal in dedicated bands for 8DPSK mode	-22	-17		dBm	824MHz<f_{in}<849 MHz 1/3*(f_{wanted}-1MHz) ±660kHz for 8DPSK mode [2)]
	-19	-14		dBm	880MHz<f_{in}<915 MHz 3/8*(f_{wanted}-1MHz) ±250kHz for 8DPSK mode [2)]
	-15	-13		dBm	1710MHz<f_{in}<1785 MHz 5/7*(f_{wanted}-1MHz) ±300kHz for 8DPSK mode [2)]
	-13	-10		dBm	1850MHz<f_{in}<1910 MHz 3/4*(f_{wanted}-1MHz) ±500kHz for 8DPSK mode [2)]
	-17	-15		dBm	1920MHz<f_{in}<1980 MHz 4/5*(f_{wanted}-1MHz) ±400kHz for 8DPSK mode [2)]

Table 7-28 Customer Related Specification: Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
Spurious responses with reduced wanted signal in dedicated bands for 8DPSK mode	-49	-46		dBm	824MHz<f_{in}<849 MHz 1/3*(f_{wanted}-1MHz) ±660kHz for 8DPSK mode [2]
	-22	-18		dBm	880MHz<f_{in}<915 MHz 3/8*(f_{wanted}-1MHz) ±250kHz for 8DPSK mode [2]
	-25	-20		dBm	1710MHz<f_{in}<1785 MHz 5/7*(f_{wanted}-1MHz) ±300kHz for 8DPSK mode [2]
	-25	-22		dBm	1850MHz<f_{in}<1910 MHz 3/4*(f_{wanted}-1MHz) ±500kHz for 8DPSK mode [2]
	-17	-16		dBm	1920MHz<f_{in}<1980 MHz 4/5*(f_{wanted}-1MHz) ±400kHz for 8DPSK mode [2]
Spurious emissions			-57	dBm	30MHz<f_{out}<12.75GHz

[1] Wanted signal level -85dBm but at least 3dB over actual sensitivity level.

[2] Wanted signal level -80dBm but at least 3dB over actual sensitivity level.

7.8.2.3 RF Block Specifications

Table 7-29 Impedances

Parameters	Min	Typ	Max	Unit	Conditions
RFIO / RFIOX		30-j30		Ω	
TXA / TXAX		30-j30		Ω	

Table 7-30 RF block specifications: Transmitter Part

Parameters	Min	Typ	Max	Unit	Conditions
Output noise without modulation measured at RFIO, RFIOX, TXA, TXAX			-100	dBc/Hz	@500kHz offset from carrier
			-110	dBc/Hz	@1.5MHz offset from carrier
			-120	dBc/Hz	@2.5MHz offset from carrier
			-130	dBc/Hz	@20MHz offset from carrier
LO feed through of modulator			-30	dBc	

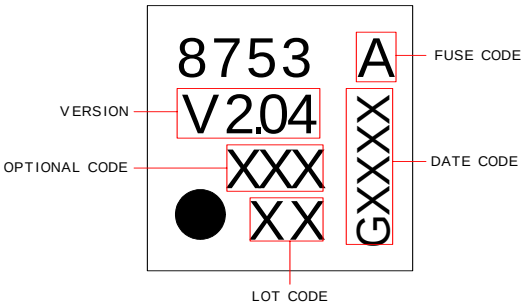
Table 7-31 RF block specifications: Receiver Part

Parameters	Min	Typ	Max	Unit	Conditions
RSSI resolution		3	6	dB	
Low RSSI limit		-85		dBm	
High RSSI limit		-45		dBm	

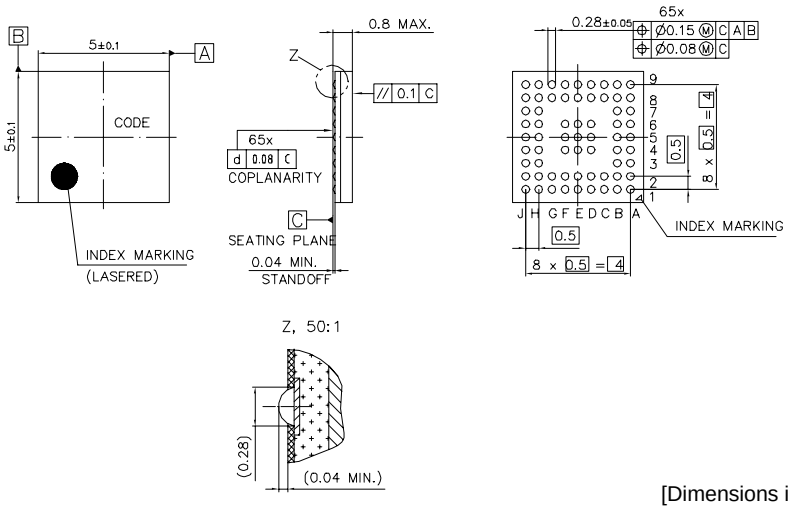
8 Package Information

8.1 Production Package, PG-WFSGA-65-1

8.1.1 Package Marking

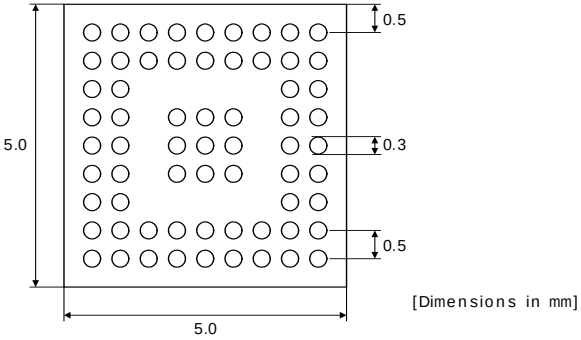


8.1.2 Package Outline

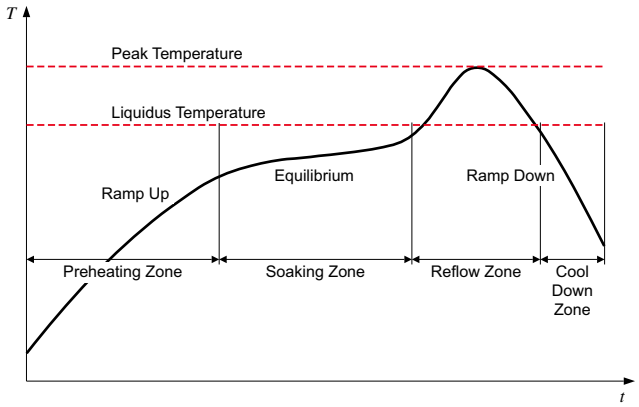


[Dimensions in mm]

8.1.3 Land Pattern



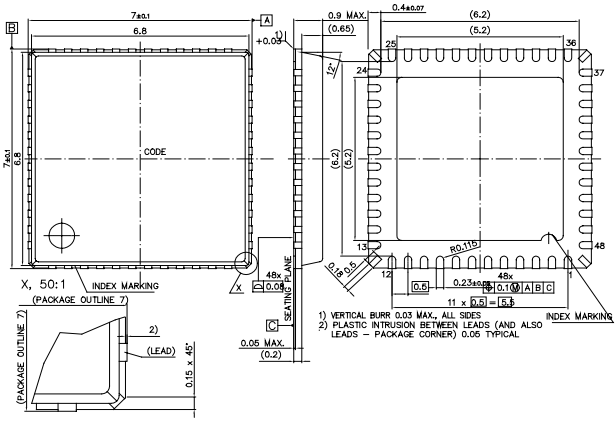
8.1.4 Solder Profile



Parameter	Lead-free Alloy (SnAgCu)	Main Requirements From
Preheating rate	2.5 K/s	Flux system (solder paste)
Soaking temperature	140 - 170 °C	Flux system (solder paste)
Soaking time	80 s	Flux system (solder paste)
Peak temperature	245 °C	Alloy (solder paste)
Reflow time over liquidus	60 s	Alloy (solder paste)
Cool down rate	2.5 K/s	

8.2 Firmware Evaluation Package, PG-VQFN-48-4

8.2.1 Package Outline



9 Reference Schematics

This section contains reference schematics for BlueMoon UniCellular.

9.1 Reference Design

The reference design in **Figure 9-1** shows an implementation of BlueMoon UniCellular in a typical application.

9.2 Golden RF Board

The Golden RF Board in **Figure 9-2** and **Figure 9-3** shows the board that has been used for measurements of RF parameters. All data regarding RF parameters in this specification are verified and valid on the Golden RF Board.

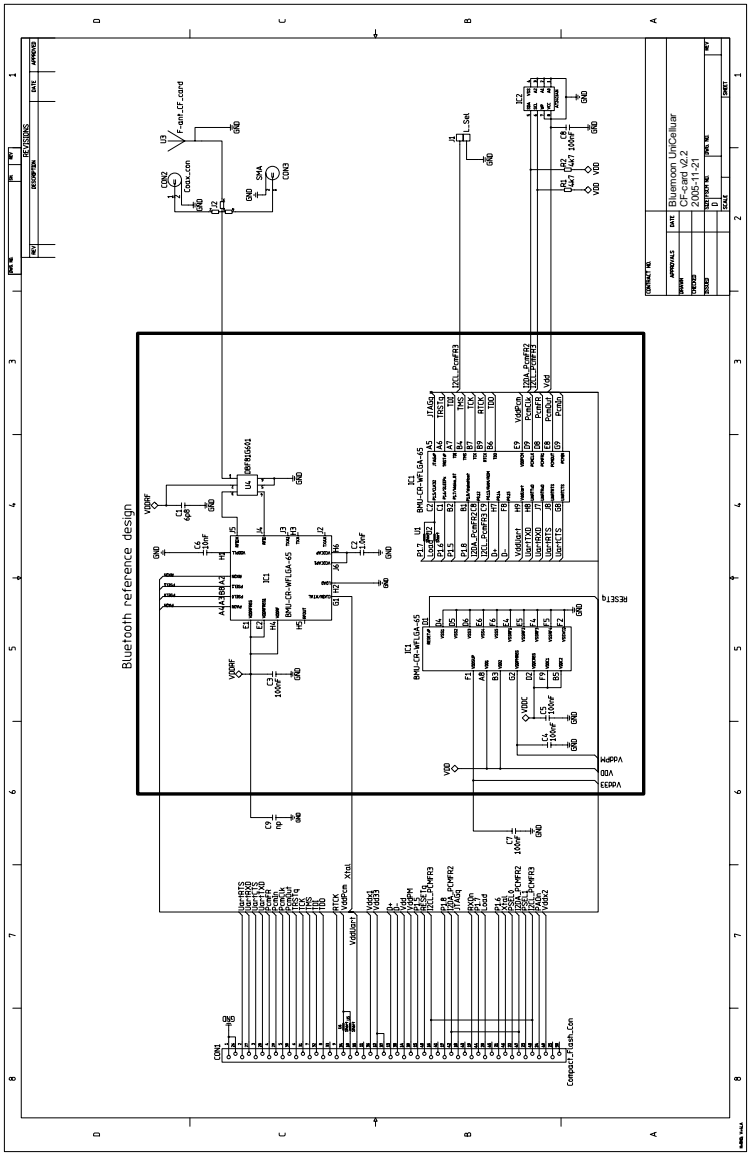


Figure 9-1 BlueMoon UniCellular Reference Design

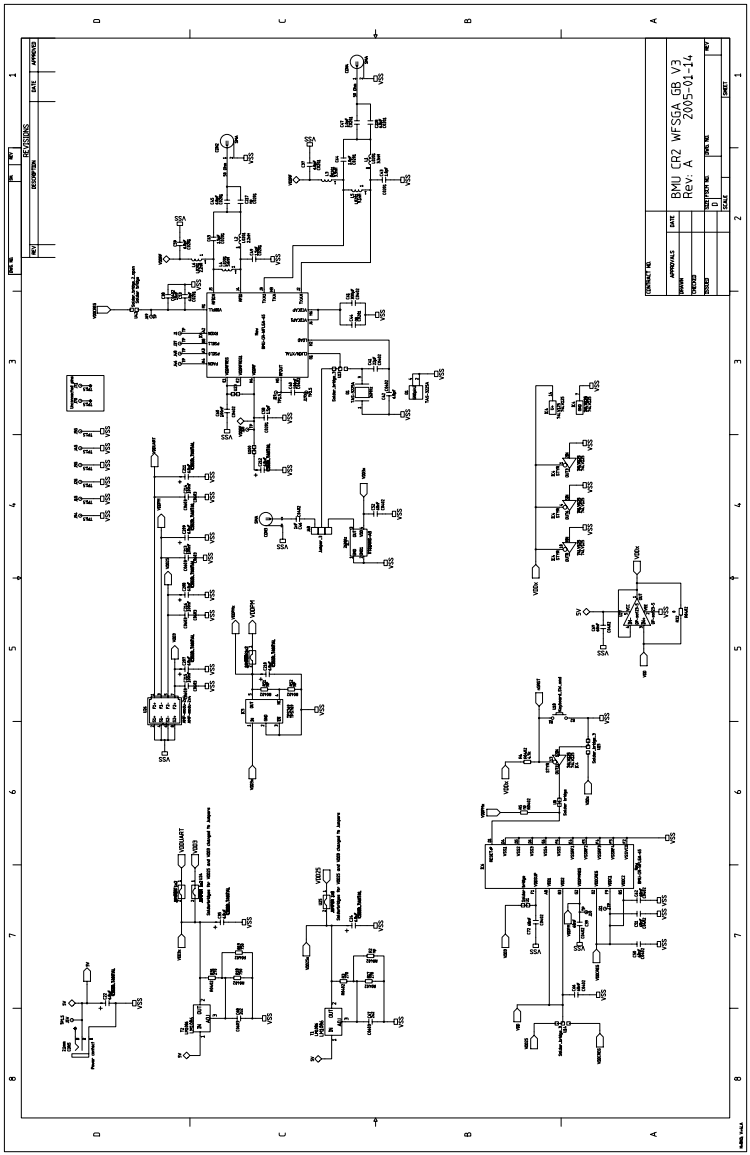


Figure 9-2 BlueMoon UniCellular Golden RF Board (1/2)

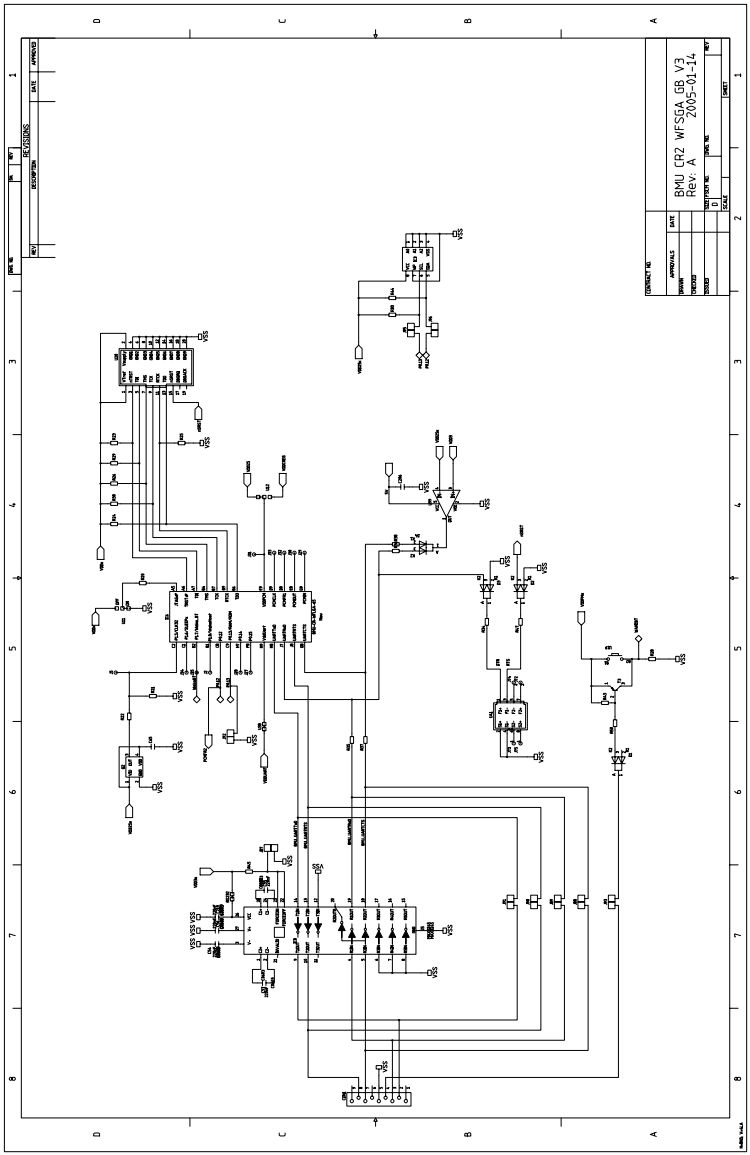


Figure 9-3 BlueMoon UniCellular Golden RF Board (2/2)

10 Acronyms & Abbreviations

Acronym or abbreviation	Writing out in full
ACK	Acknowledgement
ACL	Asynchronous Connection-oriented (logical transport)
AFH	Adaptive Frequency Hopping
AHS	Adaptive Hop Sequence
ARQ	Automatic Repeat reQuest
b	bit/bits (e.g. kb/s)
B	Byte/Bytes (e.g. kB/s)
BALUN	BALanced UNbalanced
BD_ADDR	Bluetooth Device Address
BER	Bit Error Rate
BMU	BlueMoon Universal
BOM	Bill Of Material
BT	Bluetooth
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
COD	Class Of Device
CODEC	COder/DECoder
CPU	Central Processing Unit
CQDDR	Channel Quality Driven Data Rate
CRC	Cyclic Redundancy Check
CTS	Clear To Send (UART flow control signal)
CVSD	Continuous Variable Slope Delta (modulation)
DC	Direct Current
DDC	Device Data Control
DM	Data Medium-Rate (packet type)
DMA	Direct Memory Access
DH	Data High-Rate (packet type)
DPSK	Differential Phase Shift Keying (modulation)
DQPSK	Differential Quaternary Phase Shift Keying (modulation)

Acronym or abbreviation	Writing out in full
DSP	Digital Signal Processor
DUT	Device Under Test
CDCT	Clock Drift Compensation Task
CQDDR	Channel Quality Driven Data Rate
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
eSCO	Extended Synchronous Connection-Oriented (logical transport)
EV	Extended Voice (packet type)
FEC	Forward Error Correction
FHS	Frequency Hop Synchronization (packet)
FIFO	First In First Out (buffer)
FM	Frequency Modulation
FW	Firmware
GFSK	Gaussian Frequency Shift Keying (modulation)
GPIO	General Purpose Input/Output
GSM	Global System for Mobile communication
HCI	Host Controller Interface
HCI+	Infineon Specific HCI command set
HEC	Header Error Check
HV	High quality Voice (packet type)
HW	Hardware
I2C	Inter-IC Control (bus)
I2S	Inter-IC Sound (bus)
IAC	Inquiry Access Code
ID	IDentifier
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
ISM	Industrial Scientific & Medical (frequency band)
JTAG	Joint Test Action Group
LAN	Local Area Network
LAP	Lower Address Part

Acronym or abbreviation	Writing out in full
LM	Link Manager
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
LO	Local Oscillator
LPM	Low Power Mode(s)
LPO	Low Power Oscillator
LSB	Least Significant Bit/Byte
LT_ADDR	Logical Transport Address
MSB	Most Significant Bit/Byte
MSRS	Master-Slave Role Switch
NC	No Connection
NOP	No OPeration
NVM	Non-Volatile Memory
OCF	Opcode Command Field
OGF	Opcode Group Field
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Coded Modulation
PDU	Protocol Data Unit
PER	Packet Error Rate
PIN	Personal Identification Number
PLC	Packet Loss Concealment
PLL	Phase Locked Loop
PMU	Power Management Unit
POR	Power-On Reset
PTA	Packet Traffic Arbitration
PTT	Packet Type Table
QoS	Quality Of Service
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read Only Memory

Acronym or abbreviation	Writing out in full
RSSI	Received Signal Strength Indication
RTS	Request To Send (UART flow control signal)
RX	Receive
RXD	Receive Data (UART signal)
SCO	Synchronous Connection-Oriented (logical transport)
SIG	Special Interest Group (Bluetooth SIG)
SW	Software
SYRI	Synthesizer Reference Input
TBD	To Be Determined
TCK	Test Clock (JTAG signal)
TDI	Test Data In (JTAG signal)
TDO	Test Data Out (JTAG signal)
TL	Transport Layer
TMS	Test Mode Select (JTAG signal)
TX	Transmit
TXD	Transmit Data (UART signal)
UART	Universal Asynchronous Receiver & Transmitter
ULPM	Ultra Low Power Mode
VCO	Voltage Controlled Oscillator
WLAN	Wireless LAN (Local Area Network)

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