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[OPERATIONAL DESCRIPTION]

Description: E-GSM1900 Band GPRS Terminal Equipment
FCC ID: RJAI-2000

Baseband Design Description

THIS DOCUMENT PROVIDES A SHORT DESCRIPTION OF THE BASEBAND SECTION OF THE I-2100. MOST DESIGN DECISIONS ARE EXPLAINED, BUT NO DETAILED CALCULATIONS ARE INCLUDED.

1. Control section

THE CONTROL SECTION IS DESIGNED AROUND THE ANALOG DEVICES AD20MSP430 CHIP GSM CHIPSET. THIS CHIPSET COMPRISES THE AD6526 ADVANCED DIGITAL BASEBAND PROCESSOR (ADBP), THE AD6535 ANALOG BASEBAND PROCESSOR (ABP).

1.1 The AD6526 Advanced Digital Baseband Processor

THE AD6526 ADVANCED DIGITAL BASEBAND PROCESSOR (ADBP) CONTAINS BOTH THE MICROPROCESSOR CORE AND THE DSP RUNNING THE EQUALISATION AND SPEECH CODING ALGORITHMS. A THIRD SECTION CONTAINS THE CHANNEL CODEC FUNCTIONS. IN ADDITION TO CONTROLLING THE PHONE THE ADBP IS RESPONSIBLE FOR ALL SYSTEM TIMING. THE CHANNEL CODEC UNDERTAKES THE SIGNAL PROCESSING FUNCTIONS ASSOCIATED WITH CHANNEL CODING AND DECODING, AND THE CONTROL PROCESSOR OPERATES THE REMAINING LAYER 1 FUNCTIONS, LAYER 2 AND 3 PROTOCOL, AND ALL THE REMAINING SOFTWARE OF THE PHONE.

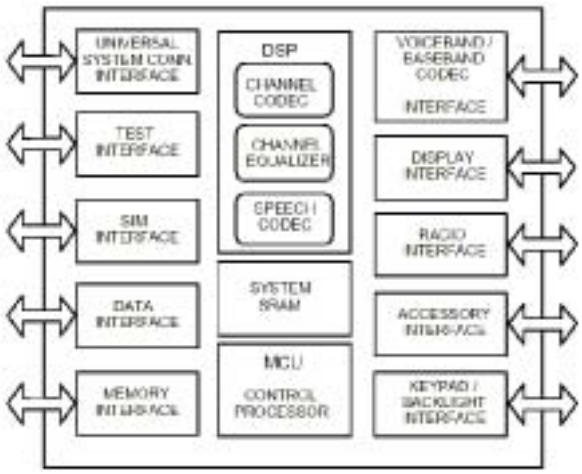


Figure 1 Block diagram for key functions of the AD6526

THE MCU CORE IS THE ARM7TDMI DEVICES, FROM ADVANCED RISC MACHINES LTD, WHICH INCLUDES THUMB CODE EXECUTION CAPABILITY, DEBUG INTERFACE, MULTIPLIER (32X8), ICE VIA EMBEDDEDICE MACROCELL.

A SMALL BUILT-IN ROM CONTAINING A BOOT CODE WHICH MAKES IT POSSIBLE TO DOWNLOAD AND RUN CODE IN THE RAM, E.G. FOR DOWNLOADING CODE INTO THE FLASH

A JTAG INTERFACE MAKES IT POSSIBLE TO PERFORM BOUNDARY SCAN AS TEST PADS ARE PLACED ON THE PCB. THIS INTERFACE CONSISTS OF A TOTAL OF 5 SIGNALS: A JTAG ENABLE LINE (JTAGEN), A CLOCK STROBE (TCK), A TEST MODE SELECT PIN (TMS) AND 2 UNIDIRECTIONAL DATA LINES, ONE FOR DATA IN (TDI) AND ONE FOR READING DATA OUT (TDO).

1.1.1 Microprocessor section

THE 32 BIT MECROPROCESSOR CORE, THE ARM7TDME DEVICES,CONTAINS VARIOUS SUPPORT CIRCUITS SUCH AS SERIAL AND PARALLEL I/O, MEMORY AND INTERRUPT CONTROL AND A WATCHDOG TIMER.

THE ADBP IS EQUIPPED WITH A 16-BIT DATA BUS (D0-D15) AND A 24-BIT ADDRESS BUS (A0-A23) FOR A MAXIMUM OF 16MB PER CONNECTED DEVICE. A21 AND A22 HAS AN ALTERNATIVE FUNCTION AS A GPIO LINE (GPIO15,GPIO14). THE MICROPROCESSOR HAS 5 DEDICATED CHIP SELECTS. ONE OF THESE CHIP SELECTS IS DEDICATED TO ROM/FLASH (NROMCS), ONE TO RAM (NRAMCS, MAY BE PLACED ON TWO DIFFERENT ADDRESS RANGES), TWO FOR GENERAL PURPOSE CHIP SELECT (NGPCS0,NGPCS1) AND A23 IS USED FOR SELECTION OF THE LCD (NDISPLAYCS). OF THE REMAINING ADDRESS SPACE A FEW HUNDRED BYTES ARE USED FOR INTERNAL SUPPORT CIRCUITS AND THE CHANNEL CODEC INTERFACE.

FOUR CONTROL SIGNALS ARE RESPONSIBLE FOR CONTROLLING DATA TRANSFERS ON THE DATA BUS. THEY COMPRISE A READ STROBE (NRD), A WRITE STROBE (NWR) AND UPPER AND LOWER BYTE WRITE STROBES FOR 8-BIT ACCESS (NLWR/LBS AND NHWR/UBS). THE INTERFACE CAN BE SWITCHED BY SOFTWARE BETWEEN TWO DIFFERENT MODES, ALLOWING GLUELESS INTERFACING TO BOTH 8-BIT AND 16-BIT WIDE SRAM MEMORY CHIPS.

THE LCD MAY BE CONTROLLED THROUGH A 8-BIT OR 16-BIT PARALLEL INTERFACE USING THE DATA AND ADDRESS LINES, A WRITE STROBE, A DISPLAY CHIP SELECT (NGPCS1) AND THE LCDCTL CONTROL OUTPUT. WHEN USED IN THIS MODE A HARDWIRED WAIT-STATE GENERATOR ENSURES CORRECT TIMING. WHEN INTERFACING TO A UNIVERSAL SYSTEM CONNECTOR (USC) INTERFACE ALLOWS A RANGE OF DIFFERENT TYPES OF SERIAL CONNECTIONS TO BE MULTIPLEXED THROUGH A COMMON INTERFACE. THE USC CONSISTS OF 7 PINS AND CAN AMONG OTHERS SUPPORT PROGRAMMING, DATA TRANSFERS OR PHONE BOOK UPDATES. THE FOLLOWING FUNCTIONS HAVE BEEN CHOSEN FOR THE USC: TWO SERIAL COMMUNICATION PORTS, IMPLEMENTED VIA GENERIC SERIAL PORTS, WHICH CAN BE CONFIGURED IN DIFFERENT MODES, E.G. RS-232 OR SYNCHRONOUS COMMUNICATION. A JTAG INTERFACE TO SUPPORT IN-CURCUIT EMULATION OR THE EMBEDDED ARM PROCESSOR. A HIGH SPEED LOGGING AND TRACE

INTERFACE FOR MONITORING DATA FLOWING IN THE DSP SYSTEM. A DAI INTERFACE, ALLOWING THE USER TO DIRECTLY CONNECT THE SYSTEM SIMULATOR FOR FULL TYPE APPROVAL. A DIRECT INTERFACE FOR MONITORING THE RX I/Q SIGNAL, TO PERMIT MEASUREMENT OF SIGNAL TO NOISE RATIO (SNR) OF THE RADIO DURING PRODUCTION TEST.

A second serial port, modified for GSM purposes, is dedicated to the SIM interface. A total of 5 signals are provided for it: One data lines (SIMDATAOP), a clock strobe output (SIMCLK), two power control outputs (SIMSUPPLY and SIMPROG/SIMDATAIP) and a reset output (SIMRESET). As SIMRESET, SIMSUPPLY and SIMPROG can be used as a general-purpose output. SIMPROG is used for switching between 1.8V and 3V SIM operation. The SIM interface supports the functionality of the GSM Phase 1 specification and also supports the functionality of the new GSM Phase 2+ specification for FAST 64 kbps SIM.

THE INTERRUPT CONTROLLER HANDLES ALL INTERRUPT SOURCES AND INTERRUPT DESTINATIONS OF THE AD6526 ARCHITECTURE. THERE ARE 3 INDEPENDENT SUB-INTERRUPT CONTROLLER. EACH SUB-INTERRUPT CONTROLLER HAS FOLLOWING CAPABILITIES: AN INTERRUPT LEVEL ASSOCIATED WITH EACH INTERRUPT. INTERRUPT MASK, ENABLE/DISABLE OF INTERRUPT SIGNAL. SUPPORTING INTERRUPT MASK BASED ON PRIORITY LEVEL. SUPPORT OF NON MASKABLE INTERRUPTS. INTERRUPT DEFINITION (EDGE, LEVEL AND POLARITY) USED FOR INTERRUPTS EXTERNAL TO THE CHIP.

THE 26MHZ SYSTEM CLOCK IS TIED TO THE CLKIN PIN. A BAND-PASS FILTER CONSISTING OF R707 AND C713 HAS BEEN INSERTED BETWEEN THE REFERENCE OSCILLATOR AND THE ADBP IN ORDER TO INSULATE THE RF SECTION FROM THE BASEBAND SECTION. THE CLOCK SIGNAL TO THE CODEC CHIP MUST BE A SQUARE WAVE SIGNAL, AND THE ADBP ACTS AS A BUFFER FOR THE 13MHZ CLOCK SIGNAL. THE BUFFERED CLOCK SIGNAL IS FOUND ON CLKOUT. A REGISTER BIT ALLOWS THE CLKOUT TO FORCE THE CODEC INTO STANDBY MODE FOR POWER SAVING PURPOSES.

UPON BEING ACTIVATED THE MICROPROCESSOR MUST BE ABLE TO KEEP ITSELF POWERED UP. ASSERTING THE PWRON PIN KEEPS THE POWER MANAGEMENT CHIP ACTIVATED.

In order to save power a 32.768KHz crystal (U601) has been added. During standby the 26MHz clock may be powered down. The system can then run at 32.768KHz instead. All necessary circuitry for slow clocking is built-in except for the crystal. The crystal is connected to the OSCIN and OSCOUT pins. As the built-in feed back resistor of 10Mohm is a bit on the high end an external parallel resistor (R600) has been added.

The use of a 32.768kHz clock oscillator has made it very simple to implement a real-time clock (RTC). The necessary hardware is therefore included in the ADBP. For back-up of the RTC while the phone is turned off

or when the main battery pack is depleted an additional power supply (back-up) input VRTC is provided, for either a battery or a low leakage capacitor. The VRTC also feeds the PWRON output driver. In the MS it is possible to mount a small battery (B1).

ADBP SUPPORTS A LIMITED NUMBER OF GENERAL PURPOSE INPUT/OUTPUT SIGNAL PINS. ANY PIN FUNCTIONALITY WHERE THE USER CAN CONFIGURE THE CHIP USAGE WILL BE OVERLAPPED WITH A GPIO PORT. THE GPIO PORT CAN BE CONFIGURED BY A SET OF REGISTERS: INPUT, CONTAINS THE INPUT VALUE OF THE PIN. OUTPUT, CONTAINS THE OUTPUT VALUE OF THE PIN. OUTPUT-ENABLE, ENABLES THE OUTPUT. FUNCTION-SELECT, SELECT BETWEEN GPIO FUNCTIONALITY BUS BITS, ETC.

1.1.2 Channel codec section

THE CHANNEL CODEC HANDLES ALL THE ENCODING AND DECODING, ENCRYPTION AND DECRYPTION, DE-INTERLEAVING AND INTERLEAVING FUNCTIONS, THE INTERFACING TO THE ANALOG BASEBAND PROCESSOR (ABP), SYSTEM TIMING AND CONTROL AS WELL AS THE RF PLL SYNTHESIZER INTERFACE. IT ALSO CONTAINS THE JTAG TEST INTERFACE AND A NUMBER OF CONTROL REGISTERS WITH DEDICATED I/O PINS ATTACHED TO THE INDIVIDUAL REGISTER BITS.

1.1.3 The control registers

THE CONTROL REGISTER SECTION IS RESPONSIBLE FOR A WIDE RANGE OF TASKS. IT PERFORMS THE KEYPAD MATRIX SCANNING (5 COLUMNS (KEYPAD_COL[0:4]) AND 5 ROWS (KEYPAD_ROW[0:4]) FOR A MAXIMUM OF 25 KEYS IN THE MAIN MATRIX) AND GENERATES AN INTERRUPT WHENEVER A KEY IS PRESSED.

THE RADIO SECTION IS POWERED UP AND DOWN USING THE CLKON SIGNAL. OTHER REGISTER BITS AND OUTPUT PINS MAKE IT POSSIBLE TO RESET THE VBC IN THE ABP SEPARATELY ($\overline{\text{VBCRESET}}$). THE RESET IS CONTROLLABLE THROUGH EITHER REGISTER BITS OR BY THE OCCURRENCE OF A POWER UP OR A BROWN OUT. THE SYSTEM IS RESET ON THE $\overline{\text{RESET}}$ INPUT PIN.

THE BASIC BACKLIGHT CONTROLLER PROVIDES 3 INDEPENDENT BACKLIGHT CONTROLS WHOSE DUTY CYCLE AND FREQUENCY CAN BE SET BY SOFTWARE. THE DUTY CYCLE IS PROGRAMMABLE IN 128 STEPS FROM 1/128 TO 127/128 AND THE FREQUENCY CAN BE SELECTED FROM A VARIETY OF PREDEFINED FREQUENCIES. THE 3 OUTPUTS CAN BE INDIVIDUALLY ENABLED AND THEIR INPUT CLOCK SOURCES CAN BE EITHER THE 13 MHZ SYSTEM CLOCK OR THE 32KHZ CLOCK.

1.1.4 Voiceband Baseband Converter auxiliary section interface

THE CHANNEL CODEC SECTION IS ALSO RESPONSIBLE FOR INTERFACING TO THE AUXILIARY SECTION OF THE VOICEBAND BASEBAND CONVERTER. THIS INTERFACE CONSISTS OF A SYNCHRONOUS SERIAL INTERFACE WITH A DATA

OUT LINE (ASDO), A DATA IN LINE (ASDI) AND AN OUTPUT FRAME STROBE (ASFS).

1.1.5 Synthesizer interface

THE SYNTHESIZER INTERFACE PROVIDES SYNCHRONOUS CONNECTIONS FOR TWO RF PLL SYNTHESIZERS WITH A DATA OUTPUT LINE (OTH_DATA), A CLOCK STROBE (OTH_CLK) AND ENABLE STROBES (OTH_EN). OTH_EN ENABLES THE POWER VCO'S FOR THE TRANSLATION LOOP IN THE TRANSMIT SECTION.

1.1.6 Timing and control

THE TIMING AND CONTROL MODULE PROVIDES THE TIMING REFERENCE FOR THE CHANNEL CODEC AND INCLUDES THE RECEIVE TIMEBASE. FURTHERMORE, SYNCHRONISATION OF THE CHANNEL CODEC TO THE AIR-INTERFACE AND ALL INTERNAL CONTROL SIGNALS ARE GENERATED IN THIS MODULE.

THE TXON SIGNAL IS USED TO SWITCH THE ABP ON. THE LEADING EDGE IS USED BY THE ABP AS TIMING REFERENCE TO DEFINE THE EXACT TIMING. THE SIGNAL IS ALSO RESPONSIBLE FOR DEFINING THE TIMING ADVANCE. RXON IS USED TO TURN THE RECEIVER PART IN ABP ON. BOTH SIGNALS ARE ALSO USED TO SWITCH ON THE TRANSCEIVER/RECEIVER IN THE RF SECTION.

OTH_TX_PA IS CONTROLLING THE POWER UP AND DOWN OF THE POWER AMPLIFIER AND AS A CONTROL SIGNAL FOR THE PA CONTROL LOOP. ALTERNATIVELY IT MAY BE USED AS A GENERAL-PURPOSE OUTPUT. IN THE MS THE OTH_TX_PA IS USED TO CONTROL THE ANTENNA SWITCH.

1.1.7 Channel Codec system functions

THE CHANNEL CODEC PROCESSES DATA FROM TWO PRINCIPAL SOURCES: TRAFFIC AND SIGNALLING. THE FORMER IS NORMALLY CONTINUOUS AND THE LATTER DETERMINED ON DEMAND. TRAFFIC COMES IN TWO FORMS: SPEECH AND USER DATA. THE VARIOUS TRAFFIC AND CONTROL SOURCES ARE ALL PROCESSED DIFFERENTLY AT THE PHYSICAL LAYER. SPEECH TRAFFIC IS SUPPLIED BY THE SPEECH TRANSCODER AND THE REMAINING DATA TYPES ARE SOURCED FROM THE CONTROL PROCESSOR AND INTERFACED VIA A DEDICATED SERIAL DATA INTERFACE.

THE TRANSMIT AND RECEIVE FUNCTIONS OF THE CHANNEL CODEC ARE TIMED BY AN INTERNAL TIMEBASE WHICH MAINTAINS ACCURATE LOW LEVEL TIMING OF ALL SUB-SYSTEMS. THIS TIMEBASE IS ALIGNED WITH THE ON-AIR RECEIVE SIGNAL AND ALL SYSTEM CONTROL SIGNALS, BOTH INTERNAL AND EXTERNAL, ARE DERIVED FROM IT.

THE PHYSICAL LAYER PROCESSING CAN BE DIVIDED INTO 4 PHASES, TWO EACH FOR THE UP AND DOWNLINK. THE UPLINK DATA, I.E. FROM THE MOBILE TO THE BASE STATION, IS GENERALLY REFERRED TO AS THE TRANSMIT PATH. THE DATA IN THE TRANSMIT PATH UNDERGOES AN ENCODE PHASE AND THEN A TRANSMIT PHASE. SIMILARLY, DATA IN

THE DOWNLINK PATH IS TERMED THE RECEIVE DATA, AND IT UNDERGOES A RECEIVE PHASE FOLLOWED BY A DECODE PHASE. NOMINALLY, THE DECODE IS AN INVERSION OF THE ENCODE AND THE RECEIVE AN INVERSE OF THE TRANSMIT.

1.1.8 The DSP subsystem

THE DSP SUBSYSTEM IS A GENERAL PURPOSE ENHANCED ADSP-2181 CORE WITH BUILT-IN RAM AND ROM CONTAINING THE REQUIRED CODE FOR TWO MAIN FUNCTIONS: SPEECH TRANSCODING AND CHANNEL EQUALISATION.

TWO SPEECH TRANSCODING ALGORITHMS ARE SUPPORTED: GSM FULL-RATE (FR) AND ENHANCED FULL-RATE (EFR). USING FR A 13BIT 8 KB/S SAMPLE DATASTREAM IS CONVERTED TO 13KB/S AND IN EFR A 104KB/S DATASTREAM IS CONVERTED INTO 12.2KB/S (SPEECH) + 1.8KBIT/S (CRC AND REPETITION BITS).

THE SPEECH TRANSCODING SUPPORTS A DISCONTINUOUS TRANSMISSION MODE (DTX) WHERE A VOICE ACTIVITY DETECTION (VAD) ALGORITHM DETERMINES IF THE LOCAL USER IS SPEAKING OR NOT AND SUBSTITUTES A PRE-DEFINED SILENCE DESCRIPTOR WHICH IS ONLY TRANSMITTED OCCASIONALLY BY THE MOBILE, THEREBY SAVING POWER.

THE DSP CORE IS ALSO RESPONSIBLE FOR A NUMBER OF OTHER FUNCTIONS INCLUDING NUMEROUS TONE GENERATION ROUTINES AND SHORT TERM ECHO CANCELLATION.

THE EQUALIZER RECOVERS AND DEMODULATES THE RECEIVE SIGNAL AND ESTABLISHES THE LOCAL TIMING REFERENCES FOR THE MOBILE. EQUALISATION IS REQUIRED BECAUSE THE PROPAGATION ENVIRONMENT FOR THE GSM AIR INTERFACE IS EXTREMELY HOSTILE AND A NUMBER OF EFFECTS CREATE SIGNAL DISTORTIONS, SUCH AS MULTI-PATH, WHICH HAVE TO BE COMPENSATED FOR BEFORE THE SOURCE DATA CAN BE RECOVERED.

TWO SEPARATE INTERFACES ARE PROVIDED BETWEEN THE DSP CORE AND THE VOICEBAND BASEBAND CONVERTER (VBC). BOTH INTERFACES ARE SERIAL, ONE CARRYING ALL VOICE CODEC DATA, AND ANOTHER TO TRANSFER DATA TO AND FROM THE BASEBAND CODEC. THE VOICEBAND DATA INTERFACE CONSISTS OF THE FOLLOWING SIGNALS: VSDI IS THE DATA STREAM FROM THE DSP TO THE VBC (ASDO ON THE ABP SIDE), AND THE VSDO SIGNAL TRANSFERS DATA IN THE OPPOSITE DIRECTION (ASDI ON THE ABP SIDE). VSFS (ASFS ON THE ABP SIDE) IS A FRAMING SIGNAL, WHICH IS GENERATED BY THE VBC.

THE BASEBAND DATA INTERFACE CONSISTS OF A TOTAL OF 4 SIGNALS: BSDI IS THE SERIAL DATA SIGNAL FROM THE DSP TO THE VBC (BSDO ON THE ABP SIDE), AND BSDO PROVIDES TRANSFERS IN THE OTHER DIRECTION (BSDI ON THE ABP SIDE). BSIFS (BSOFS ON THE ABP SIDE) IS THE FRAMING SIGNAL FOR THE BSDI SIGNAL AND ORIGINATES FROM THE DSP. SIMILARLY, THE BSOFS SIGNAL (BSIFS ON THE ABP SIDE) IS A FRAME SIGNAL FOR THE

BSDO DATA STREAM AND ORIGINATES FROM THE VBC.

1.1.9 Other considerations

The power supply for the ADBP is supplied with VCC from AD6535 (U500) and is decoupled using the capacitors C601, C602, C603, C604, C605, C606, C607, C608, C609, C610 and C611.

1.2 The AD6535 Analog Baseband Processor.

THE AD6535 IS A COMPLETE MIXED-BASEBAND PROCESSOR THAT COMBINES ALL OF THE DATA CONVERTERS AND POWR SUPPLY REGULATORS REQUIRED IN THE PHONE. THERE ARE FOUR SECTIONS: ONE CONTAINING THE CONVERTERS FOR THE I AND Q SIGNALS TO AND FROM THE RF SECTION (THE BASEBAND SECTION), ANOTHER FOR THE VOICEBAND CONVERTERS, AND A THIRD CONTAINING THE AUXILIARY CONVERTERS FOR E.G. MEASURING THE BATTERY VOLTAGE AND TEMPERATURE OR CONTROLLING THE POWER RAMP FOR THE RF PA MODULE. THE OTHER FOR THE POWER MANAGEMENT THAT IS DESCRIBED LATER.

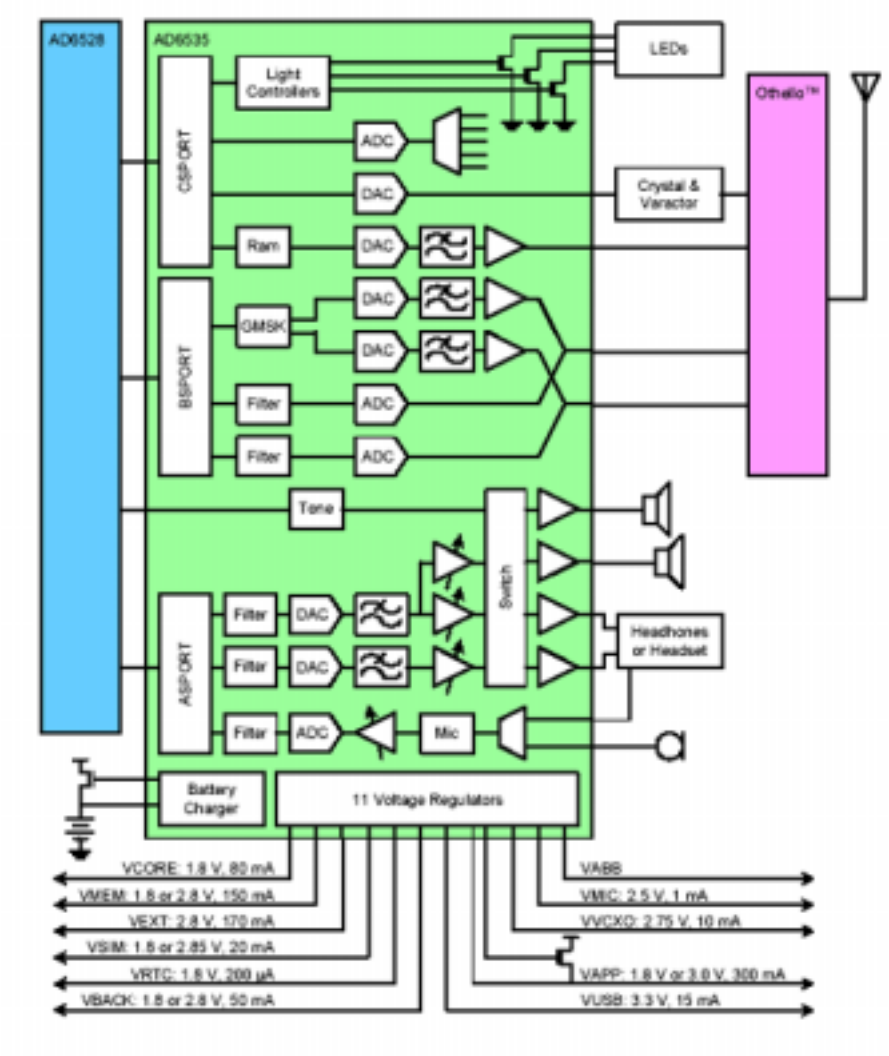


Figure 2 Functional block diagram for AD6535.

1.2.1 The baseband section

DATA TO AND FROM THE BASEBAND SECTION ARE TRANSMITTED ON A SYNCHRONOUS SERIAL INTERFACE FROM THE DSP SECTION OF THE ADBP. DATA IS INPUT ON THE BSDI PIN AND OUTPUT ON THE BSDO PIN. TWO FRAME SYNC SIGNALS ARE PROVIDED: ONE FOR THE INPUT DATA (BSIFS) WHICH IS GENERATED BY THE ADBP AND ANOTHER FOR THE OUTPUT DATA (BSOFS) WHICH IS GENERATED BY THE VBC.

THE TRANSMIT PATH CONSISTS OF A RAM FOR STORING THE BURST DATA, A ROM CONTAINING THE CODE NECESSARY FOR PERFORMING GAUSSIAN MINIMUM SHIFT KEYING (GMSK), OUTPUT OFFSET ADJUST AND TWO HIGH ACCURACY FAST 10-BIT DACS WITH RECONSTRUCTION FILTERS. DATA ARE OUTPUT AND INPUT DIFFERENTIALLY ON THE IN AND IP RESPECTIVELY QN AND QP PINS.

In the receive section, It passes through two high-performance Sigma-Delta ADCs before entering digital decimation FIR filters and an offset adjustment.

A 1.2 voltage reference for both the baseband ADC's and DAC's is included. The 1.2V reference is also used for biasing the analog signals. The raw reference is output on the REF pin for external decoupling with the capacitors C544. Buffered Output of internal voiceband reference is decoupled using C519.

1.2.2 The voiceband section

Similar to the baseband section voice data is transmitted on a synchronous serial interface from the DSP section of the ADBP. Data is input on the VSDI pin and output on the VSDO pin. A single frame sync signal is provided, VSFS (ASFS pin on the AD6535), which is also generated by the VBC.

The voiceband DAC consists of a sigma-delta digital-to-analog converter with integral digital filters, an analog smoothing filter, a programmable gain amplifier (PGA), and output drivers. After passing an analog smoothing filter the audio is led into a programmable gain amplifier with Output PGA gain settings (in 2dB steps from -48dB to +12dB) and a differential output amplifier. The signal is then fed to a MUX allowing it to be routed out on three different sets of outputs which are differential: AOUT1N and AOUT1P for the internal earpiece, AOUT2N and AOUT2P for an speaker, and finally AOUT3L and AOUT3R for an external earpiece. The two differential outputs for an earpiece are decoupled by some capacitors in order to prevent RF from being injected.

Audio signals may come from two sources: Either the built-in microphone or an external source, e.g. from a headset. Both inputs are differential and are named AIN1N and ANI1P respectively AIN2N and AIN2P. After a MUX to select the source 20dB preamplifier and programmable amplifier gain of +9dB with Input PGA gain settings in 1.5dB steps from 0 to 22.5dB is inserted before digitising the audio using a sigma-delta modulator. The ADC is followed by an anti-aliasing decimation filter and a digital high pass filter before being transmitted on the serial interface.

A 1.2 voltage reference for both the voiceband ADC's and DAC's and biasing the analog signals is also included. The raw reference is output on the REF pin for external decoupling using the capacitors C544, and a buffered output is available on the REFOUT pin.

1.2.3 The auxiliary section

The auxiliary section is addressed through a synchronous serial interface from the processor section of the ADBP, which is more or less identical with the baseband section serial interface. Data is input on the ASDI pin and output on the ASDO pin. A frame sync signals (ASFS) are provided (CSFS on the VBC side); Both pins are inputs, the signal being generated by the ADBP.

The RAMP converter is intended for controlling the power ramping of the RF power module. The ramp data is input to a built-in RAM and from here automatically clocked into the 10-bit DAC a fixed time after the TXON signal has been activated. An interpolator and a buffer are inserted between the DAC and the output pin for reducing the high frequency contents of the analog output signal.

The AGC converter is intended for controlling the gain in the receiver. It uses a fairly standard design, consisting of a 10-bit DAC with a buffer inserted before the signal reaches the output pin. In the MS AGC control is used to control gain in the receiver, but only as an on/off signal.

The AFC converter is used for controlling the 26MHz VCTCXO and consists of a 13-bit DAC. The output from this converter passes through a buffer before being output on the AFC pin.

Nine ADC inputs are provided, using a Sigma-Delta ADC with 12-bit accuracy and 16-bit resolution: Two differential inputs for temperature sensing, a differential input for the battery charger current sensor (ISENSE), a single ended input for battery voltage measurement (VBATSENSE), a single ended input for battery type identification (BATTYPE), two single ended inputs for microphone and hookswitch detection, one for each of two analog audio input channels (AIN1P, AIN2P), two general purpose external inputs (AUXADC1, AUXADC2).

1.2.4 Analog measurements

The VBC is equipped with 9 multiplexed ADC inputs. In the MS a total of 4 different measurements are required: Battery charger current sensor, Battery voltage, Battery type and earphone hook switch detect. The first three measurements are directly related to the charging of Li-Ion batteries (and to a lesser degree to the remaining battery capacity), whereas the last measurement is needed for detecting whether an hook switch of external microphone is pushed.

AUXADC1 is used to detect whether an external microphone or hook switch are connected or pushed. By measuring the bias voltage on the external microphone connection an external microphone can be detected. On hands free sets there is a hook switch which shorten the microphone

SIGNALS. THIS SWITCH FUNCTION IS SUPPORTED IN THE MS AS A HOOK ON/OFF SWITCH. AUXADC1 IS ALSO USED TO DETECT PUSHED HOOK SWITCH.

1.2.5 Other functionality

THE 13MHZ CLOCK SIGNAL MCLK IS SUPPLIED BY THE ADBP. BY BEING ABLE TO GATE IT OFF WHENEVER THE ABP IS INACTIVE IT IS POSSIBLE TO REDUCE THE CURRENT CONSUMPTION. THIS IS ESPECIALLY IMPORTANT IN STANDBY MODE.

THE TXON AND RXON PINS ARE BOTH USED FOR CONTROLLING THE TIMING OF RESPECTIVELY THE BASEBAND TRANSMIT AND RECEIVE SECTION.

THE ABBRESET PIN ALLOWS THE ADBP TO FORCE A COMPLETE RESET OF ALL REGISTERS IN THE ABP.

THE ABP IS EQUIPPED WITH A JTAG INTERFACE COMPRISED OF THE 4 STANDARD JTAG CHAIN SIGNALS: TDI, TDI, TCK AND TMS. THE JTAG TEST POINTS FOR THE AB AND THE ADBP ARE NOT DAISY CHAINED TOGETHER, AS SOME OF THE JTAG TEST POINTS ON THE ADBP ALSO ACTS AS DAI TEST POINTS.

THE POWER SUPPLY IS SPLIT INTO A DIGITAL AND AN ANALOG SECTION, EACH WITH SEPARATE GROUNDS.

2. Memory

THE MEMORY IN THE I-2100 CONSISTS OF A COMPLEX CHIP (U401), CONTAINING A 128MBIT FLASH ROM , 32MBIT SRAM.

THE FLASH IS EQUIPPED WITH A 16-BIT WIDE DATABUS D[15:0] FOR MAXIMUM SPEED AND THEREFORE ARRANGED AS 4M X 32-BIT. THE ADDRESS BUS A[21:0] IS 22-BIT WIDE, BUT AS THE FLASH IS USED IN WORD WIDE MODE A0 IS NOT USED, AND THE ADDRESS BUS IS THEREFORE CONNECTED TO A1-A21 FROM THE ADBP.

TO SELECT BETWEEN THE UPPER AND LOWER HALF OF THE FLASH, HOWEVER, IT IS BOTH NECESSARY TO GENERATE AN ADDITIONAL ADDRESS STROBE AND TO COMBINE TWO CHIP SELECTS, ONE FOR THE ORIGINAL $\overline{\text{CSROM}}$ AND ANOTHER FROM THE A23.

3 PINS ARE RESPONSIBLE FOR NORMAL OPERATION: A ROM ENABLE PIN IS F_$\overline{\text{CE}}$. F_$\overline{\text{OE}}$ IS AN OUTPUT ENABLE CONTROL AND CONNECTED TO THE $\overline{\text{RD}}$ SIGNAL ON THE ADBP. FOR CONTROLLING WRITES THE F_$\overline{\text{WE}}$ PIN IS CONNECTED TO THE $\overline{\text{WR}}$ PIN ON THE ADBP.

THE PIN IS A RESET INPUT FOR THE STATE MACHINE CONTROLLING THE OPERATION OF THE FLASH. CONNECTING MEMORY F_$\overline{\text{RST}}$ TO SYSTEM RESET SHOULD NOT CAUSE ANY PROBLEMS.

THE FLASH MEMORY HAS A MASTER WRITE PROTECT PIN (F_$\overline{WP}$; SOFT WARE LOCK). WHEN F_$\overline{WP}$ IS HIGH, LOCKED-DOWN BLOCKS CANNOT BE UNLOCKED. ERASE OR PROGRAM OPERATION CAN BE EXECUTED TO THE BLOCKS WHICH ARE NOT LOCKED AND LOCKED-DOWN. WHEN F_$\overline{WP}$ IS LOW, LOCK-DOWN IS DISABLED. F_$\overline{RY}$ /BY IS FLASH READY/BUSY OUTPUT SIGNAL.

THIS SRAM PROVIDES RUNTIME BUFFERING FOR ASSORTED VARIABLES. THE ADDRESS AND DATABUS PINS ARE SHARED WITH THE FLASH.

TRANSFERS ARE CONTROLLED BY CHIP ENABLE: S_CE1. S_CE1 IS CONNECTED TO THE ADBP $\overline{CSRAM}$ SIGNAL. VIA S_$\overline{LB}$ AND S_$\overline{UB}$ IT IS POSSIBLE TO ACCESS THE LOWER OR UPPER BYTE OF THE SRAM. S_$\overline{LB}$ IS CONNECTED TO $\overline{LBS}$ ($\overline{LWR}$) ON THE ADBP AND S_$\overline{UB}$ IS CONNECTED TO $\overline{UBS}$ ($\overline{HWR}$) ON THE ADBP.
THE POWER SUPPLY IS DECOUPLED BY THE CAPACITORS C407.

5. Microphone interface

BOTH THE INTERNAL AND EXTERNAL AUDIO INPUT MUST BE ABLE TO SUPPORT ELECTRET MICROPHONE CAPSULES, AND A BIAS VOLTAGE MUST THEREFORE BE APPLIED. THE BIAS VOLTAGE FOR THE MICROPHONE CAPSULES IS PROVIDED BY VMIC (2.5V).

THE BIAS IS PROVIDED THROUGH THE RESISTOR R508, R509 AND R513, R518 FOR THE INTERNAL AND EXTERNAL MICROPHONE. TO PREVENT TDMA NOISE INJECTION FROM THE INTERNAL MICROPHONE A CAPACITOR C507, C508 HAS BEEN PLACED FROM MIC+ TO MIC-, AND SIMILARLY CAPACITORS FOR EXTERNAL MICROPHONE + AND -. C511 IS DC BLOCKING CAPACITORS. C513 AND C514 PROVIDE DECOUPLING FOR INJECTED RF NOISE. C509 AND C510 LESSEN THE WHITE NOISE LEVEL FOR THE INTERNAL MICROPHONE, WHILE ALL OF CAPACITOR ON EXTERNAL MICROPHONE PATH PERFORM THE SAME FUNCTION.

6. Battery to Phone interface

The battery is connected to the phone with 4 connections (P101) of which two is ground. VBATT is the battery voltage. DCVOLT is the supply voltage from a charger.

6.1 Battery Charge Circuit

THE AD6535 HAS A PRECISION SINGLE CELL LI-ION BATTERY CHARGE CONTROLLER THAT CAN BE USED WITH AN EXTERNAL POWER PMOS DEVICE TO FROM A TWO-CHIP,LOW DROPOUT LINEAR BATTERY CHARGER.

CHARGE CURRENT CAN BE SET BY AN EXTERNAL RESISTOR (R519). THE AD6535 OPERATES WITH INPUT VOLTAGE RANGE IS 3.1V TO 5.25V.

7. SIM interface section

THE AD6535 (U500) PROVIDES ALL INTERFACING AND LEVEL TRANSLATION TO THE SIM CARD. THE GSM PHASE 2 SIM CARDS USES 3V LOGIC WHERE AS THE NEW GSM PHASE 2+ SIM CARDS USES 1.8V LOGIC, U500 IS CAPABLE OF OPERATING WITH BOTH TYPES OF SIM CARDS. THE INPUT AND OUTPUT CLOCK SIGNALS TO U500 ARE FILTERED BY C100 AND R103.

8. Keypad

THE KEYPAD IS FAIRLY CONVENTIONAL, CONSISTING OF A STANDARD SCAN MATRIX WITH 25 KEYS.

9. Display

THE DISPLAY IS 260,000 COLOR TFT LCD MODULE AND 65,000 COLOR CSTN SUB LCD MODULE RUNNING ON 2.7V LOGIC. ONE HAS ACTIVE AREA WHICH CONSISTS OF 128 (HORIZONTAL) BY 160 (VERTICAL) PIXELS AND THE OTHER CONSISTS OF 96 BY 64 PIXELS.

THE DOT PITCH OF MAIN LCD IS 0.078MM×3 (RGB) AND 0.234MM OF MAIN LCD. DOT SIZE OF SUB LCD IS 0.06MMX3 (RGB) WITH 0.01MM SPACING BY 0.2MM WITH 0.01MM SPACING.

THE MAIN LCD IS CONTROLLED THROUGH 16BIT PARALLEL INTERFACE USING DATA LINES AND SUB LCD IS CONTROLLED THROUGH 8BIT. THE DISPLAY IS SELECTED BY BOTH LCDCS PIN AND A4 ADDRESS PIN. A MAIN LCD SELECTION SIGNAL (LCDCS1) AND SUB LCD SELECTION SIGNAL (LCDCS2) ARE SELECTED BY DECODER (U602).

10. Backlight

BACKLIGHT CONTROL SIGNALS SUPPLIED FROM THE ADBP MAKES IT POSSIBLE TO DIVIDE THE BACKLIGHT IN DIFFERENT SECTIONS AND RUN THE BACKLIGHT IN DIFFERENT WAYS. MAIN AND SUB BACKLIGHT IS CONTROLLED BY LED DRIVER IC ON THE SUB PCB (U2). THE PIN3 ($\overline{\text{SHDN}}$) PWM SIGNAL IS HI ENABLES.

11. System connector control signal circuit

THE FUNCTIONS OF THE DIFFERENT PINS ON THE SYSTEM CONNECTOR ARE DESCRIBED IN THE PREVIOUS CHAPTERS.

PIN no	NAME	PIN no	NAME
1	VBATT	15	USC(4)
2	VBATT	16	USC(5)
3	DC VOLT	17	USC(6)

4	DC VOLT	18	DTR
5	GND	19	JTAGEN
6	NC	20	TDO
7	GND	21	TDI
8	GND	22	TMS
9	DEBUGTX	23	TCK
10	DEBUGRX	24	GND
11	USC(0)	25	GND
12	USC(1)	26	GND
13	USC(2)	27	VBATT
14	USC(3)	28	BAT-ID

RF Design Description

1 Transceiver Description

The Aero^{tm} I Transceiver is a complete RF front end for Triple band GSM and GPRS Wireless Communications. The transmit section interfaces between the baseband processor and the power amplifier. The receive section interfaces between the RF band-select SAW filters and the baseband processor.

The chipset consists of the Si4205 Multi-Band E-GSM/DCS/PCS Aero Transceiver. All sensitive components, such as RF/IF VCOs, loop filters, and tuning inductors, are completely integrated into a single package.

This RF Solution works together with the baseband chipsets AD6521 & AD6526 from Analog Devices.

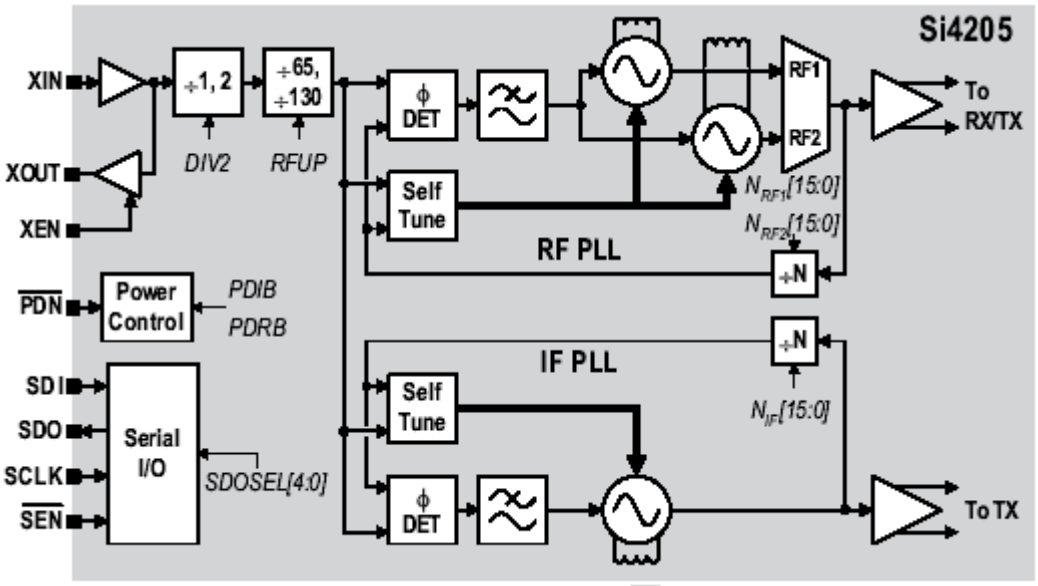
1.1 Frequency Synthesizer

The Aero transceiver integrates two complete PLLs including VCOs, varactors, resonators, loop filters, reference and VCO dividers, and phase detectors. The RF PLL uses two multiplexed VCOs. The RF1 VCO is used for receive mode, and the RF2 VCO is used for transmit mode. The IF PLL is used only during transmit mode. All VCO tuning inductors are also integrated.

The IF and RF output frequencies are set by programming the N-Divider registers, N_{RF1}, N_{RF2} and N_{IF}. Programming the N-Divider register for either RF1 or RF2 automatically selects the proper VCO. The output frequency of each PLL is as follows:

$$f_{OUT} = N * f_{\phi}$$

The DIV2 bit in register controls a programmable divider at the XIN pin to allow either a 13 or 26 MHz reference frequency. For receive mode, the RF1 PLL phase detector update rate (f_ϕ) should be programmed f_ϕ = 100 kHz for DCS 1800 or PCS 1900 bands, and f_ϕ = 200 kHz for GSM 850 and E-GSM 900 bands. For transmit mode, the RF2 and IF PLL phase detector update rates are always f_ϕ =200 kHz.



Scale : MHz

Band		RF1 VCO	RF2 VCO	IF VCO
E-GSM TX	880 ~ 895 900 ~ 915		1279 ~ 1314	798
	895 ~ 900			790
E-GSM RX		1849.8 ~ 1919.8		
DCS TX			1327 ~ 1402	766
DCS RX		1804.9 ~ 1879.9		
PCS TX			1423 ~ 1483	854
PCS RX		1929.9 ~ 1989.9		

1.2 Transmitter

The transmit (TX) section consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL) and two output buffers that can drive external power amplifiers (PA), one for the GSM 850 (824 to 849 MHz) and E-GSM 900 (880 to 915 MHz) bands and one

for the DCS 1800 (1710 to 1785 MHz) and PCS 1900
(1850 to 1910 MHz) bands. The OPLL requires no external duplexer to attenuate transmitter noise or spurious signals in the receive band. Additionally, the output of the transmit VCO (TXVCO) is a constant-envelope signal that reduces the problem of spectral spreading caused by non-linearity in the PA.

A quadrature mixer upconverts the differential in-phase (TXIP, TXIN) and quadrature (TXQP, TXQN) signals with the IFLO to generate a SSB IF signal that is filtered and used as the reference input to the OPLL. The IFLO frequency is generated between 766 and 896 MHz and internally divided by 2 to generate the quadrature LO signals for the quadrature modulator, resulting in an IF between 383 and 448 MHz. For the E-GSM 900 band, two different IFLO frequencies are required for spur management. Therefore, the IF PLL must be
programmed per channel in the E-GSM 900 band.

The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO. The TXVCO is centered between the DCS 1800 and PCS 1900 bands, and its output is divided by 2 for the E-GSM 900 bands. The RFLO frequency is generated between 1272 and 1483 MHz. To allow a single VCO to be used for the RFLO, high-side injection is used for the E-GSM 900 bands, and low-side injection is used for the DCS 1800 and PCS 1900 bands. The I and Q signals are automatically swapped when switching bands. Additionally, the SWAP bit in register can be used to manually exchange the I and Q signals. Low-pass filters before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs.

The outputs of Si4205 are used as inputs for the PA module. The power control of the PA is done by a closed loop implementation using a coupled detector at the output of the PA. The diplexer separation is obtained with a simple RX/TX switch. The antenna port of the RX/TX switch is connected to the antenna through matching circuitry.

1.3 Receiver

The Aero I transceiver uses a low-IF receiver architecture which allows for the on-chip integration of the channel selection filters, eliminating the external IF SAW filter required in conventional superheterodyne architectures.

Compared to a direct-conversion architecture, the low-IF architecture has a much greater degree of immunity to DC offsets, which can arise from RF local oscillator (RFLO) self-mixing, 2nd order distortion of blockers, and device 1/f noise. This relaxes the common-mode balance requirements on the input SAW filters.

The Si4205 integrates three differential-input LNAs for the E-GSM (925~960MHz), DCS (1805~1880MHz) and PCS (1930~1990Mhz) bands which are matched to the 150Ω differential-output SAW filters through external LC matching networks.

An image-reject mixer downconverts the RF signal to a 100KHz intermediate frequency (IF) with the RFLO from synthesizer. The RFLO frequency is between 1804.9 to 1989.8MHz, and is internally divided by 2 for E-GSM mode. The mixer output is amplified with an analog programmable gain amplifier (PGA). The quadrature IF signal is digitized with high resolution A/D converters (ADCs).

The ADC output is downconverted to baseband with a digital 100KHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interference signals.

In the analog baseband interface mode, DACs drive a differential analog signal onto the RXIP, RXIN, RXQP, and RXQN pins to interface to standard analog-input baseband ICs (AD6521).

1.4 RF Specification

E-GSM 900

Output Power

Power Level	Output Power
5	33dBm ±2dB
6	31dBm ±3dB
7	29dBm ±3dB
8	27dBm ±3dB
9	25dBm ±3dB
10	23dBm ±3dB
11	21dBm ±3dB
12	19dBm ±3dB
13	17dBm ±3dB
14	15dBm ±3dB
15	13dBm ±3dB
16	11dBm ±5dB
17	9dBm ±5dB
18	7dBm ±5dB
19	5dBm ±5dB

Power class	4
Number of RF channels	170
TX frequency range	880.2 MHz to 914.8 MHz
RX frequency range	925.2 MHz to 959.8 MHz
Duplex offset(frequency)	45 MHz

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Tel : +82-31-707-3860 / Fax :+82-31-703-7352
Home : www. Innostream.com /e-mail : erin@innostream.com

Duplex offset (time RX-TX)	3 timeslots
Channel spacing	200 KHz
Modulation type	0.3 GMSK
Modulator type	I/Q
Maximum frequency error	< ± 0.1 ppm
Maximum phase error	Peak < 20 degrees
	RMS <5 degrees
Receiver BER at -102 dBm	BER < 0.244%
	Class II RBER < 2.439%
	Class Ib RBER < 0.41%

DCS 1800

Output Power

Power Level	Output Power
0	30dBm ±2dB
1	28dBm ±3dB
2	26dBm ±3dB
3	24dBm ±3dB
4	22dBm ±3dB
5	20dBm ±3dB
6	18dBm ±3dB
7	16dBm ±3dB
8	14dBm ±3dB
9	12dBm ±4dB
10	10dBm ±4dB
11	8dBm ±4dB
12	6dBm ±4dB
13	4dBm ±4dB
14	2dBm ±5dB
15	0dBm ±5dB

Power class	1
Number of RF channels	374
TX frequency range	1710.2 MHz to 1784.8 MHz
RX frequency range	1805.2 MHz to 1879.8 MHz

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Home : www. Innostream.com /e-mail : erin@innostream.com

Duplex offset(frequency)	95 MHz
Duplex offset (time RX-TX)	3 timeslots
Channel spacing	200 KHz
Modulation type	0.3 GMSK
Modulator type	I/Q
Maximum frequency error	< ± 0.1 ppm
Maximum phase error	Peak < 20 degrees
	RMS <5 degrees
Receiver BER at -102 dBm	BER < 0.244%
	Class II RBER < 2.439%
	Class Ib RBER < 0.41%

PCS 1900

Output Power

Power Level	Output Power
0	30dBm ±2dB
1	28dBm ±3dB
2	26dBm ±3dB
3	24dBm ±3dB
4	22dBm ±3dB
5	20dBm ±3dB
6	18dBm ±3dB
7	16dBm ±3dB
8	14dBm ±3dB
9	12dBm ±4dB
10	10dBm ±4dB
11	8dBm ±4dB
12	6dBm ±4dB
13	4dBm ±4dB
14	2dBm ±5dB
15	0dBm ±5dB

Power class	1
Number of RF channels	299
TX frequency range	1850.2 MHz to 1909.8 MHz

RX frequency range	1930.2 MHz to 1989.8 MHz
Duplex offset(frequency)	80 MHz
Duplex offset (time RX-TX)	3 timeslots
Channel spacing	200 KHz
Modulation type	0.3 GMSK
Modulator type	I/Q
Maximum frequency error	< ± 0.1 ppm
Maximum phase error	Peak < 20 degrees
	RMS <5 degrees
Receiver BER at -102 dBm	BER < 0.244%
	Class II RBER < 2.439%
	Class Ib RBER < 0.41%

1.5 Initialization and Mode Control

The table below shows all the interface signals for the RF section including signals that are generated internally in the RF section.

Group	Name	Description	Type	Direction
Power Supply	VBATT	Supply from battery	Supply	← Battery
	VCC_AERO	Regulated supply for Aero^{tm} I	Supply	Internal
RF Control	VC1 note1	Control the Antenna switch (Band, TX/RX)	Digital	← AD6526
	VC2 note1	Control the Antenna switch (Band, TX/RX)	Digital	← AD6526
	VC3 note1	Control the Antenna switch (Band, TX/RX)	Digital	← AD6526
	GSM_ON	Control the band of PA (High : GSM)	Digital	← AD6526
	PDNB	Power down input (Active Low)	Digital	← AD6526
	RAMP	Control the power level and ramp	Analog	← AD6521
	TXPA	Enable the PA controller (Active High)	Digital	← AD6526
	CLKON	Activates VCC_AERO and 26MHz clock output	Digital	← AD6526
TX/RX Data	ITXP, ITXN	Differential I-signal for TX modulator	Analog	← AD6521
	QTXP,QTXN	Differential Q-signal for TX modulator	Analog	← AD6521
	IRXP, IRXN	Differential I-signal from RX demodulator	Analog	→ AD6521
	QRXP,QRXN	Differential Q-signal from RX demodulator	Analog	→ AD6521
Synth Control	SYNTHCLK	**Clock signal for serial programming bus**	Digital	← AD6526
	SYNTHDATA	Data signal for serial programming bus	Digital	← AD6526
	SYNTHEN	Enable signal for PLL programming	Digital	← AD6526

TCXO	CLK26M	26 MHz reference for baseband section	Analog	➔ AD6526
	AFC	Automatic frequency correction signal	Analog	← AD6521

Note 1. Antenna Switch control logic for Triple band (GSM / DCS / PCS)

Mode	VC1	VC2	VC3
GSM_TX	High	Low	Low
DCS/PCS_TX	Low	High	High
GSM_RX	Low	Low	Low
DCS_RX	Low	Low	Low
PCS_RX	Low	Low	High

1.5.1 Operating Modes

This section defines the various operating modes for the transceiver section along with the actions necessary to change the mode.

1.5.1.1 RF Inactive

RF Inactive mode for the transceiver section is defined as the mode where the receiver is not receiving and the transmitter is off. To reduce power consumption in RF Inactive mode, a slow clocking scheme has been designed into the baseband chip set. This allows the 26MHz-reference oscillator to be powered down when the phone is not receiving paging messages.

Conditions for RF Inactive mode :

CLKON = Low (depending on slow clocking state)

1.5.1.2 RF Receive Mode

In this mode the receiver circuits are active and the synthesizers are programmed to a RX channel.

Conditions for RF Receive mode:

CLKON = High

PDNB = High

VC1, VC2 = Low, VC3 = Low : GSM / DCS RX Mode

VC1, VC2 = Low, VC3 = High : PCS RX Mode

1.5.1.3 RF Transmit Mode

In this mode the transmitter circuits are active and the synthesizers are programmed to a TX channel. The TXPA signal is set to high and the RAMP signal is set to the appropriate power level.

Conditions for RF Transmit mode:

CLKON = High

RAMP = High

TXPA = High (only during active part of TX-burst)

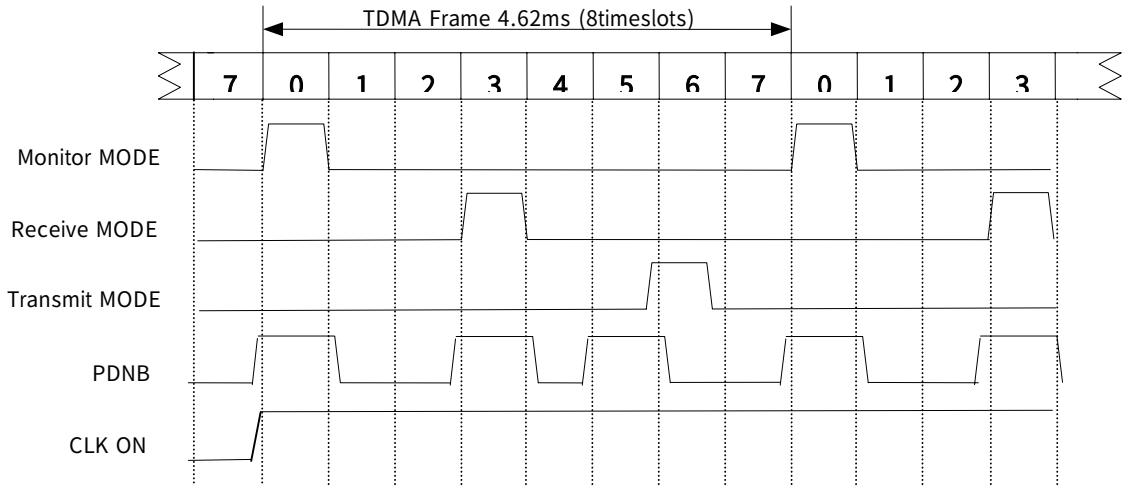
PDNB = High

VC1 = High, VC2, VC3 = Low, GSM_ON = High : GSM TX mode

VC1 = Low, VC2, VC3 = High, GSM_ON = Low : DCS / PCS TX mode

1.5.1.4 Conversation Mode

This mode consists of a combination of RF Receive, RF Monitor and RF Transmit states as shown below.



2 RF Circuit Description

This chapter contains circuit descriptions for the RF transceiver section, which is divided into 5 sub-sections. Each of the sections listed below is described in the following paragraphs.

- ＊RF Power supply description with an explanation of related control signals
- ＊Frequency Reference 26MHz and microprocessor clock oscillator
- ＊Frequency Synthesizer Section, with IF and RF PLL
- ＊Transmit Section
  - ＊Offset-PLL Transmitter
  - ＊TX Power Amplifier
  - ＊Antenna Switch and Antenna Matching Circuits
- ＊Receive Section
  - ＊RF Front-End
  - ＊Low-IF Receiver
  - ＊Universal Baseband Interface Receiver section

2.1 RF Power Supply (See Schematic 1, 7)

The power supply to the RF section consists of a low-dropout (LDO) regulator and a direct battery supply.

The LDO voltage regulator (U101) generates VCC_AERO (2.8V) with high state of CLKON signal. And the voltage regulator (U101) supplies Aero^{tm} I (U704), TCXO (U708), and APC IC (U700) with electric power. In the slow-clocking mode CLKON signal is set to low, then the voltage regulator (U101) is switched off.

The Power Amplifier (PA) module (U701) is supplied electric power directly from the battery (VBATT) through low impedance PCB lines

2.2 Frequency Reference 26MHz (See Schematic 7)

AS the frequency reference the 26MHz TCXO (U708) output is used in the MS. Most of the timings are derived from the 26MHz reference, or multiples.

The TCXO (U708) is supplied electric power from the voltage regulator (U101). During the slow clocking period, the 26MHz oscillator is periodically switched off in order to save current.

The Automatic Frequency Correction (AFC) signal is the DAC value from the baseband controller (U500) pin A10. This signal is derived from the GSM layer 1 synchronization algorithm that adjusts the 26 MHz reference to the signal received from the GSM system. AFC is filtered by RC filter (R715, C732) to prevent noise from entering the TCXO control input. The 26 MHz clock (output of TCXO) is used as frequency reference in the Aero^{tm} I (704), and buffered through the internal buffer of the Aero^{tm} I (704). The buffered frequency reference clock is sent to AD6526 (U600).

2.3 Frequency Synthesizer (See Schematic 7)

Two complete PLLs including VCOs, varactors, loop filters, reference and VCO dividers, phase detectors and tuning inductors are integrated in the Aero^{tm} I transceiver (U704). One is RF PLL that uses two

multiplexed VCOs. The RF1 VCO is used for receive mode and RF2 VCO is used for transmit mode. The other is IF PLL used only during transmit mode.

The reference clock frequency for both PLLs is 26MHz and generated by the TCXO (U708). In a GSM/DCS/PCS transceiver it is required to switch to transmit, receive, or monitor mode. Therefore the synthesizer is constantly reprogrammed. The synthesizer is programmed via a serial bus (SYNTHEN, SYNTHDATA, and SYNTHCLK). The frequencies for the RF and IF VCO in the various modes can be seen in the table below.

Scale : MHz

Band		RF1 VCO	RF2 VCO	IF VCO
E-GSM TX	880 ~ 895 900 ~ 915		1279 ~ 1314	798
	895 ~ 900			790
E-GSM RX		1849.8 ~ 1919.8		
DCS TX			1327 ~ 1402	766
DCS RX		1804.9 ~ 1879.9		
PCS TX			1423 ~ 1483	854
PCS RX		1929.9 ~ 1989.9		

2.4 Transmit Section (See Schematic 7)

2.4.1 Offset-PLL Transmitter

The transmit path consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL) and two output buffers which can drive the final power amplifier (PA) PF08127B (U701).

A quadrature mixer upconverts the differential in-phase (TXIP, TXIN) and quadrature (TXQP, TXQN) signals with the IFLO to generate a SSB IF signal that is filtered and used as the reference input to the OPLL.

The I/Q inputs to the modulator are the differential baseband signals from AD6521 (U500). The DAC in AD6521 (U500) delivers the baseband IQ signals TXIP, TXIN, TXQP and TXQN with the amplitude of approximately 1V and the common mode voltage of around 1.2V. The TXIP, TXIN, TXQP and TXQN are connected from AD6521 (U500) to Aero^{tm} I transceiver directly.

Low-pass filters before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs. Harmonics present at the phase detector can cause IM3 distortion and spurious energy in the transmit output spectrum.

2.4.2 TX Power Amplifier

The power amplifier section of the MS is designed with a triple-band PA module of PF08127B (U701). The PA section must raise the signal level to approximately 3.2W to ensure that 2.0W is present at the antenna for GSM and to 2.0W to ensure that 1.0W is present at the antenna in DCS mode. As in other cellular systems there is also a requirement for the PA section to provide means for the terminal software to set the output power at a specified level.

In phase II GSM mode, the class 4 MS has 15 power levels (5~19), ranging from 5dBm to 33dBm (at the antenna). In the phase II DCS / PCS mode, the class 1 MS has 16 power levels (0~15), ranging from 0dBm to 30dBm (at the antenna). Furthermore in the TDMA system, PA section must also allow the software to “ramp” the output power up and down as specified in the GSM 05.05 recommendation.

The outputs from the Aero^{tm} I transceiver are used as inputs for the triple band PA module, through the attenuator R703, R706, R707 for the GSM Band and R709, R710, R711 for the DCS / PCS band.

The triple-band PA module (U701) consists of high gain 3 stage MOS FET amplifiers for two chains. One is for GSM band and the other is for DCS/PCS band. GSM_ON signal injected to V_{CTRL} (pin7) from AD6526 (U600) controls which amplifier chain is active. The output level is set with an analog control voltage on the V_{APC} input (pin2).

The PA modules are intended for burst operation only, so if the PA modules are running continuously they are likely to be damaged (especially at high power levels). Likewise damage can occur if the voltage on the battery terminals is over 7V.

The directional coupler is used to supply part of the output signal to the power detector. The coupler (U702) is a dual directional coupler that can supply part of the output power from two power amplifier chains to the power detector. Therefore only one power detector is necessary to control the output power.

The power detector is built in the PA controller IC (U700). The log amp technique provides a much wider measurement range and better accuracy than using controllers based on diode detectors. Its high sensitivity (over a typical dynamic range of 50dB) allows control at low signal levels, thus reducing the amount of power that needs to be coupled to the detector.

The AD8315 (U700) provides a voltage output V_{APC} to control PA's gain. The voltage range of V_{APC} is normally 0~2.5V. Some of the output from the PA is coupled off using a dual band directional coupler. This has a coupling factor of approximately 19dB for the GSM band and 14dB for DCS / PCS band and an insertion loss of 0.4dB and 0.6dB respectively. Because the PF08127B (U701) transmits a maximum power level of +35dBm for GSM and +32dBm for DCS / PCS, additional attenuation of 20dB (R700, R704, R705) is required before the coupled signal is applied to the AD8315 (U700).

This results in peak input levels to the AD8315 of -4dBm (GSM) and -2dBm (DCS / PCS). While the AD8315 gives a linear response for input levels up to +2dBm, for highly temperature stable performance at maximum PA output power, the maximum input level should be limited to approximately -2dBm. This does, however, reduce the sensitivity of the circuit at the low end.

The V_{SET} (pin3 of U700) is supplied by an 8-bit DAC that has an output range from 0V to 2.5V. This sets the control resolution of V_{SET} the 0.4dB/bit. A RC filter (R708, C705) is used to stabilize the loop. This adds a zero to the control loop and increases the phase margin, which helps to make the step response of the circuit more stable when the PA output power is low and the slope of the PA's power control function is the steepest.

2.4.3 Antenna Switch and Antenna Matching Circuits

This section is designed with the triple-band antenna switch module (U707), which integrated two low pass filters, three switches, and one diplexer. The antenna switch (U707) is controlled by the VC1, VC2, and VC3 signal. The control logic is shown in the table below.

Mode	VC1	VC2	VC3
GSM_TX	High	Low	Low
DCS/PCS_TX	Low	High	High
GSM_RX	Low	Low	Low
DCS_RX	Low	Low	Low
PCS_RX	Low	Low	High

Antenna matching circuits need only 2~4 components for 50ohm matching and maximum power radiation.

2.5 Receiver Section (See Schematic 7)

The Aero^{tm} I transceiver uses a low-IF receiver architecture which allows for the on-chip integration of the channel selection filters, eliminating the external IF SAW filter required in the conventional Superheterodyne architectures.

Compared to a direct-conversion architecture, the low-IF architecture has a much greater degree of immunity to DC offsets, which can arise from RF local oscillator (RFLO) self-mixing, 2nd order distortion of blockers, and device 1/f noise. This relaxes the common-mode balance requirements on the input SAW filters.

2.5.1 RF Front-end

The GSM signal from the antenna switch (U707) pin9 is led to the GSM RX SAW filter (U703) pin1. The differential outputs from the SAW filter are matched to the LNA input (U704) pin 20,pin21 by the matching circuit C716, C718, L700.

The DCS signal from the antenna switch (U707) pin9 is led to the DCS RX SAW filter (U705) pin1. The differential outputs from the SAW filter are matched to the LNA input (U704) pin18, pin19 by the matching circuit C722, C726, L701.

Similarly The PCS signal from the antenna switch (U707) pin9 is led to the PCS RX SAW filter (U706) pin1. The differential outputs from the SAW filter are matched to the LNA input (U704) pin16, pin17 by the matching circuit C731, C733, L703.

2.5.2 Low-IF Receiver

The Aero^{tm} I (U704) integrates three differential-input LNAs for the E-GSM (925~ 960MHz), DCS (1805~1880MHz) and PCS (1930~1990MHz) bands that are matched to the 150ohm differential-output SAW filters through external LC matching networks.

LNA outputs are down-converted to the 100kHz IF signals through the internal quadrature mixer with RFLO from frequency synthesizer. And the mixer output is amplified with an analog programmable gain amplifier (PGA). The quadrature IF signal is digitized with high resolution A/D Converters (ADCs).

2.5.3 Universal Baseband Interface

The Aero^{tm} I (U704) integrates the universal baseband interface, which consists of an IFLO (100KHz), Channel Filters, IF Programmable Gain Amplifier, D/A Converters.

The ADC output is downconverted to baseband with a digital 100kHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking signal. After channel selection, the digital output is scaled with a digital PGA. It is required appropriate AGC algorithm using the LNA, analog PGA and digital PGA to provide a constant amplitude signal to the baseband receive inputs. In the analog baseband interface mode, DACs drive a differential analog signal onto the RXIP, RXIN, RXQP and RXQN pins to interface to standard analog input baseband ICs.