Genesis Medical Technology	Hardware Design Description Housecall 3	DWG # 490085
PREPARED DATE		PAGE 1 OF 41
APPROVED DATE		REVISION DATE **0.81** 9/8/03

Rev.	Initial	Date	Reason for Rev. Change
0.5	GL	12/10/01	First Draft
0.6	PC	1/25/02	Update document numbers and AGC description in section 5.4.4.2
0.7	GL	3/13/02	No 8K/64K transmit mode select. Section 5.4.3.2. SPORT 0/1 use swapped. SPORT 1 = A/D converter, SPORT 0 = Debug DAC, various sections updated. Modem shares the same nRESET used for the main DSP. Section 5.6.7 Device artifact 3dB frequency changed to 1kHz, and voltage threshold changed to 10mV in Section 5.5.7 nIRQE/IRQ2 usage swapped. IRQ2 = ECG VCO, nIRQE = 64K zero crossing detector. ECG power transformer is now driven by FL2. Sections 5.4.6, and 5.5.8.3 PF2/3 swapped. Lid switch is now PF3, phone detect is PF2. Sections 5.6.9, and 5.8.4 DSP resource map updated to include all the changes dated 3/13/02
0.8	GL	10/22/02	Updated DSP core logic drawing (5.3.1); edited clock frequency description and tables (5.3.3); deleted 1Mbyte Flash memory option. (5.3.5); corrected telemetry PLL description (5.3.9); added FL2 to DSP resource table (5.3.11). Updated wand Tx block diagram, description and timing diagram (5.4.3); corrected LNA description and tables – extra control signal UIF7 (5.4.4); updated DSP I/O table (5.4.6). Corrected ECG description and tables (5.5.4); also added description of surge protection and DC cutout (5.5.5); updated VCO frequency table (5.5.8); ECG power now derived from RFS0 (5.5.9). Removed TBDs from modem description (5.6); independent modem reset uses UIF6 (5.6.7); updated DSP I/O table (5.6.9); 1W speaker power rating is confirmed (5.7.1). Lid detect now uses a reed switch (5.8.1); piezo buzzer uses TLM7 and UIF4 (). Removed TBDs from power supply description (5.9); correct EMC standard is IEC60601-1-2 (5.9.4). Updated RS232 description, removed TBDs, max baud rate 57600 (5.10). DSP resource map (6.1) updated to include all the changes dated 10/22/02; deleted table (6.2) showing DSP memory requirements (moved to SDD). Updated assembly and test procedures (Section 7.x) Correct safety standard is IEC60601-1-1 (Section 8.1).

0.81	GL	1/14/03	Incorporated SJM feedback Added IEC60601-1, and IEC60601-1-2 to list of references (Section 3) Added stopband spec for 64K bandpass filter (Section 5.4.3.2) Corrected typing errors (Section 5.5.4) EMC test limits changed to Class B (Section 5.9.4) Correct safety standard is IEC60601-1 (Section 5.1 and section 8.1). Changed assembly sequence to suit a molded wand enclosure (Section 7.3)

TABLE OF CONTENTS

1. Purpose

The purpose of this document is to describe the details of the Housecall 3 Transmitter hardware architecture and design. This document will be used to guide the design of the system.

2. Scope

This document covers all Electrical, Mechanical, and Industrial design aspects of the Housecall 3 Transmitter system design. It also includes issues regarding the manufacture and/or testing of Housecall 3 Transmitter product.

3. References

GMT, 490080, Housecall 3 Hardware Requirements Specification

GMT, 490065, Housecall 3 Mechanical Requirements and Design

SJM, 10006748, Housecall 3 Transtelephonic Follow-up System Specification

SJM, QP035, Housecall 3 Quality Plan

SJM, ESXXXX, 8k/32k/64k Telemetry Implementation and Protocol

SJM, ES1164, 8K/8K Telemetry Protocol

SJM, 8010186, Scout Hardware Design

SJM, 1040152, Coil, AFP-Multi-Mode Telemetry Wand

SJM, ES1850, DTM2 Telemetry Board Hardware Specification

Conexant, 100490C, SmartSCM Modem Data Sheet

IEC60601-1 (1988) Medical Electrical Equipment , Part 1:General Requirements for Safety

IEC60601-1-2 (2001) Collateral Standard : Electromagnetic Compatibility – Requirements and Tests

4. Abbreviations and Definitions

The following terms and abbreviations are used in this document:

A/D	Analog to Digital; also known as ADC
AC	Alternating Current
AGC	Automatic Gain Control
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CRMD	Cardiac Rhythm Management Division

D/A	Digital to Analog; also known as DAC
DAA	Data Access Arrangement. A circuit consisting of passive components and high voltage discrete transistors / diodes which connects the modem to the phone line.
DC	Direct current
Device	Generic term for an implanted cardiac rhythm management device such as a bradycardia pacemaker or defibrillator
DMA	Direct Memory Access
DSP	Digital Signal Processor
ECG	Electrocardiogram
GMT	Genesis Medical Technology, Inc.
GPIO	General Purpose Input-Output
HRS	Hardware Requirement Specification
Hz	Hertz (cycles per second)
HV	High Voltage
kHz	Kilo-Hertz (Thousand Hertz)
LED	Light Emitting Diode
MHz	Mega-Hertz (Million Hertz)
nIOMS	Active-low I/O Memory Select. Chip select output pin on the DSP processor.
Operator	Any person operating the St Jude Medical CRMD Receiver. It may be a physician, clinician, technician, CRMD clinical engineer, etc.
Patient	A person who has an implantable Device
PSU	Power Supply Unit
RAM	Random Access Memory
Receiver	St Jude Medical CRMD instrument, usually located at a hospital or follow-up company, used in the transtelephonic follow-up of patients
RMS (rms)	Root Mean Square
SELV	Safety Extra Low Voltage
SJM	St. Jude Medical
SRS	Software Requirement Specification

System	Synonymous with Housecall 3 system (transmitter and receiver)
TBD	To Be Determined
TNV	Telecom Network Voltage
Transmitter	St Jude Medical CRMD instrument, usually located at a remote location such as the patient's home, used in the transtelephonic follow-up of patients
UART	Universal Asynchronous Receiver – Transmitter. A digital IC which translates data bytes between parallel and industry-standard serial signalling formats.
User	Any person operating the Transmitter. It is most likely a patient but may be an assisting family member, nurse, etc.
V; mV	Volts; millivolts

5. Electronics Design

5.1. Overall Architecture

The following diagram shows the electrical isolation barriers between the various elements of the Transmitter:

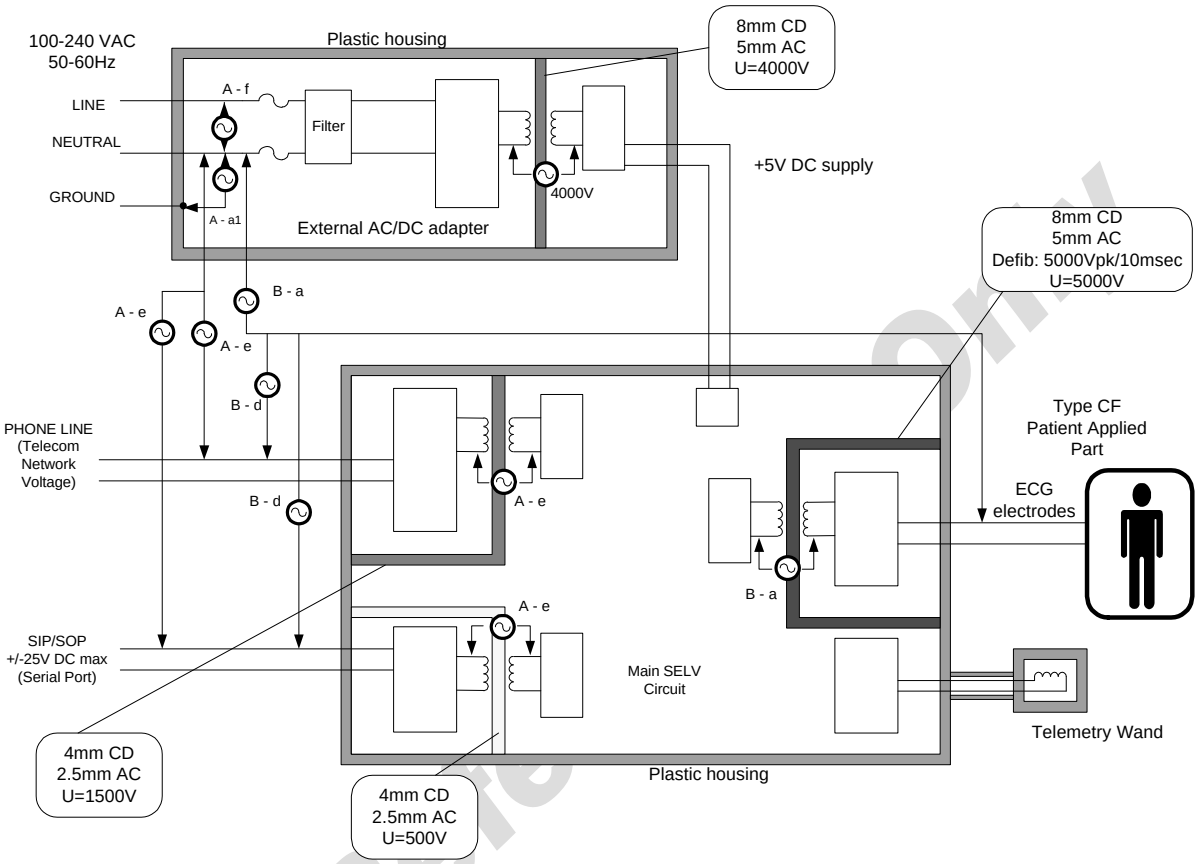

Figure 5.1a – Air Clearance (AC), Creepage Distance (CD) and Dielectric Strengths (U)

The 5 isolated circuits are: the Mains Part, the TNV part, the Signal Input and Output Part and the Patient–Applied Part, and the main SELV circuit. All signals between the Power Supply, phone line, SIP/SOP, and Patient Applied Part take place through the main SELV circuit. The letters in parenthesis such as "(A–f)" refer to IEC60601–1 Appendix E classifications. A tilde '~' denotes alternating current.

An overview of the electronics design is shown in the block diagram below:

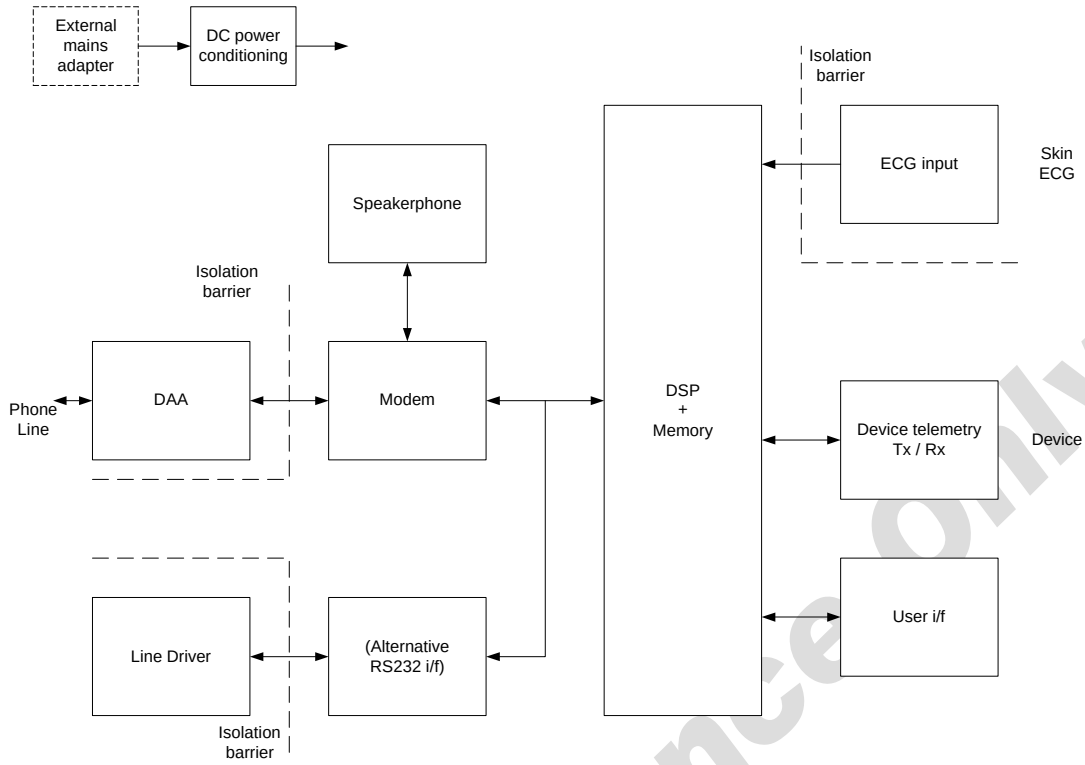

Figure 5.1b – Electronics Block Diagram

5.2. Electronics Construction

Most of the electronics will be constructed on a single PCB positioned horizontally in the base of the enclosure, with board-mounted connections for power and telephone at the rear.

A four-layer PCB will be used in order to reduce EMC emissions, using surface mount components unless cost or availability heavily favor through-hole parts. Components will be mounted on one side of the PCB only, with built-in microphone and loudspeaker connected via flying leads to low-cost connectors on the PCB. A device telemetry wand and ECG leads will be permanently connected to the unit, using low-cost connectors to mate with the PCB. User interface LEDs will be mounted to the front of the base moulding.

5.3. Control Processor and Memory

5.3.1. Block Diagram

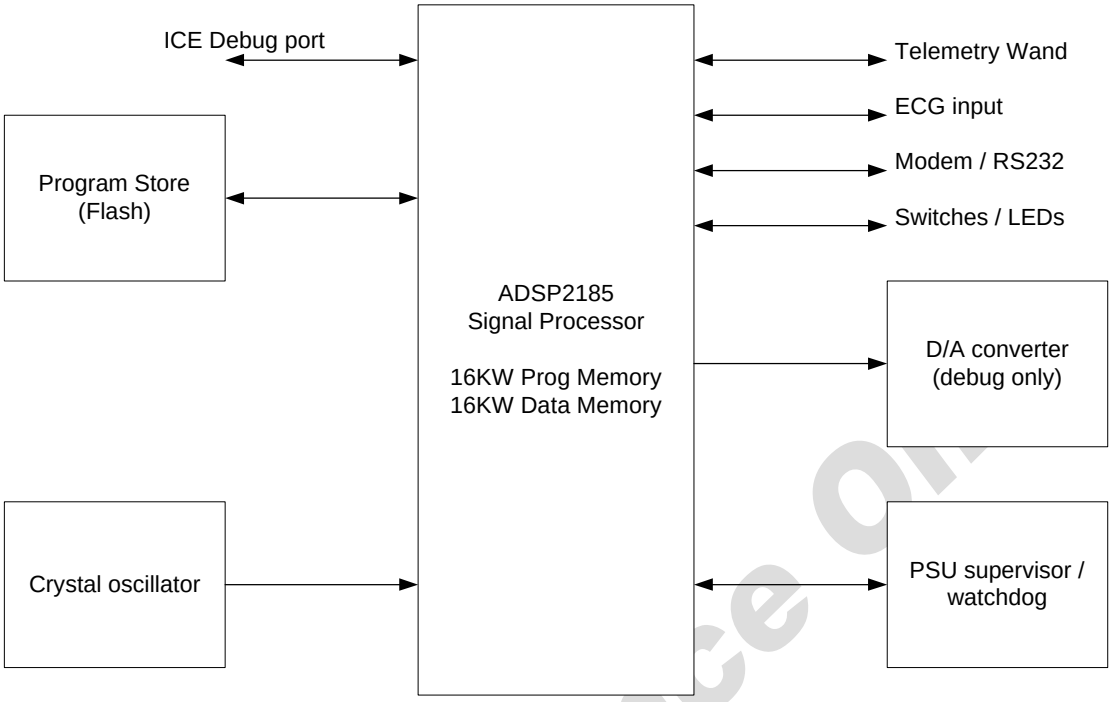

Figure 5.3.1 – DSP core logic

5.3.2. Main DSP Processor

The signal processing requirements for the HC3 divide into three main categories:

- data modem
- device telemetry operation
- ECG acquisition

For reasons discussed in Section 5.6 the data modem requires its own dedicated DSP processor. Therefore since St Jude already have a device telemetry implementation in manufacture, the natural choice for the main DSP is the same device family (Analog Devices ADSP2185). In addition to device telemetry the main processor will be required to implement signal capture from the skin ECG input, and manage the higher levels of communication with the remote Receiver station. Lastly the main DSP will implement low priority functions such as user interface control.

The required DSP hardware and memory resources are shown in the table in section 6.1 below. Several members of the ADSP218x family have this feature set, but it is most likely that the HC3 Transmitter will be built around an ADSP2185 processor.

5.3.3. Crystal Oscillator

The DSP operating frequency is set by an external crystal, which will be used as a clock source for all digital circuits except the modem and RS232 UART. In addition the crystal frequency must be in the range 15-20MHz to give the required DSP processing speed (in the ADSP2185 family this frequency is doubled internally to give an execution rate of 2 x Fosc). For the proposed design, a crystal frequency of 19.6608MHz (which is a standard comms frequency) satisfies all these requirements.

For 8K device telemetry, we need the DSP clock to be at an exact multiple of the A/D converter serial clock rate (sample rate x A/D serial clocks per sample). In addition, we need to configure the first DSP serial port SPORT1 as described in section 5.3.9.

DSP internal clock frequency (MHz)	39.3216
Device bit rate	8192
Required A/D converter sample rate	65536
Minimum A/D serial clock rate for 15 clocks/sample(MHz)	0.983040
DSP clock cycles per A/D sample	600
Serial port SCLK divisor	40
A/D converter serial clock rate (MHz)	0.983040
SCLK cycles per A/D sample	15

For 8K device telemetry, the design includes a debug D/A converter to provide real time analogue output (see section 5.3.10). SPORT1 is dedicated to the A/D converter, so this DAC uses the second DSP serial port SPORT0. The D/A clock frequency must be at least 16 times faster than the SPORT1 frame rate (to allow one D/A sample for each A/D sample on SPORT1).

DSP internal clock frequency (MHz)	39.3216
DSP clock cycles per D/A sample (same as A/D calculation above)	600
Serial port SCLK divisor	9
D/A converter serial clock rate (MHz)	4.369067
SCLK cycles per A/D sample	66.67

For 64K device telemetry, the A/D sample rate is equal to the telemetry bit rate (65536Hz), which imposes clock constraints identical to the requirements for 8K telemetry.

The last constraint is that all the chosen clock frequencies must be within the maximum allowed for each device.

Maximum allowable clock frequencies	Frequency (MHz)
ADSP218x signal processor (xtal frequency x 2)	80
MAX1248 A/D converter serial clock	2
AD5320 D/A converter serial clock	20

5.3.4. External Memory

5.3.4.1. Data Memory

External ADSP2185 data memory is not required.

5.3.4.2. Program Memory

External ADSP2185 program memory is not required.

Program code is stored in an external 8-bit Flash memory device connected to the ADSP2185 byte memory interface. The CPU includes a boot loader which copies code from the external Flash into on-chip program RAM at power up, and then begins execution.

5.3.4.3. Byte Memory

The Flash device which holds the program code is mapped onto the ADSP Byte Memory interface. This interface supports device sizes up to 4Mbytes which is well in excess of the code size for this product (expected code size <= 64k bytes). The design will support reprogramming of Flash memory contents in the field, via the phone connection.

5.3.5. Code Upgrades

Data can be read or written to the external Flash device at any time using a DMA controller integrated onto the CPU. This does not disturb execution of the current code version, since code is executed from on-chip Program RAM: it is therefore straightforward to copy a new program image into the Flash device while continuing to operate the data modem. To guard against communications errors which could cause download of a 'bad' code image, the Flash device is large enough to hold a simple boot program plus two complete application code images, each containing a CRC checksum. The software is then able to verify a new downloaded code image before the old image is erased: for details of how this procedure works see the SDD.

The most economic Flash memory size is currently 512k x 8: this is about 8 times larger than the anticipated code size, so is a convenient fit for the product requirements.

5.3.6. Watchdog / Reset

An external chip will provide Vcc supervision, power on reset, and software watchdog functions. The MAX705 provides the required functionality.

5.3.7. Debug Port

The ADSP218x family includes a dedicated ICE port allowing code and data download and debugging. Debugging tools run on a PC under any version of Windows, and require an external adapter connected via the PC RS232 serial port.

5.3.8. Additional Serial Debug Port

An additional RS232 serial port is provided to support two design requirements:

- To allow real-time software / hardware debug information to be displayed, without stopping program execution
- To allow a future product variant which will connect directly to a local PC via RS232, rather than to a Receiver via the data modem (see section 5.10)

The UART used for the RS232 data link is clocked by a separate 3.6864MHz crystal. This is divided within the UART to give a bit rate error <2% at various standard data rates:

RS-232 baud rate	**19200**	**38400**	**57600**	**115200**	**230400**
Reqd '16x' sample rate (assume industry-standard 16550 UART)	307200	614400	921600	1843200	3686400
Best CLK divisor	12	6	4	2	1
Actual sample rate	307200	614400	921600	1843200	3686400
Bit rate error (%)	0.00	0.00	0.00	0.00	0.00

These components will be depopulated in manufacture for the 'standard' Transmitter design. On the 'RS232' product variant these parts will form the interface to the local PC, and the real-time debug function will not be available.

The data modem, RS232 interface, and user interface buzzer and LEDs will be mapped onto the DSP I/O memory space, with a glue-logic decoder to gate the nIOMS output and provide individual chip select signals.

5.3.9. A/D Converter Connection

The design will include a MAX1248 multi-channel 10-bit A/D converter for wand telemetry functions. The A/D is connected directly to a DSP serial port, using the '15 clocks per sample' operating mode. This in turn allows the use of an industry standard frequency for the main crystal oscillator.

The DSP serial port is set to 15 data bits per frame. The position of the 'START' bit in the transmit word triggers the A/D to begin setting up a sample. The next serial port cycle is initiated when the A/D converter asserts its SSTRB output (eight clock cycles after receiving the 'START' bit), as shown in the diagram below

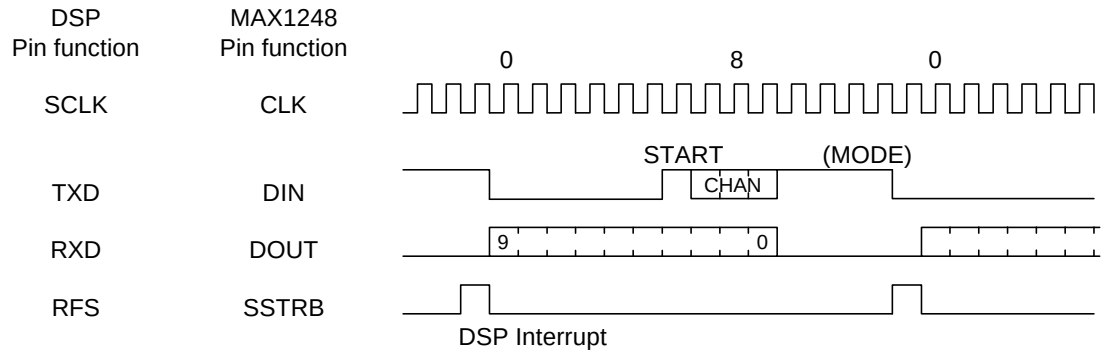

Figure 5.3.9 – A/D converter: detailed waveforms

Channel selection is accomplished in software by setting the appropriate 'CHAN' bits in the Tx word sent to the A/D converter.

Phase-locked loop control for device telemetry is implemented by increasing or decreasing the SCLK frequency for a short time. This allows the time when device Tx pulses are sent out to be brought forward, or delayed, by a small increment, providing fine adjustment of the telemetry frame period.

5.3.10.Debug D/A Converter

The board will include a header for connecting an AD5320 12-bit D/A converter, to allow debugging of the device telemetry software. The DAC provides a means of displaying the output from various DSP processing stages in real time, providing a powerful debugging tool especially when evaluating performance with poor device signal / high ambient noise.

Implementing this function via a header allows the possibility of debugging production units using the same techniques, without adding to the unit cost.

5.3.11.DSP I/O Requirements

The following table summarizes the DSP I/O resources required to operate the various core functions described in detail above.

Function	DSP pins	Notes
Watchdog	PF0, nRESET	Toggle at >1Hz from the main foreground processing loop
A/D converter	SPORT1	On each interrupt, read Rx data, then write a Tx word to trigger a new sample. Position of the START bit controls the timing of the next interrupt.
D/A converter	SPORT0	Write Tx data in response to SPORT1 interrupt.
Debug flags	FL0..FL2	Bit flags used as real time indicators for

		debugging.

5.4. Device Telemetry Interface

5.4.1. Block Diagram

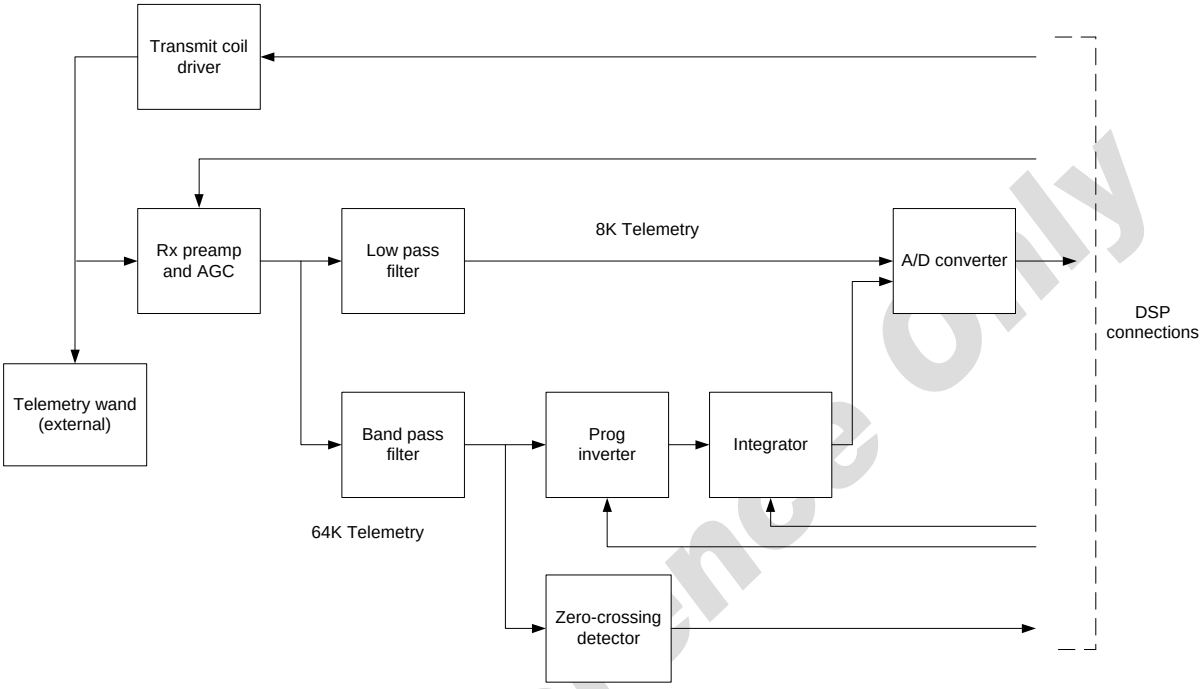

Figure 5.4.1 – Device telemetry interface

5.4.2. Device Telemetry Wand

The Transmitter implements St Jude 8K / 64K device telemetry using a hardware interface which closely resembles an existing St Jude design, as described in document 'DTM2 Telemetry Board Hardware Specification' (St Jude document ES1850). Device telemetry takes place via an external 'wand' (the same design supports both 8K and 64K telemetry) connected via a 2-core cable which is permanently fitted to the Transmitter. Inside the wand is simply an air-cored inductor, as shown on St Jude drawing 1040152: Coil, AFP-Multi-Mode Telemetry Wand.

5.4.3. Transmit

To transmit data bits to the device, the wand coil is used to generate a series of timed pulses, with a logical '1' represented by the presence of a pulse, and logical '0' by the absence of a pulse in the appropriate time slot.

The wand coil itself, together with a capacitor in the transmit circuit, forms an LC oscillator which is excited by a pair of FET switches. The shape of each transmit pulse is a single cycle at

the resonant frequency of this LC circuit, while the interval between pulses is timed by the CPU and corresponds to the telemetry bit period.

The basic transmit circuit therefore consists of three main elements:

- LC oscillator
- FET switching circuit
- dV/dt sensor

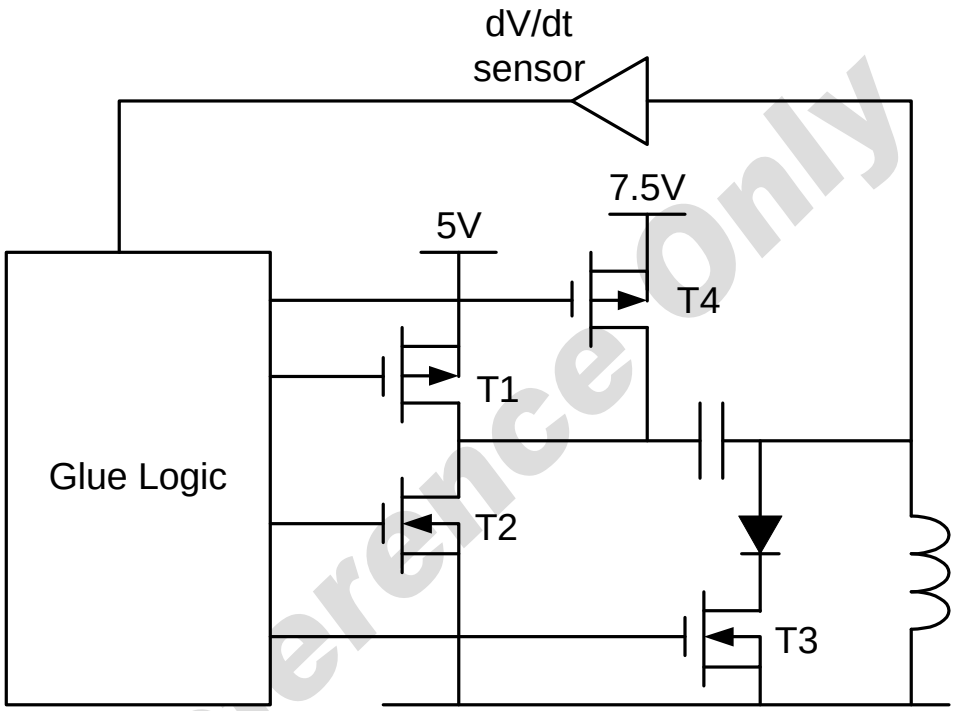

Figure 5.4.3a – Wand transmitter circuit

5.4.3.1. Timing Control

The FET switching circuit provides energy to the telemetry coil. It is 'fired' in response to a timed pulse from the CPU. In response to this pulse, FET T2 turns on to energize the coil in one direction (the design assumes that initially the capacitor has some stored energy); T2 remains on until the coil voltage reaches its maximum (dV/dt = zero), then FET T1 switches on (this applies drive current in the opposite direction). When the coil voltage returns to its negative maximum (dV/dt = zero again), both T1 and T2 switch off, and T3 switches on to prevent 'ringing' due to the coil and its stray capacitance. As this is a resonant circuit the amplitude of the output pulses builds with every transmit cycle until circuit losses balance the energy supplied by the switching FETs. In practice this gives a typical signal amplitude of 70V pk-pk.

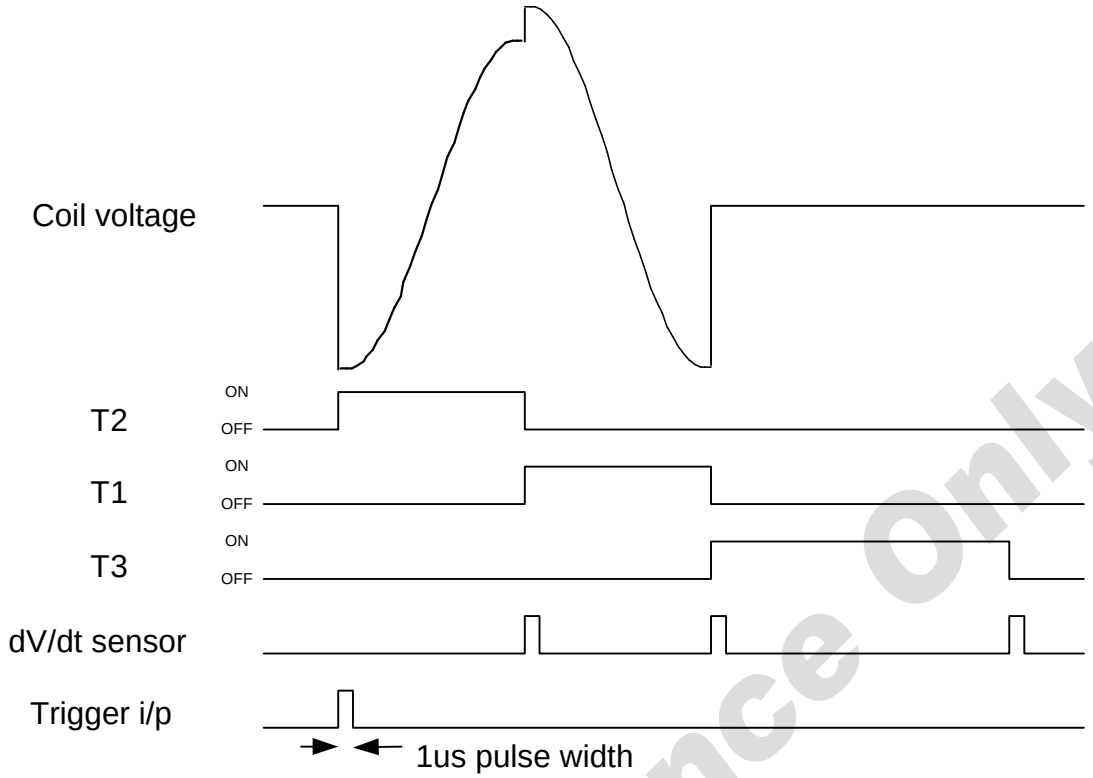

Figure 5.4.3b – Wand transmitter waveforms

5.4.3.2. 8K / 64K Operation

8K and 64K telemetry have different transmit bit rates, but use the same self-resonant frequency. The same coil drive circuit is therefore used for both telemetry protocols.

5.4.3.3. Tx Output Level

An additional control signal causes the glue logic to enable T4 rather than T1, increasing the coil drive voltage: this provides software selection of high / low output power levels. (Note: This capability may be depopulated in order to save cost, once a thorough evaluation has been performed on prototype 64K implants)

5.4.4. 8K Receive

For 8K telemetry, the signal from the device is amplified and then sampled by an A/D converter; the A/D result is then subjected to further filtering and processing in digital form by DSP software. The analog signal path includes the following elements:

- Low noise preamplifier
- AGC amplifier

- Band pass filter
- A/D converter

5.4.4.1. Preamplifier

The preamplifier is a wideband amplifier which senses the telemetry coil voltage directly, and has a voltage gain of approximately 1200. Obviously this amplifier is driven into saturation by wand transmit pulses: in order to protect the amplifier input a conventional virtual earth configuration (with a series input resistor) is used, with a pair of back to back diodes to limit the voltage swing at the input to +/-700mV once the amplifier saturates.

Amplifier noise in the band 6-12kHz is significantly lower than the smallest expected input signal level

	8K telemetry	64K telemetry
Minimum input signal level	6uV rms	6uV rms
Preamplifier gain	62 dB	41 dB
3dB bandwidth	7.95 – 14.5kHz	110 – 200kHz

The change in gain and 3dB bandwidth is achieved using analogue switches to connect different resistor and capacitor values, using control signal n8K_TLM.

.

5.4.4.2. AGC

AGC is needed to compensate for the wide variation in operating distance between the drive/sense coil and the device itself. Overall AGC range is 32 linear gain steps or 30dB.

Minimum gain	-30 dB
Maximum gain	0 dB

The AGC function is provided by a simple op amp gain stage, including a MAX5467 digital potentiometer which sets the gain under DSP control.

5.4.4.3. 3-pole Lowpass Filter

The lowpass filter provides additional gain over the narrow frequency band of interest. The lowpass rolloff improves rejection of most ambient noise sources, and prevents 'aliasing' by the A/D converter.

Midband gain	31 dB
3dB frequency for 8K telemetry	15.3kHz
Combined stopband attenuation (together with preamplifier)	50 dB at 60kHz

No DSP control is required for the lowpass filter.

5.4.4.4. A/D Converter

The 10-bit A/D converter is connected to one of the two dedicated synchronous serial ports on the DSP processor. During 8K telemetry the ADC takes data samples at 8 times the serial bit rate (65536Hz).

Phase and frequency lock to the device is achieved using a phase-locked loop implemented in DSP software. The DSP adjusts its frame rate in small increments by advancing or delaying the transmit pulses which occur at the start of each device telemetry frame. No further hardware support is needed for this function.

A multi-channel A/D converter will be used, so that a second A/D input can be used for 64K device telemetry (see below).

5.4.5. 64K Receive

5.4.5.1. Preamplifier and AGC

Shared with the 8K telemetry receive signal path.

5.4.5.2. 4-pole Bandpass Filter

Provides additional midband gain, and rejects ambient noise.

Midband gain	26 dB
3dB bandwidth	100 – 200kHz
Combined stopband attenuation (together with preamplifier)	>30dB attenuation at 5kHz and at 400kHz

No DSP control is required for the bandpass filter.

5.4.5.3. Programmable Inverter

To perform active 64K Telemetry, integration of the absolute value of the signal is necessary. To achieve this task, a phase selector is switched part way through each receive bit period (under DSP control) so that a constant signal polarity is presented to the integrator.

The phase selector consists of an op amp with an analogue switch to change its function from 'x1 follower' to 'x1 inverter'.

5.4.5.4. Integrator

The absolute value of the bandpass filter output is integrated by a simple op amp integrator. The integrating capacitor is discharged by closing an analog switch at the start of every bit period, under DSP control.

5.4.5.5. Zero-Crossing Detector

A zero crossing detector is connected to one of the DSP interrupt pins. During 64K telemetry the DSP has a counter running at a high multiple of the serial bit rate (the St Jude prototype implementation uses 384 * bit rate = 25165824Hz = DSP clock rate for the prototype hardware). Each zero-crossing interrupt logs the counter value, and this is compared with a theoretical value to give the control signal required by the software phase-locked-loop.

5.4.5.6. A/D Converter

During 64K telemetry the ADC samples the integrator output once during each serial bit period (sample rate = 65536Hz).

Phase and frequency lock to the device is achieved using a phase-locked loop implemented in DSP software. Just like 8K telemetry, the DSP adjusts its frame rate in small increments by advancing or delaying the transmit pulses which occur at the start of each device telemetry frame. No hardware support is needed for this function.

5.4.6. DSP I/O Requirements

The following table summarizes the DSP I/O resources required to operate the various device telemetry functions described above. All these resources are controlled by low-level device telemetry code originally supplied by SJM (but with I/O functions modified to support the HouseCall3 hardware implementation) :

Function	DSP pins	Notes
Transmit		
- Pulse timing	(TLM0..1)	Hardware timing circuit needs two control signals: CLR to initialize, accurately-timed FIRE triggers one output pulse.
- level control	(UIF5)	Select between two drive voltage levels, depending on device type
Receiver AGC (shared)	(TLM4..5)	Select one of 32 possible gain settings using 2 control signals. UP/nDOWN sets the desired 'direction'; then cycle CLK to change gain by the required number of steps.
8K receive		
- A/D converter	SPORT1	See section 5.3.9. Chan 0 used for 8K telemetry.
- LNA bandwidth	(UIF7)	Set low to select gain / bandwidth for 8K telemetry
64K receive		
- phase switch	(TLM2)	Analogue switch selects gain x1/x-1
- clear integrator	(TLM3)	Analogue switch clears integrator to zero
- zero-crossing detect	nIRQE	Generates a short pulse on each zero crossing of the amplified Rx signal
- A/D converter	SPORT1	See section 5.3.9. Chan 1 used for 64K telemetry.
- LNA bandwidth	(UIF7)	Set high to select gain / bandwidth for 64K telemetry

5.5. ECG Input

5.5.1. Block Diagram

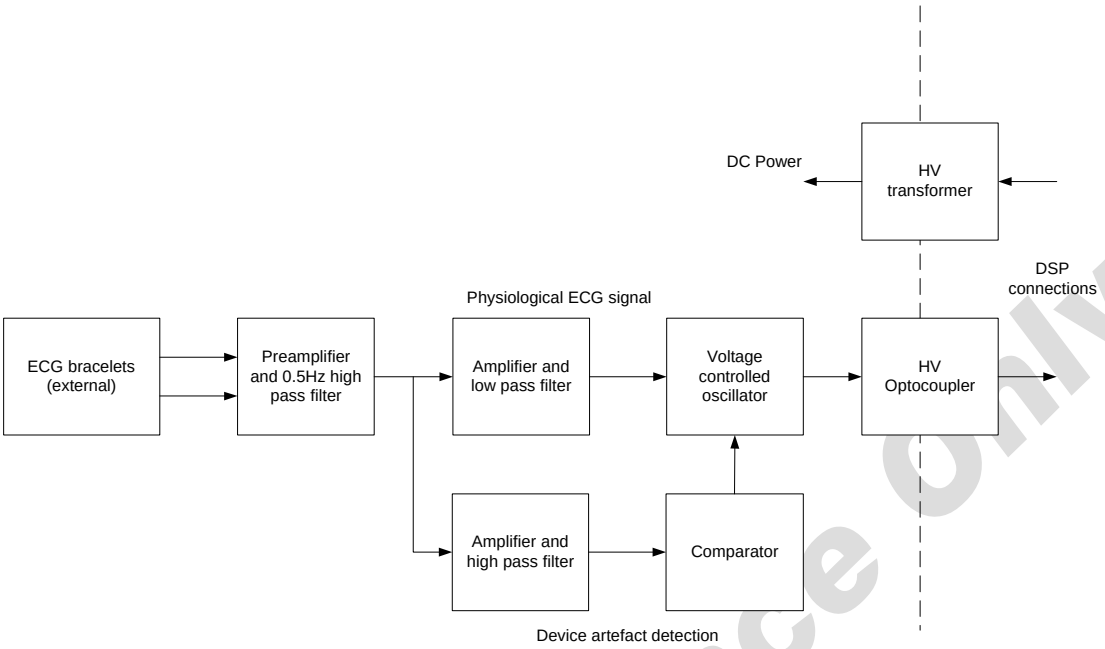

Figure 5.5.1 – Skin ECG input

5.5.2. Safety Isolation

The ECG input is separated from the main Transmitter circuit by a high-voltage isolation barrier. This provides maximum possible patient protection against overvoltage on the mains and telephone connections, while allowing a standard medical grade PSU, and standard modem components, to be used. The specification for this isolation barrier is shown in Section 8.1

Only two signals cross this HV isolation barrier:

- DC power is obtained via a high voltage transformer, driven by a square wave signal (frequency approx 135kHz) which is rectified on the ECG 'island'
- the filtered analog ECG signal is converted to a serial digital signal, which is coupled back to the main circuit using a high-voltage optocoupler.

5.5.3. Patient Leads

Connection to the patient's skin is via 2 individual leads which are permanently connected to the ECG 'island' on the Transmitter. The leads are terminated in standard snap connectors which accept wrist bracelets, finger pads, or stick-on ECG electrodes.

5.5.4. Analogue Preamp

The raw skin ECG signal contains physiological signals and also larger amplitude voltage spikes emanating from the device. The input preamplifier provides wideband gain, has a defined input impedance, and includes a single-pole high-pass filter to remove the DC component.

The ECG inputs are able to withstand 5kV defibrillation pulses. To achieve this, each preamp input is protected with a large series resistor to limit the input current, and a pair of diodes 'downstream' of the series resistor, limiting voltage excursions at the amplifier to one diode drop beyond the power rails.

Input impedance	>1Mohm
Input noise level	<25uV rms
Max DC offset	+/-300mV
Full-scale input signal level	+/-10mV
Absolute maximum input signal level	+/-5000V
Midband gain	24 dB
High-pass 3dB frequency	0.5Hz

5.5.5. DC cutout

The preamplifier becomes inoperable when a large input DC signal is applied. This condition is detected by a comparator circuit which monitors the DC level after the first preamplifier stage (all subsequent analogue circuits are AC coupled).

Maximum input DC level	+/-320mV

5.5.6. Physiological ECG Amplifier

The next amplifier stage provides additional gain for the frequency band of interest, and includes a 3-pole low-pass filter to remove ambient noise (and the device artifact signal). No attempt is made to remove mains pickup at 50/60Hz: under normal conditions the analog amplifier does not saturate, and the mains-frequency component is removed by a digital notch filter within the DSP.

Midband gain	14 dB
Low-pass 3dB frequency	100Hz
Passband flatness	+/-0.5dB 0.5 – 30Hz

5.5.7. Artifact Detection

The preamplifier output is also processed by a parallel signal path including a high-pass filter which removes the physiological signal, and a pair of comparators which are set to detect the edges of device artifacts (high-frequency voltage spikes), but ignore ambient noise.

Midband gain	40 dB
High-pass 3dB frequency	1 kHz
Device artifact threshold (referred to input)	10 mV

5.5.8. VCO

5.5.8.1. ECG Signal

The physiological ECG signal is fed to a voltage-controlled oscillator which generates a square wave output at around 70kHz (modulated by the ECG signal level so that the VCO period is proportional to ECG voltage). This signal is used to drive an optocoupler which is connected to an interrupt input on the main DSP. By measuring the period of the square wave signal against its own clock oscillator, the DSP completes an A/D conversion process.

VCO frequency range	50-90 kHz
DSP sample frequency	512 Hz
Minimum complete VCO cycles in each sample	97
DSP clock frequency	39.3216 MHz
#DSP clock cycles required to count 97 complete VCO cycles	76283 - 42379
Effective number of A/D steps	34k approx
Effective 'A/D resolution'	15 bits
Device artifact pulse width resolution (= one VCO period)	<20us

5.5.8.2. Device Artifact Signal

The device artifact detector provides a short output pulse on both edges of every device pulse. In order to pass this information across the isolation barrier, each time an edge is detected a complete cycle is 'stolen' from square wave produced by the VCO (at the end of the physiological ECG signal path). The DSP is able to detect these missing cycles and therefore measure the width of each device pulse, and can also add a software correction to reconstruct the original VCO square wave, before decoding the physiological ECG signal.

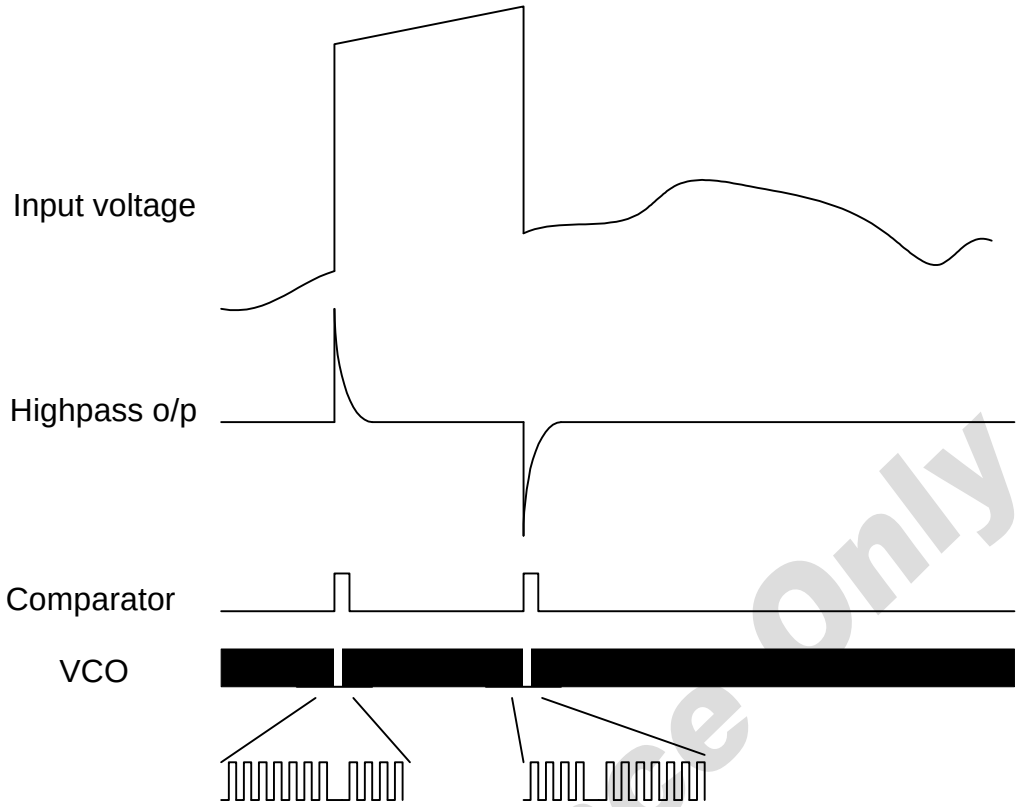

Figure 5.5.8– Artefact detection

5.5.8.3. ECG Inoperable Signal

The DC comparator simply disables the VCO if the input DC value goes beyond the specified limits. The DSP is able to detect that the VCO has stopped, and report the error condition as required.

5.5.9. DSP I/O Requirements

The following table summarizes DSP I/O resources required to operate the skin ECG functions described above:

Function	DSP pins	Notes
DC power	RFS0	Drive square wave output at approx 135kHz to provide DC power. The Rx section of SPORT0 is left free-running to generate this frequency.
VCO frequency measurement	IRQ2	Compare average interrupt period with system timer running at CPU CLK rate. Compare individual periods with 20us maximum, to detect missing cycles.

5.6. Modem / DAA

The modem is built around a 'SmartSCM' chip set purchased from Conexant, consisting of a mask-programmed DSP, a line-side codec, and a voice codec, as shown in the block diagram. Modem components will be depopulated on the 'RS232' build variant.

5.6.1. Block Diagram

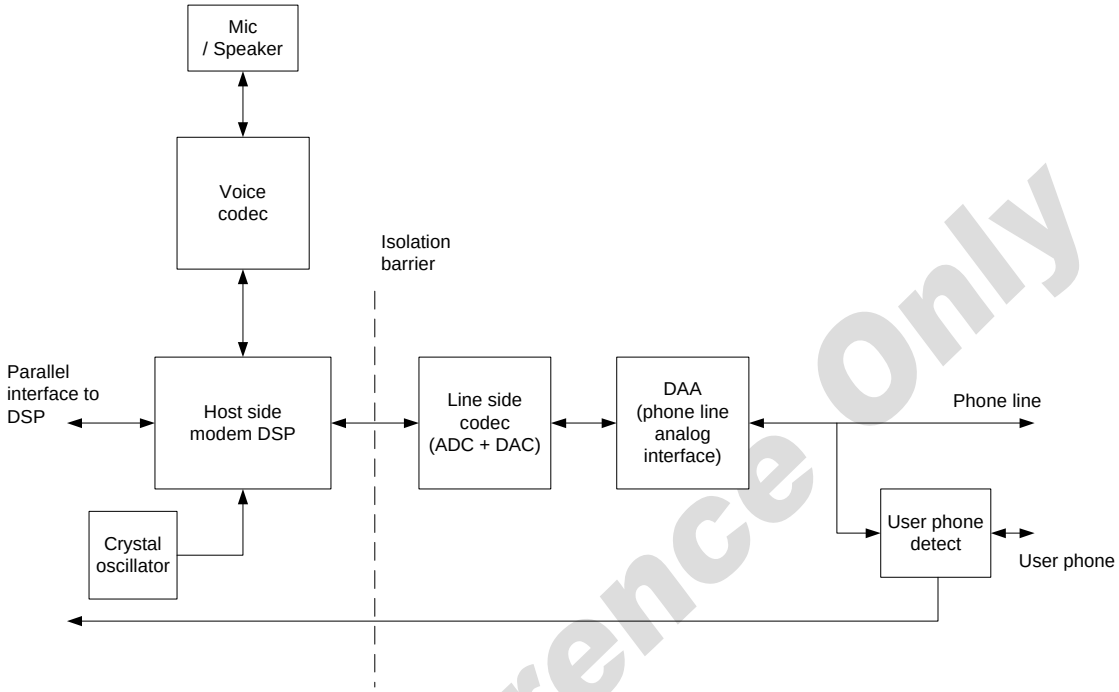

Figure 5.6.1 – Modem / Speakerphone

5.6.2. Safety Isolation

A conventional safety isolation barrier is required between the telephone network and the main part of the Transmitter circuit, which is classified as an SELV circuit according to the applicable safety standards. The modem chip set includes a line-side codec device (A/D and D/A converter) and passes digital data across the isolation barrier via high-voltage capacitors.

The speakerphone design is discussed in detail below: the speaker and microphone connect to the 'host side' of the isolation barrier.

The specification for this isolation barrier is shown in Section 8.1

5.6.3. User Phone Loopthrough

The Transmitter will connect directly to the phone network, and will provide a socket on the rear panel for connecting the patient's normal phone. The phone hook status will be determined by including a 'line current' relay in series with the phone socket: the relay coil is energized by DC

current drawn by the phone; the relay contacts are connected to a logic input on the host side of the isolation barrier.

5.6.4. International Usage Requirements

Telephone signaling requirements (DC voltage and current requirements, call progress tones etc) vary considerably between different countries. Many countries also have a formal approvals process before equipment can legally be connected to the telephone system, although there is currently no mandatory standard in use in the European Union (however most equipment manufacturers choose to test against the voluntary TBR21 standard).

Support for these differing signaling requirements will be provided by the modem chipset as a software-programmable feature. An 8-pin serial NVRAM (connected to the modem DSP) will be included in the design, providing an upgrade path for countries not supported by the mask-programmed code version. It is therefore likely that once the HC3 enters manufacture, one common build standard can be used for the main electronics board regardless of the end-user country. The following standards will be supported by the initial manufactured version:

Priority	**Country**	**Standard**
1	N America / Japan	FCC68
2	European Union	TBR21
2	Australia	AS/ACIF S002:2001

A complete list of target countries is contained in the document 'Housecall 3 International Market Analysis' (7 Aug 2001)

5.6.5. DTMF Detection

The modem chipset will provide DTMF tone decoding when it is off-hook and not in 'data transfer' mode. When a DTMF tone occurs, the modem sends a character sequence to the main CPU, so no additional hardware support is required for this function.

Each DTMF command consists of a sequence of 2 tones with specified duration and separation: this makes it very unlikely that a DTMF command could accidentally be triggered by pressing keys on the patient phone.

5.6.6. Connector Types

Two RJ11 sockets will be provided on the rear of the unit: one for connection to the phone network, the other for the patient phone. Since telephone connector types also differ widely between countries, a country-specific lead will be required for connection to the phone network; in some countries a second country-specific adapter will be required to connect the patient phone.

5.6.7. Modem Control

The modem chipset has an independent RESET signal, allowing software to seize immediate control, regardless of the current operating state of the modem.

Data transfers to and from the modem take place via a simple parallel interface, which emulates the industry-standard 16550 UART. The modem is connected directly to the main CPU address and data bus, with no additional glue logic required except for a decoder on the nIOMS chip select.

All modem software functions including country configuration, speakerphone, and DTMF detect, can be accessed using an extended version of the standard text-based 'AT Command Set'.

5.6.8. Crystal Oscillator

The modem chipset requires its own dedicated 28.224MHz crystal oscillator.

5.6.9. DSP I/O Requirements

The following table summarizes DSP I/O resources required to operate the modem functions described above:

Function	**DSP pins**	**Notes**
Data modem control	nIOMS, D0..7 A0..2, nRD, nWR, nIRQL0	8-byte shared-memory interface mapped into DSP I/O address space Addr Read Write 0 Rx data Tx data 1 Intr enable Intr enable 2 Intr status FIFO control 3 Line control Line control 4 Modem control Modem control 5 Line status Reserved 6 Modem status Reserved 7 (scratchpad) (scratchpad)
Patient phone status	PF2	Bit flag indicates on/off hook
Independent modem reset	(UIF6)	Logic low resets the modem hardware

5.7. Speakerphone

The speakerphone connects to the modem's 'host side DSP' via a dedicated codec IC, as shown in the block diagram in Section 5.6.1 above. Digitized signals connect to the phone network via the existing capacitive isolation barrier. Speakerphone components will be depopulated on the 'RS232' build variant.

5.7.1. Mic / Speaker

A standard low-cost condenser microphone will be provided in the base of the Transmitter unit, with a small-diameter opening on the underside to allow sound to enter. The microphone will be connected to the PCB with a short flying lead.

Audio output will be provided by a 1 Watt speaker fitted inside the top cover of the Transmitter, with a grille to allow sound to exit. The microphone connects via a simple preamplifier to an audio codec (A/D and D/A converter) which is part of the modem chipset. The speaker is connected via a small power amplifier as the codec is unable to drive a 1W output.

DSP-intensive audio attenuation and acoustic echo cancellation functions are implemented within the modem chipset, by the host side DSP part.

5.7.2. Speakerphone Control

Speaker and microphone enable/disable, and speaker output level, are controlled by the main ADSP2185 CPU, using an extended version of the 'AT command set'. The main CPU therefore monitors the user interface switches, volume slider, and incoming DTMF commands, and sends appropriate command strings to configure the speakerphone.

5.7.3. Isolation

The speakerphone circuit connects to the host side of the phone isolation barrier. No additional isolation components are required.

5.7.4. DSP I/O Requirements

No additional DSP I/O resources are required for the speakerphone.

5.8. User Interface

5.8.1. Switches

The transmitter lid includes a small magnet in the hinge mechanism. A single reed switch inside the main body of the Transmitter detects whether this magnet is nearby, and therefore whether the lid is open or closed. This switch is connected to a logic input which is interrogated by the main DSP as required.

The hook status of the user phone is also interrogated by the main DSP as described in section 5.6.3 above.

These two input signals are both debounced in software.

5.8.2. Audio Volume Control

A sliding audio volume control will be provided on the side of the Transmitter unit. The position of the slider is read by the main DSP using a spare A/D converter channel, and the modem chipset is then commanded to set the appropriate speaker output level. There is no user control over microphone input level.

5.8.3. LEDs / Buzzer

Three LEDs, and a small audio buzzer, are used to indicate the status of the Transmitter hardware to the patient. These resources are mapped onto an 8-bit latch connected directly to the main CPU address and data bus, with no additional glue logic required except for a decoder on the nIOMS chip select.

5.8.4. DSP I/O Resources

Function	**DSP pins**	**Notes**
Lid open switch	PF3	Bit flag indicates open/closed
LEDs	(UIF0..3)	Mapped onto an external latch. One bit flag to set the status of each LED. Note that the 'power' LED is a bi-color device so has two drive signals.
Buzzer	(UIF4) (TLM7)	A hardware AND gate combines these two external latch bits. TLM7 generates the excitation frequency, UIF4 holds the enable control.
Patient phone status		See data modem section 5.6 above
Volume control	(SPORT1)	See section 5.3.9. A/D converter Chan 2 used to read the slider position

5.9. Power Supply

5.9.1. External AC/DC Supply

The transmitter is powered by an external medical-grade AC/DC plug-top or cassette adapter (as used on most laptop PCs) providing a regulated 5V DC supply. The DC output from this adapter will not be connected to mains earth.

DC power will be connected to the main Transmitter unit using a 2.0mm barrel connector.

A number of specialist PSU manufacturers are able to supply a suitable AC/DC power unit with the relevant medical safety approvals.

5.9.2. International Usage

AC supply voltage and frequency, and connector types, vary between countries. Country-specific hardware will be provided within the external AC/DC adapter, allowing a common build standard for the main Transmitter unit.

Either a dedicated plug-top adapter for each country, or a cassette-style unit, with a separate power cord for each country, are equally acceptable manufacturing options.

5.9.3. Estimated Power Requirements

The 5V DC input from the external adapter will be subregulated to 3.3V by a simple linear regulator: this 3.3V rail supplies almost all of the Transmitter hardware. The exceptions are the audio power amplifier for the speakerphone (this requires 5V directly from the DC input jack) and the wand Tx circuit (which uses 5V power direct from the DC jack, and also has a small step up converter to provide 7.5V).

Function	**DC voltage**	**Current (mA)**
DSP	3V3	100
LEDs	3V3	50
Modem	3V3	~100
Device telemetry	3V3	20
	5V	10
	7V5	10
ECG (5V 'island' powered by a 3V3 logic signal)	(3V3)	~30
Speakerphone audio out	5V	100

Minimum current required from the AC/DC adapter	100 mA
Maximum current required from the AC/DC adapter	1000 mA
Total power required from the AC/DC adapter	<5 W
Estimated dissipation in the 3V3 regulator	500mW

5.9.4. EMC Filtering

The Transmitter is required to comply with IEC60601-1-2 , Class B EMC test limits.

On a unit with this architecture (a high speed processor on a 4-layer PCB) the worst EMC problems are typically related to cables rather than the layout of the board itself. Careful layout rules will therefore be followed in order to minimize any potential EMC problems:

- LC filtering on every off-board signal, positioned close to each cable (DC input jack, phone connectors, wand and ECG cables, and internal mic/speaker leads).
- All cables will be connected via 'quiet I/O islands' at the edges of the PCB. Only the signals connecting to the cables will be tracked onto these 'islands', all other traces, including power and ground planes, will stay clear of I/O connectors.

5.9.5. Power Switch

The Transmitter has no power switch. It is powered on whenever it is connected to an AC source, but spends most of its life in an 'inactive' state with most circuits disabled.

5.10.RS232 Interface (build option)

5.10.1.Safety Isolation

A safety isolation barrier is required between the RS232 cable and the main part of the Transmitter circuit. This allows the RS232 product variant to be connected to a standard PC and peripherals.

This isolation barrier is implemented using SFH6316 optocouplers.

The specification for this isolation barrier is shown in Section 8.1

5.10.2.Additional Components

A 3-wire RS232 serial interface is included in the Transmitter design, allowing the modem to be replaced with a serial link to a local PC running a version of the Receiver software.

Additional components are a hardware UART providing industry-standard data rates, an 'isolated' RS232 level transceiver, and a D9 connector accessed via a punch-out in the rear panel. These components are depopulated on the 'standard' Transmitter design (on the 'RS232' version, the modem chipset is depopulated instead).

Due to the speed of the SFH6316 optocouplers, the maximum data rate is 57600baud.

5.10.3.Clock Source

The RS232 serial baud rate is generated inside the UART using an internal baud rate generator to divide down the 3.6864MHz clock input signal.

5.10.4.RS232 Control

The RS232 port is controlled via a simple industry standard parallel interface, identical to the modem control interface described in section 5.6.9. The UART is connected directly to the main CPU address and data bus, with no additional glue logic required except for a decoder on the nIOMS chip select.

5.10.5.DSP I/O Requirements

There are no additional DSP I/O pin requirements. As far as the application software is concerned, the RS232 interface is identical to the modem chipset on the standard Transmitter implementation, except that it is mapped onto a different base address. However, a number of supporting software changes will be required as there is no speakerphone or user phone in the system.

Function	**DSP pins**	**Notes**
RS232 control	nIOMS, D0..7 A0..2, nRD, nWR, nIRQL1	8-byte shared-memory interface mapped into DSP I/O address space Addr Read Write 0 Rx data Tx data 1 Intr enable Intr enable 2 Intr status FIFO control 3 Line control Line control 4 Modem control Modem control 5 Line status Reserved 6 Modem status Reserved 7 (scratchpad) (scratchpad)

6. DSP Software Implications

6.1. DSP Resource Map

The following table shows the DSP addresses used to control each hardware resource. Note that there are two external 8-bit output-only latches TLM0..7 and UIF0..7 mapped into I/O address space.

Function	**ADSP2185 Resource Use**	**ADSP2185 Address Range**
Watchdog	PF0 nRESET	DM:0x3EF6 (direction), DM:0x3EF5 (value) -
External Program Flash	External addr and data bus (max 4M x 8), nWR, nRD, nBMS chip select BDMA registers	BM:0x00000 – 0x7FFFF (each access requires BDMA registers at DM:0x3FE1 – 0x3FE4 to be set up first)
Wand telemetry - A/D converter - AGC - Tx drive - 64K phase sw - 64K integrator - Tx power level - LNA bandwidth - 64K zero detect - Debug DAC	 DR1, DT1, SCLK1, RFS1, TFS1 TLM4..5 TLM0..1 TLM2 TLM3 UIF5 UIF7 nIRQE DT0, TFS0, SCLK0	 DM:0x3FEF - 0x3FF2 (control), RX1, TX1 IOM:0x300 (value) (as above) (as above) (as above) IOM:0x200 (value) (as above) - DM:0x3FF3 - 0x3FFA (control), TX0
ECG capture	RFS0 IRQ2	DM:0x3FF3 - 0x3FFA (control) -
Modem - independent reset	D0..7, A0..2, nRD, nWR, nIRQL0, nIOMS (gated by A8..9) DMWAIT UIF6	IOM:0x001 – 0x007 (control) IOM:0x000 (data) Set DMWAIT to provide 7 wait states IOM:0x200 (value)
Speakerphone	None (controlled via the modem)	

Function	**ADSP2185 Resource Use**	**Description**
User i/f - Lid switch - Phone detect - 3 LEDs - Buzzer	 PF3 PF2 UIF0..3 UIF4, TLM7	 DM:0x3EF6 (direction), DM:0x3EF5 (value) (as above) IOM:0x200 (value) IOM:0x200 (value), IOM:0x300 (value)
RS232 (not standard)	D0..7, A0..2, nRD, nWR, nIOMS, nIRQL1 (gated by A8..9) DMWAIT	IOM:0x501 – 0x507 (control) IOM:0x500 (data) Set DMWAIT to provide 3 wait states
External TLM register	D0..7, nWR, DMWAIT, nIOMS (gated by A8..9)	IOM:0x300 Set DMWAIT to provide 15 wait states
External UIF register	D0..7, nWR, DMWAIT, nIOMS (gated by A8..9)	IOM:0x200 Set DMWAIT to provide 15 wait states
ICE interface	JTAG emulator port	-
Debug flags	FL0, FL1, FL2	-
I/O wait state control	DMWAIT	DM:0x3FFE Bits 8 - 6 : RS232 wait states Bits 5 – 3 : TLM / UIF latch wait states Bits 2 – 0 : modem wait states

6.2. DSP Memory Requirements

DSP Program and data memory requirements are listed in the SDD.

7. Manufacturing Considerations

7.1. Board Level Test

The main PCB layout will include test points on every circuit node, on the solder side, to allow connection to a bed-of-nails test fixture. It is envisaged that an ICT fixture will be used to check passive component values, and to exercise active components.

It is possible that a board-level functional test may also be required. For such a test the built in LEDs and piezo speaker can be used to indicate detailed functional test results. This level of information is not appropriate for the final user, so needs a different self test algorithm to be executed. There are several possible approaches, which should be discussed with the manufacturer:

- Assuming the functional tester is a bed of nails fixture, reprogram the Flash device with a special 'factory test' code version
- Download a special 'factory test' software version via the modem
- Add a new command to the Transmitter-Receiver interface to branch to a more complex version of BIST (built –in self test)
- Have the bed of nails tester force one or more test points to 'unusual' voltages, causing code to branch to the 'factory test' option

It is assumed that the small LED board will not need a board-level test.

7.2. Subassemblies / Interconnect

There will be several subassemblies

- Wand
- ECG cables
- Base moulding + main PCB + microphone +volume slider + LEDs
- Inner moulding + speaker
- Top moulding and lid

Low cost crimp connectors will be used for all internal signals and for the wand cable (JST PH series – 2mm crimp connectors). ECG cables use single-pin connectors to achieve a large physical separation between the inputs. Strain relief for wand and ECG cables is provided by labyrinths in the inner cover moulding.

The cable lengths must be short enough so that cables do not 'droop' across the main board within the assembled unit, in order to prevent EMC coupling bypassing the filtering measures taken around the connectors themselves.

Connectors for the microphone, speaker, wand and ECG cables will be accessible with the inner cover moulding fitted. This allows assembly of a functionally complete unit with all internal cable routing correctly dressed before the top cover is fitted.

7.3. Assembly

A typical assembly sequence would be:

- Assemble the main board + microphone +LED board into the base
- Connect the telemetry wand (already molded into its enclosure) to the main board
- Assemble speaker into the inner cover
- Add the inner cover moulding. Position strain reliefs for the wand and ECG cables in the inner cover moulding, connect up LED board and speaker/mic/wand/ECG leads to the main board.
- Dress internal cables into retention features on the inner cover moulding
- Assemble the top cover and lid together
- Add the top cover and lid to the base and inner cover assembly

7.4. Final Functional Test

A short functional test will be required to test the fully assembled unit. This will involve connection to DC power, dummy phone network (probably a small office PBX unit), a dummy device, and dummy ECG signal source.

The unit will then run through a series of test functions, including its built-in self test, and connection to the modem and the dummy device, all using the final user software version.

7.5. Final Safety Test

Hipot and leakage current tests will be required on every unit, after final assembly.

8. Safety Considerations

8.1. Electrical Isolation

Electrical isolation between the ECG leads and the power / phone leads is the primary safety concern. The interface between the ECG island and the main circuit will be designed to withstand 5kV which complies with all known regulatory requirements. Since the barrier around the ECG 'island' has the highest breakdown voltage rating, the mains and modem circuits can be constructed with standard components, giving the levels of protection required by IEC60601-1.

The housing will be constructed so that creepage and clearance distances will not be reduced by the ECG cables coming close to any part of the main SELV circuit. Cables will not droop across the surface of the PCB, and will not come close to the wand, speaker or microphone wiring.

	Withstand voltage (Volts dc)	Creepage distance (mm)	Clearance distance (mm)	Leakage current (uA)
ECG leads – SELV circuit	5000	8	5	10
Modem lead – SELV circuit	1500	4	2.5	-
RS232 lead – SELV circuit	500	4	2.5	-
Mains input – SELV circuit (within the external AC/DC adapter)	4000	8	5	
Mains power pins – mains earth (within the external AC/DC adapter)	1500	4	2.5	100

8.2. Earth Continuity

The main SELV circuit is double insulated (i.e. there is no mains earth connection: the main Transmitter circuit floats with respect to mains earth). In the RS232 product variant, use of an electrically isolated serial interface allows connection to a standard PC (see Section 5.10).

9. Distribution

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