WL865E4-P
HW User Guide

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APPLICABILITY TABLE (REMOVE UNUSED)

PRODUCTS

- WL865E4-P

Contents

1. INTRODUCTION

1.1. Scope

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit WL865E4-P module.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our WL865E4-P modules.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. 2019-01-08.

1.5. Related Documents

WL865E4-P AT Command Reference Guide

WL865E4-P_EVB_User_Guide

WL865_PCB_Antenna_Integration_Guide

2. OVERVIEW

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit WL865E4-P module. In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit WL865E4-P module. For further hardware details that may not be explained in this document refer to the Telit WL865E4-P Product Description document where all the hardware information is reported.

NOTE:

(EN) The integration of the WL865E4-P module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare WL865E4-P all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des WL865E4-P Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija WL865E4-P modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo WL865E4-P debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire WL865E4-P dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי WL865E4 עם המוצר.

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3. PINS ALLOCATION

3.1. Pin-out Table

Pin	Signal	I/O	Function	Type	Comment
USB HS 2.0 COMMUNICATION PORT					
12	VUSB	I	Power Supply for the internal USB transceiver.	POWER	Connect to VDD_BLE
13	USB_D-	AIO	USB differential Data -	AIO	Used only for programming and testing
14	USB_D+	AIO	USB differential Data +	AIO	Used only for programming and testing
High Speed Asynchronous Serial Port (USIF0)					
23	UART0_CTS / GPIO_22	DI	Input	VDD_VIO	Max baud rate 3 Mbps
24	UART0_RTS / GPIO_23	DO	Output	VDD_VIO	Max baud rate 3 Mbps
25	UART0_RXD / GPIO_24	DI	Serial data input	VDD_VIO	Max baud rate 3 Mbps
26	UART0_TXD / GPIO_25	DO	Serial data output	VDD_VIO	Max baud rate 3 Mbps
Low Speed Asynchronous Serial Port (USIF1)					
27	UART1_RXD / GPIO_26	DI	Serial data input	VDD_VIO	Max baud rate 115200 bps
28	UART1_TXD / GPIO_27	DO	Serial data output	VDD_VIO	Max baud rate 115200 bps
Serial Peripheral Interface (SPI)					
53	SPI_M_CS / GPIO_11	DIO	General Purpose Input/Output	VDD_VIO	SPI Chip Select (Master) (Active LOW)
54	SPI_M_CLK / GPIO_12	DIO	General Purpose Input/Output	VDD_VIO	SPI Clock (Master)

Serial Peripheral Interface (SPI) (cont…)					
55	SPI_M_MISO / GPIO_14	DIO	General Purpose Input/Output	VDD_VIO	SPI MISO (Master)
56	SPI_M_MOSI / GPIO_13	DIO	General Purpose Input/Output	VDD_VIO	SPI MOSI (Master)
Secure Digital Input Output (SDIO)					
46	SDIO_CLK / SPI_S_CLK GPIO_32	DIO	SDIO card CLK signal	VDD_VIO	SPI_S_CLK Slave (PWM)
47	SDIO_CMD / SPI_S_CS GPIO_33	DIO	SDIO card Command signal	VDD_VIO	SPI_S_CS (Active LOW) Slave (PWM)
48	SDIO_D3 / SPI_S_MOSI GPIO_34	DIO	SDIO card DAT[3] signal	VDD_VIO	SPI_S_MOSI Slave (PWM)
49	SDIO_D2 / USB_BOOT GPIO_35	DIO	SDIO card DAT[2] signal	VDD_VIO	USB BOOT Mode (Active HIGH) (PWM)
50	SDIO_D1 / GPIO_36	DIO	SDIO card DAT[1] signal	VDD_VIO	(PWM)
51	SDIO_D0 / SPI_S_MISO GPIO_37	DIO	SDIO card DAT[0] signal	VDD_VIO	SPI_S_MISO Slave (PWM)
Inter-Integrated Circuit Interface (I2C)					
21	I2C_SDA / GPIO_06	DIO	Data	VDD_VIO	I2C Data (Master)
22	I2C_SCL / GPIO_07	DIO	Clock	VDD_VIO	I2C Clock (Master)
Analog Interface (ADC)					
3	ADC_IN3 / GPIO_17	DIO	12 BITS 1Mhz	VDD_VIO AI	In ADC mode VDD_VIO must be 1V8 only
4	ADC_IN2 / GPIO_16	DIO	12 BITS 1Mhz	VDD_VIO AI	In ADC mode VDD_VIO must be 1V8 only
5	ADC_IN1 / GPIO_15	DIO	12 BITS 1Mhz	VDD_VIO AI	In ADC mode VDD_VIO must be 1V8 only

Digital Audio Interface (I2S) Master/Slave					
17	I2S_SYNC / GPIO_28	DIO	I2S - Frame Sync or LR Clock	VDD_VIO	
18	I2S_SCK / GPIO_30	DIO	I2S - Bit Clock	VDD_VIO	
19	I2S_SDO / GPIO_31	DIO	I2S - Data Ouput	VDD_VIO	
20	I2S_SDI / GPIO_29	DIO	I2S - Data Input	VDD_VIO	
Miscellaneous Fuctions					
1	RESET#	DIO	Hardware RESET Power Disable	VDD_VIO	Open Drain Active LOW
2	BT_PRIORITY / GPIO_02	DIO	GENERIC IO	VDD_VIO	BT_PRIORITY
15	PWM_OUT0 / GPIO_05	DIO	GENERIC IO	VDD_VIO	DAC (PWM)
16	LF_CLK_IN / GPIO_08	DIO	GENERIC IO	VDD_VIO	Optional External 32KHz Clock Input
33	WIFI_ACTIVE / GPIO_03	DIO	GENERIC IO	VDD_VIO	WIFI_ACTIVE
34	BT_ACTIVE / GPIO_04	DIO	GENERIC IO	VDD_VIO	BT_ACTIVE
43	WAKEUP / GPIO_01	DIO	GENERIC IO	VDD_VIO	WAKEUP
44	WoW / GPIO_09	DIO	GENERIC IO	VDD_VIO	Wake on Wireless LAN (WoW) (OD) (PWM)
45	GPIO_10	DIO	General Purpose Input/Output	VDD_VIO	Programmable: WPS, Whatchdog, SW_Reset
JTAG Pads					
30	JTAG / GPIO_18	DIO	GENERIC IO	VDD_VIO	JTAG
31	JTAG / GPIO_19	DIO	GENERIC IO	VDD_VIO	JTAG
29	JTAG / GPIO_20	DIO	GENERIC IO	VDD_VIO	JTAG
32	JTAG / GPIO_21	DIO	GENERIC IO	VDD_VIO	JTAG

RF Pads					
37	ANT_BLE	AIO	BT 2.4G	RF	50 ohm
40	ANT_WIFI	AIO	WIFI 2.4G and 5G	RF	50 ohm
Power Supply					
6	**VDD_WLAN**	I	WiFi main power supply	Power	(3.0V to 3.6V) 3.3V Nominal Power Supply
9	**VDD_VIO**	I	Digital Input/Output power supply	Power	(1.8V to 3.6V) 3.3V Nominal Power Supply
11	**VDD_BLE**	I	Bluetooth main power supply	Power	(3.0V to 3.6V) 3.3V Nominal Power Supply
7	**GND**	-	Ground	Power	
8	**GND**	-	Ground	Power	
10	**GND**	-	Ground	Power	
35	**GND**	-	Ground	Power	
36	**GND**	-	Ground	Power	
38	**GND**	-	Ground	Power	
39	**GND**	-	Ground	Power	
41	**GND**	-	Ground	Power	
42	**GND**	-	Ground	Power	
52	**GND**	-	Ground	Power	
57	**GND**	-	Ground	Power	

Table 1: WL865E4-P Pinout Table

3.2. Pads Layout

The figure 1 shows the pads layout configuration for the module (top view)

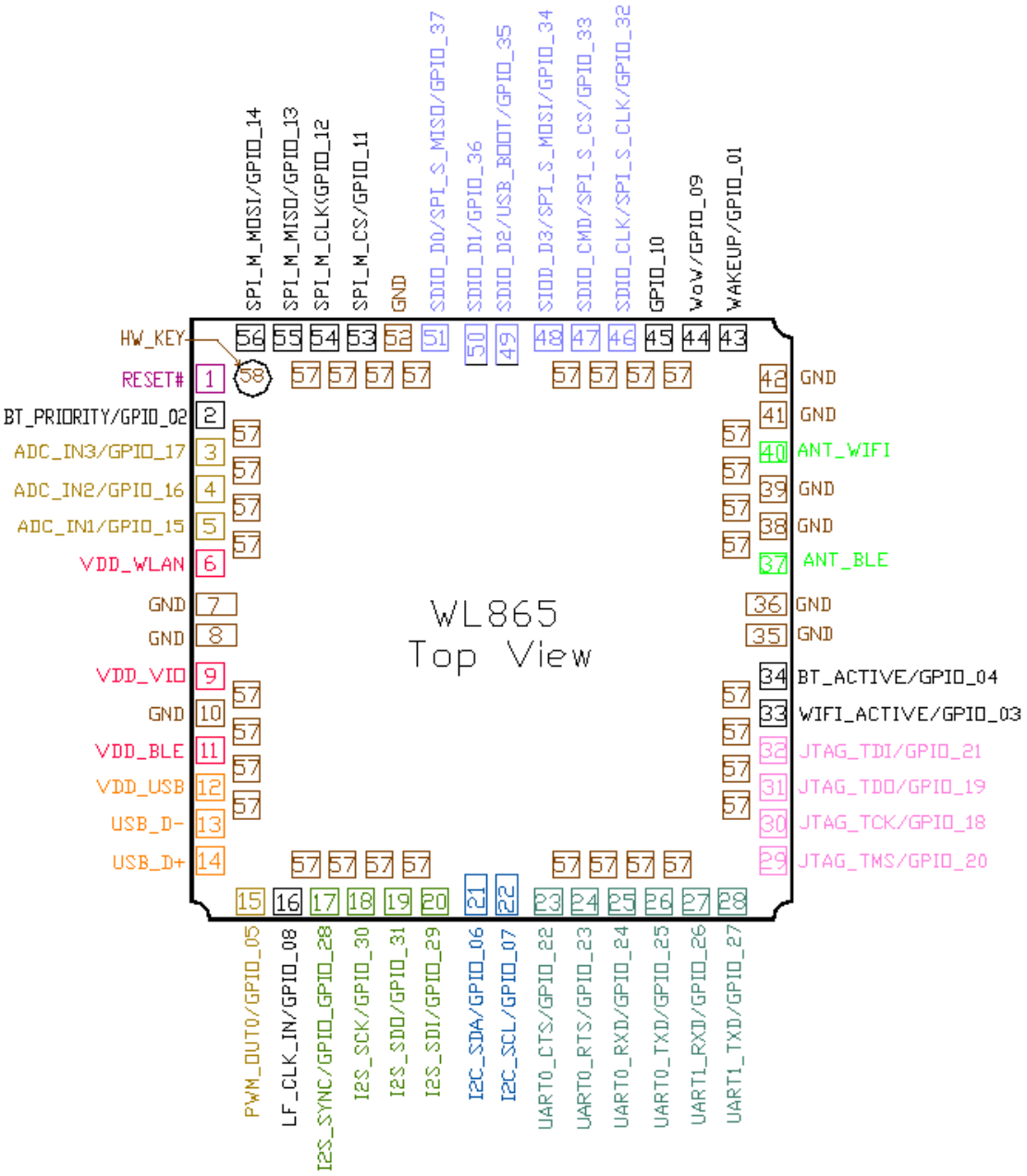

Figure 1: Top View Pad Layout

4. POWER SUPPLY

4.1. Power Supply Requirements

Power Supply	Minimum	Typical	Maximum
Absolute Maximum to avoid permanent damage. At any power supply pin.	-0.3 V		4.0V
Recommended VDD_BLE, VDD_WLAN, USB_VDD	3.14 V	3.3V	3.46V
Recommended VDD_VIO (see notes)	3.14V or 1.71V	3.3V or 1.8V	3.46V or 1.89V

Table 2: Wl865E4-P power supply requirements

Note: The ADC can be used only if VDD_VIO is equal to 1V8.

Power Consumption vs TX power at 2.4 GHz

WIFI 2G4 / CH 6 Standard 802.11x	Modulation	Data rates (Mbps)	RF Output (dBm)	Current @3.3V	Unit
b	BPSK	**1 Mbps**	19	339	mA
b	QPSK	**2 Mbps**	19	342	mA
b	CCK	**5.5 Mbps**	19	327	mA
b	CCK	**11 Mbps**	19	326	mA
g	BPSK	**6 Mbps**	19	332	mA
g	BPSK	**9 Mbps**	19	330	mA
g	QPSK	**12 Mbps**	19	326	mA
g	QPSK	**18 Mbps**	18	294	mA
g	16 QAM	**24 Mbps**	18	286	mA
g	16 QAM	**36 Mbps**	18	276	mA
g	64 QAM	**48 Mbps**	17	266	mA
g	64 QAM	**54 Mbps**	16	230	mA
n	BPSK	**MCS0_20**	19	320	mA
n	QPSK	**MCS1_20**	19	324	mA
n	QPSK	**MCS2_20**	19	309	mA
n	16 QAM	**MCS3_20**	18	285	mA
n	16 QAM	**MCS4_20**	18	277	mA
n	64 QAM	**MCS5_20**	17	252	mA
n	64 QAM	**MCS6_20**	17	232	mA
n	64 QAM	**MCS7_20**	17	224	mA

Table 3: WL865E4-P TX Table consumption @ 2.4 GHz

Power Consumption vs TX power at 5 GHz

WIFI 5G / CH 100 Standard 802.11x	Modulation	Data rates	RF Output (dBm)	Current @3.3V	Unit
a	BPSK	**6 Mbps**	15.5	267	mA
a	BPSK	**9 Mbps**	15.5	265	mA
a	QPSK	**12 Mbps**	15.5	265	mA
a	QPSK	**18 Mbps**	15.5	263	mA
a	16 QAM	**24 Mbps**	15.5	265	mA
a	16 QAM	**36 Mbps**	14	230	mA
a	64 QAM	**48 Mbps**	13	218	mA
a	64 QAM	**54 Mbps**	13	216	mA
n	BPSK	**MCS0_20**	15.5	267	mA
n	QPSK	**MCS1_20**	15.5	263	mA
n	QPSK	**MCS2_20**	15	253	mA
n	16 QAM	**MCS3_20**	15	250	mA
n	16 QAM	**MCS4_20**	14	230	mA
n	64 QAM	**MCS5_20**	14	227	mA
n	64 QAM	**MCS6_20**	13	219	mA
n	64 QAM	**MCS7_20**	13	218	mA

Table 4: WL865E4-P TX Table consumption @5GHz

The equipment must be supplied by an external limited power source in compliance with the clause 2.5 of the standard EN 60950-1.

4.2. General Design Rules

It is recommended to provide at least 10µF capacitors right next to the VDD_WLAN and BT pins, and 2.2µF at each of the other power supply pins like VDD_VIO and VUSB.

5. DIGITAL SECTION

5.1. Logic Levels

Parameter	Min	Max
Input level on any digital pin	-0.3V	VDD_VIO + 0.3V

Levels with VDD_VIO = 3.3V	Min	Max
V_{IH} Input high level	2.4V	3.6V
V_{IL} Input low level	-0.3V	0.3V
V_{OH} Output high level	3.0V	3.6V
V_{OL} Output low level	-0.3V	0.4V

Levels with VDD_VIO = 3.3V	Typical
I_{IH} Input current	60 µA (Rod is ON) 0.1 µA (Rpd is OFF)
I_{IL} Input current	60 µA (Rod is ON) 0.1 µA (Rpd is OFF)
I_{OH} Output current	5 mA (x4 drive strength) 3.3 mA (x2 drive strength) 2.6 mA (x1 drive strength)
I_{OL} Output current	5 mA (x4 drive strength) 3.3 mA (x2 drive strength) 2.6 mA(x1 drive strength)

Table 5: WL865E4-P IO levels

5.2. Power Up/Down Sequence

The RESET# is the main power disable/enable pin, including both the WIFI and BLE. All supplies should be stable for a minimum of 10 µs before RESET# is de-asserted (that is, when greater than VIL for VDD_VIO). If VDD_VIO = 3.3V, then VDD_BLE, VDD_WLAN, and VDD_VIO can share same 3.3V power

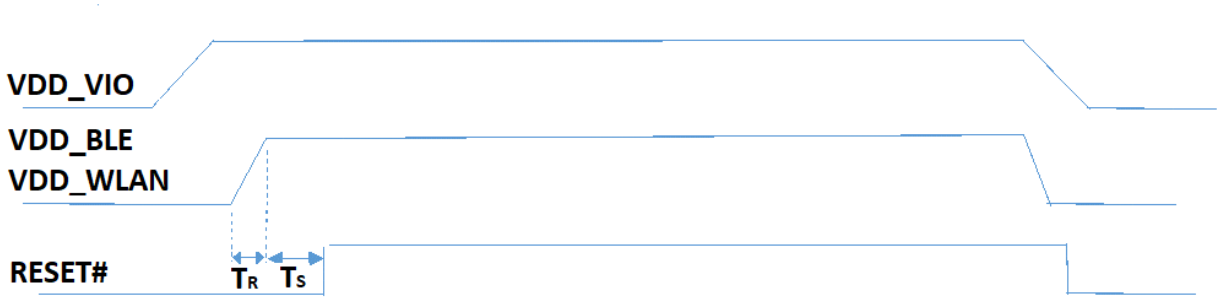

Figure 2: WL865E4-P P on RESET

5.2.1. Power-on reset timing

Parameter	Description	Min	Max	Unit
T_R	Rise time of the power to 90% of final voltage	N/A	25	ms
T_S	Minimum time before RESET# is de-asserted	10	N/A	µs

Table 6: Wl865E4-P on Reset Table

Be sure that VDD_VIO will be powered before or at same time than VDD_BLE and VDD_WLAN.

Either do a VDD_BLE and VDD_WLAN enable circuittry controlled by VDD_VIO or guarantee that all 3 power nets are connected together with bigger bypass capacitances at PAD VDD_BLE and VDD_WLAN.

Do to possible instant peak absorbtion, each of the 3 main Power nets should be dimensioned for a 1A@3V3.

5.3. Unconditional Shutdown

Control the RESET# pin only in Open Drain configuration.

The RESET# is used for unconditional Hardware RESET.

RESET# pin has an internal PU of 120 KOhm resistor.

Make provisioning at RESET# pin of a 10 KOhm PU resistor to VDD_VIO. Initialy do NOT MOUNT.

5.4. Periferals Interface Summary

The module has the following peripherals Interfaces.

Peripherals	Features
QSPI	Internal Serial Flash, 8/64/96MHz
SDIO 2.0Slave	48Mhz clockrate
SPI Master/Slave	48Mhz clock rate,4-wire
USB2.0 Peripherals	FW upgrade, Manufacture interface
I2S Master/Slave	One port –2 audiochannels
PCM	Master/Slave, 8/16-bit,48KHz.
I2CMaster	One I2C interface
UART	One Debug UART upto 115kbps
HighSpeed UART	One HSUART up to 3Mbps
SensorADC	1 ADC, 12-bit, 1M samples/sec, 1.8Vinput. 3-channels single ended or 1 single +1 differential.
PWM	8-channels
Co-existence	PTA3-wire

Table 7: WL865E4-P Periferals Interface Summary

5.5. Communication ports

5.5.1. High Speed UART

High-Speed Universal Asynchronous Receiver/Transmitter (HS-UART) interfaces, which may be configured to serve as either a host interface link or a debug message console.

Property	WL865E4-P Configuration
Baud rate	115200 bps by default, no auto-baud rate detection, it can be changed by the host to up to 3 Mbps by using a special command
Data bits	8 bits
Flow control	CTS/RTS
Parity	None
Stop bits	1
Bit order	LSBit first

Table 8: WL865E4-P Configurations

5.5.2. Low Speed UART

Low-Speed Universal Asynchronous Receiver/Transmitter (UART) interface, which is configured to serve as a debug port

Property	WL865E4-P Configuration
Baud rate	Up to 115200 bps, no auto-baud rate detection, debug port
Data bits	8 bits
Flow control	None
Parity	None
Stop bits	1
Bit order	LSBit first

Table 9: WL865E4-P Configurations

5.5.3. SDIO

One SDIO Slave interface:

- Compliant to SDIO v2.0 specification
- Interface clock frequency up to 48 MHz
- Data transfer modes: 4-bit SDIO, 1-bit SDIO, SPI

5.5.4. SPI

Two general-purpose SPI interfaces. One configured as master only and a second one can be configured as master or slave where pin-mux with SDIO interface pins.

- Interface clock frequency up to 48 MHz

5.5.5. I2C

The I2C Master/Salve interface has weak internal pull-up. If necessary add external ones of 10K down to 1K.

5.5.6. USB

USB 2.0 device interface provides a simplified, high-speed, and scalable manufacturing test and configuration interface for QCA4020-based systems.
It is not used for normal operation, use it only for testing and Bootloader interface.
VUSB is only 3V3 volts. You can directly connect it to VDD_BLE. The USB plug/unplug detection is done through the data pins.

5.6. General purpose I/O

The module has 37 GPIO which can be configured as Input, Output or as Alternate Function.

The default Function, GPIO or Alternate, direction and Internal PU/PD at startup are described here.

GPIO	Alternate Function	Direction	Internal PU/PD
GPIO_01	WAKEUP	Input	PD
GPIO_02	BT_PRIORITY 3 wire PTA, INPUT when slave, OUTPUT when master	Input/Output	
GPIO_03	WIFI_ACTIVE 3 wire PTA, INPUT when slave, OUTPUT when master	Input/Output	
GPIO_04	BT_ACTIVE 3 wire PTA, INPUT when slave, OUTPUT when master	Input/Output	
GPIO_05	PWM_OUT0 (Digital to Analog Converter, DAC)(PWM)	Output	
GPIO_06	I2C_SDA	Input/Output	PU

GPIO	Alternate Function	Direction	Internal PU/PD
GPIO_07	I2C_SCL	Output	PU
GPIO_08	LF_CLK_IN from an external 32KHz for Low Power Accurancy	Input	
GPIO_09	WoW (Wakeup On Wireless) (PWM)	Input	
GPIO_10	SW_RESET, WHATCH DOG, etc	Input/Output	
GPIO_11	SPI_MASTER_CS	Output	PU
GPIO_12	SPI_MASTER_CLK	Output	PD
GPIO_13	SPI_MASTER_MISO	Input	PU
GPIO_14	SPI_MASTER_MOSI	Output	PU
GPIO_15	ADC_IN1 (Analog to Digital Converter) (VDD_VIO=1V8)	Input	
GPIO_16	ADC_IN2 (Analog to Digital Converter) (VDD_VIO=1V8)	Input	
GPIO_17	ADC_IN3 (Analog to Digital Converter) (VDD_VIO=1V8)	Input	
GPIO_18	JTAG_TCK	Output	PU
GPIO_19	JTAG_TDO	Output	
GPIO_20	JTAG_TMS	Output	PU
GPIO_21	JTAG_TDI	Input	PU
GPIO_22	UART0_CTS	Input	
GPIO_23	UART0_RTS	Output	
GPIO_24	UART0_RXD	Input	
GPIO_25	UART0_TXD	Output	
GPIO_26	UART1_RXD	Input	PU
GPIO_27	UART1_TXD	Output	PD
GPIO_28	I2S_SYNC	Input/Output	

GPIO_29	I2S_SDI	Input	
GPIO_30	I2S_SCK	Input/Output	
GPIO_31	I2S_SDO	Output	
GPIO_32	SDIO_CLK (PWM)	Input	PD
GPIO_33	SDIO_CMD (PWM)	Input	
GPIO_34	SDIO_D3 (PWM)	Input/Output	PD
GPIO_35	SDIO_D2 (PWM)	Input/Output	PD
GPIO_36	SDIO_D1 (PWM)	Input/Output	PD
GPIO_37	SDIO_D0 (PWM)	Input/Output	PD

Table 10: WL865E4-P GPIO Alternate Function

5.7. ADC Converter

- 12-bit ADC up to 1Msps
- Alternatively 1 differential input, -1.75V to +1.75V, common mode 0.875V.

5.8. General Digital Interface Recommendations

If components interfacing Telit component's digital signals have levels higher than modem's I/O interface voltage, then a voltage translator must be used.

Using voltage translator component in your design makes the system ready for working at full VDD_VIO voltage range, 1.8V to 3V3.
The use of resistor divider and/or emitter follower, as voltage translators, even if not totally wrong, does not protect the modem against latch-up in case of power-off and furthermore you cannot guarantee a constant voltage on the divider net.

The use of comparators as voltage shifter in principle are correct but they are less immune to RF and dependent on a constant VBATT value without ripple.

The use of open collector buffers or bidirectional voltage level translators with unidirectional signals is in principle correct but they are less immune to RF and dependent on Pull-Up/Down that could be present at any side of the voltage translator; some have different power range for both Vcca and Vccb, in some cases you must guarantee Vcca < Vccb, and their OE should be powered only from Vcca signal. We prefer unidirectional level shifters; if you anyway decide for bidirectional buffers, then those designed for PU/PD like TXS, NXS, FXLA and NVT200x are preferable, they work better if strong PU/PD are internally present like in some of our modems.

We strongly suggest using a dual supply buffer component for unidirectional signals like UART. Example of this are SN74AVC2T245, SN74AVC4T774 or SN74LVC2T45, for 5V signals. They are more immune to RF and are independent on Pull-Up or Pull-Down that could be present at any side of the voltage translator. Place 33pF on both power supplies. The Power bank side connected to the modem should be powered with same VDD_VIO to prevent latch-up from happening.

When using level shifters, for better testability, prefer the use of those having OE pins. Test pointing the “EN” lines of the level shifts, along with the addition of the 10K resistor to GND or VCC, depending on level shifter used. This will create access points that put shifts in tristate and can be conveniently used for testing and firmware updates originating from external serial ports such as PC if needed.

6. RF SECTION

6.1. Bands Variants

6.1.1. WIFI

Supported Frequency Bands

Technology	Frequency Range (GHz)	Channel spacing (MHz)
WIFI 2.4 GHz	2.401 ≤ Fc ≤ 2.495	5
WIFI 5 GHz	5.170 ≤ Fc ≤ 5.835	5

Table 11: WL865E4-P supported Frequency Bands for WiFi

6.1.2. BlueTooth

Technology	Frequency Range (GHz)	Channel Number (k)
BLE 5	2.402 ≤ Fc ≤ 2.480	Fc=2402 + k × 2 MHz, where k = 0, ..., 39.

Table 32: WL865E4-P supported Frequency Bands for BLE

6.2. TX Output power

6.2.1. WIFI

6.2.1.1. 2.4GHz

WIFI 2G4 Transmit power with IEEE 802.11 EVM and spectral mask compliance at RF output Pad at 25 °C

WIFI 2G4 / CH 6 Standard 802.11x	Modulation	Data rates	RF Output (dBm)	EVM (dB)	IEEE EVM (dB)
b	BPSK	**1 Mbps**	19	-30,4	-14
b	QPSK	**2 Mbps**	19	-25,6	-14
b	CCK	**5.5 Mbps**	19	-27,5	-14
b	CCK	**11 Mbps**	19	-26,5	-14
g	BPSK	**6 Mbps**	19	-17.0	-5
g	BPSK	**9 Mbps**	19	-16,9	-8
g	QPSK	**12 Mbps**	19	-16,5	-10
g	QPSK	**18 Mbps**	18	-17,4	-13
g	16 QAM	**24 Mbps**	18	-22,6	-16
g	16 QAM	**36 Mbps**	18	-21,9	-19
g	64 QAM	**48 Mbps**	17	-23,8	-22
g	64 QAM	**54 Mbps**	16	-27,7	-25
n	BPSK	**MCS0_20**	19	-16,5	-5
n	QPSK	**MCS1_20**	19	-15,6	-10
n	QPSK	**MCS2_20**	19	-16.0	-13
n	16 QAM	**MCS3_20**	18	-21,4	-16
n	16 QAM	**MCS4_20**	18	-21,5	-19
n	64 QAM	**MCS5_20**	17	-23,8	-22
n	64 QAM	**MCS6_20**	17	-27.0	-25
n	64 QAM	**MCS7_20**	17	-28,6	-27

Table 43: WL865E4-P IEEE 802.11 EVM @2.4GHz

6.2.1.2. 5GHz

WIFI 5G Transmit power with IEEE 802.11 EVM and spectral mask compliance at RF output Pad at 25 °C

WIFI 5G / CH 100 Standard 802.11x	Modulation	Data rates	RF Output (dBm)	EVM (dB)	IEEE limit (dB)
a	BPSK	**6 Mbps**	15.5	-18.4	-5
a	BPSK	**9 Mbps**	15.5	-18.5	-8
a	QPSK	**12 Mbps**	15.5	-17.9	-10
a	QPSK	**18 Mbps**	15.5	-18.0	-13
a	16 QAM	**24 Mbps**	15.5	-22.8	-16
a	16 QAM	**36 Mbps**	14	-29.8	-19
a	64 QAM	**48 Mbps**	13	-31.7	-22
a	64 QAM	**54 Mbps**	13	-31.8	-25
n	BPSK	**MCS0_20**	16	-17.5	-5
n	QPSK	**MCS1_20**	16	-17.0	-10
n	QPSK	**MCS2_20**	15	-17.6	-13
n	16 QAM	**MCS3_20**	15	-25.2	-16
n	16 QAM	**MCS4_20**	14	-28.7	-19
n	64 QAM	**MCS5_20**	14	-28.6	-22
n	64 QAM	**MCS6_20**	13	-30.3	-25
n	64 QAM	**MCS7_20**	13	-30.5	-27

Table 54: WL865E4-P IEEE 802.11 EVM @5GHz

6.2.2. BlueTooth

BLE Transmit power with at RF output Pad at 25 °C

Packet Type	Channel Number	Output Power (dBm)
LE 1M	1	2.1
LE 2M	1	2.1

Table 65: WL865E4-P BLE transmit power

6.3. RX Sensitivity

6.3.1. WIFI

6.3.1.1. 2.4GHz

WIFI 2G4 RX Sensibility Tested at RF output Pad at 25 °C

WIFI 2G4 / CH 6 Standard 802.11x	Modulation	Data rates	Sensibilty (dBm)	IEEE limit (dB)
b	BPSK	**1 Mbps**	-96.5	-80
b	QPSK	**2 Mbps**	-94.1	-80
b	CCK	**5.5 Mbps**	-93.7	-76
b	CCK	**11 Mbps**	-90.0	-76
g	BPSK	**6 Mbps**	-94.4	-82
g	BPSK	**9 Mbps**	-93.0	-81
g	QPSK	**12 Mbps**	-92.1	-79
g	QPSK	**18 Mbps**	-89.2	-77
g	16 QAM	**24 Mbps**	-86.3	-74
g	16 QAM	**36 Mbps**	-82.8	-70
g	64 QAM	**48 Mbps**	-78.8	-66
g	64 QAM	**54 Mbps**	-77.2	-65
n	BPSK	**MCS0_20**	-94.3	-82
n	QPSK	**MCS1_20**	-91.4	-79
n	QPSK	**MCS2_20**	-89.0	-77
n	16 QAM	**MCS3_20**	-85.0	-74
n	16 QAM	**MCS4_20**	-81.5	-70
n	64 QAM	**MCS5_20**	-77.2	-66
n	64 QAM	**MCS6_20**	-75.4	-65
n	64 QAM	**MCS7_20**	-73.8	-64

Table 76: WL865E4-P Sensitivity @2.4GHz

6.3.1.2. 5GHz

WIFI 5G RX Sensibility Tested at RF output Pad at 25 °C

WIFI 5G / CH 100 Standard 802.11x	Modulation	Data rates	Sensibilty (dBm)	IEEE limit (dBm)
a	BPSK	**6 Mbps**	-95.4	-82
a	BPSK	**9 Mbps**	-94.1	-81
a	QPSK	**12 Mbps**	-93.0	-79
a	QPSK	**18 Mbps**	-90.6	-77
a	16 QAM	**24 Mbps**	-87.1	-74
a	16 QAM	**36 Mbps**	-84.0	-70
a	64 QAM	**48 Mbps**	-80.0	-66
a	64 QAM	**54 Mbps**	-78.2	-65
n	BPSK	**MCS0_20**	-95.2	-82
n	QPSK	**MCS1_20**	-92.5	-79
n	QPSK	**MCS2_20**	-90.2	-77
n	16 QAM	**MCS3_20**	-85.6	-74
n	16 QAM	**MCS4_20**	-82.5	-70
n	64 QAM	**MCS5_20**	-78.2	-66
n	64 QAM	**MCS6_20**	-76.6	-65
n	64 QAM	**MCS7_20**	-75.1	-64

Table 87: WL865E4-P Sensitivity @5GHz

6.3.2. BlueTooth

RX Sensisbilty Tested at RF output Pad at 25 °C

Packet Type	Channel Number	RX sensibility (dBm)
LE 1M	1	-97.1
LE 2M	1	-94.3

Table 98: WL865E4-P Sensitivity at RF Output

6.4. WIFI Antenna requirements

Special care must be taken during the design of the RF section on the application board.

RF performance degradation, and infringements of emission limits, may arise if the following recommendations are not respected.

A 50Ω antenna is required. Telit's WL865E4-P interface features an SMA connector for an external antenna, but other antenna integrated choices are possible, such as a chip or a printed one. In case an integrated antenna is used, it is recommended to place it at the edge of the application board.

Since it may be necessary to tune the antenna impedance to 50Ω, it is recommended to foresee a PI matching network between the WL865E4-P and the antenna, at least during first prototyping: if not required, a series 0Ω-resistor can be used, leaving the two shunt components unpopulated.

In order to be able to reuse Telit's FCC certification for our module, the antenna on the application board shall have a gain equal or lower to the one recommended by Telit, the separation distance between the user and/or bystander and the device's radiating element is greater than 20cm and no other radiating element is present inside the application closer than 20cm to our antennas. A separate test for any other radiating element could be necessary.

As external antenna we recommend the T-AT9552 from Antel.
It is a WIRELESS LAN DUALBAND 2.4-5.8GHz with SMA M.
It has a Gain of 2.5 dBi at 2400 ÷ 2500MHz and 4.5 dBi at 4900 ÷ 5925MHz.

6.5. BlueTooth Antenna requirements

Please follow the same raccomandation given for the WiFi antenna.

6.6. PCB Antenna Design Guidelines

Refer to "*WL865_PCB_Antenna_Integration_Guide*"

6.7. PCB Design Guidelines

6.7.1. PCB General Guidelines

The Ground of the PCB or Chip RF antenna is part of antenna when using a monopole, especially the part that lies in front of the monopole. Leave a wide ground area, without components and tracks, in front of antenna on all layers. In the inner layers, the width could be less. 5mm is an optimum value but not always reachable.

If antenna is placed directly on onboard connector, it is important to consider leaving a wide ground area for it.

The position of the external antenna with respect to other boards is of maximum importance, since conductive planes close to antenna modify the impedance seen by the antenna and any board of the system must be RF proof, not only the modem board.

Move components, tracks, vias and connectors away from antenna area to reduce their coupling with RF signal; you can also bury tracks in the inner layers of a multi-layer PCB.

Since components and PCBs are getting smaller while component's density increases,another problem that becomes important is the heat dissipation. For that reason, we must pay special attention to PCB layup and component placement. We strongly suggest following these PCB design rule to help not only RF immunity but improving heat dissipation.

- We suggest to use at least a 6 layers PCB technology.
- Layer2 and Layer4 mainly ground.
- On top Layer1 and bottom Layer6 place mainly ground plane interrupted just by component pads and RF antenna tracks doing minimum necessary tracks to arrive to drills connecting to Layer3 and Layer5. This is to avoid ground interruption and consequently its heat dissipation.
- Use Layer3 and Layer5 only for signals, where power lines are wider tracks surrounded of ground not to have crosstalk with other signals.
- One layer for horizontal lines only and the other one for vertical lines. Fill remaining empty space with ground.
- Use many vias to connect all ground planes and areas in all layers with possible through hole drills.
- Place warmer components, like modem, on PCB side facing up and do not place anything on top of them, leaving space to the air.
- If it is a closed application, consider opening holes on top and bottom of the cover for ventilation or use the modem for short time.

The design can be done in 4 layers only if the number of interconnection gives you the possibility to route them on layer2 and layer3 in a way that power lines and signals lines do not intersect and the modem do not work continuously so the heat dissipation is not a must. All the rest suggestion described above must be fulfilling. The audio, USB and ADC lines must be route avoiding intersection with any other track.

Top and Bottom layers should be mainly a ground plane interrupted just by component's pads, vias and RF tracks. Connect all ground areas avoiding isolated island with several vias. In this way, the signal tracks are more protected from picking up RF due to the Faraday-Cage effect. Long exposed tracks can easily pick-up RF power and especially in your case with many RF power sources you can generate high frequency intermodulation harmonics that the same exposed tracks can then irradiate very efficiently.

All the PCB borders should be ground in ALL layers and fill all the free space in internal planes with ground. All the ground, either planes or areas, must be well interconnected, with a fence of GND vias one each 2mm, to guarantee a strong equipotential node. Avoid unconnected copper islands and signal or vias on PCB border.

Power tracks should face only ground tracks or planes. Power lines should not run externally and/or side by side with other signal lines, place ground in between. Power lines should not have signal lines running or crossing under them, place ground plane area under and above all its path.

The Bypass capacitors must be placed close to the Telit modem's power input pads or at least on the same path. In case of switching power supply another Bypass low ESR capacitor must be placed close to the inductor output to reduce the ripple.

Some protection diode must be placed close to the input connector where the power source is drained.
It is not advisable to route analog or digital audio lines, memory address and data bus, fast digital signals, clocks, quartz, serial and long signal tracks on an outer layer. It'll be better to bury it on an inner layer with a ground plane under and above it to shield the signal from RF and crosstalk, see figure below.

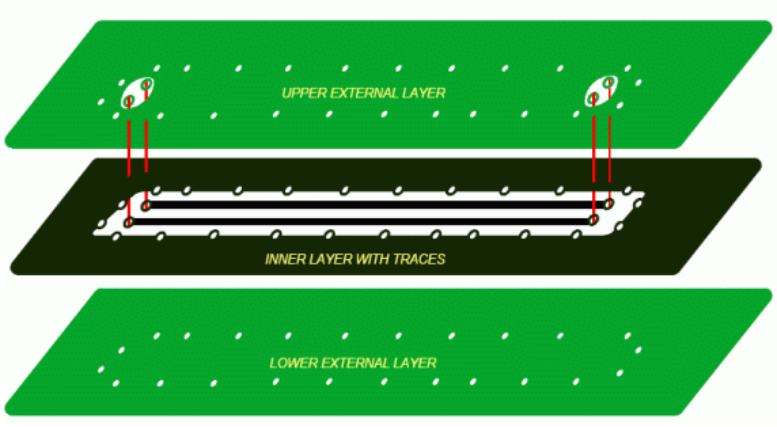

Figure 3: Example of buried lines

6.7.2. RF PCB Guidelines

The WL865E4-P module provides a 50Ω antenna pad, which has to be routed to the antenna connector (or the integrated antenna) by means of a transmission line.

Keep as close ad possible to 50 Ω impedance in the RF track including the RF Pad. It is important to make RF trace equal or wider than the Pad width to avoid step impedance.

The line should be as short as possible, and keep a constant cross section, avoiding stubs, sharp bends and meanders. Eliminate the right angle on your antenna waveguide design. It shall be isolated from any other noise source: in particular, trace shall not be crossed by other lines in adjacent layers. Instead, a continuous ground plane is recommended under the antenna trace, and a ground via curtain should connect it to the coplanar ground planes.

The size depends by the stackup and by the structure that you're going to realize.

As an example of a possible implementation, the details of the antenna trace on the WL865 interface board are described in this section.

A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.

The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity εr = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.

An example of a waveguide having the same width as the RF Pad are shown in figures below.

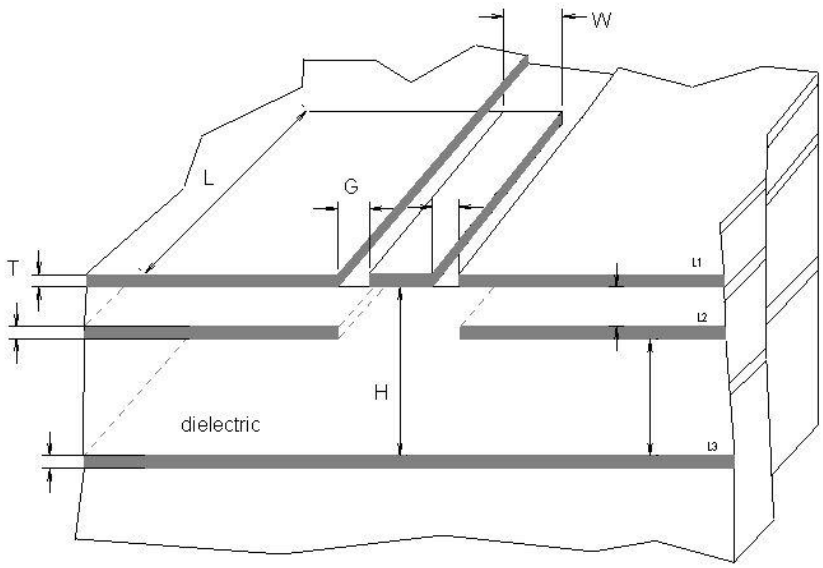

Figure 4: Coplanar Waveguide dimensioning example

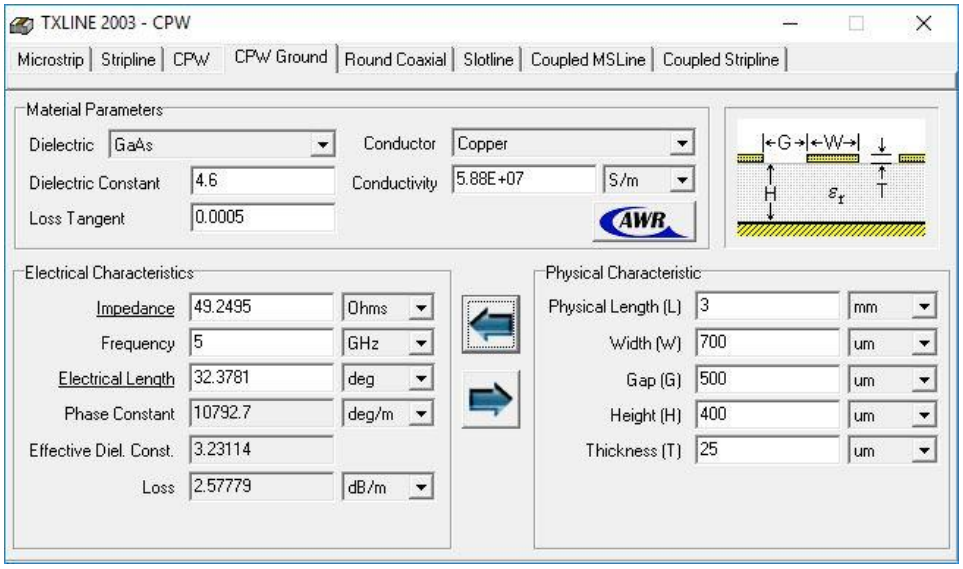

Figure 5: Coplanar Waveguide calculation tool example

Please pay attention to cut the GND plane close to the Antenna pad, otherwise you can change drastically the impedance value.

To give you an idea below we are showing the RF track used in our EVB.

Please consider to keep an appropriate clear area from RF PAD to GND in you board.

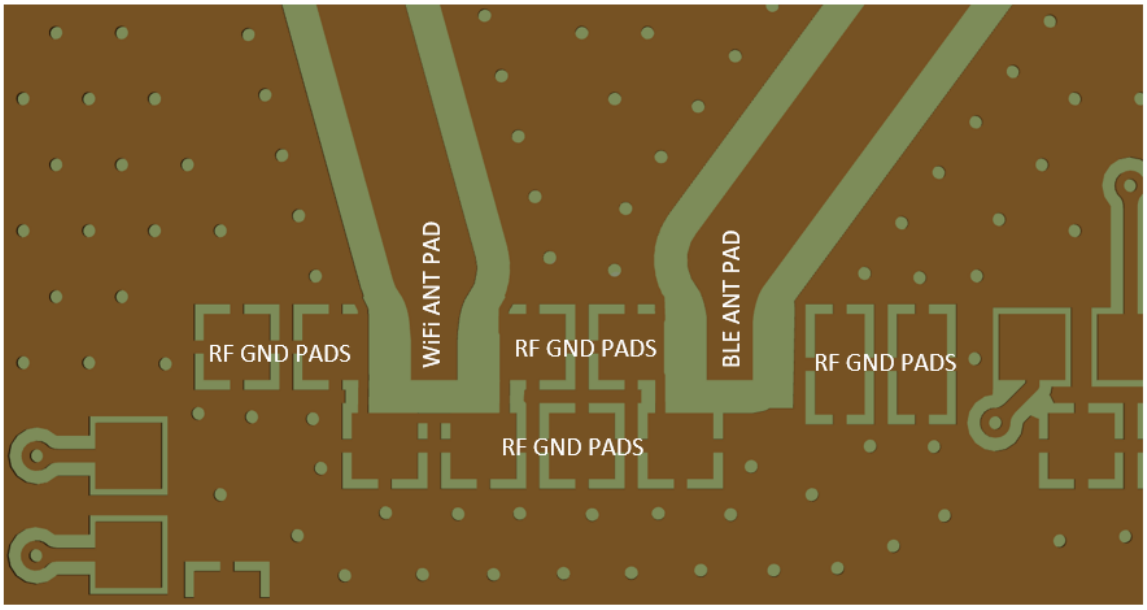

Figure 6: RF Track on EVB

7. AUDIO SECTION

7.1. Electrical Characteristics

The audio interface is only digital, through the I2S.

The voltage of this interface pins have same electrical characteristics as for digital pins and are related to the power bank VDD_VIO.

8. MECHANICAL DESIGN

8.1. Drawing

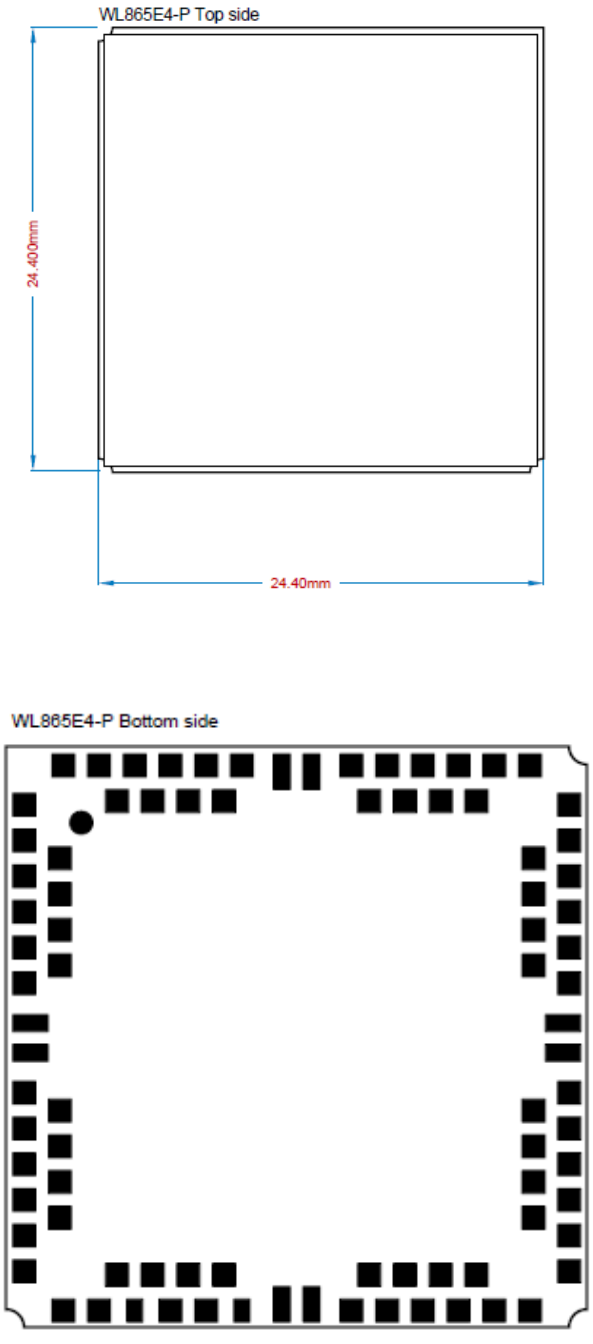

Figure 7: WL865E4-P Top and bottom side mechanical Drawing

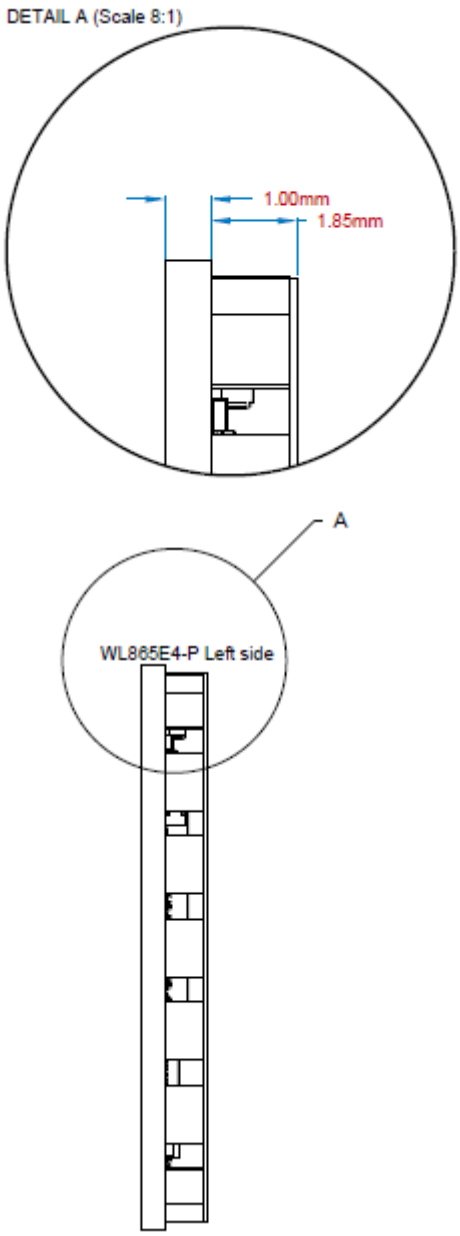

Figure 8: WL865E4-P side view

9. APPLICATION PCB DESIGN

9.1. Footprint

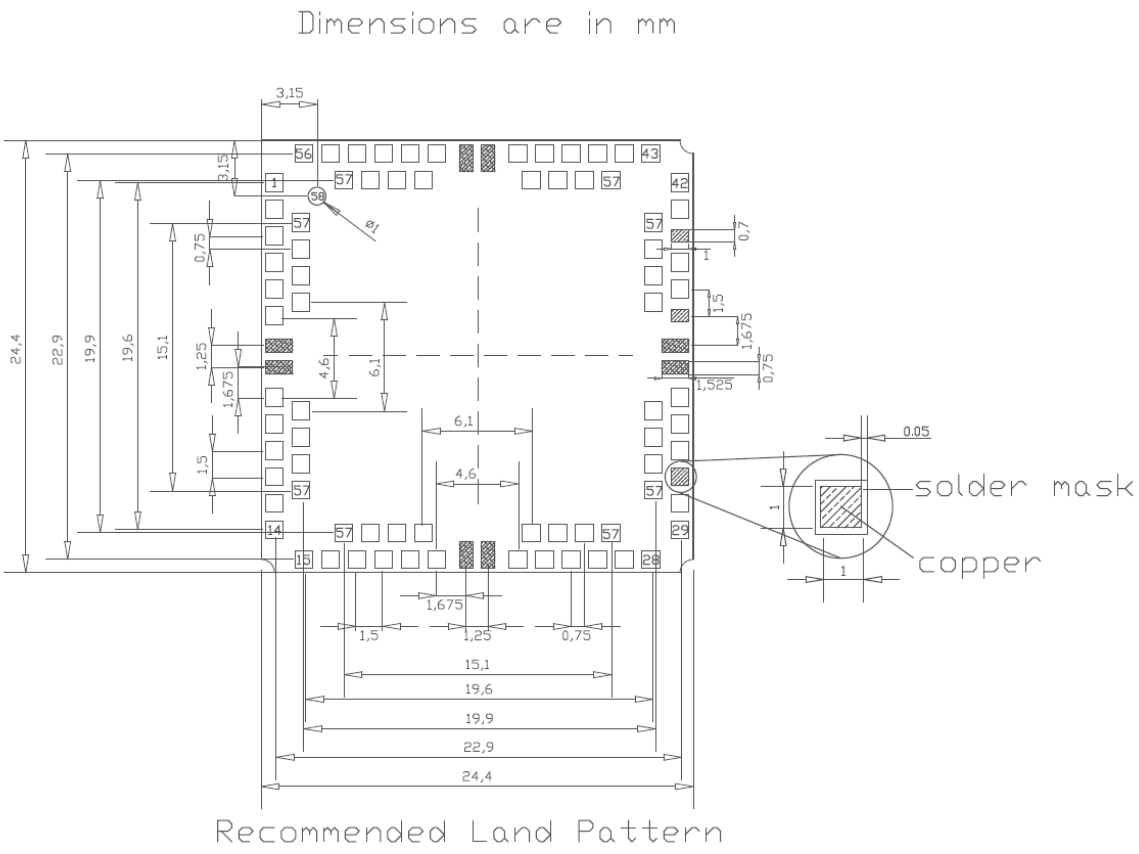

Figure 9: WL865E4-P recommended footprint

9.2. PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.

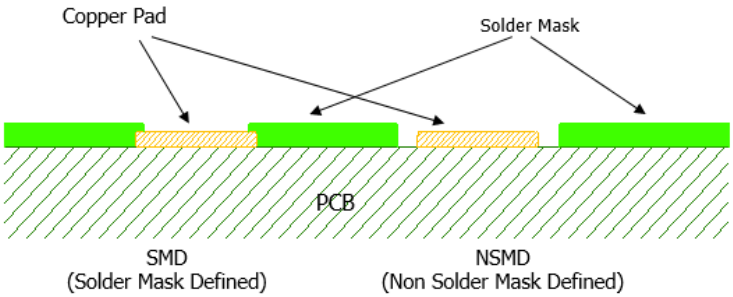

Figure 10: SMD and NSMD PAD

9.3. PCB pad dimensions

It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself (see following figure).

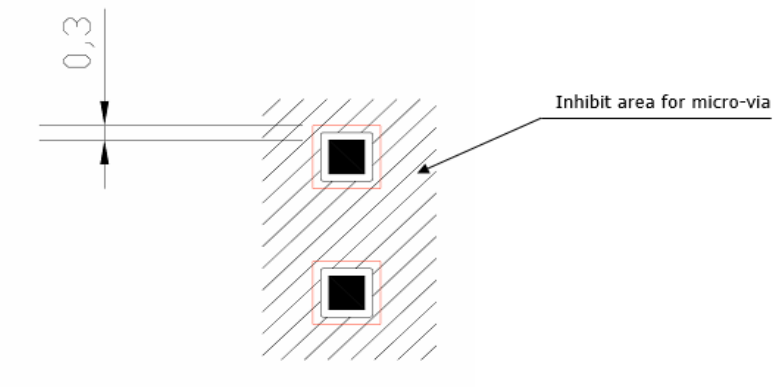

Figure 5: inhibit area for not solder covered vias

Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Finish	Layer thickness [µm]	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.03 – 0.15	Good solderability protection, high shear force values

Table 1910: PSB Finishing recommendation

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

It is not necessary to panel the application PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

9.4. Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120 µm.

9.5. Solder paste

	Lead free
Solder paste	Sn/Ag/Cu

Table 110:Recommended Solder Paste Type

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

9.6. Solder Reflow

Recommended solder reflow profile

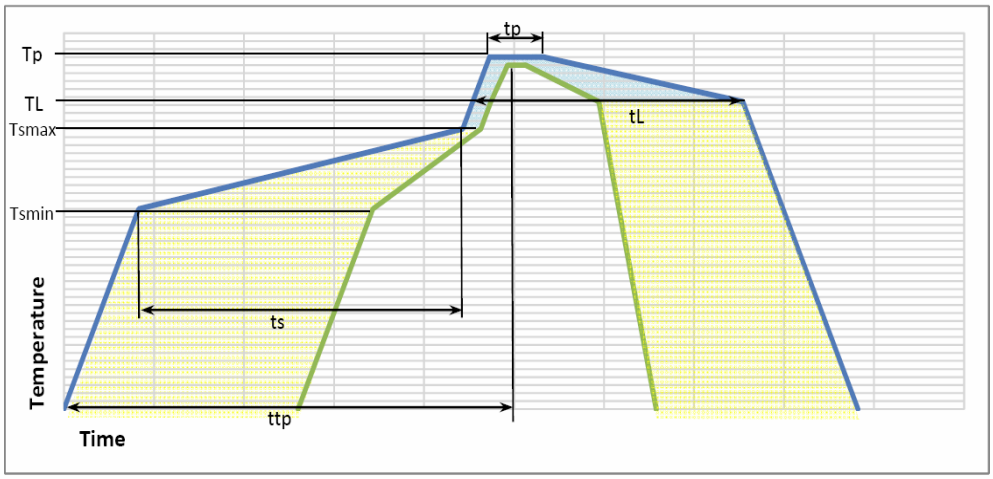

Figure 12: Solder Reflow profile

Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	3°C/second max
Preheat **– Temperature Min (Tsmin)** **– Temperature Max (Tsmax)** **– Time (min to max) (ts)**	 150°C 200°C 60-180 seconds
Tsmax to TL **– Ramp-up Rate**	 3°C/second max
Time maintained above: **– Temperature (TL)** **– Time (tL)**	 217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Table 21: Solder Reflow Table

All temperatures refer to topside of the package, measured on the package body surface.

WL865E4-P module withstands one reflow process only.

Warning: The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customer must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage.

10. PACKAGING

10.1. Tray

The WL865E4-P modules are packaged on trays of 50 pieces each when small quantities are required (i.e. for test and evaluation purposes). Trays are not designed to be used in SMT processes for pick and place handling.

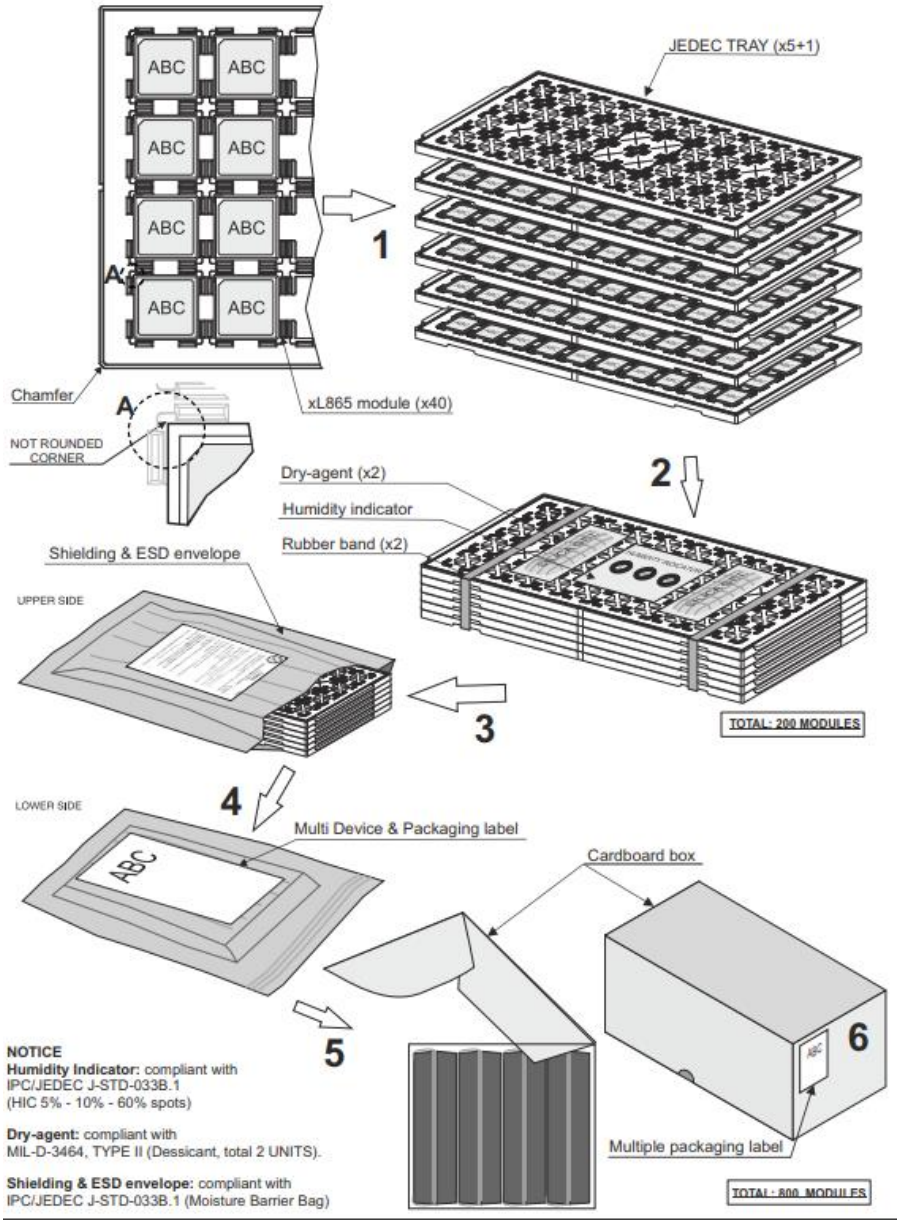

Figure 63: WL865E4-P Packaging

Caution or Warning –These trays can withstand at the maximum temperature of 65°C.

10.2. Moisture sensitivity

The moisture sensitivity level of the Product is “3” according with standard IPC/JEDEC J-STD-020, take care of all the relative requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) The shelf life of the Product inside of the dry bag is 12 months from the bag seal date, when stored in a non-condensing atmospheric environment of < 40°C and < 90% RH.

b) Environmental condition during the production: <= 30°C / 60% RH according to IPC/JEDEC J-STD-033B.

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033B paragraph 5.2” is respected.

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

11. CONFORMITY ASSESSMENT ISSUES

11.1. FCC/IC Regulatory notices

Hereby, Telit Communications S.p.A declares that the NB IOT Module is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following internet address: http://www.telit.com\red

12. FCC/IC COMPLIANCE

Modification statement

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Telit n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference statement

This device complies with Part 15 of the FCC Rules and Industry Canada licence-exempt

RSS standard(s). Operation is subject to the following two conditions:

(1) this device may not cause interference, and

(2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils

radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le

brouillage est susceptible d'en compromettre le fonctionnement.

Wireless notice

This device complies with FCC/ISED radiation exposure limits set forth for an uncontrolled environment and meets the FCC radio frequency (RF) Exposure Guidelines and RSS-102 of the ISED radio frequency (RF) Exposure rules. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. The antenna should be installed and operated with minimum distance of 20 cm between the radiator and your body.

Le présent appareil est conforme à l'exposition aux radiations FCC / ISED définies pour un environnement non contrôlé et répond aux directives d'exposition de la fréquence de la FCC radiofréquence (RF) et RSS-102 de la fréquence radio (RF) ISED règles d'exposition. L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur. L'antenne doit être installée de façon à garder une distance minimale de 20 centimètres entre la source de rayonnements et votre corps.

FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to

radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

CAN ICES-3 (B) / NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

List of applicable FCC rules

Parts 15C, 15E, 2.1091

Limited module procedures

N/A

Trace antenna designs

See 6.4 Antenna design

Antennas

This radio transmitter has been approved by FCC and ISED to operate with the antenna types listed below with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Type	Max Gain
Omnidirectional	4.5 dBi

Le présent émetteur radio a été approuvé par ISDE pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Type	Gain maximal
Omnidirectional	4.5 dBi

Label and compliance information

The product has a FCC ID label on the device itself. Also, the OEM host end product manufacturer will be informed to display a label referring to the enclosed module. The exterior label will read as follows: “Contains Transmitter Module FCC ID: RI7WL865E4” or “Contains FCC ID: RI7WL865E4”.

Information on test modes and additional testing requirements

The module has been evaluated in mobile stand-alone conditions. For different operational conditions from a stand-alone modular transmitter in a host (multiple, simultaneously transmitting modules or other transmitters in a host), additional testing may be required (collocation, retesting…).

If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements of FCC Part 2.1093 and IC RSS-102.

Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed. The end product with an embedded module may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15.

13. SAFETY RECOMMENDATIONS

13.1. READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipment is available,

while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/

14. ACRONYMS

TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
UART	Universal Asynchronous Receiver Transmitter
HSIC	High Speed Inter Chip
BLE	Bluetooth low energy
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output
GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
MOSI	Master Output – Slave Input
MISO	Master Input – Slave Output
CLK	Clock
MRDY	Master Ready

SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio
VNA	Vector Network Analyzer

15. DOCUMENT HISTORY

Revision	Date	Changes
0	2017-12-15	First issue
1	2019-03-29	General Review of all chapters
2	2019-05-01	Minor changes
3	2019-07-02	Updated GPIO and RF tables
4	2019-08-08	Added FCC/IC COMPLIANCE

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

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