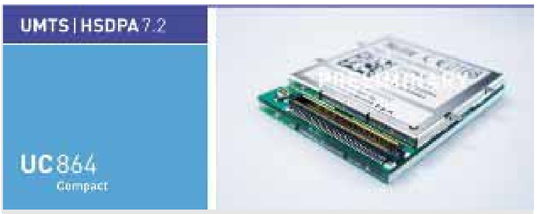
UC864-G Hardware User Guide

DRAFT - 29/10/07

Making machines talk.

This document is relating to the following products:



UC864-G

Contents

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1 Overview

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit UC864-G module.
In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit UC864-G module. For further hardware details that may not be explained in this document refer to the Telit UC864-G Product Description document where all the hardware information is reported.

NOTICE

(EN) The integration of the GSM/GPRS/EGPRS/WCDMA/HSDPA UC864G cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare GSM/GPRS/EGPRS/WCDMA/HSDPA UC864-G all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die integration des UC864-G GSM/GPRS/EGPRS/WCDMA/HSDPA Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen

(SL) Integracija GSM/GPRS/EGPRS/WCDMA/HSDPA UC864-G modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem piročniku.

(SP) La utilización del modulo GSM/GPRS/EGPRS/WCDMA/HSDPA UC864-G debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire GSM/GPRS/EGPRS/WCDMA/HSDPA UC864-G dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי *UC864-G* עם המוצר.

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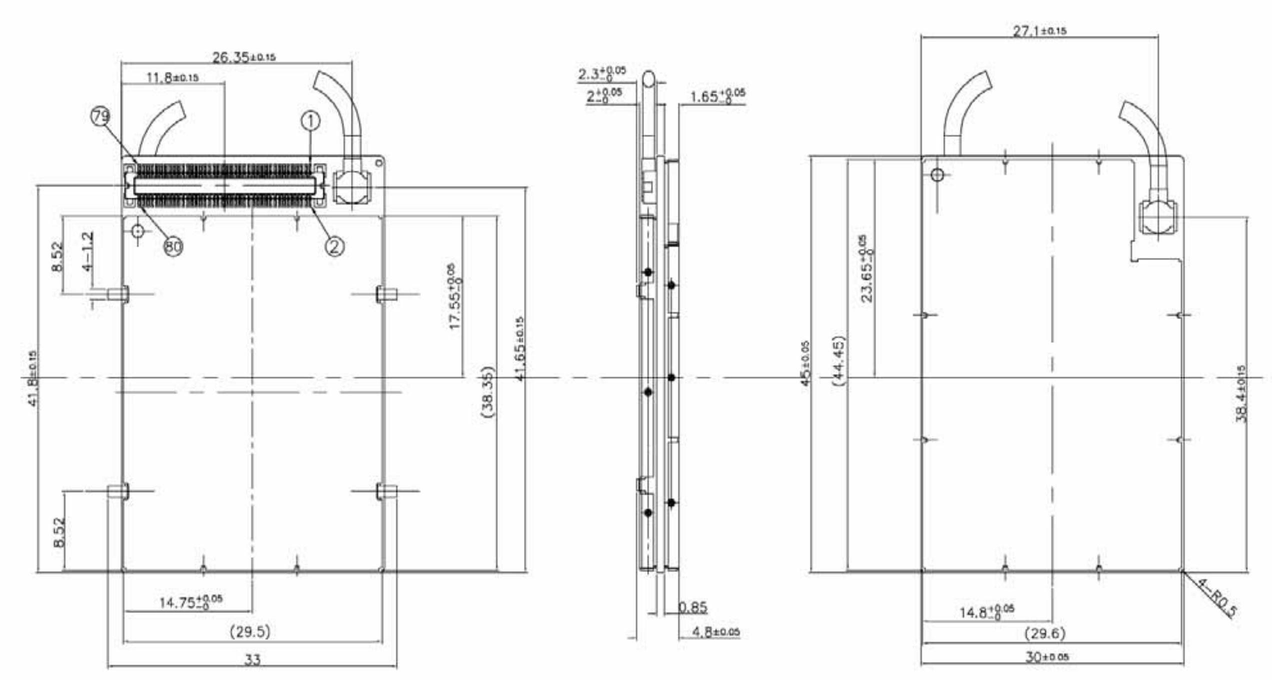
2 Mechanical Dimensions

The Telit UC864-G module overall dimensions are:

- **Length:** **45 mm**
- **Width:** **30 mm**
- **Thickness:** **4.8mm**



3 UC864-G module connections

3.1 PIN-OUT

UC864-G uses an 80 pin Molex p.n. 53949-0878 male connector for the connections with the external applications. This connector matches the 54150-0878 models.

Pin	Signal	I/O	Function	Internal Pull up	Type UC864-E
			Power Supply		
1	VBATT	-	Main power supply		Power
2	VBATT	-	Main power supply		Power
3	VBATT	-	Main power supply		Power
4	VBATT	-	Main power supply		Power
5	GND	-	Ground		Power
6	GND	-	Ground		Power
7	GND	-	Ground		Power
			Audio		
8	AXE	I	Hands-free switching	100KΩ	CMOS 2.6V
9	EAR_HF+	AO	Hands-free ear output, phase +		Audio
10	EAR_HF-	AO	Hands-free ear output, phase -		Audio
11	EAR_MT+	AO	Handset earphone signal output, phase +		Audio
12	EAR_MT-	AO	Handset earphone signal output, phase -		Audio
13	MIC_HF+	AI	Hands-free microphone input; phase +, nominal level 3mVrms		Audio
14	MIC_HF-	AI	Hands-free microphone input; phase -, nominal level 3mVrms		Audio
15	MIC_MT+	AI	Handset microphone signal input; phase+, nominal level 50mVrms		Audio
16	MIC_MT-	AI	Handset microphone signal input; phase-, nominal level 50mVrms		Audio
			SIM Card Interface		
18[1]	SIMVCC	-	External SIM signal – Power supply for the SIM		1.8 / 3V
19	SIMRST	O	External SIM signal – Reset		1.8 / 3V
20	SIMIO	I/O	External SIM signal - Data I/O		1.8 / 3V
21	SIMIN	I	External SIM signal - Presence (active low)	47KΩ	1.8 / 3V
22	SIMCLK	O	External SIM signal – Clock		1.8 / 3V
			Trace		
23	RX_TRACE	I	RX Data for debug monitor		CMOS 2.6V

[1] On this line a maximum of 10nF bypass capacitor is allowed

Pin	Signal	I/O	Function	Internal Pull up	Type UC864-E
24	TX_TRACE	O	TX Data for debug monitor		CMOS 2.6V
			Prog. / Data + Hw Flow Control		
25	C103/TXD	I	Serial data input (TXD) from DTE		CMOS 2.6V
26	C104/RXD	O	Serial data output to DTE		CMOS 2.6V
27	C107/DSR	O	Output for Data set ready signal (DSR) to DTE		CMOS 2.6V
28	C106/CTS	O	Output for Clear to send signal (CTS) to DTE		CMOS 2.6V
29	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE		CMOS 2.6V
30	C125/RING	O	Output for Ring indicator signal (RI) to DTE		CMOS 2.6V
31	C105/RTS	I	Input for Request to send signal (RTS) from DTE		CMOS 2.6V
32	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE		CMOS 2.6V
			IIC		
33	I2C_SCL	I/O	IIC Hardware interface		CMOS 2.6V
34	I2C_SDA	I/O	IIC Hardware interface		CMOS 2.6V
			Miscellaneous Functions		
35	USB_ID	AI	Analog input used to sense whether a peripheral device is connected, and determine the peripheral type, a host or a peripheral		Analog
36	PCM_CLOCK	I/O	PCM clock out		CMOS 2.6V
			DAC and ADC		
37	ADC_IN1	AI	Analog/Digital converter input		A/D
38	ADC_IN2	AI	Analog/Digital converter input		A/D
39	ADC_IN3	AI	Analog/Digital converter input		A/D
40	DAC_OUT	AO	Digital/Analog converter output		D/A(PDM)
			Miscellaneous Functions		
45	STAT_LED	O	Status indicator led		CMOS 1.8V
46	GND	-	Ground		Ground
48	USB_VBUS	AI /AO	Power supply for the internal USB transceiver. This pin is configured as an analog input or an analog output depending upon the type of peripheral device connected.		4.4V ~5.25V
49	PWRMON	O	Power ON Monitor		CMOS 2.6V
50	VAUX1	-	Power output for external accessories		2.85V
51	CHARGE	AI	Charger input (*)		Power
52	CHARGE	AI	Charger input (*)		Power
53	ON/OFF*	I	Input command for switching power ON or OFF (toggle command). The pulse to be sent to the UC864-E must be equal or greater than 1 second.		Pull up to VBATT
54	RESET*	I	Reset input		
55	VRTC	AO	VRTC Backup capacitor		Power
			Telit GPIOs		
56	TGPIO_19	I/O	Telit GPIO19 Configurable GPIO		CMOS 2.6V
57	TGPIO_11	I/O	Telit GPIO11 Configurable GPIO		CMOS 2.6V

Pin	Signal	I/O	Function	Internal Pull up	Type UC864-E
58	TGPIO_20	I/O	Telit GPIO20 Configurable GPIO		CMOS 2.6V
59	TGPIO_04	I/O	Telit GPIO4 Configurable GPIO		CMOS 2.6V
60	TGPIO_14	I/O	Telit GPIO14 Configurable GPIO		CMOS 2.6V
61	TGPIO_15	I/O	Telit GPIO15 Configurable GPIO		CMOS 2.6V
62	TGPIO_12	I/O	Telit GPIO12 Configurable GPIO		CMOS 2.6V
63	TGPIO_10/ PCM_TX	I/O	Telit GPIO10 Configurable GPIO / PCM Data Output		CMOS 2.6V
64	TGPIO_22	I/O	Telit GPIO22 Configurable GPIO		CMOS 1.8V
65	TGPIO_18/ PCM_RX	I/O	Telit GPIO18 Configurable GPIO / PCM Data input		CMOS 2.6V
66	TGPIO_03	I/O	Telit GPIO3 Configurable GPIO		CMOS 2.6V
67	TGPIO_08	I/O	Telit GPIO8 Configurable GPIO		CMOS 2.6V
68	TGPIO_06 / ALARM	I/O	Telit GPIO6 Configurable GPIO / ALARM		CMOS 2.6V
70	TGPIO_01	I/O	Telit GPIO1 Configurable GPIO		CMOS 2.6V
71	TGPIO_17/ PCM_SYNC	I/O	Telit GPIO17 Configurable GPIO / PCM Sync		CMOS 2.6V
72	TGPIO_21	I/O	Telit GPIO21 Configurable GPIO		CMOS 2.6V
73	TGPIO_07/ BUZZER	I/O	Telit GPIO7 Configurable GPIO / Buzzer		CMOS 2.6V
74	TGPIO_02	I/O	Telit GPIO02 I/O pin		CMOS 2.6V
75	TGPIO_16	I/O	Telit GPIO16 Configurable GPIO		CMOS 2.6V
76	TGPIO_09	I/O	Telit GPIO9 Configurable GPIO		CMOS 2.6V
77	TGPIO_13	I/O	Telit GPIO13 Configurable		CMOS 2.6V
78	TGPIO_05/ RFTXMON	I/O	Telit GPIO05 Configurable GPIO / Transmitter ON monitor		CMOS 2.6V
USB Interface					
79	USB_D+	I/O	USB differential Data (+)		2.8V~3.6V
80	USB_D-	I/O	USB differential Data (-)		2.8V~3.6V
RESERVED					
17		-			
41		-			
42		-			
43		-			
44		-			
47		-			
69		-			

NOTE: RESERVED pins must not be connected

RTS should be connected to the GND (on the module side) if flow control is not used

NOTE: If not used, almost all pins should be left disconnected. The only exceptions are the following pins:

Pin	Signal	Function
1	VBATT	Main power supply
2	VBATT	Main power supply
3	VBATT	Main power supply
4	VBATT	Main power supply
5	GND	Ground
6	GND	Ground
7	GND	Ground
46	GND	Ground
25	C103/TXD	Serial data input (TXD) from DTE
26	C104/RXD	Serial data output to DTE
31	C105/RTS	Input for Request to send signal (RTS) from DTE
53	ON/OFF*	Input command for switching power ON or OFF (toggle command).
54	RESET*	Reset input

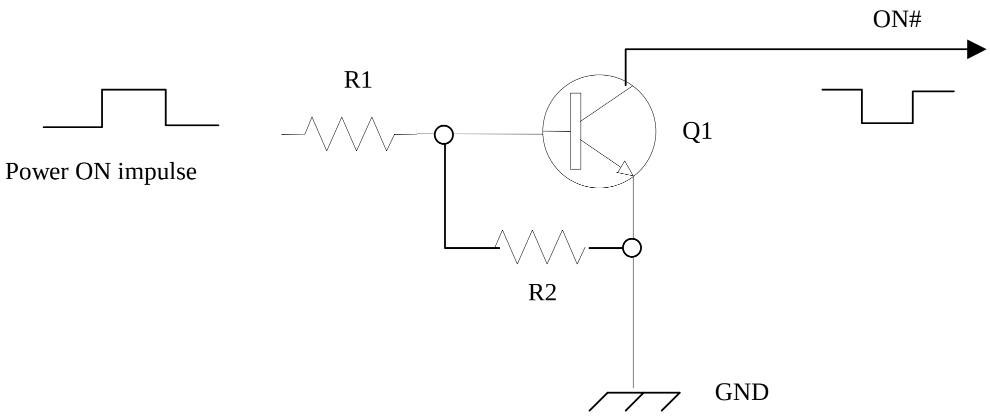
3.1.1 UC864-G Antenna connector

The UC864-G module is equipped with a 50 Ohm RF connector from Murata, GSC type P/N **MM9329-2700B**.
The counterpart suitable is Murata **MXTK92** Type or **MXTK88** Type.

4 Hardware Commands

4.1 Turning ON the UC864-G

To turn on UC864- G, the pad ON# must be tied low for at least 1 second and then released.
The maximum current that can be drained from the ON# pad is 0,1 mA.
A simple circuit to do it is:



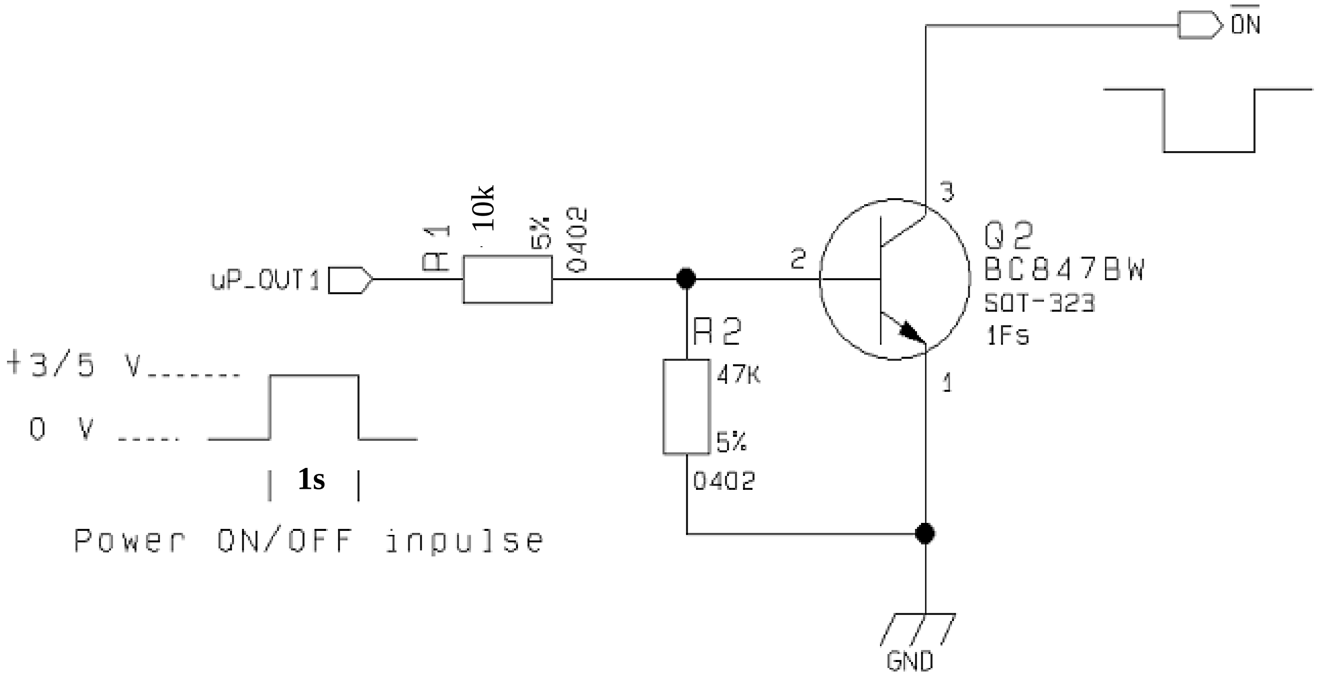
NOTE: UC864-G turns fully on also by supplying power to the USB_VBUS pin (provided there's a battery on the VBATT pads). Care must be taken to avoid supplying power to the USB_VBUS pin before the module turns on.
To check if the UC864-G has powered on, the hardware line PWRMON should be monitored. When PWRMON goes high, the module has powered on.

NOTE: don't use any pull up resistor on the ON# line, it is internally pulled up. Using pull up resistor may bring to latch up problems on the UC864-G power regulator and improper power on/off of the module. The line ON# must be connected only in open collector configuration.

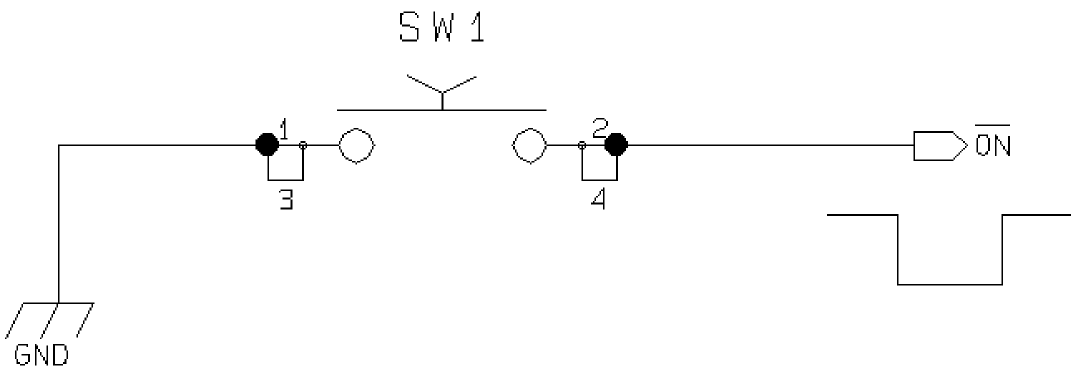
NOTE: In this document all the lines that are inverted, hence have active low signals are labeled with a name that ends with a "#" or with a bar over the name.

NOTE: UC864-G turns fully on also by supplying power to the Charge pad (provided there's a battery on the VBATT pads).

For example:
1- Let's assume you need to drive the ON# pad with a totem pole output of a +3/5 V microcontroller (uP_OUT1):



2- Let's assume you need to drive the ON# pad directly with an ON/OFF button:



4.2 Turning OFF the UC864-G

The turning off of the device can be done in three ways:

- by software command (see UC864-G Software User Guide)
- by hardware shutdown
- by Hardware Unconditional Restart

When the device is shut down by software command or by hardware shutdown, it issues to the network a detach request that informs the network that the device will not be reachable any more.

4.2.1 Hardware shutdown

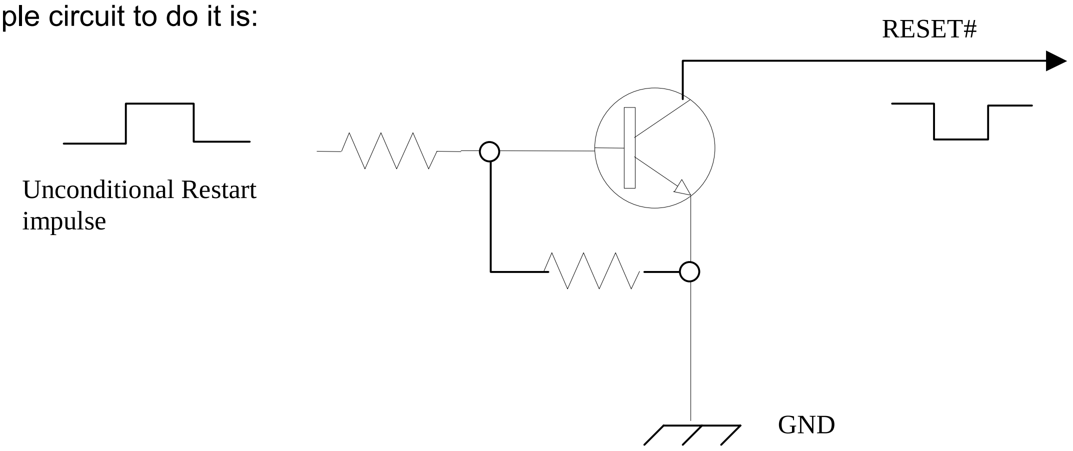
To turn OFF UC864-G, first, you MUST cut off supplying power to the USB_VBUS pin, then the pad ON# must be tied low for at least 2 seconds and then released.
The same circuitry and timing for the power on shall be used.
The device shuts down after the release of the ON# pad.

NOTE: To turn OFF UC864-G, first of all, you MUST cut off supplying power to the USB_VBUS, or the module does not turn off

TIP: To check if the device has powered off, the hardware line PWRMON should be monitored. When PWRMON goes low, the device has powered off.

4.2.2 Hardware Unconditional Restart

To unconditionally restart UC864-G, the pad RESET# must be tied low for at least 200 milliseconds and then released.
The maximum current that can be drained from the ON# pad is 0,15 mA.
A simple circuit to do it is:

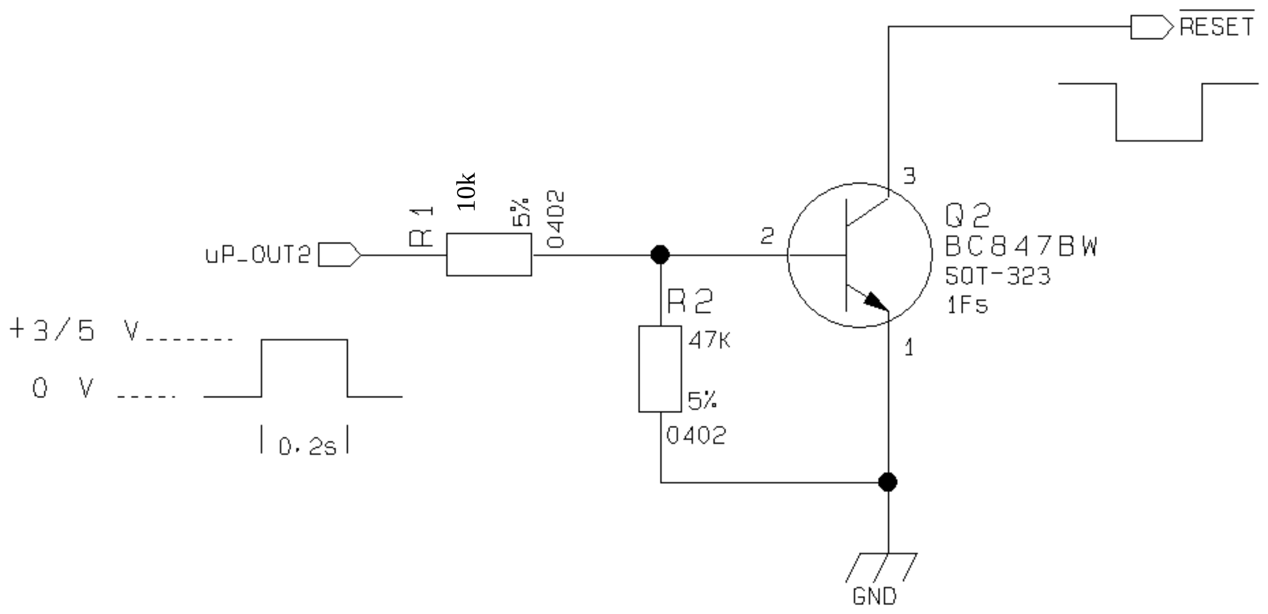


NOTE: Do not use any pull up resistor on the RESET# line or any totem pole digital output. Using pull up resistor may bring to latch up problems on the UC864-G power regulator and improper functioning of the module. The line RESET# must be connected only in open collector configuration.

TIP: The unconditional hardware Restart should be always implemented on the boards and software should use it as an emergency exit procedure.

For example:

1- Let's assume you need to drive the RESET# pad with a totem pole output of a +3/5 V microcontroller (uP_OUT2):



Reset Signal Operating levels:

Signal	Min	Max
RESET Input high	2.2V*	3.3V
RESET Input low	0V	0.2V

* This signal is internally pulled up so the pin can be left floating if not used.

5 Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

5.1 Power Supply Requirements

The UC864-G power requirements are:

• *Nominal Supply Voltage:*	*3.8 V*
• *Max Supply Voltage:*	*4.2 V*
• *Supply voltage range:*	*3.4 V - 4.2 V*
• *Max Peak current consumption (impulsive):*	*1.8A*
• *Max Average current consumption during WCDMA transmission:*	*700mA*
• *Max Average current consumption during class 12 GPRS transmission(@4TX):*	*930mA*
• *Max Average current consumption during GPS Tracking :*	*TBD*
• *Max Average current consumption during VOICE/CSD transmission:*	*340mA*
• *Average current during Power Saving (with CFUN=5) during WCDMA mode:*	*TBD*
• *Average current during idle (Power Saving disabled) during WCDMA mode:*	*TBD*
• *Average current during Power Saving (with CFUN=5) during GSM/GPRS mode:*	*TBD*
• *Average current during idle (Power Saving disabled) during GSM/GPRS mode:*	*37mA*
• *Average GPS current during Power Saving :*	*TBD*

In GSM/GPRS mode, RF transmission is not continuous and it is packed into bursts at a base frequency of about 216 Hz, and the relative current peaks can be as high as about 2A. Therefore the power supply has to be designed in order to withstand with these current peaks without big voltage drops; this means that both the electrical design and the board layout must be designed for this current flow.
If the layout of the PCB is not well designed a strong noise floor is generated on the ground and the supply; this will reflect on all the audio paths producing an audible annoying noise at 216 Hz; if the voltage drop during the peak current absorption is too much, then the device may even shutdown as a consequence of the supply voltage drop.

TIP: The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 2 A.

5.2 General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout.

5.2.1 Electrical Design Guidelines

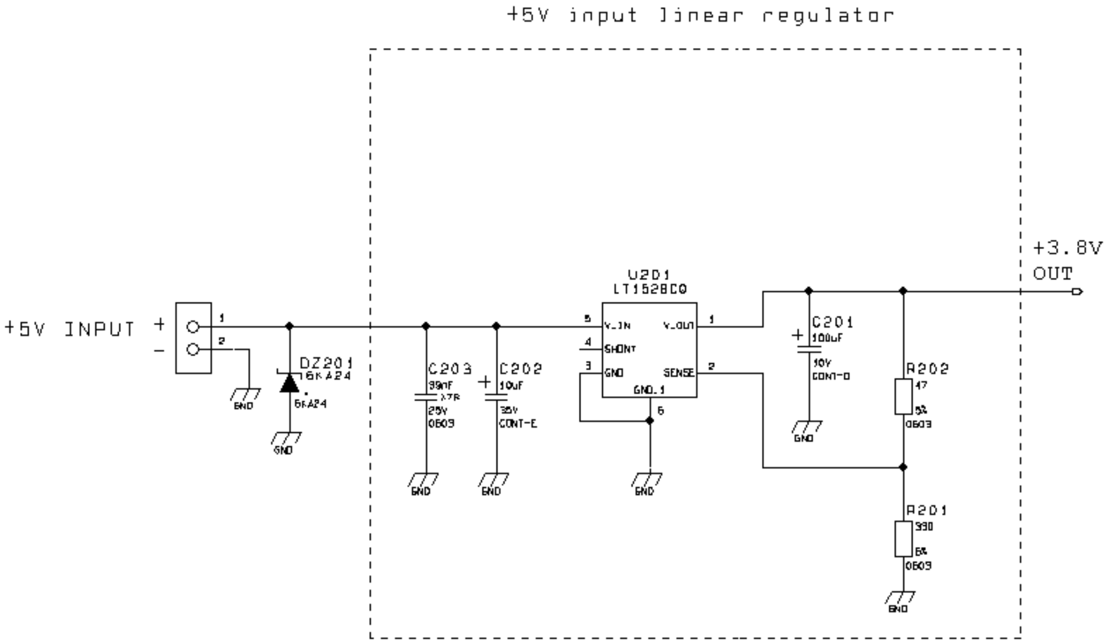
The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

5.2.1.1 + 5V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to UC864-G, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save UC864-G from power polarity inversion.

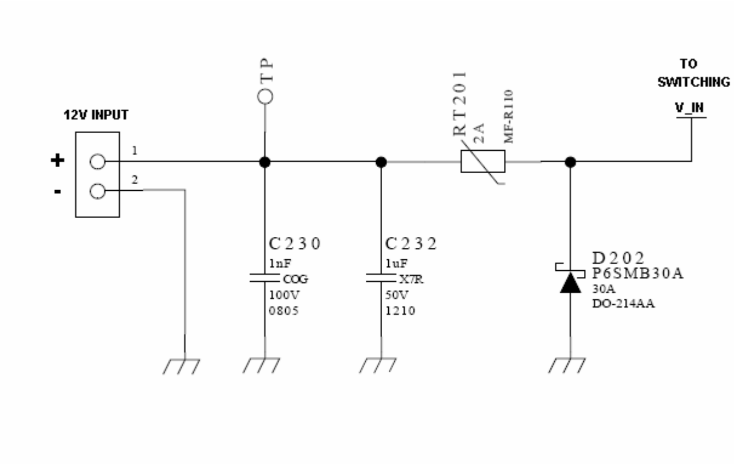
An example of linear regulator with 5V input is:

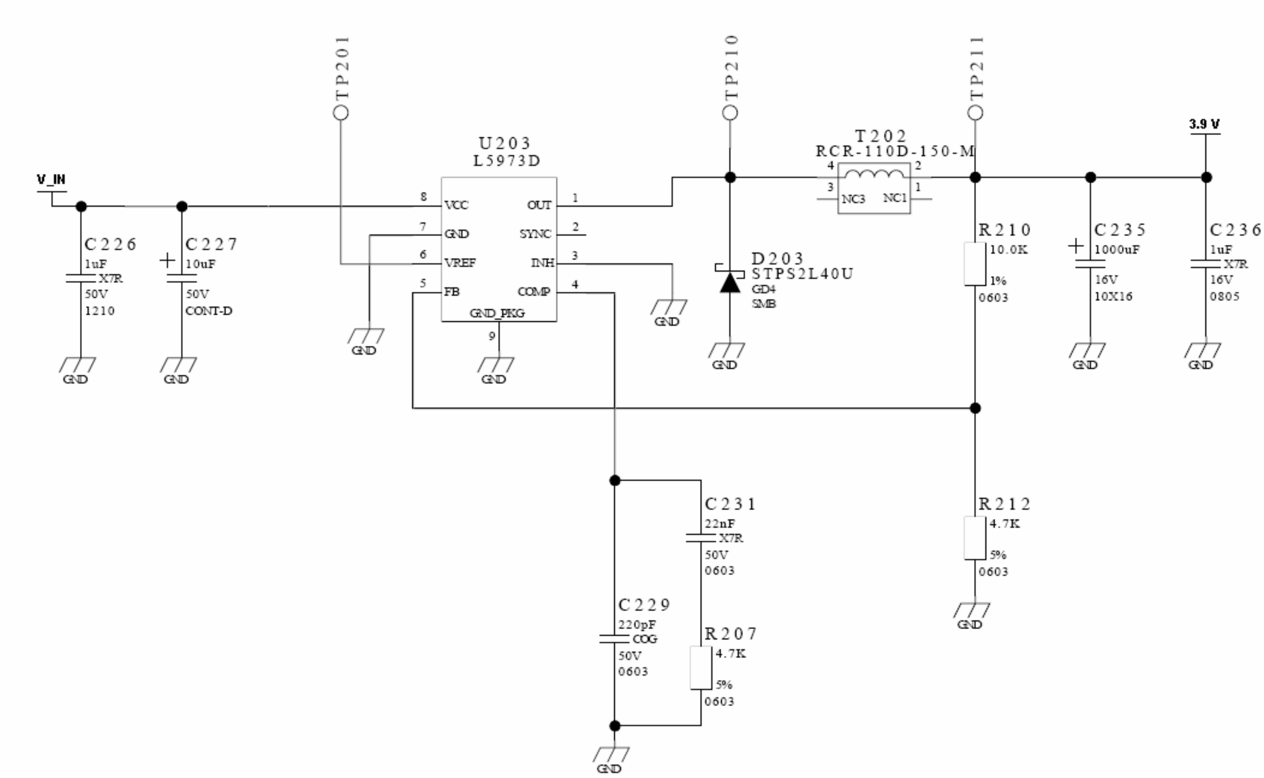


5.2.1.2 + 12V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency especially with the 2A peak current load represented by UC864-G.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- For car PB battery the input voltage can rise up to 15.8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100μF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode should be inserted close to the power input, in order to save UC864-G from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is in the below schematic (it is split in 2 parts):





SWITCHING REGULATOR

5.2.1.3 Battery Source Power Supply Design Guidelines

- The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit UC864-G module.
  The three cells Ni/Cd or Ni/MH 3.6 V Nom. battery types or 4V PB types ***MUST NOT BE USED DIRECTLY*** since their maximum voltage can rise over the absolute maximum voltage for UC864-G and damage it.

NOTE: DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with UC864-G. Their use can lead to overvoltage on UC864-G and damage it. USE ONLY Li-Ion battery types.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100μF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save UC864-G from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 2A; the suggested capacity is from 500mAh to 1000mAh.

5.2.1.4 Battery Charge control Circuitry Design Guidelines

The charging process for Li-Ion Batteries can be divided into 4 phases:

- Qualification and trickle charging
- Fast charge 1 - constant current
- Final charge - constant voltage or pulsed charging
- Maintenance charge

The qualification process consists in a battery voltage measure, indicating roughly its charge status. If the battery is deeply discharged, that means its voltage is lower than the trickle charging threshold, then the charge must start slowly possibly with a current limited pre-charging process where the current is kept very low with respect to the fast charge value: the trickle charging.
During the trickle charging the voltage across the battery terminals rises; when it reaches the fast charge threshold level the charging process goes into fast charge phase.
During the fast charge phase the process proceeds with a current limited charging; this current limit depends on the required time for the complete charge and from the battery pack capacity. During this phase the voltage across the battery terminals still raises but at a lower rate.
Once the battery voltage reaches its maximum voltage then the process goes into its third state: Final charging. The voltage measure to change the process status into final charge is very important. It must be ensured that the maximum battery voltage is never exceeded, otherwise the battery may be damaged and even explode. Moreover for the constant voltage final chargers, the constant voltage phase (final charge) must not start before the battery voltage has reached its maximum value; otherwise the battery capacity will be highly reduced.
The final charge can be of two different types: constant voltage or pulsed. UC864-G uses constant voltage.

The constant voltage charge proceeds with a fixed voltage regulator (very accurately set to the maximum battery voltage) and hence the current will decrease while the battery is becoming charged. When the charging current falls below a certain fraction of the fast charge current value, then the battery is considered fully charged, the final charge stops and eventually starts the maintenance.
The pulsed charge process has no voltage regulation, instead the charge continues with pulses. Usually the pulse charge works in the following manner: the charge is stopped for some time, let's say few hundreds of ms, then the battery voltage will be measured and when it drops below its maximum value a fixed time length charging pulse is issued. As the battery approaches its full charge the off time will become longer, hence the duty-cycle of the pulses will decrease. The battery is considered fully charged when the pulse duty-cycle is less than a threshold value, typically 10%, the pulse charge stops and eventually the maintenance starts.
The last phase is not properly a charging phase, since the battery at this point is fully charged and the process may stop after the final charge. The maintenance charge provides an additional charging process to compensate for the charge leak typical of a Li-Ion battery. It is done by issuing pulses with a fixed time length, again few hundreds of ms, and a duty-cycle around 5% or less.
This last phase is not implemented in the UC864-G internal charging algorithm, so that the battery once charged is left discharging down to a certain threshold so that it is cycled from full charge to slight discharge even if the battery charger is always inserted. This guarantees that anyway the remaining charge in the battery is a good percentage and that the battery is not damaged by keeping it always fully charged (Li-Ion rechargeable battery usually deteriorates when kept fully charged).
Last but not least, in some applications it is highly desired that the charging process restarts when the battery is discharged and its voltage drops below a certain threshold, UC864-G internal charger does it.

As you can see, the charging process is not a trivial task to be done; moreover all these operations should start only if battery temperature is inside a charging range, usually 5°C - 45°C.
UC864-G measures the temperature of its internal component, in order to satisfy this last requirement, it's not exactly the same as the battery temperature but in common application the two temperature should not differ too much and the charging temperature range should be guaranteed.

NOTE: For all the threshold voltages, inside UC864-G, all thresholds are fixed in order to maximize Li-Ion battery performances and do not need to be changed.

NOTE: In this application the battery charger input current must be limited to less than 400mA. This can be done by using a current limited wall adapter as the power source.

NOTE: When starting the charger from Module powered off the startup will be in CFUN4; to activate the normal mode a command AT+CFUN=1 has to be provided.

5.2.2 Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specifications:

- *Average current consumption during WCDMA transmission @PWR level max: 700mA*
- *Average current consumption during class12 GPRS transmission @PWR level max: 930mA*
- *Average GPS current during Tracking (Power Saving disabled) TBD*

NOTE: The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

TIP: The thermal design for the Power supply should be made keeping an average consumption at the max transmitting level during calls of 700mA rms plus GPS current during tracking.

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.
If we assume that the device stays into transmission for short periods of time (let's say few minutes) and then remains for a quite long time in idle (let's say one hour), then the power supply has always the time to cool down between the calls and the heat sink could be smaller than the calculated one for 930mA maximum RMS current, or even could be the simple chip package (no heat sink).
Moreover in the average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than the 930mA, being usually around 150mA.
For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating.
For the heat generated by the UC864-G, you can consider it to be during transmission 1W max during CSD/VOICE calls and 2W max during class12 GPRS upload.
This generated heat will be mostly conducted to the ground plane under the UC864-G; you must ensure that your application can dissipate it.

In the WCDMA mode, since UC864-G emits RF signals continuously during WCDMA transmission, you should pay special attention on how to dissipate the heat generated.
The current consumption will be up to about 700mA continuously at the maximum TX output power(24dBm). Thus, you should arrange the PCB area as large as possible under UC864-G which you will mount.You can mount UC864-G on the large ground area of your application board and make many ground vias for heat sink.
The peak current consumption in the GSM mode is higher than that in WCDMA. However, considering the heat sink is more important with WCDMA.
As mentioned before, GSM signal is bursty. Thus, the temperature drift is more insensible than WCDMA. Consequently, if you prescribe the heat dissipation in the WCDMA mode, you don’t need to think more about the GSM mode

5.2.3 Power Supply PCB layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The Bypass low ESR capacitor must be placed close to the Telit UC864-G power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to UC864-G is wide enough to ensure a drop-less connection even during the 2A current peaks.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 2A current peaks are absorbed. Note that this is not made in order to save power loss but especially to avoid the voltage drops on the power line at the current peaks frequency of 216 Hz that will reflect on all the components connected to that supply, introducing the noise floor at the burst base frequency. For this reason while a voltage drop of 300-400 mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If your application doesn't have audio interface but only uses the data feature of the Telit UC864-G, then this noise is not so disturbing and power supply layout design can be more forgiving.
- The PCB traces to UC864-G and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 2A current peaks are absorbed. This is for the same reason as previous point. Try to keep this trace as short as possible.
- The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.

6 Antenna

The antenna connection and board layout design are the most important part in the full product design and they strongly reflect on the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.

6.1 GSM/WCDMA Antenna Requirements

As suggested on the Product Description the antenna for a Telit UC864-G device shall fulfill the following requirements:

GSM /WCDMA ANTENNA REQUIREMENTS	
Frequency range	Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Bandwidth	70 MHz in GSM850, 80 MHz in GSM900, 170 MHz in DCS & 140 MHz PCS 70 MHZ in WCDMA850, 140 MHz in WCDMA1900 & 250 MHz in WCDMA2100 band
Gain	Gain < 3dBi
Impedance	50 ohm
Input power	> 33dBm(2 W) peak power in GSM > 24dBm Average power in WCDMA
VSWR absolute max	<= 10:1
VSWR recommended	<= 2:1

If the device is developed for the US market and/or Canada market, it shall comply to the FCC and/or IC approval requirements:
This device is to be used only for mobile and fixed application. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-Users must be provided with transmitter operation conditions for satisfying RF exposure compliance. OEM integrators must ensure that the end user has no manual instructions to remove or install the UC864-G module. Antennas used for this OEM module must not exceed 3dBi gain for mobile and fixed operating configurations.

6.2 GSM/WCDMA Antenna - Installation Guidelines

- Install the antenna in a place covered by the GSM/WCDMA signal.
- The Antenna must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter;
- Antenna shall not be installed inside metal cases
- Antenna shall be installed also according Antenna manufacturer instructions.

6.3 GPS Antenna Requirements (TBD)

- The use of an active antenna is recommended to achieve a good performance.
- The use of combined GPS antennas is NOT recommended; this solution could generate an extremely poor GPS reception and also the combination antenna requires additional diplexer and adds a loss in the RF route.

GPS ANTENNA REQUIREMENTS	
Frequency range	1575.42 MHz(GPS L1 band)
Bandwidth	+/- 2 MHz
Gain	TBD
Impedance	50 ohm
Amplification	TBD
Supply voltage	Must accept from 3 to 4V DC
Current consumption	TBD

If the device is developed for the US market and/or Canada market, it shall comply to the FCC and/or IC approval requirements:
This device is to be used only for mobile and fixed application.

6.4 GPS Antenna - Installation Guidelines

- The UC864-G due to its characteristics of sensitivity is capable to perform a Fix inside the buildings. (In any case the sensitivity could be affected by the building characteristics i.e. shielding)
- The Antenna must not be co-located or operating in conjunction with any other antenna or transmitter.
- Antenna shall not be installed inside metal cases.
- Antenna shall be installed also according Antenna manufacturer instructions.

7 Logic level specifications

Where not specifically stated, all the interface circuits work at 2.6V CMOS logic levels. The following table shows the logic level specifications used in the Telit UC864-G interface circuits:

For 2.6V CMOS signals:

Absolute Maximum Ratings -Not Functional

Parameter	UC864-G	
	Min	Max
Input level on any digital pin when on	-0.3V	+3.0V
Input voltage on analog pins when on	-0.3V	+3.0 V

Operating Range - Interface levels

Level	UC864-G	
	Min	Max
Input high level	2.0V	2.9 V
Input low level	-0.3V	0.6V
Output high level	2.2V	2.6V
Output low level	0V	0.35V

For 2,0V signals:

Operating Range - Interface levels (2.0V CMOS)

Level	UC864-G	
	Min	Max
Input high level	1.5V	2.1V
Input low level	-0.3V	0.5V
Output high level	1.4V	1.8V
Output low level	0V	0.35V

7.1 Reset signal

Signal	Function	I/O	PIN Number
RESET	Phone reset	I	54

RESET is used to reset the UC864-G module. Whenever this signal is pulled low, UC864-G is reset. When the device is reset it stops any operation. After the release of the reset UC864-G is unconditionally shut down, without doing any detach operation from the network where it is registered. This behaviour is not a proper shut down because any device is requested to issue a detach request on turn off. For this reason the Reset signal must not be used to normally shutting down the device, but only as an emergency exit in the rare case the device remains stuck waiting for some network response.
The RESET is internally controlled on start-up to achieve always a proper power-on reset sequence, so there's no need to control this pin on start-up. It may only be used to reset a device already on that is not responding to any command.

***NOTE**: do not use this signal to power off **UC864-G**. Use the ON/OFF signal to perform this function or the AT#SHDN command.*

Reset Signal Operating levels:

Signal	Min	Max
RESET Input high	2.0V*	2.2V
RESET Input low	0V	0.2V

* This signal is internally pulled up so the pin can be left floating if not used.

If unused, this signal may be left unconnected. If used, then it **must always be connected with an open collector transistor**, to permit to the internal circuitry the power on reset and under voltage lockout functions.

8 Serial Ports

The serial port on the Telit UC864-G is the interface between the module and OEM hardware.
2 serial ports are available on the module:

- MODEM SERIAL PORT
- MODEM SERIAL PORT 2 (DEBUG)

8.1 MODEM SERIAL PORT

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 2.8V - 3V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 5V or other voltages different from 2.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work. The only configuration that doesn't need a level translation is the 2.8V UART.
The serial port on UC864-G is a +2.6V UART with all the 7 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels. The levels for UC864-G UART are the CMOS levels:

Absolute Maximum Ratings -Not Functional

Parameter	UC864-G	
	Min	Max
Input level on any digital pin when on	-0.3V	+3.0V
Input voltage on analog pins when on	-0.3V	+3.0 V

Operating Range - Interface levels

Level	UC864-G	
	Min	Max
Input high level	2.0V	2.9 V
Input low level	-0.3V	0.6V
Output high level	2.2V	2.6V
Output low level	0V	0.35V

The signals of the UC864-G serial port are:

RS232 Pin Number	Signal	UC864-G Pad Number	Name	Usage
1	DCD - dcd_uart	32	Data Carrier Detect	Output from the UC864-G that indicates the carrier presence
2	RXD - tx_uart	26	Transmit line *see Note	Output transmit line of UC864-G UART
3	TXD - rx_uart	25	Receive line *see Note	Input receive of the UC864-G UART
4	DTR - dtr_uart	29	Data Terminal Ready	Input to the UC864-G that controls the DTE READY condition
5	GND	5,6,7	Ground	ground
6	DSR - dsr_uart	27	Data Set Ready	Output from the UC864-G that indicates the module is ready
7	RTS - rts_uart	31	Request to Send	Input to the UC864-G that controls the Hardware flow control
8	CTS - cts_uart	28	Clear to Send	Output from the UC864-G that controls the Hardware flow control
9	RI - ri_uart	30	Ring Indicator	Output from the UC864-G that indicates the incoming call condition

NOTE: According to V.24, RX/TX signal names are referred to the application side, therefore on the UC864-G side these signal are on the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ rx_uart) of the UC864-G serial port and vice versa for RX.

TIP: For a minimum implementation, only the TXD and RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

8.2 RS232 level translation

In order to interface the Telit UC864-G with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must

- invert the electrical signal in both directions
- change the level from 0/3V to +15/-15V

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing for a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.
The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of driver and receiver and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).
By convention the driver is the level translator from the 0-3V UART level to the RS232 level, while the receiver is the translator from RS232 level to 0-3V UART.

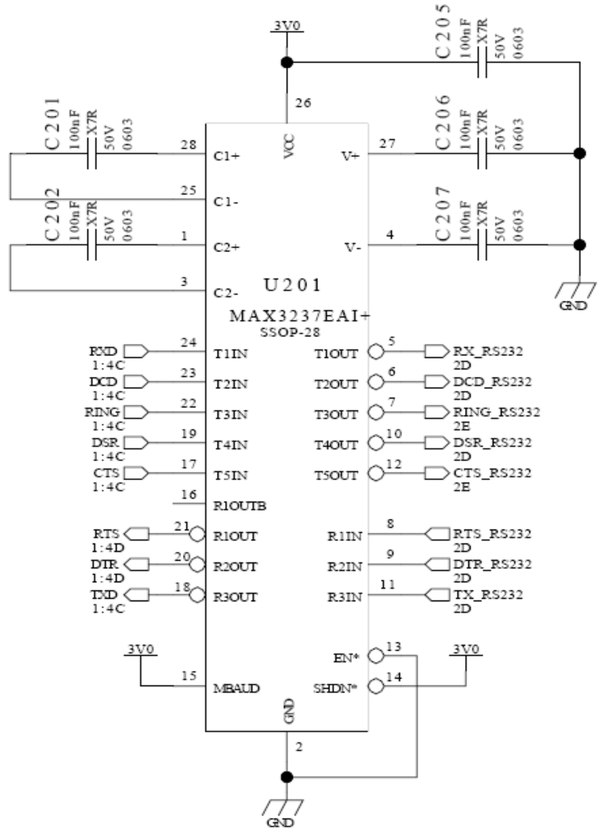
In order to translate the whole set of control lines of the UART you will need:

- 5 drivers
- 3 receivers

NOTE: The digital input lines working at 2.6V CMOS have an absolute maximum input voltage of 3.0V; therefore the level translator IC shall not be powered by the +3.8V supply of the module. Instead it shall be powered from a +2.6V / +3.0V (dedicated) power supply.
This is because in this way the level translator IC outputs on the module side (i.e. UC864-G inputs) will work at +3.8V interface levels, stressing the module inputs at its maximum input voltage.
This can be acceptable for evaluation purposes, but not on production devices.

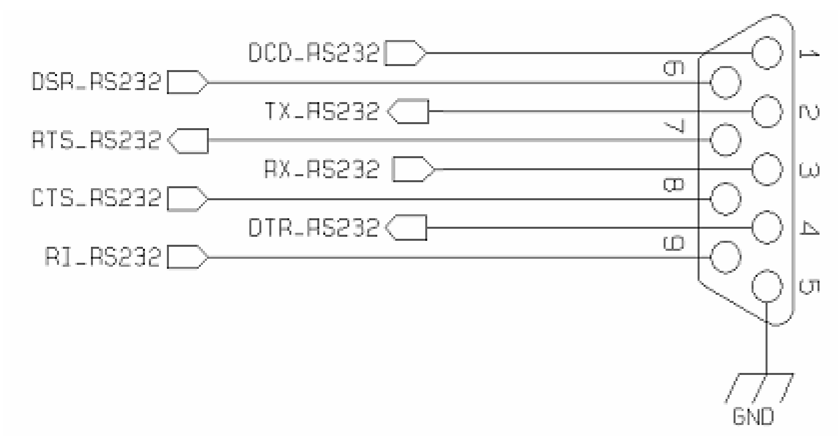
NOTE: In order to be able to do in circuit reprogramming of the UC864-G firmware, the serial port on the Telit UC864-G shall be available for translation into RS232 and either it's controlling device shall be placed into tri-state, disconnected or as a gateway for the serial data when module reprogramming occurs.
Only RXD, TXD, GND and the On/off module turn on pad are required to the reprogramming of the module, the other lines are unused.
All applicator shall include in their design such a way of reprogramming UC864-G.

An example of level translation circuitry of this kind is:



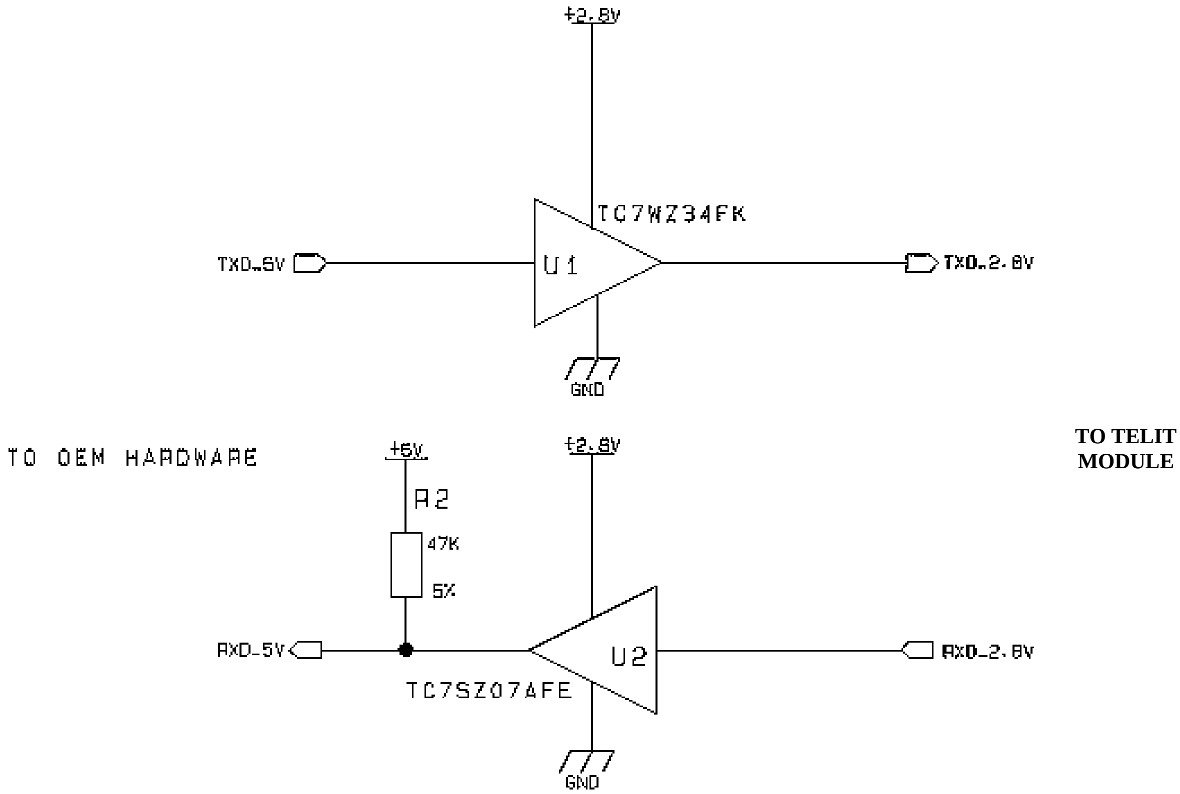
RS232 LEVEL TRSANSLATOR

The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



8.3 5V UART level translation

If the OEM application uses a microcontroller with a serial port (UART) that works at a voltage different from 2.6 - 3V, then a circuitry has to be provided to adapt the different levels of the two set of signals. As for the RS232 translation there are a multitude of single chip translators. For example a possible translator circuit for a 5V TRANSMITTER/RECEIVER can be:



TIP: This logic IC for the level translator and 2.8V pull-ups (not the 5V one) can be powered directly from PWRMON line of UC864-G. Note that the TC7SZ07AE has open drain output; therefore the resistor R2 is mandatory.

NOTE: The UART input line TXD (rx_uart) of UC864-G is NOT internally pulled up with a resistor, so there may be the need to place an external 47KΩ pull-up resistor, either the DTR (dtr_uart) and RTS (rts_uart) input lines are not pulled up internally, so an external pull-up resistor of 47KΩ may be required.

A power source of the internal interface voltage corresponding to the 2.6V CMOS high level is available at the PWRMON pin on the connector, whose absolute maximum output current is 1mA.
A maximum of 9 resistors of 47 KΩ pull-up can be connected to the PWRMON pin, provided no other devices are connected to it and the pulled-up lines are UC864-G input lines connected to open collector outputs in order to avoid latch-up problems on UC864-G.
Care must be taken to avoid latch-up on UC864-G and the use of this output line to power electronic devices shall be avoided, especially for devices that generate spikes and noise such as switching level translators, micro controllers, failure in any of these condition can severely compromise the UC864-G functionality.

NOTE: The input lines working at 2.6VCMOS can be pulled-up with 47KΩ resistors that can be connected directly to the PWRMON line provided they are connected as in this example.
NO OTHER devices than those suggested should be powered with the PWRMON line; otherwise the module functionality may be compromised.

It is important to consider that the added circuit must have consumption lower than 1mA.
In case of reprogramming of the module has to be considered the use of the RESET line to start correctly the activity.

The preferable configuration is having an external supply for the buffer.

9 USB Port

UC864-G includes an integrated universal serial bus (USB) transceiver, compliant with USB 2.0 specification, for interfacing UC864-G to a computer as a USB peripheral or connecting the UC864-G to other peripherals. It supports the USB low-speed (1.5 Mbits/s) and full-speed (12 Mb/s) modes. In HSDPA (High Speed download Packet Access) mode, the downlink data speed rates up to 7.2Mbps. Hence you need to interface UC864-G to your applications in full-speed (12Mbits/s) mode.
You can use USB for the following purposes: communication with external peripheral devices, debug monitor

USB Pin No.	Signal	UC864-G Pad No.	Usage
1	USB_VBUS	48	Power supply for the internal USB transceiver. This pin is configured as an analog input or an analog output depending upon the type of peripheral device connected.
2	USB_D-	80	Minus (-) line of the differential, bi-directional USB signal to/from the peripheral device
3	USB D+	79	Plus (+) line of the differential, bi-directional USB signal to/from the peripheral device
4	USB_ID	35	Analog input used to sense whether a peripheral device is connected, and determine the peripheral type, a host or a slave

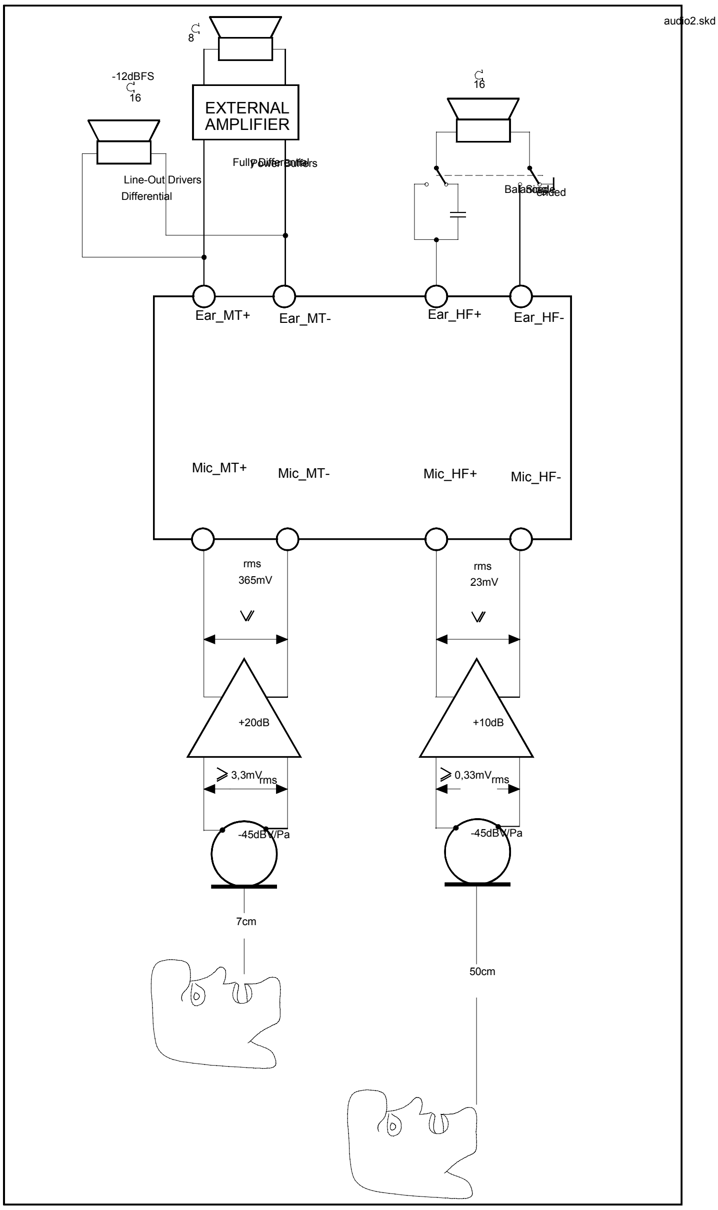
10 Audio Section Overview

The Base Band Chip of the UC864-G Telit Module provides two different audio blocks; both in transmit (*Uplink*) and in receive (*Downlink*) direction:

"*MT lines*" should be used for handset function,

"*HF lines*" is suited for hands -free function (car kit).

These two blocks can be active only one at a time, selectable by *AXE* hardware line or by AT command. The audio characteristics are equivalent in transmit blocks, but are different in the receive ones and this should be kept in mind when designing.



10.1 Microphone Paths Characteristic and Requirements

TIP: Being the microphone circuitry the more noise sensitive, its design and layout must be done with particular care. Both microphone paths are balanced and the OEM circuitry should be balanced designed to reduce the common mode noise typically generated on the ground plane. However an unbalanced circuitry can be also used for particular OEM application needs.

TIP: Due to the difference in the echo canceller type, the "Mic_MT" audio path is suited for Handset applications, while the "Mic_HF"audio path is suited for hands-free function (car kit). The Earphone applications should be made using the "Mic_HF" audio path but DISABLING the echo canceller by software AT command. If the echo canceller is left active with the Earphone, then some echo might be introduced by the echo cancel algorithm.

UC864-G;

"Mic_MT" 1st differential microphone path

- **line coupling** — **AC**
- **line type** — **balanced**
- **coupling capacitor** — **≥ 100nF**
- **differential input impedance** — **20kΩ**
- **differential input voltage** — **≤ 1,03V_{pp} (365mV_{rms})**
- **microphone nominal sensitivity** — **-45 dBV_{rms}/Pa**
- **analog gain suggested** — **+20dB**
- **echo canceller type** — **handset**

"Mic_HF" 2nd differential microphone path

- **line coupling** — **AC**
- **line type** — **balanced**
- **coupling capacitor** — **≥ 100nF**
- **differential input resistance** — **20kΩ**
- **differential input voltage** — **≤ 65mV_{pp} (23mV_{rms})**
- **microphone nominal sensitivity** — **-45 dBV_{rms}/Pa**
- **analog gain suggested** — **+10dB**
- **echo canceller type** — **car kit hands-free**

TIP: Definition of the nominal sensitivity of the microphone lines.

The nominal sensitivity of the microphone lines indicates the voltage level on the UC864-G pins present during "*normal spoken*" conditions.
For a handset , the "*normal spoken"* conditions take place when the talker mouth is 7cm far from the microphone ; under these conditions the voice will produce an acoustic pressure of *-4,7dBPa @1kHz* on the microphone membrane .

TIP: Electrical equivalent signal and operating voice levels.

At "*normal spoken*" conditions, a microphone having the suggested nominal sensitivity of *-45dBV$_{rms}$/Pa*, will produce

the electrical equivalent signal : *MicLevel = (-45) + (-4.7) = -49.7 dB$_{Vrms}$*

that means : *MicVoltage = $10^{(-49.7/20)}$ = 3.3* 10^{-3} V$_{rms}$*

During a call, this level varies according to the volume of the talker voice; usually the following rough thumb rule for the dynamic range may be used:

1) the talker is screaming . This is the *strongest voice level* condition: the signal increases by +20dB;
2) the talker is whispering. This is the *lowest voice level* condition: the voice level decreases by –50dB.

These changes must be considered for designing the external microphone amplifier.

TIP: Example of external microphone amplifier calculation

Let's suppose to use the 1st*differential* microphone path .In this case the maximum differential input voltage to "*Mic_MT*" lines is 365mV$_{rms}$(1,03V$_{pp}$) corresponding to –8,76dBV.
Now we can calculate the maximum voltage gain of an external microphone amplifier **G_A** :

$$[(MicLevel + 20dB) + G_A] = -8{,}76dBV$$

$$[-49{,}7 + 20 + G_A] = -8{,}76$$

$$-40{,}9 + 20 = -G_A$$

$$G_A = 20{,}94dB$$

→ You can set G_A= ***+20dB*** to use standard resistor values .

TIP: Environment consideration

For *handsfree/car kit* microphone, you must take into account the voice attenuation, due to the distance between the microphone itself and the talker, when designing the external microphone amplifier.
Not only, you must consider that the microphone will pick up also ambient noise; to overcome this problem it is preferable to set the gain of the microphone *10dB* lower with respect to the calculated value for a nominal sensitivity. The corresponding reduction in signal level will be compensated by an increased voice volume of the talker which will speak louder because of the ambient noise.
For a car cabin usually the distance between the microphone itself and the talker is *40/50cm*; in these conditions the attenuation can be considered as a thumb rule around *20dB*.

For the earphone we shall distinguish two different types: the earphones having the microphone sustained close to the mouth and the ones having the microphone on the earpiece cable.
The same considerations for the additional voice attenuation due to the distance from the microphone and the noise pick up can be made for the earphone having the microphone on the earpiece cable, while the other kind of earphone shall be threaten as a handset.

TIP: How to compensate the losses in the car cabin hands-free condition

The voice signal , that in the "normal spoken" conditions produces on the microphone membrane an acoustic pressure of -4,7dBPa at 1kHz , will have a further attenuation of 20dB due the 50cm distance .

Therefore a microphone having the suggested nominal sensitivity of -45dBV$_{rms}$/Pa, will produce a lower electrical

equivalent signal : *MicLevel = (-45) + (-4.7)-20 = -69.7*

that means : *MicVoltage = 10 $^{(-49.7/20)}$ = 0,33* 10 $^{-3}$*

Setting the "microphone gain" at +10dB (3 times), the signal in the nominal conditions on the "Mic_HF" inputs s of UC864-G Telit Module will be:

*"**Mic_HF**" Level = 0,33* 10 $^{-3}$ * 3=1* 10 $^{-3}$*

Hence in these conditions the signal level on the"***Mic_HF***" input pads of UC864-E is 10 dB (3 times) lower than the nominal, as suggested.

10.2 General Design Rules

There are several configurations for the audio paths, but the most effective difference is between balanced and unbalanced microphone configuration.
It is highly recommended to keep the whole microphone path balanced even if this means having 2 wires connecting the microphone instead of one needed (plus ground) in the unbalanced case. The balanced circuitry is more suited because of its good common mode noise rejection, reducing the *216 Hz* burst noise produced during the GSM transmissions.

- Where possible use balanced microphone circuitry
- Keep the microphone traces on the PCB and wires as short as possible.
- If your application requires an unbalanced microphone, then keep the lines on the PCB balanced and "unbalance" the path close to the microphone wire connector if possible.
- For the microphone biasing voltage use a dedicated voltage regulator and a capacitor multiply circuit.
- Make sure that the microphone traces in the PCB don't cross or run parallel to noisy traces (especially the power line)
- If possible put all around to the microphone lines a ground trace connected to the ground plane by several vias. This is done in order to simulate a shielded trace on the PCB.
- The biasing circuit and eventually the buffer can be designed in the same manner for the internal and external microphones.

10.3 Other considerations

If your application is a hands-free/car kit scenario, but you need to put microphone and speaker inside the same box:

- try to have the maximum possible distance between them, at least 7cm ;
- because the microphone type is very important, if you use an omni-directional one (and this is the typical application) please seal it on the rear side (no back cavity) in order not to collect unwanted signals ;
- try to make divergent the main axes of the two devices .

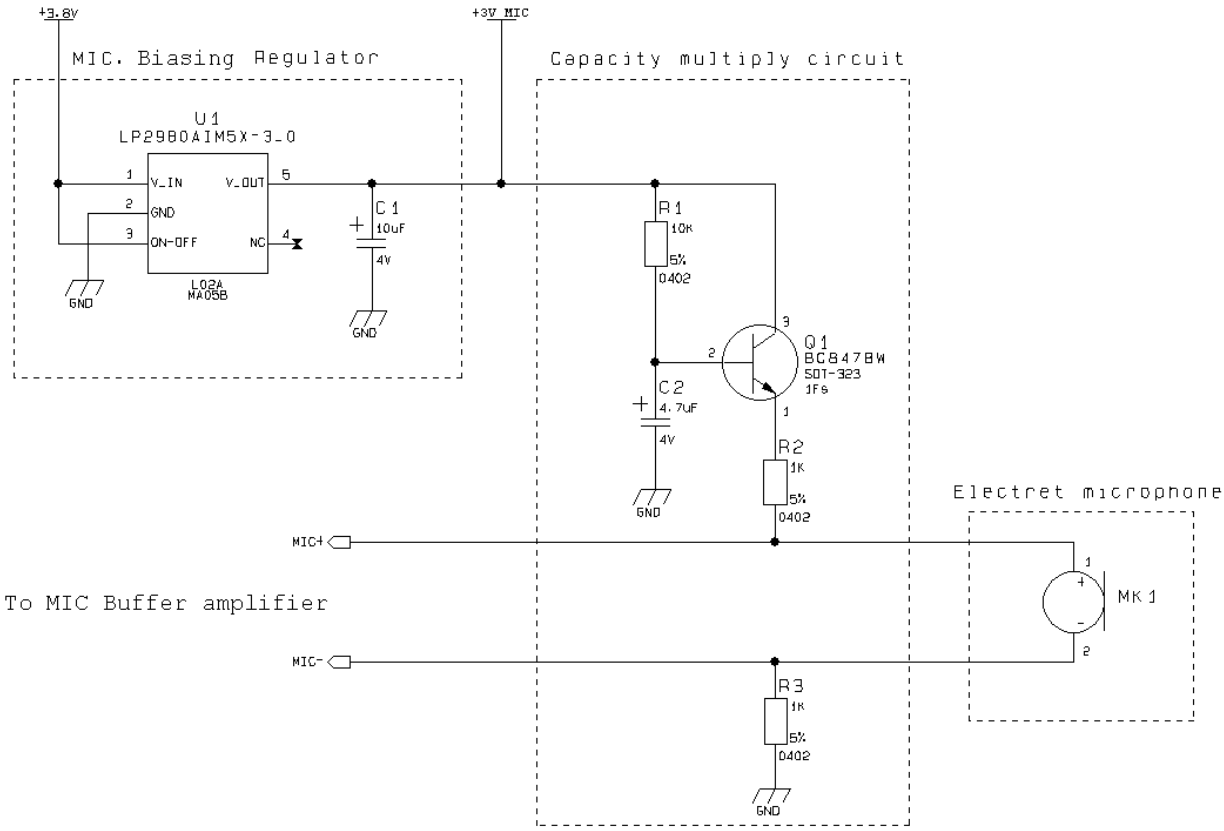
10.4 Microphone Biasing

The electret microphones usually need a biasing voltage to work properly. Refer to your microphone provider for the characteristics required.

NOTE: The microphones have a hot wire were the positive biasing must be connected. Usually it is indicated by a + symbol or a red point. If the polarity of the bias is reversed, then the microphone will not work properly. For this reason be sure to respect the mic. biasing polarity.

10.4.1 Balanced Microphone Biasing

The balanced microphone bias voltage should be obtained from a dedicated voltage regulator, in order to eliminate the noise present on the power lines. This regulator can be the same for all the audio paths. The microphone should be supplied from a capacitor multiply circuit.
For example a circuit for the balanced microphone biasing can be:



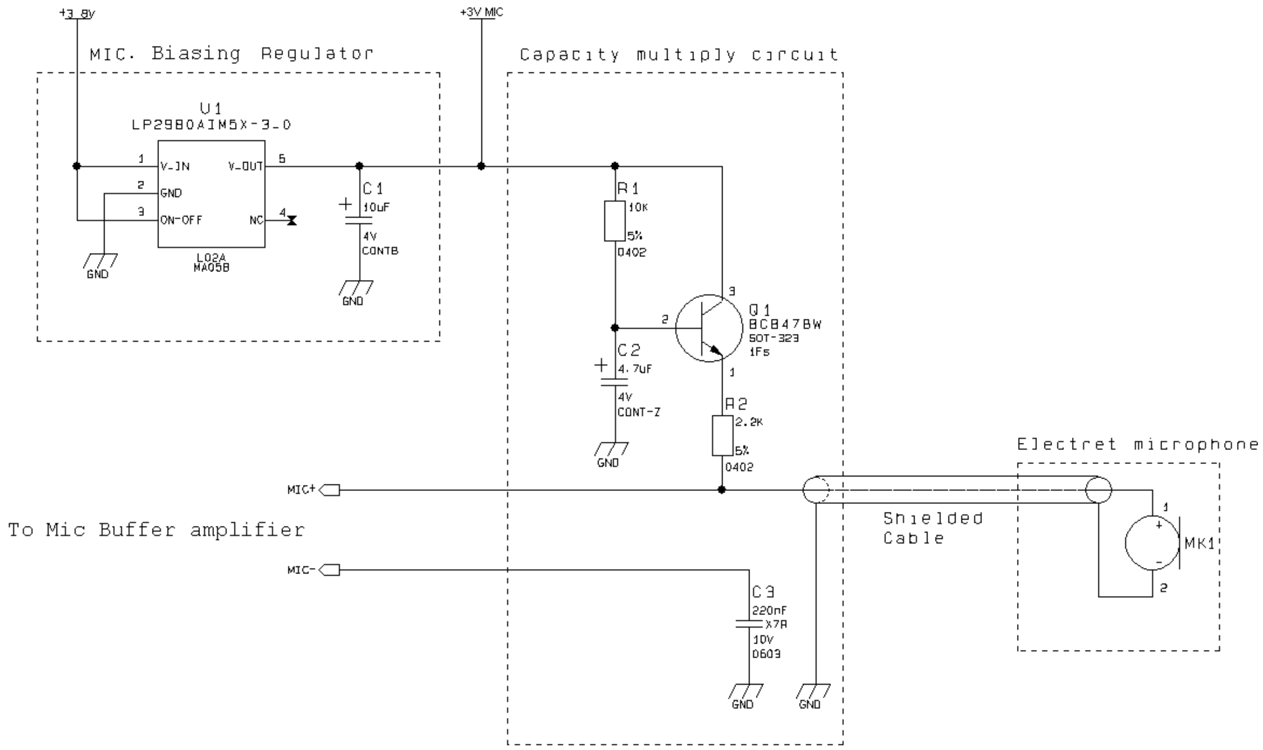
NOTE: In the balanced application the resistors R2 and R3 must have the same value to keep the circuit balanced.

NOTE: The cable to the microphone should not be shielded, instead a twisted pair cable shall be used.

NOTE: The microphone sensitivity changes with the value of R2 and R3. Usually the microphones are characterized with 2kΩ biasing resistance, so try to keep the sum of R2 and R3 around 2kΩ. Refer to your microphone manufacturer for the mic. characteristics.

10.4.2 Unbalanced Microphone Biasing

The unbalanced microphone biasing voltage should be obtained from a dedicated voltage regulator, in order to eliminate the noise present on the power lines. This regulator can be the same for all the audio paths. The microphone should be supplied from a capacitor multiply circuit.
For example a circuit for the unbalanced microphone biasing can be:



NOTE: In the unbalanced application the capacitor C3 shall be > 200nF otherwise the frequency response will be cut at low band frequencies (down to 300Hz). This capacitor can be placed close to the MIC- pad (MIC_HF- or MIC_MT- depending on the audio path chosen) or if possible it should be placed close to the shielded cable connector. If the ground return path is well designed, then it is possible to eliminate the C3 capacitor, provided the buffer is close to the mic. input.

NOTE: The cable to the microphone should be shielded.

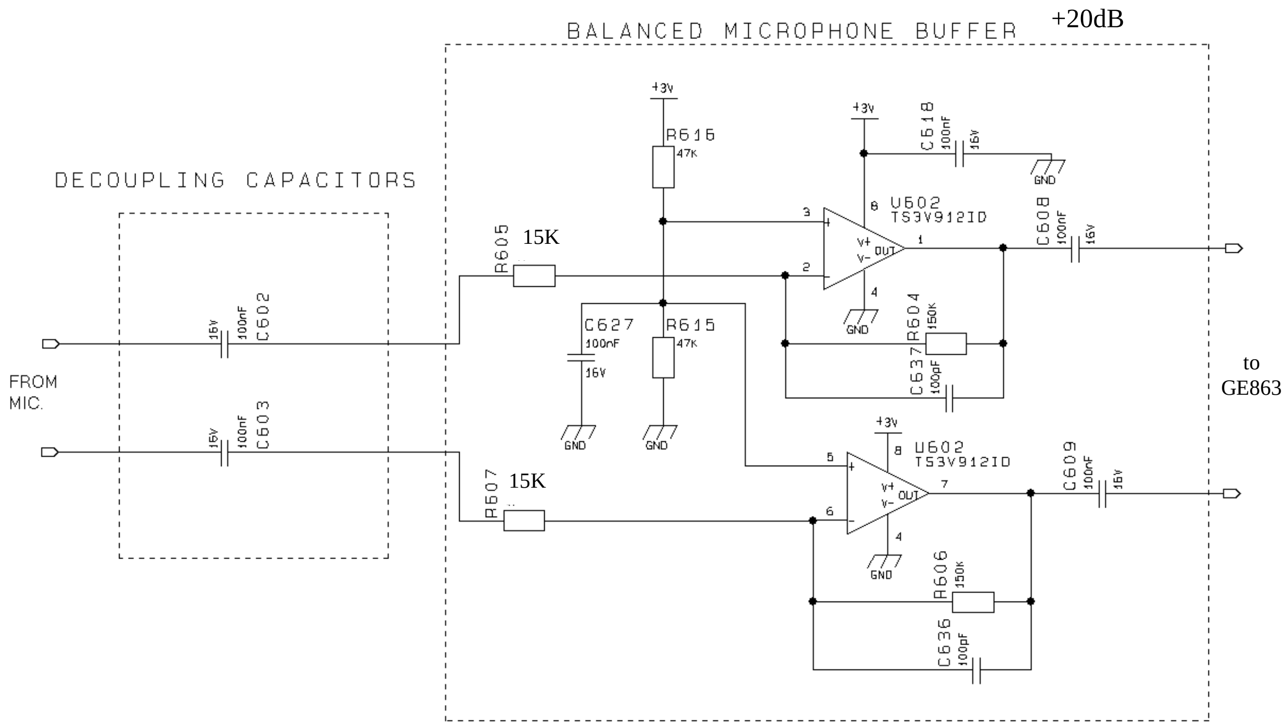
NOTE: The microphone changes with the value of R2. Usually the microphone sensitivity is characterized with 2kΩ biasing resistance, so try to keep the value of R2 around 2kΩ. For mic. characteristics refer to the manufacturer.

10.5 Microphone Buffering

As seen previously, a microphone shall be connected to the input pins of UC864-G through a buffer amplifier that boosts the signal level to the required value.
Again the buffered microphone circuitry can be balanced or unbalanced: where possible it is always preferable a balanced solution. The buffering circuit shall be placed close to the microphone or close to the microphone wire connector.

10.5.1 Buffered Balanced Mic

A sample circuit can be:



This circuit has a gain of 10 times (+20 dB), and is therefore suited for the "***Mic_MT*** " input if you have a microphone with a sensitivity close to the suggested one *(-45 dBV_{rms}/Pa)*. If your microphone has a different sensitivity or if the buffer is connected to the "***Mic_HF*** " inputs, then a gain adjustment shall be done by changing resistors R604 and R606 (if the required value is not a standard one , you can change R605 and R607) and as a consequence the capacitors C636 and C637 to maintain the bandwidth 150-4000Hz (at -3dB).

The buffer gain is given by the formula:

$$Gain = \frac{R604}{R605} = \frac{R606}{R607}$$

The C636 and C637 capacitors are placed in order to cut off the gain at higher frequencies than the transmitted GSM band, the cutoff frequency (-3dB) should be 3500Hz in order to have -1dB at 3kHz.
The cutoff frequency is given by the formula:

$$freq. = \frac{1}{2\pi * R604 * C637} = \frac{1}{2\pi * R606 * C636} \text{ [Hz]}$$

TIP: Example of calculation

*Let's assume you have a microphone with a sensitivity of -45 dBV_{rms}/Pa and you want to use it in 1st differential microphone path (“**Mic_MT**” inputs) in “normal spoken" conditions at acoustic pressure of -4.7dBPa.*
As reported at page 33, the electrical level output from the microphone will be:

MicLevel = (-45) + (-4.7) = -49.7 dB_{Vrms}

corresponding to:

MicVoltage = $10^{(-49.7/20)}$ = 3.3 10^{-3} V_{rms}*

*When the talker is screaming ,we will have a signal of 330 mV_{rms} on the “**Mic_MT**“ inputs due to a 20dB higher Mic Level (see TIP 1) with a buffer gain G_A :*

G_A** =20 log (AmplifierOutput / MicVoltage) =20 log (330 * 10^{-3})/(33 * 10^{-3}) = 20 log 10=**20dB

The corresponding values for the resistors on the buffer could be (if we keep the input resistance 10kΩ)

R604 = R606 = gain R607= gain* R605 = 10* 15 = 150 kΩ*

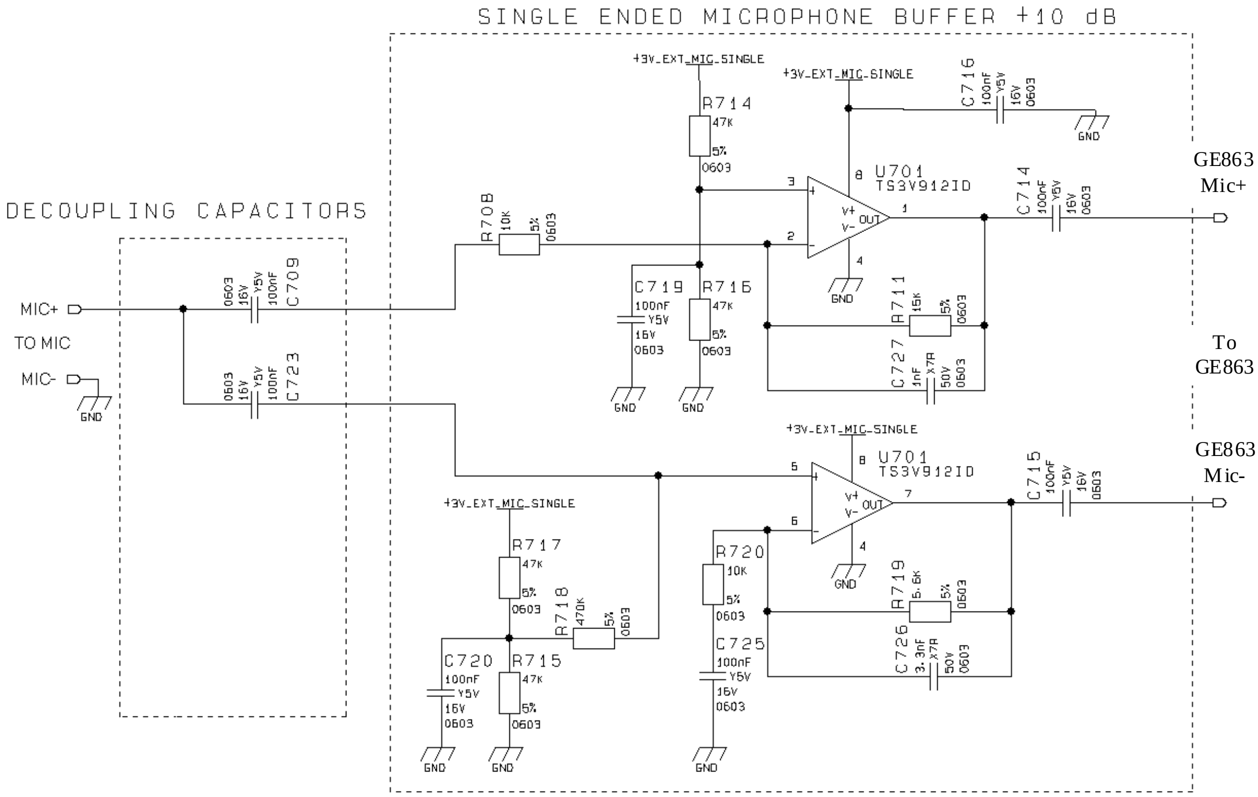
The commercial values of 150kΩ & 15kΩ are then chosen.

As a consequence the values of the capacitors C636 and C637 shall be:

*C636=C637= 1/ (2π*4000*R606)= 265 *10^{-12} F*

A commercial value of 270pF gives a cutoff frequency of 3931Hz with an errorless than 1,8% .

10.5.2 Buffered Unbalanced (Single Ended) Microphone



The above schematic can be used for a single ended (*buffered unbalanced*) microphone; the required biasing circuitry is not included. Note also that the capacitor C3 is not needed
The gains of the two amplifiers are given by the formulas:

$$Gain(\text{not inverting buffer}) = 1 + \frac{R719}{R720} \qquad Gain(\text{inverting buffer}) = \frac{R711}{R708}$$

Assigning half of overall gain to each amplifier, you will obtain the requested gain because of doubling the microphone signal path; in fact by the use of two amplifiers (the upper as “inverting” and the lower as “not inverting” configuration) we obtain an additional +6dB gain (2 times).

Remember: the “not inverting “amplifier section gain shall not be less than 1.
Like for the balanced buffered microphone, the amplifier overall gain can be modify changing the value of resistor R719/R720 and R711 and as a consequence the capacitors C726 and C727. It is advisable to change R708 only if you have difficulty to find a commercial value for R711; in this case change R708 as little as possible.

The -3dB bandwidth is given by the approximated formula (considering C725 >> C726):

$$freq. = \frac{1}{2\pi * R719 * C726} = \frac{1}{2\pi * R711 * C727} \text{ [Hz]}$$

The buffer bandwidth at -3dB shall be 4KHz.
Note that the biasing of the operational amplifier is given for the inverting amplifier by the series divider R714-R715. The 100nF capacitor C719 is needed to filter the noise that could be coupled to that divider. For the not inverting operational amplifier the biasing is given by a different divider R715-R717 with the capacitor C720 and through a series resistor R718 of 470KΩ.

TIP: Example of calculation.

*Llet's assume you have a microphone with a sensitivity of -45dBV$_{rms}$/Pa and you want to use it in 2nd differential microphone path (“**Mic_HF**” inputs) in "normal spoken" conditions at acoustic pressure of -4.7dBPa.*
As reported at page XX,, the electrical level output from the microphone will be :

MicLevel = (-45) + (-4.7) = -49.7 dBV$_{rms}$

but we have to consider 20dB loss due to the higher distance from the mouth of the talker (50cm) .

MicLevel = (-49.7) + (-20) = -69.7 dBV$_{rms}$

corresponding to *MicVoltage = $10^{(-69.7/20)}$ = 0,33* 10^{-3}*

*In order to have a signal of 1 mV$_{rms}$ at the **“Mic_HF”** inputs , as suggested at **TIP** “**environment consideration** “,*

the buffer must have a gain ***G$_A$**= “**Mic_HF** /MicVoltage = (1*10^{-3})/(0,33*10^{-3})=3* *or +10 dB*

*Keeping in mind that “balancing the line will double the signal”, to calculate the resistor values assign half of required gain **G$_A$** to each amplifier section . And therefore, **G$_S$** =1,5times (or +3,52dB).*

Choosing as 10kΩ as the input resistance, the corresponding values for the resistors on the buffer will be:

R711** = **G$_S$** * R708= 1.5*10 =**15 kΩ

R719** = (**G$_S$** -1) * R720 = (1.5 -1)*10 =**5 kΩ

*The commercial values of **15kΩ** and **5.6kΩ** be accepted.*
As a consequence of the assigned values of the resistors, the nominal values of C726 and C727 are:

$$C726 = 1/(2\pi * 4000 * R719) = 7.10 * 10^{-9}\ F$$

$$C727 = 1/(2\pi * 4000 * R711) = 2,65 * 10^{-9}\ F$$

*modified in **6,8nF** (f_{c1}=4181Hz) and **2,7nF** (f_{c2}=3931Hz) because of commercial values .*

11 OUTPUT LINES (Speaker)

11.1 Short description

The Telit UC864-G provides two audio paths in receive section. Only one of the two paths can be active at a time, selectable by *AXE* hardware line or by AT command.

You must keep in mind the different audio characteristics of the receive blocks when designing:

→ the *"**Ear_MT**"* lines *EPN1* and *EPP1* are the *Differential Line-Out Drivers* ; they can drive an external amplifier or directly a ***32 Ω earpiece*** at –12dBFS (*) ;
→ the "***Ear_HF***" lines *EPPA1_2* and *EPPA2* are the *Fully Differential Power Buffers ;* they can directly drive a *32**Ω** speaker* in differential (*balanced*) or single ended (*unbalanced*) operation mode .

(*) *FS*: acronym of *Full Scale.* It is equal to 0dB, the maximum Hardware Analog Receive Gain of BaseBand Chip.

The *"**Ear_MT**"* audio path should be used for handset function, while the "***Ear_HF***" audio path is suited for hands-free function (car kit).

Both receiver outputs are B.T.L. type (Bridged Tie Load) and the OEM circuitry shall be designed bridged to reduce the common mode noise typically generated on the ground plane and to get the maximum power output from the device; however also a single ended circuitry can be designed for particular OEM application needs.

11.2 Output Lines Characteristics

UC864-G;

"Ear_MT" <u>Differential output path</u>

• line coupling:	DC
• line type:	differential
• output load resistance :	32 Ω
• max. load capacitance	500pF(max.)
• differential output impedance:	1 Ω (max) @1.02KHz
• signal bandwidth:	150 - 4000 Hz @ -3 dB
• differential output voltage	1060mV_{rms} (typ.)@0dBm0
• SW volume level step	-2dB
• number of SW volume steps	10

"Ear_HF" <u>differential output</u> path

• line coupling:	DC
• line type:	differential
• output load resistance :	32 Ω
• max. load capacitance	500pF(max.)
• differential output impedance:	1 Ω (max) @1.02KHz
• signal bandwidth:	150 - 4000 Hz @ -3 dB
• differential output voltage	833 mV_{rms} (typ,)@0dBm0
• SW volume level step	-2dB
• number of SW volume steps	10

11.3 General Design Rules

There are several configurations for the audio output path, but the various design requirements can be grouped into three different categories:

- handset earphone (low power, typically a handset)
- hands-free earphone (low power, typically a earphone)
- car kit speakerphone (high power, typically a speaker)

The three groups have different power requirements; usually the first two applications need only few mW of power, which can be directly drained from the UC864-G pads, provided a suited speaker is used. This direct connect design is the cheaper and simpler solution and will be suited for the most of the earphone design requirements. There's no need to decouple the output ear lines if a suited earpiece is connected. For the last group, the speakerphone, a power amplifier is required to raise the output power up to 5-10W required in a car cabin application.
All the designs shall comply with the following guidelines:

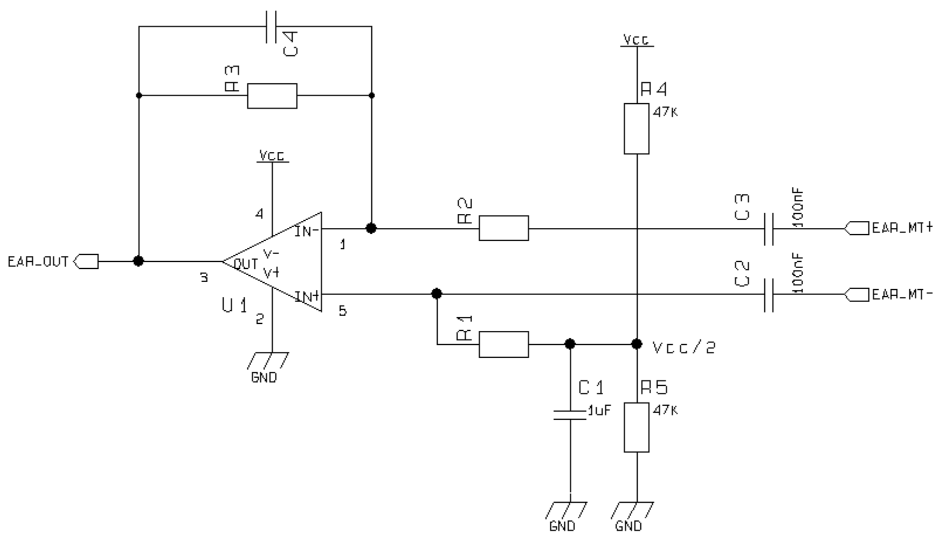
- Where possible use a bridged earphone circuitry, to achieve the maximum power output from the device.
- Keep the earphone traces on the PCB and wires as short as possible.
- If your application requires a single ended earpiece and you want a direct connection, then leave one of the two output lines open and use only the other referred to ground. Remember that in this case the power output is 4 times lower than the bridged circuit and may not be enough to ensure a good voice volume.
- Make sure that the earphone traces in the PCB don't cross or run parallel to noisy traces (especially the power line)
- The cable to the speaker shall be a twisted pair with both the lines floating for the bridged output type, shielded with the shield to ground for the single ended output type.

11.3.1 Noise Filtering

The I/O of the PCB should have a noise filter close to the connector, to filter the high frequency GSM noise. The filter can be a Π formed by 2 capacitor and a inductance, with the one capacitor of 39pF - *0603* case, and the other capacitor of *1nF - 0603*; the inductance shall have a value of *39μH*.

11.4 Handset Earphone Design

As seen previously, a 32Ω earpiece can be directly connected to the output pads EAR_MT+ and EAR_MT- of the *UC864-G*.
This solution is often the more cost effective, reducing the components count to a minimum. There are several limitations to the use of this solution: speaker direct connect imposes the speaker characteristics to be almost exactly the suggested ones, otherwise the power output may be reduced (if speaker impedance is bigger than 32Ω) or the *UC864-G* ear port may be damaged (if speaker impedance is less than 15Ω).
The other limitation of the speaker direct connection is the power output capability of the *UC864-G* which is limited and for some particular applications may not be enough.
For these reasons, when the power output of the *UC864-G* is not enough or if the speaker characteristics are different from the suggested, then it is preferable to use an amplifier to increase the power and current output capabilities.
Again the output from the *UC864-G* is bridged and both lines should be used, where possible, as inputs to the power amplifier. This ensures a higher common mode rejection ratio, reducing the GSM current busts noise on the speaker output.
In this case the "***EAR_MT***" lines from the *UC864-G* should be AC coupled with a ceramic capacitor of 100nF (or bigger).
It is always desirable to have a mute control on the amplifier, in order to turn it off while the device is not sending signal to the output, in this manner the amplifier background noise which may be audible during idle conditions is cut off.
A principle schematic may be:

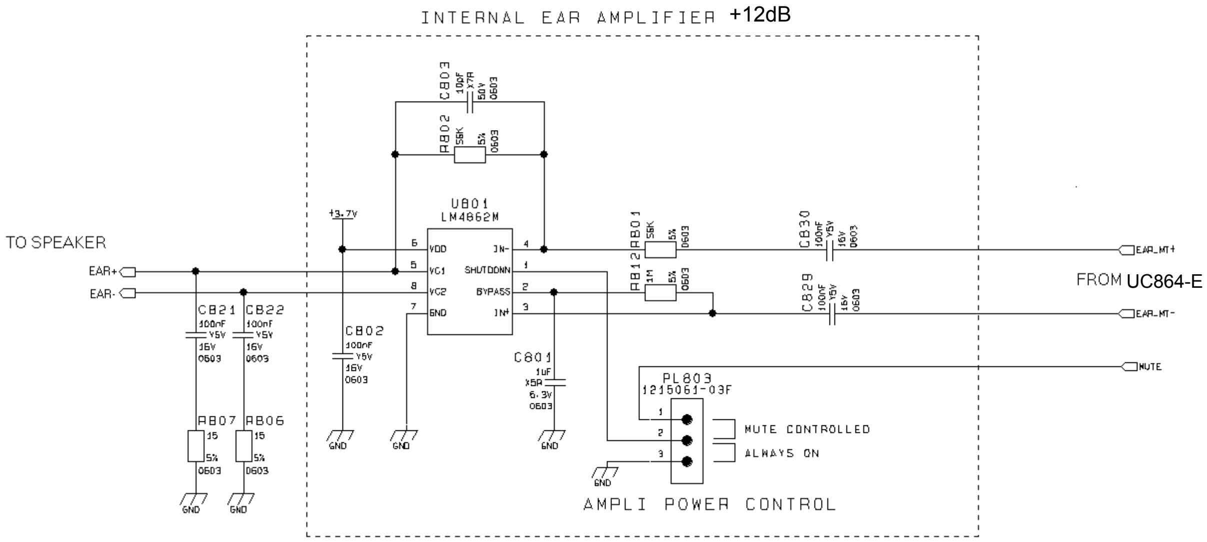


The resulting gain and high pass cut can be obtained with the formula:

$$Gain = \frac{R3}{R2}$$

$$freq. = \frac{1}{2\pi * R3 * C4} \text{ [Hz]}$$

And an example of internal Ear amplifier could be:



Some amplifier require a low impedance load at high frequency in order to avoid auto oscillation, this can be made with a capacitor (1*00nF*) in series with a resistor (*15Ω*).

When designing your application, remember to provide an adequate bypass capacitor to the amplifier and place it close to the power input pin of the IC, keeping the traces as short as possible.

11.5 Hands-Free Earphone (Low Power) Design

The same design considerations made for the handset are valid for the hands-free earphone.

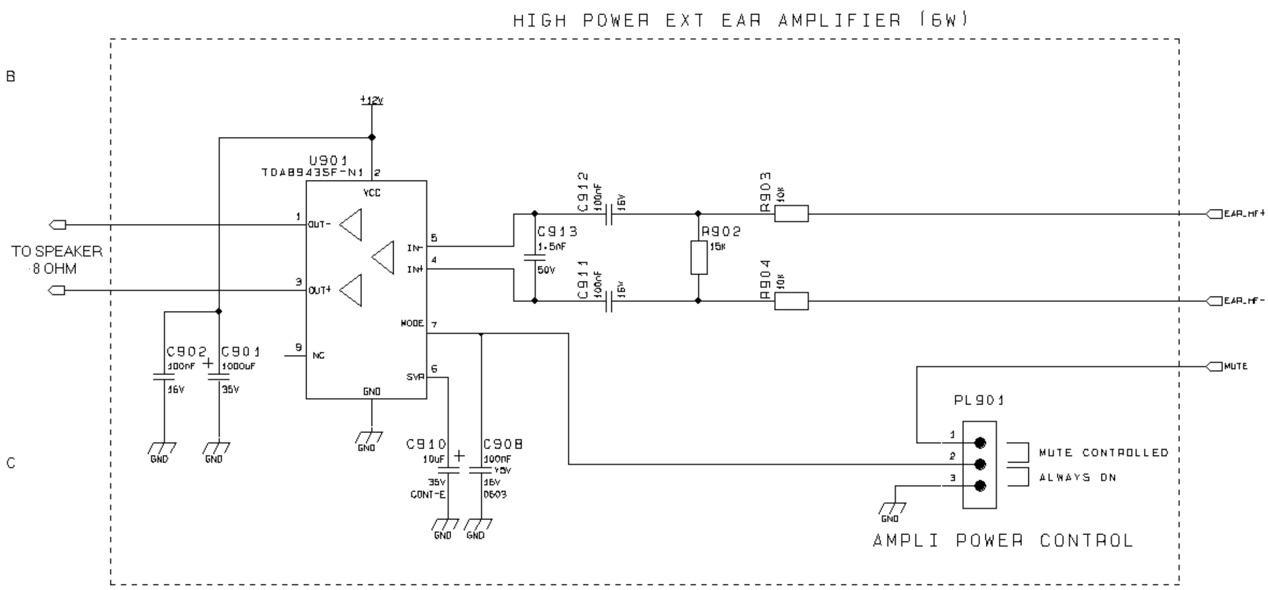
11.6 Car Kit Speakerphone Design

For the car kit speaker phone function the power output requirement is usually at least 4W, therefore an amplifier is needed to boost the *UC864-G* output.
The design of the amplifier shall comply with the following guidelines:

- The input to the amplifier MUST be taken from the "***Ear_HF***" audio path of *UC864-G*, because of its echo canceller parameters suited to a car cabin use.
- The amplifier shall have a gain of 30-40 times (29-32 dB) to provide the desired output power of 5-10W with the signal from the *UC864-G* "***Ear_HF***" audio output lines.
- If the amplifier has a fixed gain then it can be adjusted to the desired value by reducing the input signal with a resistor divider network.
- The amplifier shall have a mute control to be used while not in conversation. This provides two benefits: eliminating the background noise when not in conversation and saving power.
- The power to the amplifier should be decoupled as much as possible from the *UC864-G* power supply, by either keeping separate wires and placing bypass capacitors of adequate value close to the amplifier power input pads.
- The biasing voltage of the amplifier shall be stabilized with a low ESR (e.g. a tantalum) capacitor of adequate value.

NOTE: The UC864-G audio path connected to the car kit hands-free amplifier MUST be "Ear_HF" one, otherwise the echo cancellation will not be done due to the difference in the echo canceller characteristics of the UC864-G internal audio path from the external audio path.

Example of car kit amplifier schematic



12 General Purpose I/O

The general-purpose I/O pads can be configured to act in three different ways:

- Input
- Output
- Alternate function (internally controlled)

Input pads can only be read and report the digital value (high or low) present on the pad at the read time; output pads can only be written or queried and set the value of the pad output; an alternate function pad is internally controlled by the UC864-G firmware and acts depending on the function implemented.

Not all GPIO pads support all these three modes:

- GPIO5 supports all three modes and can be input, output, RFTX monitor output (Alternate function)
- GPIO6 supports all three modes and can be input, output, alarm output (Alternate function)
- GPIO7 supports all three modes and can be input, output, buzzer output (Alternate function)

Some alternate functions for UC864-G may be added later on

12.1 Logic level specifications

Where not specifically stated, all the interface circuits work at 2.6V CMOS logic levels.
The following table shows the logic level specifications used in the UC864-G interface circuits:

Absolute Maximum Ratings -Not Functional

Parameter	UC864-G	
	Min	Max
Input level on any digital pin when on	-0.3V	+3.0V
Input voltage on analog pins when on	-0.3V	+3.0 V

For 2.6V CMOS signals;

Operating Range - Interface levels

Level	UC864-G	
	Min	Max
Input high level	2.0V	2.9 V
Input low level	-0.3V	0.6V
Output high level	2.2V	2.6V
Output low level	0V	0.35V

For 2,0V signals:

Operating Range - Interface levels (2.0V CMOS)

Level	UC864-G	
	Min	Max
Input high level	1.5V	2.1V
Input low level	-0.3V	0.5V
Output high level	1.4V	1.8V
Output low level	0V	0.35V

12.2 Using a GPIO Pad as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 2.6V CMOS levels of the GPIO.
NOTE: If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 2.6V CMOS, it can be buffered with an open collector transistor, provided a 47KΩ pull-up resistor is connected as seen in the paragraph 8.3

12.3 Using a GPIO Pad as OUTPUT

The GPIO pads, when used as outputs, can drive 2.6V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

12.4 Using the RFTXMON Output GPIO5

The GPIO5 pin, when configured as RFTXMON Output, is controlled by the UC864-G module and will rise when the transmitter is active and fall after the transmitter activity is completed.
For example, if a call is started, the line will be HIGH during all the conversation and it will be again LOW after hanged up.
The line rises up 300ms before first TX burst and will become again LOW from 500ms to 1sec after last TX burst.

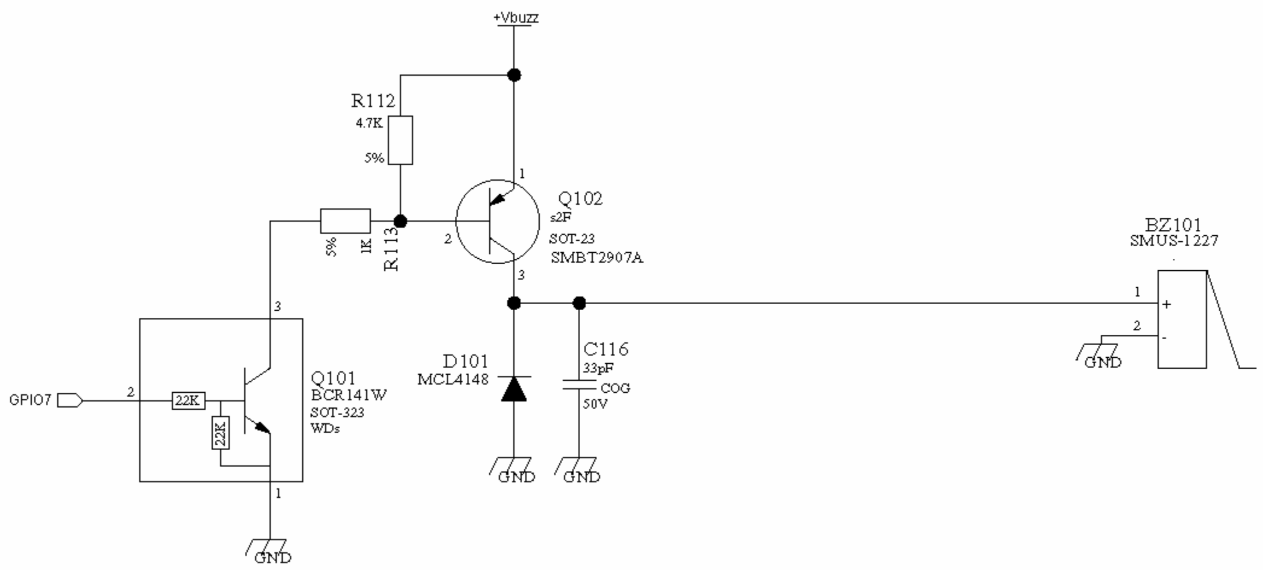
12.5 Using the Alarm Output GPIO6

The GPIO6 pad, when configured as Alarm Output, is controlled by the UC864-G module and will rise when the alarm starts and fall after the issue of a dedicated AT command.
This output can be used to power up the UC864-G controlling microcontroller or application at the alarm time, giving you the possibility to program a timely system wake-up to achieve some periodic actions and completely turn off either the application and the UC864-G during sleep periods, dramatically reducing the sleep consumption to few μA.
In battery-powered devices this feature will greatly improve the autonomy of the device.

NOTE: During RESET the line is set to HIGH logic level.

12.6 Using the Buzzer Output GPIO7

The GPIO7 pad, when configured as Buzzer Output, is controlled by the UC864-G module and will drive with appropriate square waves a Buzzer driver.
This permits to your application to easily implement Buzzer feature with ringing tones or melody played at the call incoming, tone playing on SMS incoming or simply playing a tone or melody when needed by your application.



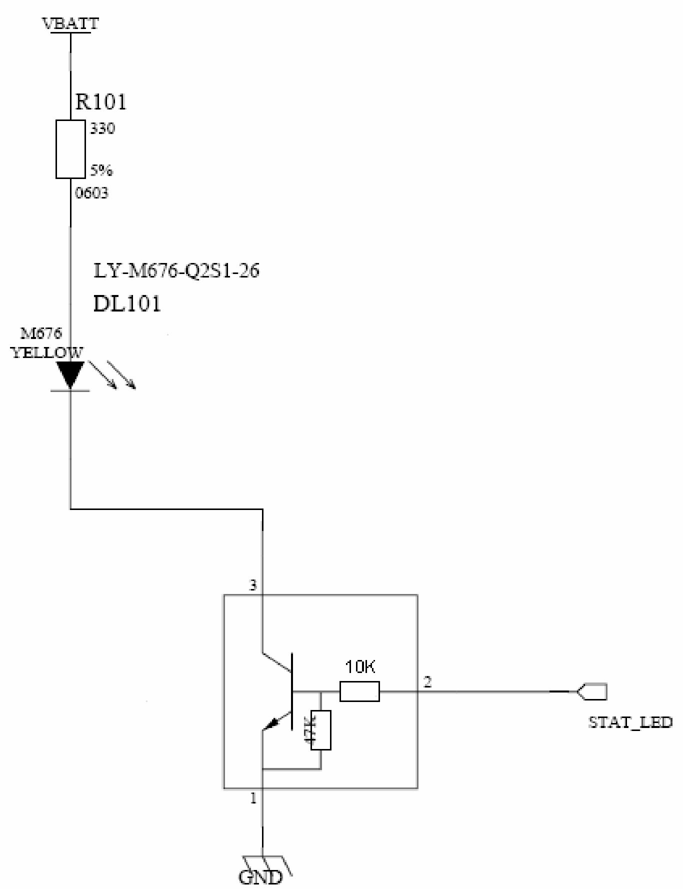
A sample interface scheme is included below to give you an idea of how to interface a Buzzer to the GPIO7:

NOTE: To correctly drive a buzzer a driver must be provided, its characteristics depend on the Buzzer and for them refer to your buzzer vendor.

12.7 Indication of network service availability

The STAT_LED pin status shows information on the network service availability and Call status.
In the UC864-G modules, the STAT_LED usually needs an external transistor to drive an external LED.
Therefore, the status indicated in the following table is reversed with respect to the pin status.

LED status	Device Status
Permanently off	Device off
Fast blinking (Period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (Period 3s, Ton 0,3s)	Registered full service
Permanently on	a call is active



12.8 RTC Bypass out

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing having only RTC going on when all the other parts of the device are off.
To this power output a backup capacitor can be added in order to increase the RTC autonomy during power off of the battery.
NOTE: NO Devices must be powered from this pin.

12.9 VAUX1 power output

A regulated power supply output is provided in order to supply small devices from the module.
This output is active when the module is ON and goes OFF when the module is shut down.
The operating range characteristics of the supply are:

Operating Range – VAUX1 power supply

	Min	Typical	Max
Output voltage	2.75V	2.85V	2.95V
Output current			100mA
Output bypass capacitor			2.2μF

13 DAC and ADC section

13.1 DAC Converter(TBD)

13.1.1 Description

The UC864-G module provides a Digital to Analog Converter. The signal (named DAC_OUT) is available on pin 40 of the UC864-G module and on pin 17 of PL102 on EVK2 Board (CS1203).
The on board DAC is a 16-bit converter, able to generate a analogue value based a specific input in the range from 0 up to 65535. However, an external low-pass filter is necessary

	Min	**Max**	**Units**
Voltage range (filtered)	0	2,6	Volt
Range	0	65535	Steps

The precision is 16 bits so, if we consider that the maximum voltage is 2V, the integrated voltage could be calculated with the following formula:

Integrated output voltage = 2 * value / 65535

DAC_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.

13.1.2 Enabling DAC

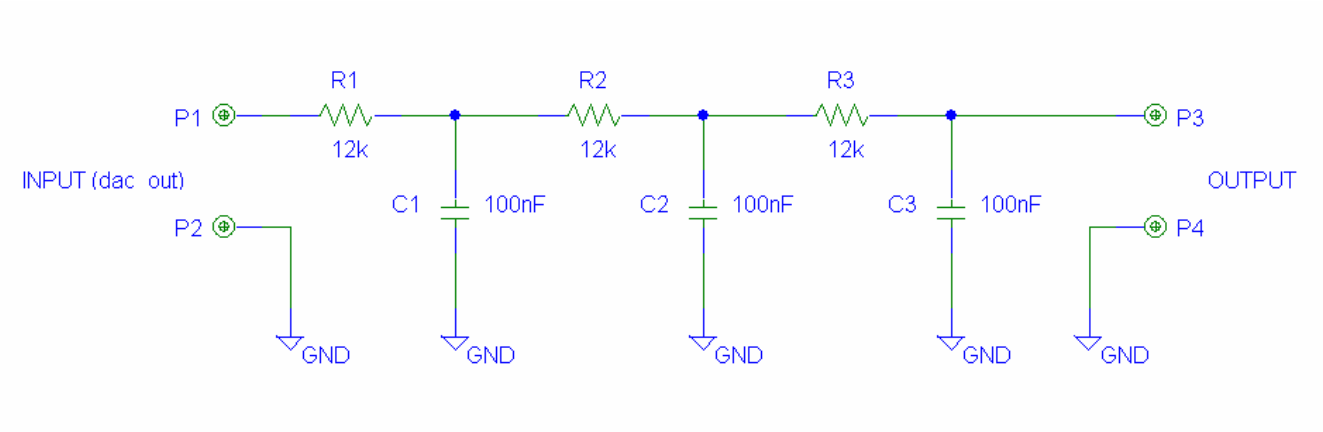
An AT command is available to use the DAC function.
The command is **AT#DAC[=<enable>[,<value>]]**

<value> - scale factor of the integrated output voltage (0..65535 - 16 bit precision)
it must be present if **<enable>=1**

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

NOTE: **The DAC frequency is selected internally. D/A converter must not be used during POWERSAVING.**

13.1.1 Low Pass Filter Example



13.2 ADC Converter

13.2.1 Description

The on board ADCs are 8-bit converters. They are able to read a voltage level in the range of 0-2.6 volts applied on the ADC pin input, store and convert it into 8 bit word.

	Min	Max	Units
Input Voltage range	0	2.6	Volt
AD conversion	-	8	bits
Resolution	-	<11	mV

The UC864-G module provides 3 Analog to Digital Converters. The input lines are:

ADC_IN1 available on Pin 37 and Pin 19 of PL102 on EVK2 Board (CS1203).
ADC_IN2 available on Pin 38 and Pin 20 of PL102 on EVK2 Board (CS1203).
ADC_IN3 available on Pin 39 and Pin 21 of PL102 on EVK2 Board (CS1203).

13.2.2 Using ADC Converter

An AT command is available to use the ADC function.

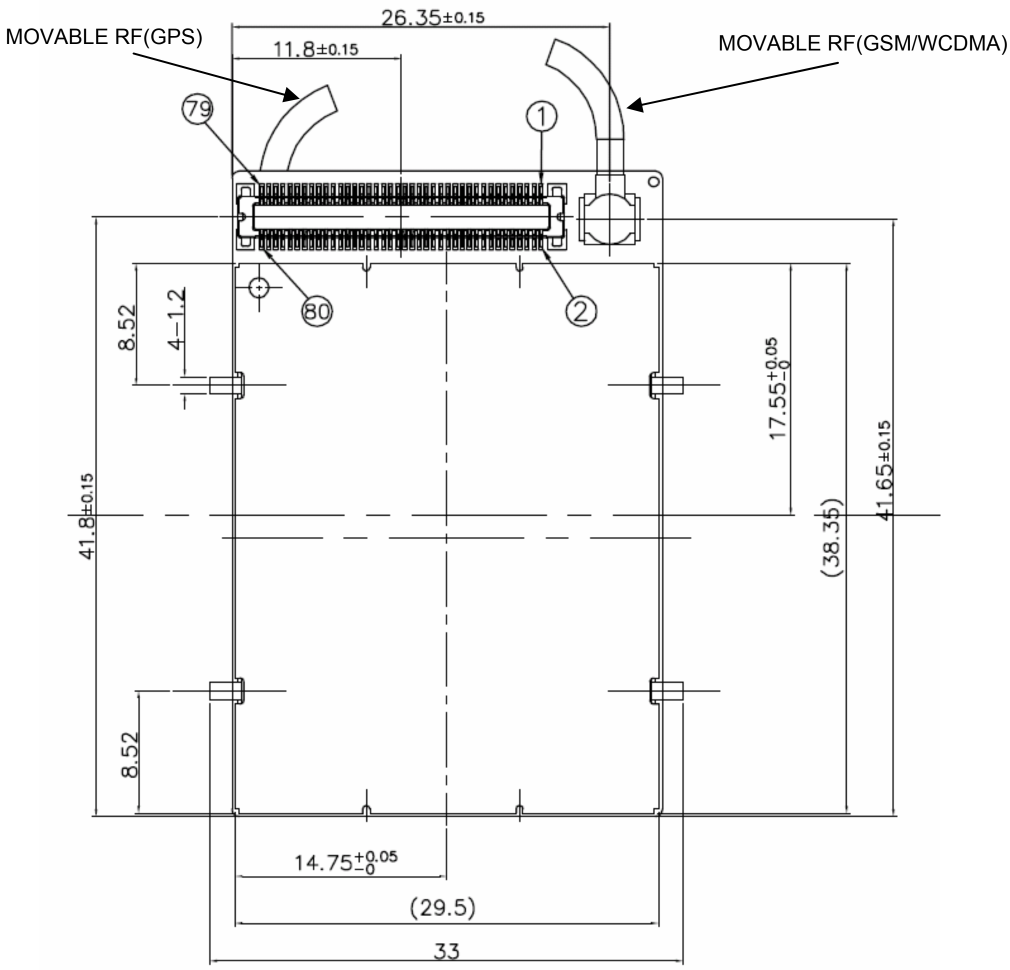
The command is **AT#ADC=1,2**

The read value is expressed in mV

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

13.3 Mounting UC864-G on your board

The position of the Molex board to board connector and the pin 1 are shown in the following picture.



NOTE: metal tabs present on UC864-G should be connected to GND

13.3.1 Debug of the UC864-G in production

To test and debug the mounting of the UC864-G, we strongly recommend to foreseen test pads on the host PCB, in order to check the connection between the UC864-G itself and the application and to test the performance of the module connecting it with an external computer. Depending by the customer application, these pads include, but are not limited to the following signals:

- TXD
- RXD
- ON/OFF
- RESET
- GND
- VBATT
- TX_TRACE
- RX_TRACE
- PWRMON

14 Document Change Log

Revision	Date	Changes
DRAFT	29/10/07	

Regulatory Notices

This device is compliant with Parts 15, 22 and 24 of the FCC Rules.
Operation of this device is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operations.