GC864 Hardware User Guide

1vv0300733 Rev.12 – 2010-06-04

Making machines talk.

APPLICABILITY TABLE

PRODUCT
GC864-QUAD
GC864-PY

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Such changes will, nevertheless be incorporated into new editions of this document.

Contents

1. Introduction

1.1. Scope

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit GC864-QUAD / PY module.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our GC864 module.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
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Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

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To register for product news and announcements or for product questions contact Telit's Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Document Organization

This document contains the following chapters:

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "Overview" provides an overview of the document.

Chapter 3: "GC864 Mechanical Dimensions"

Chapter 4: "GC864 Module Connections" deals with the pin out configuration and layout.

Chapter 5: "Hardware Commands" How to control the module via hardware.

Chapter 6: "Power supply" Power supply requirements and general design rules.

Chapter 7: "Antenna" The antenna connection and board layout design are the most important parts in the full product design

Chapter 8: "Logic Level specifications" Specific values adopted in the implementation of logic levels for this module.

Chapter 9: "Serial ports" The serial port on the Telit GC864 is the core of the interface between the module and OEM hardware

Chapter 10: "Audio Section overview" Refers to the audio blocks of the Base Band Chip of the GC864 Telit Modules.

Chapter 11: "General Purpose I/O" How the general purpose I/O pads can be configured.

Chapter 12 "DAC and ADC Section" Deals with these two kind of converters.

Chapter 13: "Mounting the GC864 on the application board" Recommendations and specifics on how to mount the module on the user's board.

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- Telit's GSM/GPRS Family Software User Guide, 1vv0300784
- Audio settings application note , 80000NT10007a
- Digital voice Interface Application Note, 80000NT10004a
- GC864 Product description, 80273ST10008a
- SIM Holder Design Guides, 80000NT10001a
- AT Commands Reference Guide, 80000ST10025a
- Telit EVK2 User Guide, 1vv0300704

1.7. Document History

Revision	Date	Changes
ISSUE#0	2006-06-12	Release First ISSUE# 0
ISSUE #1	2006-09-07	Full Review of the manual Added ADC description Added DAC description Added Pinout and Process flow description Added Packaging
ISSUE #2	2006-10-03	TGPIO23 now RESERVED
ISSUE #3	2006-11-07	3.1 (table on page 12); PWRCTL must be PWRMON
ISSUE #4	2007-02-08	Pinout updated, Camera removed, Added Stat Led and GPIO5 description, added VAUX, schematics updated for On_off, reset, level adapter 5V, RS232 transceiver, Power supply. Modified Charger description.
ISSUE#5	2007-06-07	Updated DISCLAIMER, Added note on charger (CFUN4 and ON_OFF), Added Power consumptions table, Added new table for GPIO status in Reset and Power on, added RFTXMON timing, modified DB9 picture in par 8.2, Switching description modified in "+ 12V input Source Power Supply Design Guidelines", Added Alternate Function for GPIO4.
ISSUE#6	2007-06-21	Updated Absolute maximum ratings, Added Alternate Function for GPIO2; added PWRMON description during ON_OFF, updated chapter
ISSUE#7	2008-05-21	Added GC864-QUAD with SIM holder product p/n Par 3.1: Removed nominal values on Audio, Added DVI pins descriptions Par 5.1: Added Supply Voltage Range Par 10.7: GPIO7 description; added section on Buzzer description Par 9: Audio section removed (a dedicated User guide on audio has been created) Par 5.2.1.4: added note on Charger Par 8.1: tip on RXD pull up added 11.3 added note on reflow not possible 8.3 pull ups referred to VAUX 10.9 Temperature monitor function added 4.2.2 removed table with logic levels 7 removed reference to buffered pins
ISSUE#8	2008-06-30	Added GC864-QUAD with SIM holder drawings (2.1) 4.1 and 4.22 modified example 7 Updated 1.8V CMOS voltage range
ISSUE#9	2009-01-22	Updated operating voltage and P/N list Updated GC864-PY with SIM Holder module in the list of modules concerned by this document Added useful parameters for ATEX Applications Updated Audio Block Diagram
ISSUE#10	2009-08-31	Applied new layout + minor editing Modified idle consumption values Added on/off/reset block diagrams procedures Added DVI info in the pin-out section + notice Added DVI App Note in the related documents list

		Noted in the pin-out section about rts in need of being connected to ground p.18 Updated all schematic drawings Updated Chapter 10 Audio Section
ISSUE#11	2009-12-16	Modified power consumption values Fixed minor adobe acrobat issues
ISSUE#12	2010-06-04	Updated Chapter 7.1 Gain values

2. Overview

In this document all the basic functions of a mobile phone are taken into account; for each one of them a proper hardware solution is suggested and eventually the wrong solutions and common errors to be avoided are evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit GC864-QUAD / PY module. For further hardware details that may not be explained in this document refer to the Telit GC864-QUAD / PY Product Description document where all the hardware information is reported.

NOTICE:

(EN) The integration of the GSM/GPRS GC864-QUAD / PY cellular module within user application shall be done according to the design rules described in this manual.

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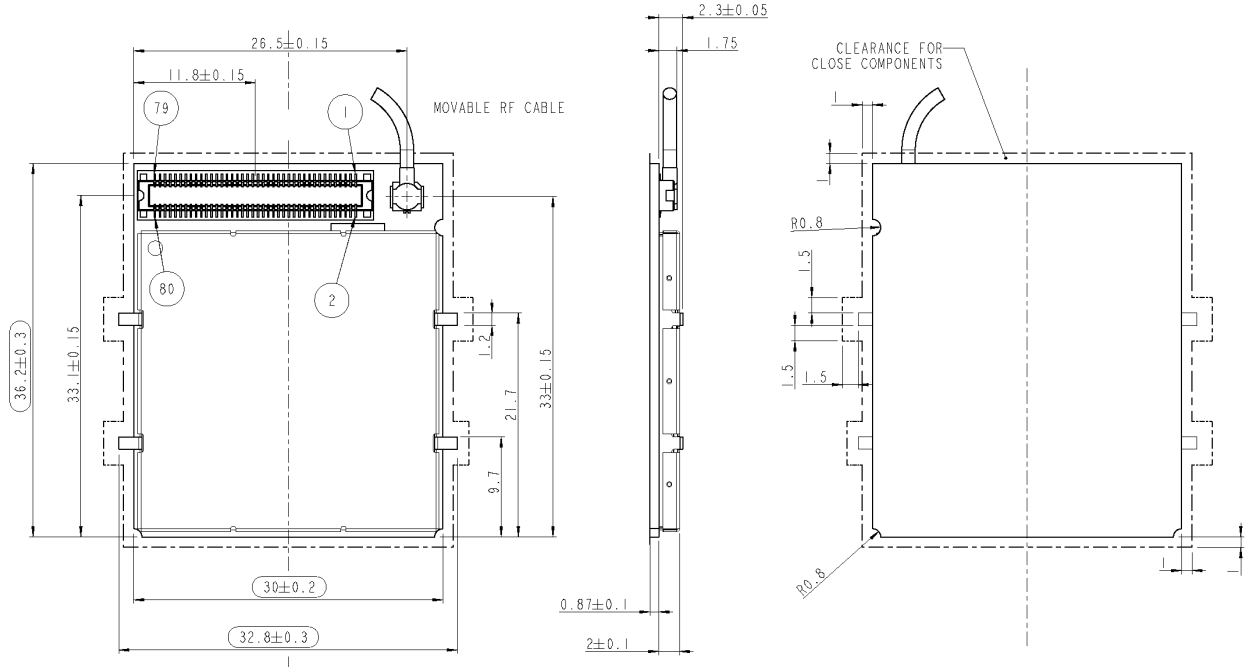
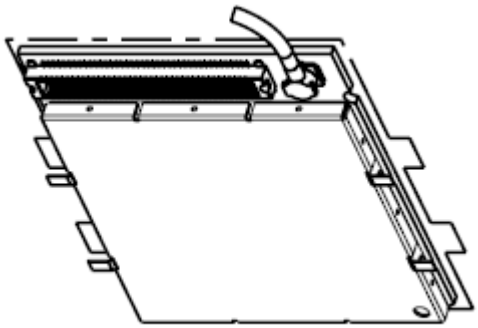
3. GC864 Mechanical Dimensions

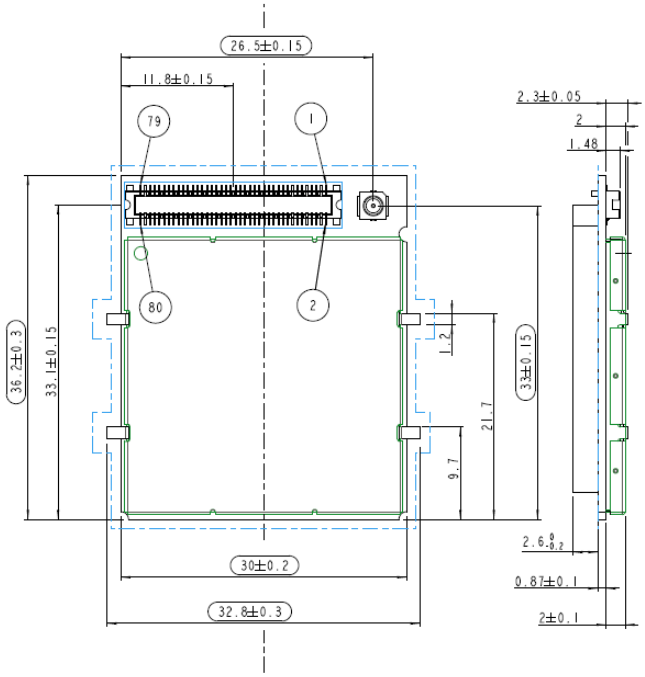
The Telit GC864-QUAD/PY module overall dimensions are:

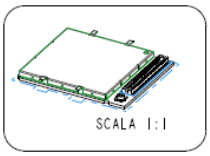
- Length: 36.2 mm
- Width: 30 mm
- Thickness: 3.2 mm

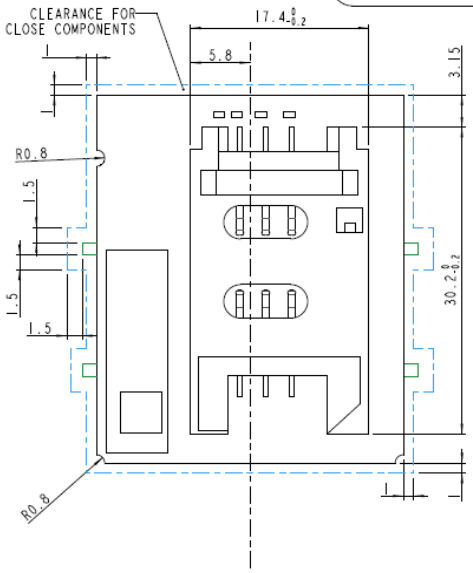




3.1. Mechanical View of Telit GC864-QUAD with SIM Holder







4. GC864-QUAD/PY Module Connections

4.1. PIN-OUT

The GC864-QUAD/PY uses a 80 pin Molex p.n. 53949-0878 male connector for the connections with the external applications. This connector matches the 54150-0878 models.

Pin	Signal	I/O	Function	Internal Pull up	Type
Power Supply					
1	VBATT	-	Main power supply		Power
2	VBATT	-	Main power supply		Power
3	VBATT	-	Main power supply		Power
4	VBATT	-	Main power supply		Power
5	GND	-	Ground		Power
6	GND	-	Ground		Power
7	GND	-	Ground		Power
Audio					
8	AXE	I	Handsfree switching	100KΩ	CMOS 2.8V
9	EAR_HF+	AO	Handsfree ear output, phase +		Audio
10	EAR_HF-	AO	Handsfree ear output, phase -		Audio
11	EAR_MT+	AO	Handset earphone signal output, phase +		Audio
12	EAR_MT-	AO	Handset earphone signal output, phase -		Audio
13	MIC_HF+	AI	Handsfree microphone input; phase		Audio
14	MIC_HF-	AI	Handsfree microphone input; phase		Audio
15	MIC_MT+	AI	Handset microphone signal input; phase+		Audio
16	MIC_MT-	AI	Handset microphone signal input; phase-		Audio
SIM Card Interface					
18[1]	SIMVCC	-	External SIM signal – Power supply for the SIM		1.8 / 3V
19	SIMRST	O	External SIM signal – Reset		1.8 / 3V
20	SIMIO	I/O	External SIM signal - Data I/O		1.8 / 3V
21	SIMIN	I	External SIM signal - Presence (active low)	47KΩ	1.8 / 3V
22	SIMCLK	O	External SIM signal – Clock		1.8 / 3V
Trace					
23	RX_TRACE	I	RX Data for debug monitor/ DVI1_WA (Digital Voice Interface)		CMOS 2.8V
24	TX_TRACE	O	TX Data for debug monitor/ DVI1_CLK (Digital Voice Interface)		CMOS 2.8V
Prog. / Data + Hw Flow Control					

[1] On this line a maximum of 10nF bypass capacitor is allowed

Pin	Signal	I/O	Function	Internal Pull up	Type
25	C103/TXD	I	Serial data input (TXD) from DTE		CMOS 2.8V
26	C104/RXD	O	Serial data output to DTE		CMOS 2.8V
27	C107/DSR	O	Output for Data set ready signal (DSR) to DTE/ DVI1_RX (Digital Voice Interface)		CMOS 2.8V
28	C106/CTS	O	Output for Clear to send signal (CTS) to DTE		CMOS 2.8V
29	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE		CMOS 2.8V
30	C125/RING	O	Output for Ring indicator signal (RI) to DTE		CMOS 2.8V
31	C105/RTS	I	Input for Request to send signal (RTS) from DTE		CMOS 2.8V
32	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE		CMOS 2.8V
DAC and ADC					
37	ADC_IN1	AI	Analog/Digital converter input		A/D
38	ADC_IN2	AI	Analog/Digital converter input		A/D
39	ADC_IN3	AI	Analog/Digital converter input		A/D
40	DAC_OUT	AO	Digital/Analog converter output		D/A
Miscellaneous Functions					
45	STAT_LED	O	Status indicator led		CMOS 1.8V
46	GND	-	Ground		Ground
49	PWRMON	O	Power ON Monitor		CMOS 2.8V
50	VAUX1	-	Power output for external accessories		-
51	CHARGE	AI	Charger input		Power
52	CHARGE	AI	Charger input		Power
53	ON/OFF*	I	Input command for switching power ON or OFF (toggle command). The pulse to be sent to the GC864-QUAD/PY must be equal or greater than 1 second.	47KΩ	Pull up to VBATT
54	RESET*	I	Reset input		
55	VRTC	AO	VRTC Backup capacitor		Power
36	DVI2_CLK	-	Digital Voice Interface Clock	4.7KΩ	CMOS 2.8V
Telit GPIO					
56	TGPIO_19	I/O	Telit GPIO19 Configurable GPIO		CMOS 2.8V
57	TGPIO_11	I/O	Telit GPIO11 Configurable GPIO		CMOS 2.8V
58	TGPIO_20	I/O	Telit GPIO20 Configurable GPIO		CMOS 2.8V
59	TGPIO_04	I/O	Telit GPIO4 Configurable GPIO / RF Transmission Control		CMOS 2.8V
60	TGPIO_14	I/O	Telit GPIO14 Configurable GPIO		CMOS 2.8V
61	TGPIO_15	I/O	Telit GPIO15 Configurable GPIO		CMOS 2.8V
62	TGPIO_12	I/O	Telit GPIO12 Configurable GPIO		CMOS 2.8V
63	TGPIO_10	I/O	Telit GPIO10 Configurable GPIO / DVI2_TX (Digital Voice Interface)		CMOS 2.8V
64	TGPIO_22	I/O	Telit GPIO22 Configurable GPIO		CMOS 1.8V
65	TGPIO_18	I/O	Telit GPIO18 Configurable GPIO / DVI2_RX (Digital Voice Interface)		CMOS 2.8V
66	TGPIO_03	I/O	Telit GPIO3 Configurable GPIO		CMOS 2.8V
67	TGPIO_08	I/O	Telit GPIO8 Configurable GPIO		CMOS 2.8V

Pin	Signal	I/O	Function	Internal Pull up	Type
68	TGPIO_06 / ALARM	I/O	Telit GPIO6 Configurable GPIO / ALARM		CMOS 2.8V
70	TGPIO_01	I/O	Telit GPIO1 Configurable GPIO		CMOS 2.8V
71	TGPIO_17	I/O	Telit GPIO17 Configurable GPIO / DVI2_WA (Digital Voice Interface)		CMOS 2.8V
72	TGPIO_21	I/O	Telit GPIO21 Configurable GPIO		CMOS 2.8V
73	TGPIO_07 / BUZZER	I/O	Telit GPIO7 Configurable GPIO / Buzzer		CMOS 2.8V
74	TGPIO_02 / JDR	I/O	Telit GPIO02 I/O pin / Jammer detect report		CMOS 2.8V
75	TGPIO_16	I/O	Telit GPIO16 Configurable GPIO		CMOS 2.8V
76	TGPIO_09	I/O	Telit GPIO9 Configurable GPIO		CMOS 2.8V
77	TGPIO_13	I/O	Telit GPIO13 Configurable GPIO		CMOS 2.8V
78	TGPIO_05/ RFTXMON	I/O	Telit GPIO05 Configurable GPIO / Transmitter ON monitor		CMOS 2.8V
RESERVED					
17		-			
33		-			
34		-			
41		-			
42		-			
43		-			
44		-			
47		-			
48		-			
79		-			
69		-			
80		-			
35	DVI1_TX	-	Digital Voice Interface Transmitted Data	4.7KΩ	CMOS 2.8V

NOTE:

The GC864 family Wireless Modules (GC864-QUAD and GC864-PY) has two DVI ports on the system interface.

Only one port can be selected and be active at the time. The choice of DVI port depends on the needs of the application, but Telit suggests that applications only use the DVI2 port as this minimizes the impact on the module functionality.

NOTE:

Reserved pins must not be connected.

NOTE:

RTS must be connected to the GND (on the module side) if flow control is not used.

NOTE:

If not used, almost all pins must be left disconnected. The only exceptions are the following pins[2]:

Pin	Signal	Function
1	VBATT	Main power supply
2	VBATT	Main power supply
3	VBATT	Main power supply
4	VBATT	Main power supply
5	GND	Ground
6	GND	Ground
7	GND	Ground
46	GND	Ground
25	C103/TXD	Serial data input (TXD) from DTE
26	C104/RXD	Serial data output to DTE
31	C105/RTS	Input for Request to send signal (RTS) from DTE
53	ON/OFF*	Input command for switching power ON or OFF (toggle command).
54	RESET*	Reset input

4.1.1. GC864-QUAD/PY Antenna Connector

The GC864-QUAD/PY module is equipped with a 50 Ω RF connector from Murata, GSC type P/N MM9329-2700B.
The counterpart suitable is Murata MXTK92 Type or MXTK88 Type.

Moreover, the GC864-QUAD/PY has the antenna pads on the back side of the PCB. This allows the manual soldering of the coaxial cable directly on the back side of the PCB. However, the soldering is not an advisable solution for a reliable connection of the antenna.

[2] RTS should be connected to the GND (on the module side) if flow control is not used.

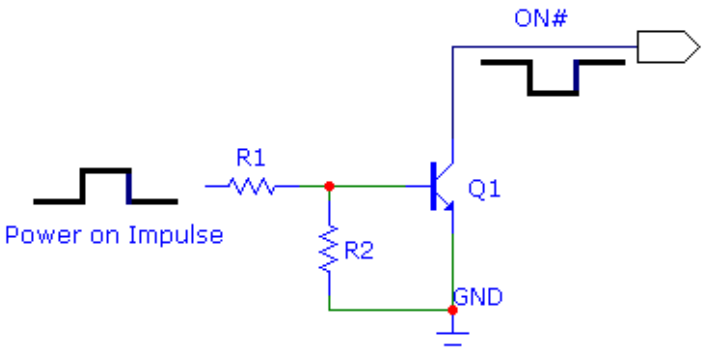
5. Hardware Commands

5.1. Turning ON the GC864-QUAD / PY

To turn the GC864-QUAD / PY on, the pad ON# must be tied low for at least 1 second and then released. A pulse duration less than 1 second should also start the power on procedure, but this is not guaranteed.

The maximum current that can be drained from the ON# pad is 0,1 mA.

A simple circuit to do it is:



TIP:

To check if the device has powered on, the hardware line PWRMON must be monitored. After 900ms the line raised up the device could be considered powered on.

PWRMON line rises up also when supplying power to the Charge pad.

NOTE:

Do not use any pull up resistor on the ON# line, it is internally pulled up. Using pull up resistor may bring to latch up problems on the GC864-QUAD / PY power regulator and improper power on/off of the module. The line ON# must be connected only in open collector configuration.

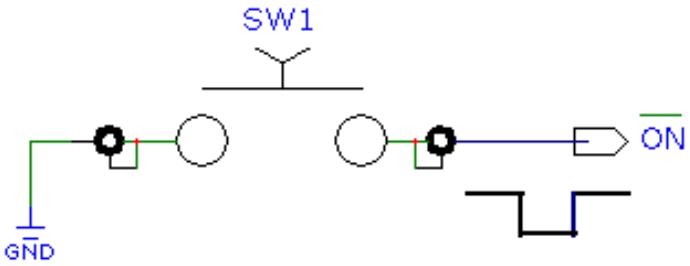
In this document all the lines that are inverted, hence have active low signals are labeled with a name that ends with a "#" or with a bar over the name.

The GC864-QUAD / PY turns fully on also by supplying power to the Charge pad (Module provided with a battery on the VBATT pads).

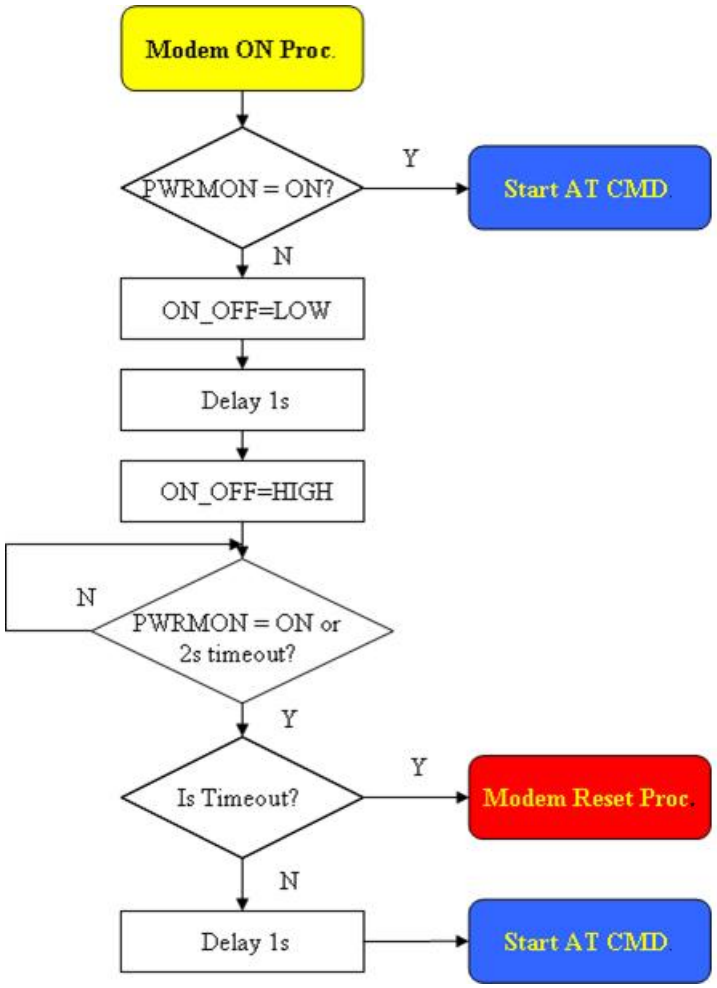
For example:

1- Let us assume you need to drive the ON# pad with a totem pole output of a +3/5 V microcontroller (uP_OUT1):

2- Let us assume you need to drive the ON# pad directly with an ON/OFF button:



A flow chart with proper turn on procedure is detailed below:



5.2. Turning OFF the GC864-QUAD / PY

Turning off of the device can be done in three ways:

- by software command (see GC864-QUAD / PY Software User Guide)
- by tying low pin ON#

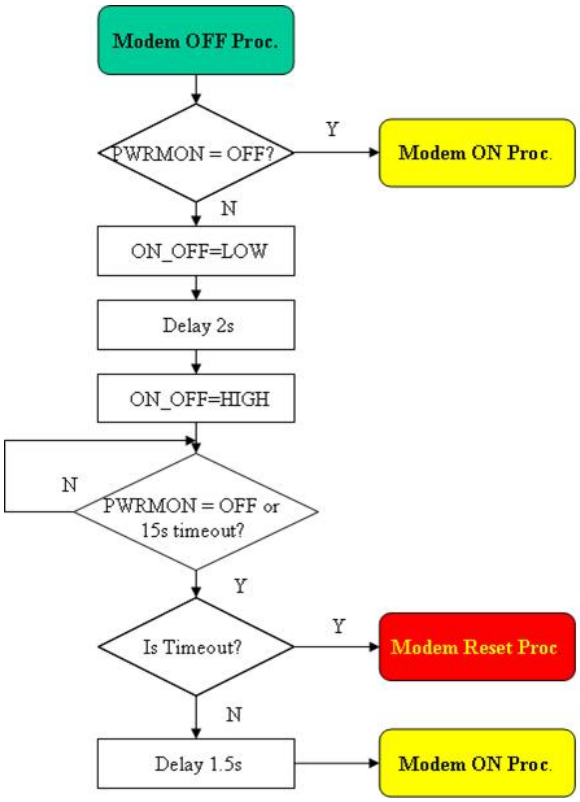
Either ways, the device issues a detach request to network informing that the device will not be reachable any more.

To turn OFF the GC864 via pin ON#, this must be tied low for at least 1s and then released.

The same circuitry and timing for the power on shall be used.

The device shuts down after the release of the ON# pin.

The following flow chart shows the proper turnoff procedure:



TIP:

To check if the device has powered off, the hardware line PWRMON must be monitored. When PWRMON goes low, then the device has powered off.

5.2.1. Hardware Unconditional Restart

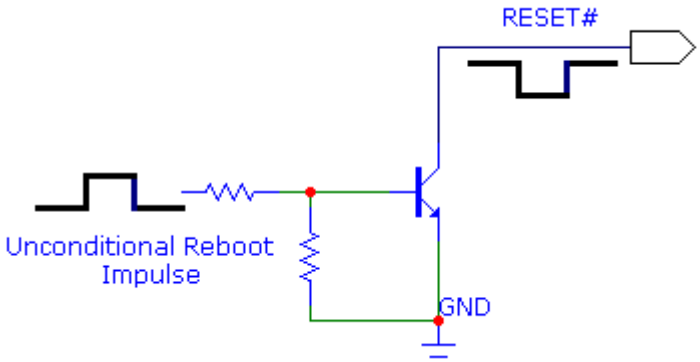
WARNING:

The hardware unconditional Restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure to be done in the rare case that the device gets stacked waiting for some network or SIM responses.

To unconditionally Restart the GC864-QUAD / PY, the pad RESET# must be tied low for at least 200 milliseconds and then released.

The maximum current that can be drained from the ON# pad is 0,15 mA.

A simple circuit to do it is:



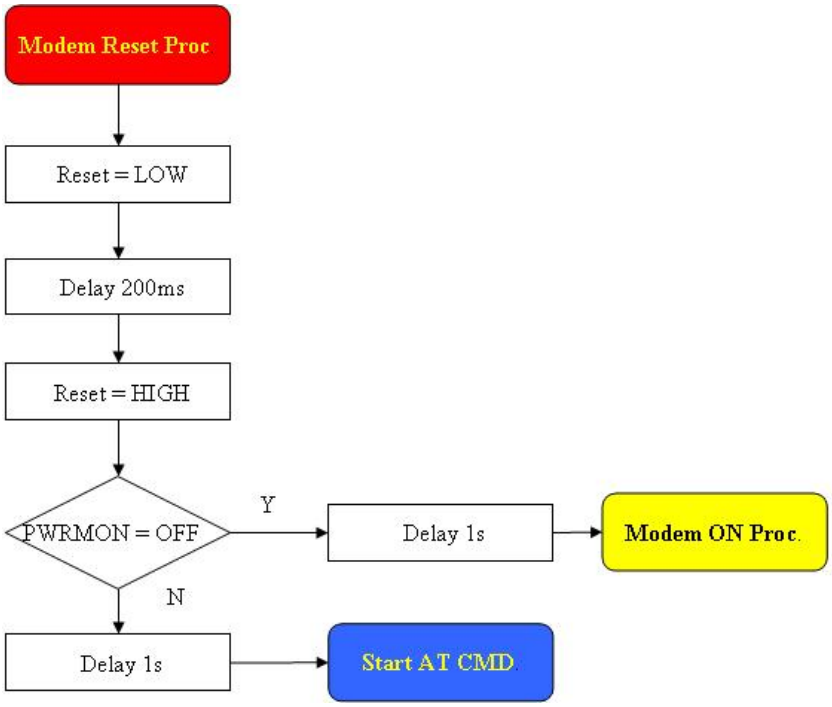
NOTE:

Do not use any pull up resistor on the RESET* line nor any totem pole digital output. Using pull up resistor may cause latch up problems on the GC864-QUAD / PY power regulator and improper functioning of the module. The line RESET* must be connected only in open collector configuration.

TIP:

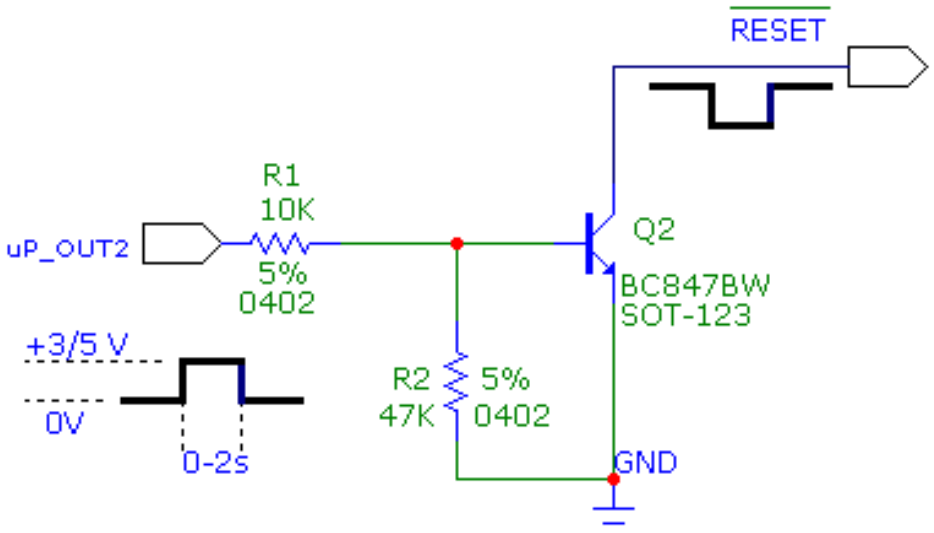
The unconditional hardware reboot must always be implemented on the boards and the software must use it as an emergency exit procedure.

In the following flow chart is detailed the proper restart procedure:



For example:

1- Let us assume you need to drive the RESET# pad with a totem pole output of a +3/5 V microcontroller (uP_OUT2):



6. Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the following requirements and guidelines for a proper design.

6.1. Power Supply Requirements

POWER SUPPLY		
	SW rel. 7.02.xx4 or older	SW rel. 7.03.x00 or newer
Nominal Supply Voltage	3.8 V	3.8 V
Max Supply Voltage	4.2 V	4.5 V
Supply voltage range	3.4 V - 4.2 V	3.22 V – 4.5 V

The GC864-QUAD / PY power consumptions are:

GC864-QUAD / PY		
Mode	Average (mA)	Mode description
SWITCHED OFF		Module supplied but Switched Off
Switched Off	<26 uA	
IDLE mode		
AT+CFUN=1	19.0	Normal mode: full functionality of the module
AT+CFUN=4	18.2	Disabled TX and RX; module is not registered on the network
AT+CFUN=0 or =5	6.6	Paging Multiframe 2
	4.5	Paging Multiframe 4
	3.3	Paging Multiframe 6
	3.2	Paging Multiframe 8
	2.5	Paging Multiframe 9
CSD TX and RX mode		GSM VOICE CALL
GSM900 CSD PL5	237.3	
DCS1800 CSD PL0	223.8	
GPRS (class 10) 1TX		GPRS Sending data mode
GSM900 PL5	264,0	
DCS1800 PL0	176,0	
GPRS (class 10) 2TX		GPRS Sending data mode
GSM900 PL5	473,8	
DCS1800 PL0	307,8	

The GSM system is made in a way that the RF transmission is not continuous but it is packed into bursts at a base frequency of about 216 Hz. The relative current peaks can be as high as about 2A. Therefore the power supply has to be designed in order to withstand with these current peaks without big voltage drops; this means that both the electrical design and the board layout must be designed for this current flow.

If the layout of the PCB is not well designed, then a strong noise floor is generated on the ground and the supply; this will reflect on all the audio paths producing an audible and annoying noise at 216 Hz; if the voltage drop during the peak current absorption is too much, then the device may even shutdown as a consequence of the supply voltage drop.

TIP:

The power supply must be designed so that it is capable of a peak current output of at least 2 A.

6.2. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout.

6.2.1. Electrical Design Guidelines

The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

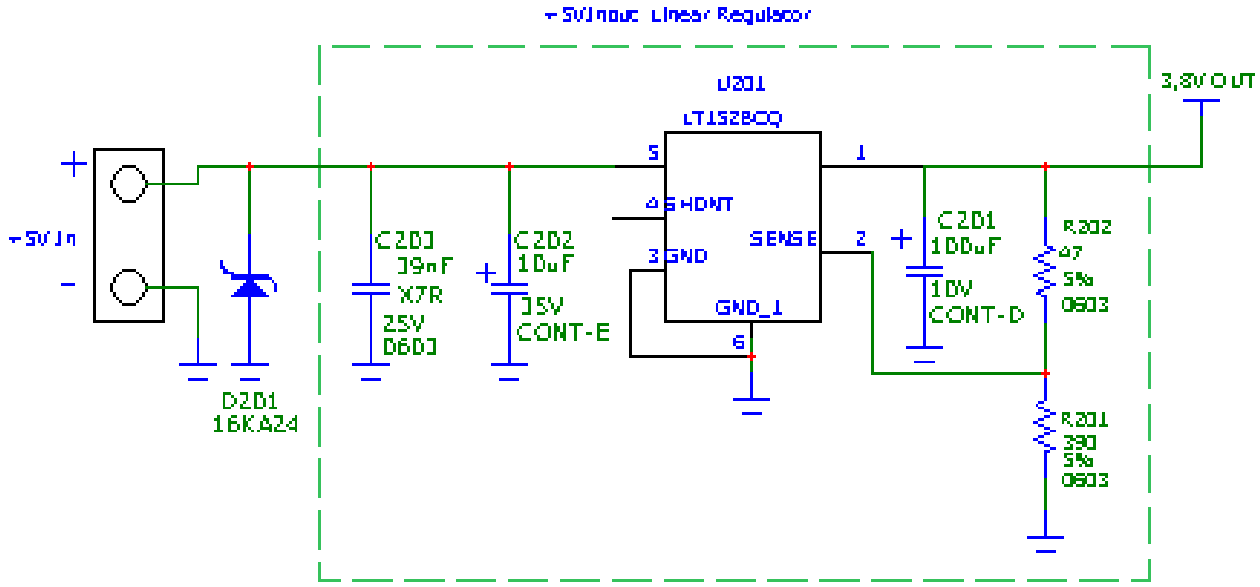
- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

6.2.1.1. +5V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there is no big difference between the input source and the desired output. A linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the GC864-QUAD / PY, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode must be inserted close to the power input, in order to save the GC864-QUAD / PY from power polarity inversion.

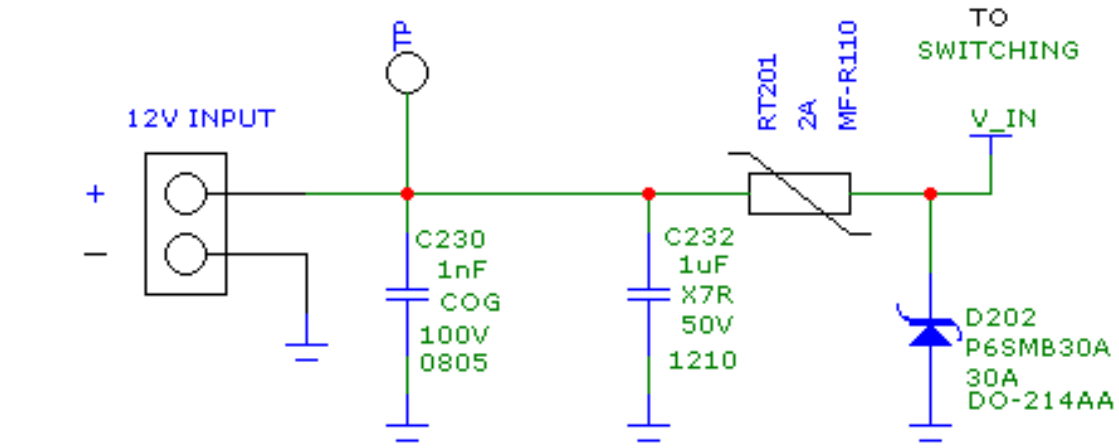
An example of linear regulator with 5V input is:

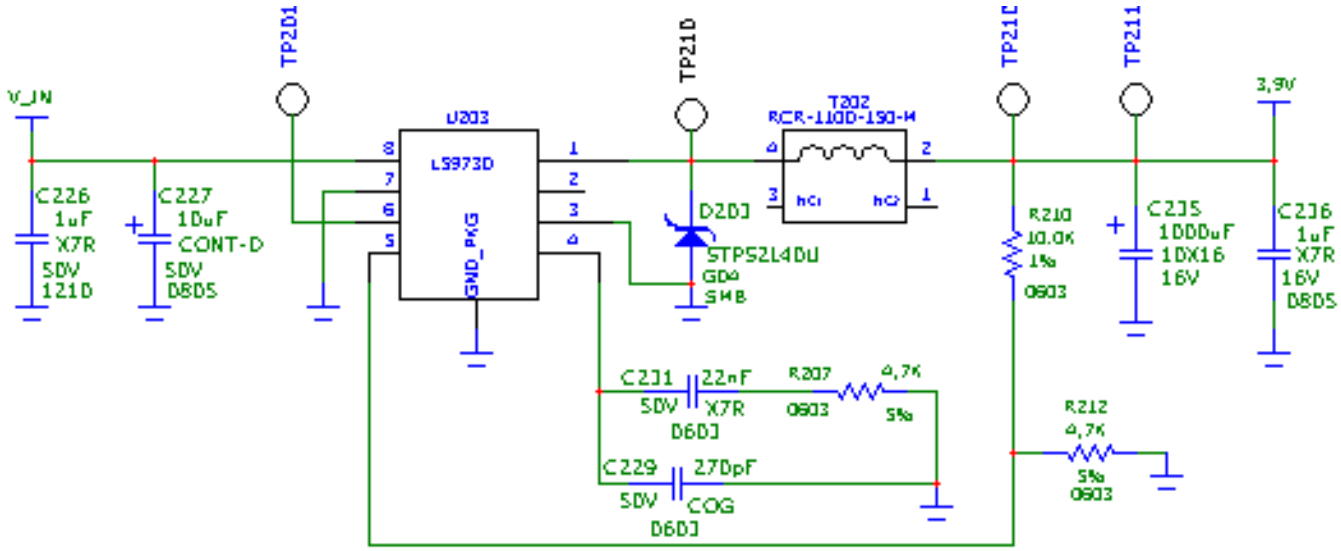


6.2.1.2. +12V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence, due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency especially with the 2A peak current load represented by the GC864-QUAD/PY.
- When using a switching regulator, a 500kHz (or more) switching frequency regulator is preferable, because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and switching design selection is related to the application to be developed, due to the fact that the switching frequency could also generate EMC interferences.
- As far as car PB battery, the input voltage can rise up to 15.8V. This must be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided, in order to cut the current absorption peaks. A 100µF tantalum capacitor is typically used.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- As far as car applications, a spike protection diode must be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode must be inserted close to the power input, in order to save the GC864-QUAD/PY from power polarity inversion. This can be the same diode used for spike protection.

An example of switching regulator with 12V input is in the schematic below (split in 2 parts):





SWITCHING REGULATOR

6.2.1.3. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V (4.5 if using SW release 7.03.x00 or newer). A single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit GC864-QUAD/PY module.

CAUTION:

The three cells Ni/Cd or Ni/MH 3,6 V Nom. Battery types or 4V PB types MUST NOT BE USED DIRECTLY since their maximum voltage can rise over the absolute maximum voltage for the GC864-QUAD/PY and damage it.

CAUTION:

DO NOT USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with GC864-QUAD/PY. Their use can lead to overvoltage on the GC864-QUAD/PY and damage it. USE ONLY Li-Ion battery types.

A Bypass low ESR capacitor of adequate capacity must be provided, in order to cut the current absorption peaks. A 100µF tantalum capacitor is typically used.

Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.

A protection diode must be inserted close to the power input, in order to save the GC864-QUAD/PY from power polarity inversion. Otherwise the battery connector must be done in a way to avoid polarity inversions when connecting the battery.

The battery capacity must be at least 500mAh in order to withstand the current peaks of 2A; the suggested capacity is from 500mAh to 1000mAh.

6.2.1.4. Battery Charge Control Circuitry Design Guidelines

The charging process for Li-Ion Batteries can be divided into 4 phases:

- Qualification and trickle charging
- Fast charge 1 – constant current
- Final charge – constant voltage or pulsed charging
- Maintenance charge

The qualification process consists in a battery voltage measure, indicating roughly its charge status. If the battery is deeply discharged, then its voltage is lower than the trickle charging threshold and the charge must start slowly, possibly with a current limited pre-charging process where the current is kept very low with respect to the fast charge value, aka the trickle charging.

During the trickle charging, the voltage across the battery terminals rises; when it reaches the fast charge threshold level the charging process goes into fast charge phase.

During the fast charge phase the process proceeds with a current limited charging; this current limit depends on the required time for the complete charge and from the battery pack capacity. During this phase the voltage across the battery terminals still raises but at a lower rate.

Once the battery voltage reaches its maximum voltage then the process goes into its third state: Final charging. The voltage measure to change the process status into final charge is very important. It must be ensured that the maximum battery voltage is never exceeded, otherwise the battery may be damaged and even explode. Moreover for the constant voltage final chargers, the constant voltage phase (final charge) must not start before the battery voltage has reached its maximum value, otherwise the battery capacity will be highly reduced.

The final charge can be of two different types: constant voltage or pulsed. GC864-QUAD/PY uses constant voltage.

The constant voltage charge proceeds with a fixed voltage regulator (very accurately set to the maximum battery voltage) and hence the current will decrease while the battery is becoming charged. When the charging current falls below a certain fraction of the fast charge current value, then the battery is considered fully charged, the final charge stops and eventually starts the maintenance.

The pulsed charge process has no voltage regulation, instead the charge continues with pulses. Usually the pulse charge works in the following manner: the charge is stopped for some time, let us say few hundreds of ms, then the battery voltage will be measured and when it drops below its maximum value a fixed time length charging pulse is issued. As the battery approaches its full charge the off time will become longer, hence the duty-cycle of the pulses will decrease. The battery is considered fully charged when the pulse duty-cycle is less than a threshold value, typically 10%, the pulse charge stops and eventually the maintenance starts.

The last phase is not properly a charging phase, since the battery at this point is fully charged and the process may stop after the final charge. The maintenance charge provides an additional charging process to compensate for the charge leak typical of a Li-Ion battery. It is done by issuing pulses with a fixed time length, again few hundreds of ms, and a duty-cycle around 5% or less.

This last phase is not implemented in the GC864-QUAD/PY internal charging algorithm, so that the battery once charged is left discharging down to a certain threshold so that it is cycled from full charge to slight discharge even if the battery charger is always inserted. This guarantees that anyway the remaining charge in the battery is a good percentage and that the battery is not damaged by keeping it always fully charged (Li-Ion rechargeable battery usually deteriorate when kept fully charged).

Last but not least, in some applications it is highly desired that the charging process restarts when the battery is discharged and its voltage drops below a certain threshold, GC864-QUAD/PY internal charger does it.

As you can see, the charging process is not a trivial task to be done; moreover all these operations must start only if battery temperature is inside a charging range, usually 5°C – 45°C.

The GC864-QUAD/PY measures the temperature of its internal component, in order to satisfy this last requirement, it is not exactly the same as the battery temperature but in common application the two temperature must not differ too much and the charging temperature range must be guaranteed.

NOTE:

For all the threshold voltages, inside the GC864-QUAD/PY all thresholds are fixed in order to maximize Li-Ion battery performances and do not need to be changed.

NOTE:

In this application the battery charger input current must be limited to less than 400mA. This can be done by using a current limited wall adapter as the power source.

NOTE:

When starting the charger from Module powered off the startup will be in CFUN4; to activate the normal mode, a command AT+CFUN=1 has to be provided.
There is also the possibility to activate the normal mode using the ON_OFF* signal. In this case, when HW powering off the module with the same line (ON_OFF*) and having the charger still connected, the module will go back to CFUN4.

NOTE:

It is important having a 100uF Capacitor to VBAT in order to avoid instability of the charger circuit if the battery is accidentally disconnected during the charging activity.

6.2.2. Thermal Design Guidelines

The thermal design for the power supply heat sink must be done with the following specifications:

- Average current consumption during transmission @PWR level max: 500mA
- Average current consumption during transmission @ PWR level min: 100mA
- Average current during Power Saving (CFUN=5): 4mA
- Average current during idle (Power Saving disabled): 23mA

NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

If we assume that the device stays into transmission for short periods of time (let us say few minutes) and then remains for a quite long time in idle (let us say one hour), then the power supply has always the time to cool down between the calls, and the heat sink could be smaller than the calculated one for 500mA maximum RMS current, or even could be the simple chip package (no heat sink).

Moreover, in the average network conditions, the device is requested to transmit at a lower power level than the maximum, hence the current consumption will be less than 500mA, usually around 150mA.

For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed grants a good thermal condition to avoid overheating as well.

As far as the heat generated by the GC864-QUAD / PY, you can consider it to be during transmissions of 1W max during CSD/VOICE calls and 2W max during class10 GPRS upload.

This generated heat will be mostly conducted to the ground plane under the GC864-QUAD / PY; you must ensure that your application can dissipate it.

6.2.3. Power Supply PCB Layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The Bypass low ESR capacitor must be placed close to the Telit GC864-QUAD / PY power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the GC864-QUAD / PY is wide enough to ensure a dropless connection even during the 2A current peaks.
- The protection diode must be placed close to the input connector where the power source is drained.

- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 2A current peaks are absorbed. Note that this is not made in order to save power loss but especially to avoid the voltage drops on the power line at the current peaks frequency of 216 Hz that will reflect on all the components connected to that supply, introducing the noise floor at the burst base frequency. For this reason while a voltage drop of 300-400 mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If your application does not have audio interface but only uses the data feature of the Telit GC864-QUAD / PY, then this noise is not so disturbing and power supply layout design can be more forgiving.
- The PCB traces to the GC864-QUAD / PY and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 2A current peaks are absorbed. This is for the same reason as previous point. Try to keep this trace as short as possible.
- The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board must be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables must be kept separate from noise sensitive lines such as microphone/earphone cables.

6.2.4. Parameters for ATEX Applications

In order to integrate the Telit's GC864 module into an ATEX application, the appropriate reference standard IEC EN xx and integrations shall be followed.

Below are listed parameters and useful information to integrate the module in your application:

- Total capacity: 78.494 uF
- Total inductance: 10.163 uH
- No voltage upper than supply voltage is present in the module.
- No step-up converters are present in the module.

- In abnormal conditions, the maximum RF output power is up to 34 dBm for few seconds.

For this particular application, we recommend the customer to involve TTSC (Telit Technical Support Center) in the design phase of the application.

7. Antenna

The antenna connection and board layout design are the most important part in the full product design and they strongly reflect on the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.

7.1. GSM Antenna Requirements

As suggested on the Product Description the antenna for a Telit GC864-QUAD / PY device shall fulfill the following requirements:

ANTENNA REQUIREMENTS	
Frequency range	Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Bandwidth	70 MHz in GSM850, 80 MHz in GSM900, 170 MHz in DCS & 140 MHz PCS band
Gain	Gain < 1,4dBi in GSM 850 & 900 and < 3,0dBi DCS & PCS
Impedance	50 Ω
Input power	> 2 W peak power
VSWR absolute max	<= 10:1
VSWR recommended	<= 2:1

Furthermore if the device is developed for the US market and/or Canada market, it shall comply to the FCC and/or IC approval requirements:

This device is to be used only for mobile and fixed application. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-Users must be provided with transmitter operation conditions for satisfying RF exposure compliance. OEM integrators must ensure that the end user has no manual instructions to remove or install the GC864-QUAD / PY module. Antennas used for this OEM module must not exceed 3dBi gain for mobile and fixed operating configurations.

7.2. GSM Antenna – Installation Guidelines

- Install the antenna in a place covered by the GSM signal.
- The Antenna must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter;
- Antenna shall not be installed inside metal cases
- Antenna shall be installed also according Antenna manufacturer instructions.

8. Logic Level Specifications

Where not specifically stated, all the interface circuits work at 2.8V CMOS logic levels. The following table shows the logic level specifications used in the Telit GC864-QUAD / PY interface circuits:

Absolute Maximum Ratings – Not Functional

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.6V
Input voltage on analog pins when on	-0.3V	+3.0 V

Operating Range – Interface Levels (2.8V CMOS)

Level	Min	Max
Input high level	2.1V	3.3V
Input low level	0V	0.5V
Output high level	2.2V	3.0V
Output low level	0V	0.35V

For 1,8V signals:

Operating Range – Interface Levels (1.8V CMOS)

Level	Min	Max
Input high level	1.6V	2.2V
Input low level	0V	0.4V
Output high level	1,65V	2.2V
Output low level	0V	0.35V

Current characteristics

Level	Typical
Output Current	1mA
Input Current	1uA

8.1. Reset Signal

Signal	Function	I/O	PIN Number
RESET	Phone reset	I	54

RESET is used to reset the GC864-QUAD / PY modules. Whenever this signal is pulled low, the GC864-QUAD / PY is reset. When the device is reset it stops any operation. After the release of the reset GC864-QUAD / PY is unconditionally shut down, without doing any detach operation from the network where it is registered. This behaviour is not a proper shut down because any GSM device is requested to issue a detach request on turn off. For this reason the Reset signal must not be used to normally shutting down the device, but only as an emergency exit in the rare case the device remains stuck waiting for some network response.

The RESET is internally controlled on start-up to achieve always a proper power-on reset sequence, so there is no need to control this pin on start-up. It may only be used to reset a device already on that is not responding to any command.

NOTE:

Do not use this signal to power off the GC864-QUAD / PY. Use the ON/OFF signal to perform this function or the AT#SHDN command.

Reset Signal Operating Levels:

Signal	Min	Max
RESET Input high	2.0V*	2.2V
RESET Input low	0V	0.2V

* this signal is internally pulled up so the pin can be left floating if not used.

If unused, this signal may be left unconnected. If used, then it **must always be connected with an open collector transistor**, to permit to the internal circuitry the power on reset and under voltage lockout functions.

9. Serial Ports

The serial port on the Telit GC864-QUAD/PY is the core of the interface between the module and OEM hardware.

2 serial ports are available on the module:

- MODEM SERIAL PORT
- MODEM SERIAL PORT 2 (DEBUG)

9.1. MODEM SERIAL PORT

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 2.8V – 3V (Universal Asynchronous Receive Transmit)
- microcontroller UART@ 5V or other voltages different from 2.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work. The only configuration that does not need a level translation is the 2.8V UART.

The serial port on the GC864-QUAD/PY is a +2.8V UART with all the 7 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels. The levels for the GC864-QUAD/PY UART are the CMOS levels:

Absolute Maximum Ratings –Not Functional

Parameter	Min	Max
Input level on any digital pad when on	-0.3V	+3.6V
Input voltage on analog pads when on	-0.3V	+3.0 V

Operating Range – Interface levels (2.8V CMOS)

Level	Min	Max
Input high level V_{IH}	2.1V	3.3V
Input low level V_{IL}	0V	0.5V
Output high level V_{OH}	2.2V	3.0V
Output low level V_{OL}	0V	0.35V

The table below shows the signals of the GC864-QUAD/PY serial port:

RS232 Pin Number	Signal	GC864-QUAD / PY Pad Number	Name	Usage
1	DCD – dcd_uart	32	Data Carrier Detect	Output from the GC864-QUAD / PY that indicates the carrier presence
2	RXD – tx_uart	26	Transmit line *see Note	Output transmit line of GC864-QUAD / PY UART
3	TXD – rx_uart	25	Receive line *see Note	Input receive of the GC864-QUAD / PY UART
4	DTR – dtr_uart	29	Data Terminal Ready	Input to the GC864-QUAD / PY that controls the DTE READY condition
5	GND	5,6,7	Ground	ground
6	DSR – dsr_uart	27	Data Set Ready	Output from the GC864-QUAD / PY that indicates the module is ready
7	RTS – rts_uart	31	Request to Send	Input to the GC864-QUAD / PY that controls the Hardware flow control
8	CTS – cts_uart	28	Clear to Send	Output from the GC864-QUAD / PY that controls the Hardware flow control
9	RI – ri_uart	30	Ring Indicator	Output from the GC864-QUAD / PY that indicates the incoming call condition

***NOTE:**

According to V.24, RX/TX signal names are referred to the application side, therefore on the GC864-QUAD/PY side these signal are on the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ rx_uart) of the GC864-QUAD/PY serial port and viceversa for RX.

TIP:

For a minimum implementation, only the TXD and RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

TIP:

In order to avoid noise or interferences on the RXD lines it is suggested to add a pull up resistor (100KΩ to 2.8V)

9.2. RS232 Level Translation

In order to interface the Telit GC864-QUAD/PY with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must

- invert the electrical signal in both directions
- change the level from 0/3V to +15/-15V

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing for a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.

The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of driver and receiver and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).

By convention the driver is the level translator from the 0-3V UART level to the RS232 level, while the receiver is the translator from RS232 level to 0-3V UART.

In order to translate the whole set of control lines of the UART you will need:

- 5 driver
- 3 receiver

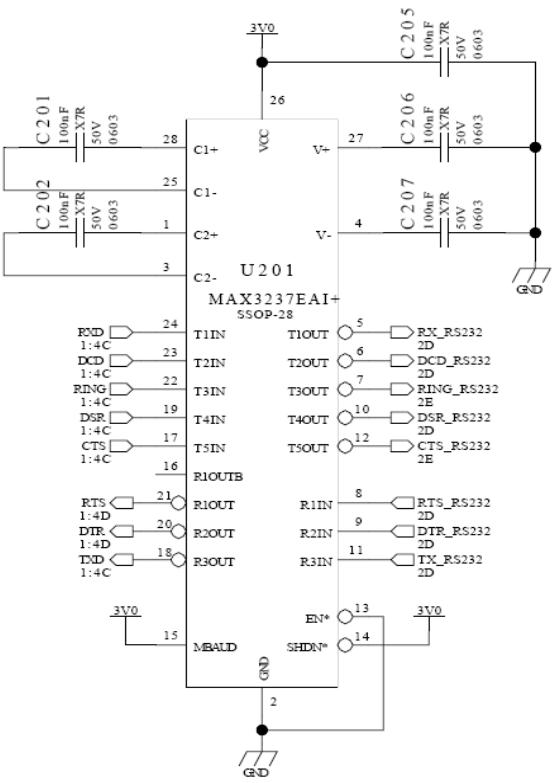
NOTE:

The digital input lines working at 2.8VCMOS have an absolute maximum input voltage of 3,75V; therefore the level translator IC shall not be powered by the +3.8V supply of the module. Instead it shall be powered from a +2.8V / +3.0V (dedicated) power supply.
This is because in this way the level translator IC outputs on the module side (i.e. GC864-QUAD/PY inputs) will work at +3.8V interface levels, stressing the module inputs at its maximum input voltage.
This can be acceptable for evaluation purposes, but not on production devices.

NOTE:

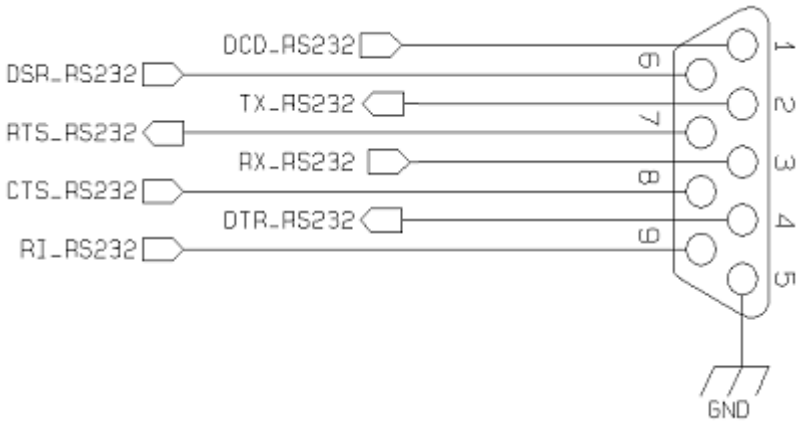
In order to be able to do in circuit reprogramming of the GC864-QUAD/PY firmware, the serial port on the Telit GC864-QUAD/PY shall be available for translation into RS232 and either it is controlling device shall be placed into tristate, disconnected or as a gateway for the serial data when module reprogramming occurs.
Only RXD, TXD, GND and the On/off module turn on pad are required to the reprogramming of the module, the other lines are unused.
All applicator shall include in their design such a way of reprogramming the GC864.

An example of level translation circuitry of this kind is:



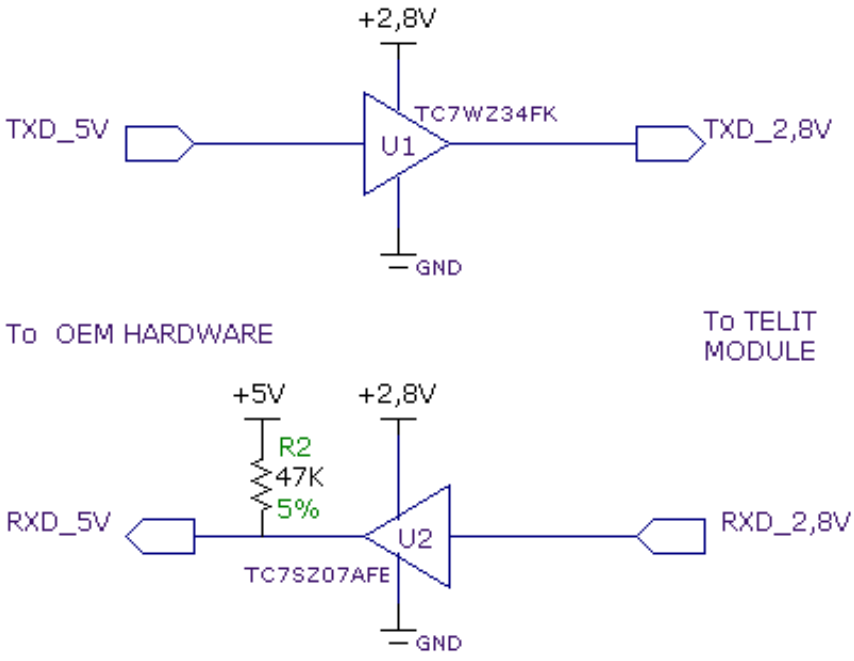
RS232 LEVEL TRSANSLATOR

The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



9.3. 5V UART Level Translation

If the OEM application uses a microcontroller with a serial port (UART) that works at a voltage different from 2.8 – 3V, then a circuitry has to be provided to adapt the different levels of the two set of signals. As for the RS232 translation there are a multitude of single chip translators. For example a possible translator circuit for a 5V TRANSMITTER/RECEIVER can be:



TIP:

This logic IC for the level translator and 2.8V pull-ups (not the 5V one) can be powered directly from VAUX line of the GC864-QUAD / PY. Note that the TC7SZ07AE has open drain output; therefore the resistor R2 is mandatory.

NOTE:

The UART input line TXD (rx_uart) of the GC864-QUAD / PY is NOT internally pulled up with a resistor, so there may be the need to place an external 47KΩ pull-up resistor, either the DTR (dtr_uart) and RTS (rts_uart) input lines are not pulled up internally, so an external pull-up resistor of 47KΩ may be required.

A power source of the internal interface voltage corresponding to the 2.8VCMOS high level is available at the VAUX pin on the connector,

A maximum of 9 resistors of 47 KΩ pull-up can be connected to the VAUX pin, provided no other devices are connected to it and the pulled-up lines are GC864-QUAD / PY input lines connected to open collector outputs in order to avoid latch-up problems on the GC864-QUAD / PY.

Care must be taken to avoid latch-up on the GC864-QUAD / PY and the use of this output line to power electronic devices shall be avoided, especially for devices that generate spikes and noise such as switching level translators, micro controllers, failure in any of these condition can severely compromise the GC864-QUAD / PY functionality.

NOTE:

The input lines working at 2.8VCMOS can be pulled-up with 47KΩ resistors that can be connected directly to the VAUX line provided they are connected as in this example.

In case of reprogramming of the module has to be considered the use of the RESET line to start correctly the activity.

The preferable configuration is having an external supply for the buffer.

10. Audio Section Overview

The Baseband chip was developed for the cellular phones, which needed two separated amplifiers both in RX and in TX section.

A couple of amplifiers had to be used with internal audio transducers while the other couple of amplifiers had to be used with external audio transducers.

To distinguish the schematic signals and the Software identifiers, two different definitions were introduced, with the following meaning:

- internal audio transducers → *HS/MT* (from HandSet or MicroTelephone)
- external audio transducers → *HF* (from HandsFree)

Actually the acronyms have not the original importance.

In other words this distinction is not necessary, being the performances between the two blocks like the same.

Only if the customer needs higher output power to the speaker , he has a constraint. Otherwise the choice could be done in order to overcome the PCB design difficulties.

For these reasons we have not changed the HS and HF acronyms, keeping them in the Software and on the schematics.

The Base Band Chip of the GC864Telit Module maintains the same architecture.

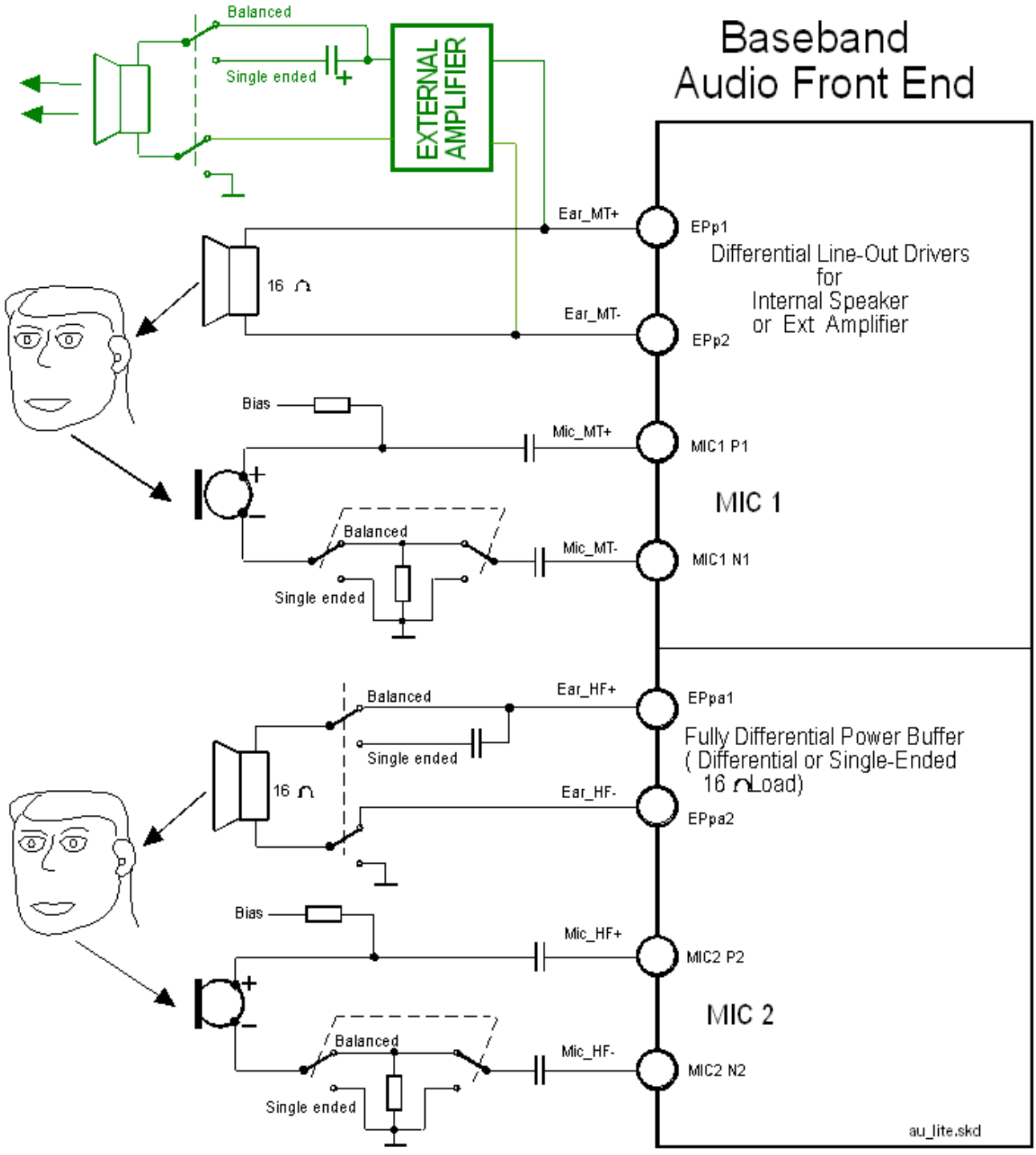
For more information refer to Telit document :

" *80000NT10007a Audio Settings Application Note*".

10.1. Selection mode

Only one block can be active at a time , and the activation of the requested audio path is done via hardware by *AXE* line or via software by *AT#CAP* command .

Moreover the Sidetone functionality could be implemented by the amplifier fitted between the transmit path and the receive path, enabled at request in both modes.



EGold Lite Audio Section Block Diagram

10.2. Electrical Characteristics

TIP: Being the microphone circuitry the more noise sensitive, its design and layout must be done with particular care. Both microphone paths are balanced and the OEM circuitry must be balanced designed to reduce the common mode noise typically generated on the ground plane. However the customer can use the unbalanced circuitry for particular application.

10.2.1. Input Lines Characteristics

"MIC_MT" and "MIC_HF" differential microphone paths	
Line Coupling	AC*
Line Type	Balanced
Coupling capacitor	≥ 100nF
Differential input resistance	50KΩ
Differential input voltage	≤ 1,03V_{pp} @ *MicG=0dB*

(*) WARNING : AC means that the signals from the microphone have to be connected to input lines of the module through capacitors which value has to be ≥ 100nf. not respecting this constraint, the input stages will be damaged.

WARNING: when particular OEM application needs a *Single Ended Input* configuration, it is forbidden connecting the unused input directly to Ground, but only through a 100nF capacitor. Don't forget that in Single Ended configuration the useful input signal will be halved.

10.2.2. Output Lines Characteristics

TIP:

We suggest driving the load differentially from both output drivers, thus the output swing will double and the need for the output coupling capacitor avoided. However if particular OEM application needs also a Single Ended circuitry can be implemented, but the output power will be reduced four times .

The OEM circuitry shall be designed to reduce the common mode noise typically generated on the ground plane and to get the maximum power output from the device (low resistance tracks).

WARNING:

The loads are directly connected to the amplifier outputs when in *Differential* configuration, through a capacitor when in *Single Ended* configuration. Using Single Ended configuration, the unused output line must be left open . Not respecting this constraint, the output stage will be damaged.

TIP :

Remember that there are slightly different electrical performances between the two internal audio amplifiers:

- the *"Ear_MT"* lines can directly drive a ***16 Ω load*** at –12dBFS **(**)** in *Differential* configuration
- the "***Ear_HF***" lines can directly drive a ***16Ω load*** in *Differential* or *Single Ended* configurations
- There is no difference if the amplifiers drive an external amplifier

(**) *0dBFS* is the normalized overall Analog Gain for each Output channel equal to $3,7V_{pp}$ differential

"EAR_MT" Output Lines	
line coupling	AC single-ended DC differential
output load resistance	≥ 14 Ω
internal output resistance	4 Ω (*typical*)
signal bandwidth	150 - 4000 Hz @ -3 dB
max. differential output voltage	1.31 V_{rms} (*typical, open circuit*)
differential output voltage	328mV_{rms} /16 Ω /@ *-12dBFS*
volume increment	2 dB per step
volume steps	10

"EAR_HF" Output Lines	
line coupling:	AC single-ended DC differential
output load resistance :	≥ 14 Ω
internal output resistance:	4 Ω (>1,7 Ω)
signal bandwidth:	150 - 4000 Hz @ -3 dB
max. differential output voltage	1.31 V_{rms} (*typical, open circuit*)
max. S.E. output voltage	656 mV_{rms} (*typical, open circuit*)
volume increment	2 dB per step
volume steps	10

11. General Purpose I/O

The general-purpose I/O pads can be configured to act in three different ways:

- Input
- Output
- Alternate function (internally controlled)

Input pads can only be read and report the digital value (high or low) present on the pad at the read time; output pads can only be written or queried and set the value of the pad output; an alternate function pad is internally controlled by the GC864-QUAD / PY firmware and acts depending on the function implemented.

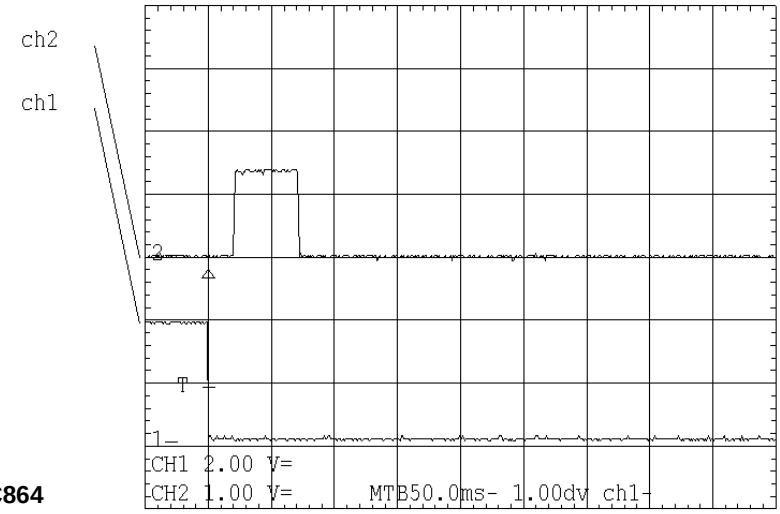
The following GPIO are available on the GC864-QUAD and GC864-PY:

Pin	Signal	I/O	Function	Type	Input / output current	Default State	ON_OFF state	State during Reset	Note
70	TGPIO_01	I/O	GPIO01 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
74	TGPIO_02	I/O	GPIO02 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (JDR)
66	TGPIO_03	I/O	GPIO03 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
59	TGPIO_04	I/O	GPIO04 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (RF Transmission Control)
78	TGPIO_05	I/O	GPIO05 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (RFTXMON)
68	TGPIO_06	I/O	GPIO06 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	Pict 01	1	Alternate function (ALARM)
73	TGPIO_07	I/O	GPIO07 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (BUZZER)
67	TGPIO_08	I/O	GPIO08 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
76	TGPIO_09	I/O	GPIO09 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
63	TGPIO_10	I/O	GPIO10 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
57	TGPIO_11	I/O	GPIO11 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
62	TGPIO_12	I/O	GPIO12 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
77	TGPIO_13	I/O	GPIO13 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
60	TGPIO_14	I/O	GPIO14 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
61	TGPIO_15	I/O	GPIO15 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
75	TGPIO_16	I/O	GPIO16 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
71	TGPIO_17	I/O	GPIO17 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
65	TGPIO_18	I/O	GPIO18 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
56	TGPIO_19	I/O	GPIO19 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
58	TGPIO_20	I/O	GPIO20 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
72	TGPIO_21	I/O	GPIO21 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	1		
64	TGPIO_22	I/O	GPIO22 Configurable GPIO	CMOS 1.8V (not 2.8V !!)	1uA / 1mA	INPUT	0		

Not all GPIO pads support all these three modes:

- GPIO2 supports all three modes and can be input, output, Jamming Detect Output (Alternate function)
- GPIO4 supports all three modes and can be input, output, RF Transmission Control (Alternate function)
- GPIO5 supports all three modes and can be input, output, RFTX monitor output (Alternate function)
- GPIO6 supports all three modes and can be input, output, alarm output (Alternate function)
- GPIO7 supports all three modes and can be input, output, buzzer output (Alternate function)

ch1: ON_OFF (2sec)
ch2: GPIO 06 [bis]



GC864

11.1. GPIO Logic Levels

Where not specifically stated, all the interface circuits work at 2.8V CMOS logic levels.

The following tables show the logic level specifications used in the GC864-QUAD/PY interface circuits:

Absolute Maximum Ratings –Not Functional

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.6V
Input voltage on analog pins when on	-0.3V	+3.0 V

Operating Range – Interface Levels (2.8V CMOS)

Level	Min	Max
Input high level	2.1V	3.3V
Input low level	0V	0.5V
Output high level	2.2V	3.0V
Output low level	0V	0.35V

For 1.8V signals:

Operating Range – Interface Levels (1.8V CMOS)

Level	Min	Max
Input high level	1.6V	2.2V
Input low level	0V	0.4V
Output high level	1,65V	2.2V
Output low level	0V	0.35V

11.2. Using a GPIO Pad as INPUT

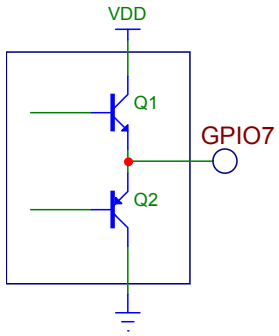
The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 2.8V CMOS levels of the GPIO.

If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 2.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to 2.8V.

11.3. Using a GPIO Pad as OUTPUT

The GPIO pads, when used as outputs, can drive 2.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

The illustration below shows the base circuit of a push-pull stage:



11.4. Using the RF Transmission Control GPIO4

The GPIO4 pin, when configured as RF Transmission Control Input, permits to disable the Transmitter when the GPIO is set to Low by the application.

In the design is necessary to add a pull up resistor (47K to VAUX).

11.5. Using the RFTXMON Output GPIO5

The GPIO5 pin, when configured as RFTXMON Output, is controlled by the GC864-QUAD / PY module and will rise when the transmitter is active and fall after the transmitter activity is completed.

For example, if a call is started, the line will be HIGH during all the conversation and it will be again LOW after hanged up.

The line rises up 300ms before first TX burst and will became again LOW from 500ms to 1sec after last TX burst.

11.6. Using the Alarm Output GPIO6

The GPIO6 pad, when configured as Alarm Output, is controlled by the GC864-QUAD / PY module and will rise when the alarm starts and fall after the issue of a dedicated AT command.

This output can be used to power up the GC864-QUAD / PY controlling micro controller or application at the alarm time, giving you the possibility to program a timely system wake-up to achieve some periodic actions and completely turn off either the application and the GC864-QUAD / PY during sleep periods, dramatically reducing the sleep consumption to few µA.

In battery-powered devices this feature will greatly improve the autonomy of the device.

NOTE:

During RESET the line is set to HIGH logic level.

11.7. Using the Buzzer Output GPIO7

As *Alternate Function*, the GPIO7 is controlled by the firmware that depends on the function implemented internally.

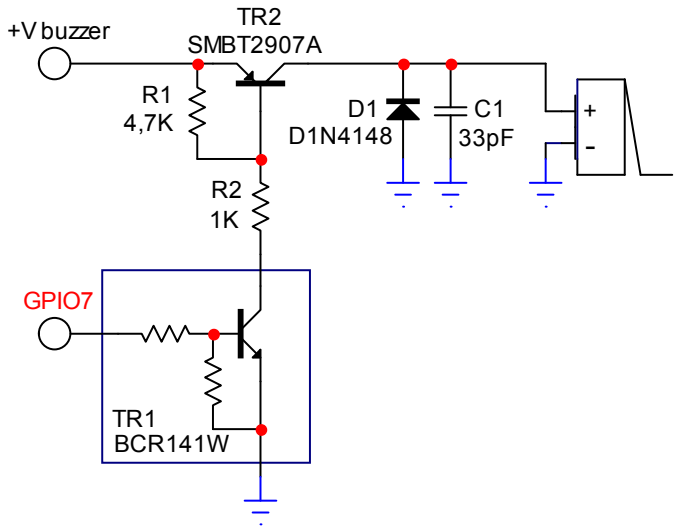
This setup places always the GPIO7 pin in *OUTPUT* direction and the corresponding function must be activated properly by **AT#SRP** command (refer to *AT commands specification*).

Also in this case, the *dummy value* for the pin state can be both "*0*" or "*1*".

- Send the command AT#GPIO=7, 1, 2<cr>:
- Wait for response OK
- Send the command AT#SRP=3

The GPIO7 pin will be set as *Alternate Function* pin with its *dummy* logic status set to *HIGH* value.

The "*Alternate Function*" permits your application to easily implement **Buzzer feature** with some small hardware extension of your application as shown in the sample figure below.



Example of Buzzer's driving circuit

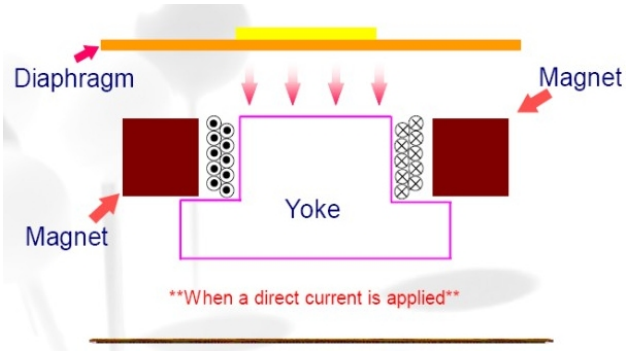
NOTE:

To correctly drive a buzzer, a driver must be provided; its characteristics depend on the Buzzer and for them refer to your buzzer vendor.

11.8. Magnetic Buzzer Concepts

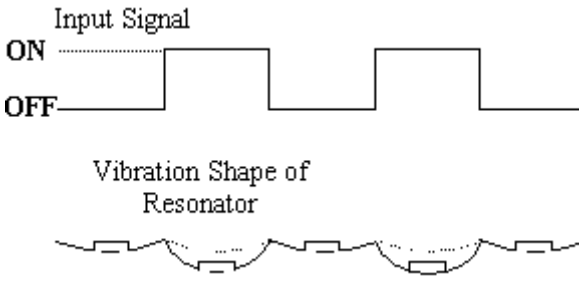
11.8.1. Short Description

A magnetic Buzzer is a sound-generating device with a coil located in the magnetic circuit consisting of a permanent magnet, an iron core, a high permeable metal disk, and a vibrating diaphragm.



Drawing of the Magnetic Buzzer

The disk and diaphragm are attracted to the core by the magnetic field. When an oscillating signal is moved through the coil, it produces a fluctuating magnetic field, which vibrates the diaphragm at a frequency of the drive signal. Thus the sound is produced relative to the frequency applied.



Diaphragm movement

11.8.1 Frequency Behavior

The frequency behavior represents the effectiveness of the reproduction of the applied signals.

Because its performance is related to a square driving waveform (whose amplitude varies from 0V to Vpp), if you modify the waveform (e.g. from square to sinus) the frequency response will change.

11.8.2. Power Supply Influence

Applying a signal whose amplitude is different from that suggested by manufacturer, the performance change following the rule:
if resonance frequency f_o increases, amplitude decreases.

Because of resonance frequency depends from acoustic design, lowering the amplitude of the driving signal the response bandwidth tends to become narrow, and vice versa.

Summarizing: Vpp ↑ → f_o ↓ Vpp ↓ → f_o ↑

The risk is that the f_o could easily fall outside of new bandwidth; consequently the SPL could be much lower than the expected.

11.8.3. Warning

It is very important to respect the sense of the applied voltage: never apply to the "-" *pin* a voltage more positive than the "+" *pin*. If this happens, the diaphragm vibrates in the opposite sense with a high probability to be expelled from its physical position, damaging the device forever.

11.8.4. Working Current Influence

In the component data sheet you will find the value of MAX CURRENT that represents the maximum average current that can flow at nominal voltage without current limitation.

In other words it is not the peak current, which could be twice or three times higher.

If driving circuitry does not support these peak values, the SPL will never reach the declared level or the oscillations will stop.

11.9. Using the Temperature Monitor Function

11.9.1. Short Description

The Temperature Monitor is a function of the module that permits to control its internal temperature and if properly set (see the #TEMPMON command on AT Interface guide) it raise to High Logic level a GPIO when the maximum temperature is reached.

11.9.2. Allowed GPIO

The AT#TEMPMON set command could be used with one of the following GPIO:

Signal	Function	Type	Input / output current	Note
TGPIO_01	GPIO01 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_03	GPIO03 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_08	GPIO08 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_09	GPIO09 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_10	GPIO10 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_11	GPIO11 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_12	GPIO12 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_13	GPIO13 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_14	GPIO14 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_15	GPIO15 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_16	GPIO16 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_17	GPIO17 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_18	GPIO18 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_19	GPIO19 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_20	GPIO20 Configurable GPIO	CMOS 2.8V	1µA / 1mA	
TGPIO_22	GPIO22 Configurable GPIO	**CMOS 1.8V (not 2.8V !!)**	1µA / 1mA	

The set command could be used also with one of the following GPIO but in that case the alternate function is not usable:

Signal	Function	Type	Input / output current	Note
TGPIO_02	GPIO02 Configurable GPIO	CMOS 2.8V	1µA / 1mA	Alternate function (JDR)
TGPIO_04	GPIO04 Configurable GPIO	CMOS 2.8V	1µA / 1mA	Alternate function (RF Transmission Control)
TGPIO_05	GPIO05 Configurable GPIO	CMOS 2.8V	1µA / 1mA	Alternate function (RFTXMON)
TGPIO_07	GPIO07 Configurable GPIO	CMOS 2.8V	1µA / 1mA	Alternate function (BUZZER)

11.10. Indication of Network Service Availability

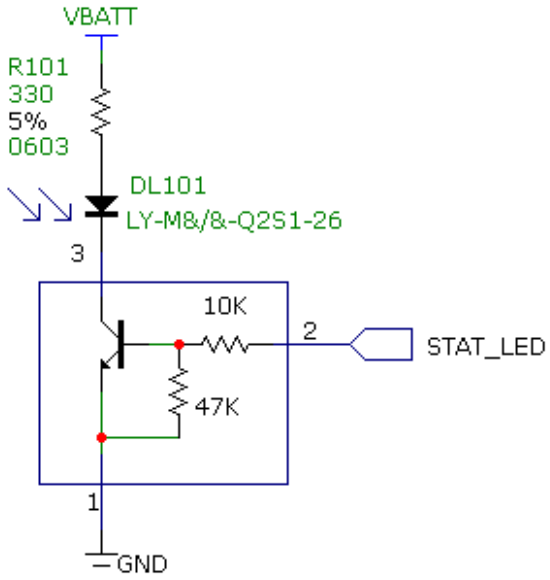
The STAT_LED pin status shows information on the network service availability and Call status.

In the GC864-QUAD/PY modules, the STAT_LED usually needs an external transistor to drive an external LED.

Therefore, the status indicated in the following table is reversed with respect to the pin status.

LED status	Device Status
Permanently off	Device off
Fast blinking (Period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (Period 3s, Ton 0,3s)	Registered full service
Permanently on	a call is active

A schematic example could be:



11.11. RTC Bypass Out

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing having only RTC going on when all the other parts of the device are off.

To this power output a backup capacitor can be added in order to increase the RTC autonomy during power off of the battery. NO Devices must be powered from this pin.

11.12. VAUX1 Power Output

A regulated power supply output is provided in order to supply small devices from the module.

This output is active when the module is ON and goes OFF when the module is shut down.

The table below shows the operating range characteristics of the supply:

Operating Range – VAUX1 Power Supply

	Min	Typical	Max
Output voltage	2.75V	2.85V	2.95V
Output current			100mA
Output bypass capacitor (inside the module)			2.2µF

12. DAC and ADC Section

12.1. DAC Converter

12.1.1. Description

The GC864-QUAD / PY module provides a Digital to Analog Converter. The signal (named DAC_OUT) is available on pin 40 of the GC864-QUAD / PY module and on pin 17 of PL102 on EVK2 Board (CS1203).

The on board DAC is a 10-bit converter, able to generate a analogue value based a specific input in the range from 0 up to 1023. However, an external low-pass filter is necessary.

	Min	Max	Units
Voltage range (filtered)	0	2,6	Volt
Range	0	1023	Steps

The precision is 10 bits, so if we consider that the maximum voltage is 2V, the integrated voltage could be calculated with the following formula:

Integrated output voltage = 2 * value / 1023

DAC_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.

12.1.2. Enabling DAC

The AT command below is available to use the DAC function:

AT#DAC[=<enable>[,<value>]]

<value> – scale factor of the integrated output voltage (0–1023, with 10 bit precision), and it must be present if <enable>=1.

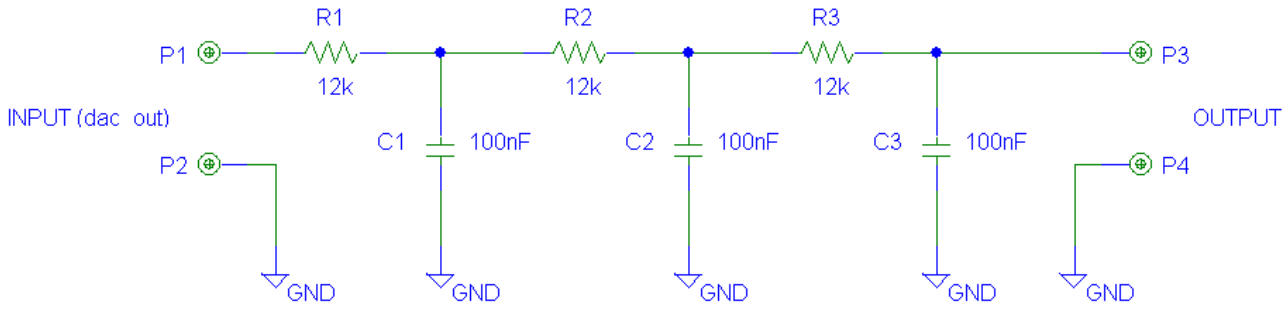
Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

NOTE:

The DAC frequency is selected internally. D/A converter must not be used during POWERSAVING.

12.1.3. Low Pass Filter Example



12.2. ADC Converter

12.2.1. Description

The on board A/D are 11-bit converter. They are able to read a voltage level in the range of 0÷2 volts applied on the ADC pin input, store and convert it into 11 bit word.

	Min	Max	Units
Input Voltage range	0	2	Volt
AD conversion	-	11	bits
Resolution	-	< 1	mV

The GC864-QUAD / PY module provides 3 Analog to Digital Converters. The input lines are:

ADC_IN1 available on Pin 37 and Pin 19 of PL102 on EVK2 Board (CS1203).

ADC_IN2 available on Pin 38 and Pin 20 of PL102 on EVK2 Board (CS1203).

ADC_IN3 available on Pin 39 and Pin 21 of PL102 on EVK2 Board (CS1203).

12.2.2. Using ADC Converter

The AT command below is available to use the ADC function:

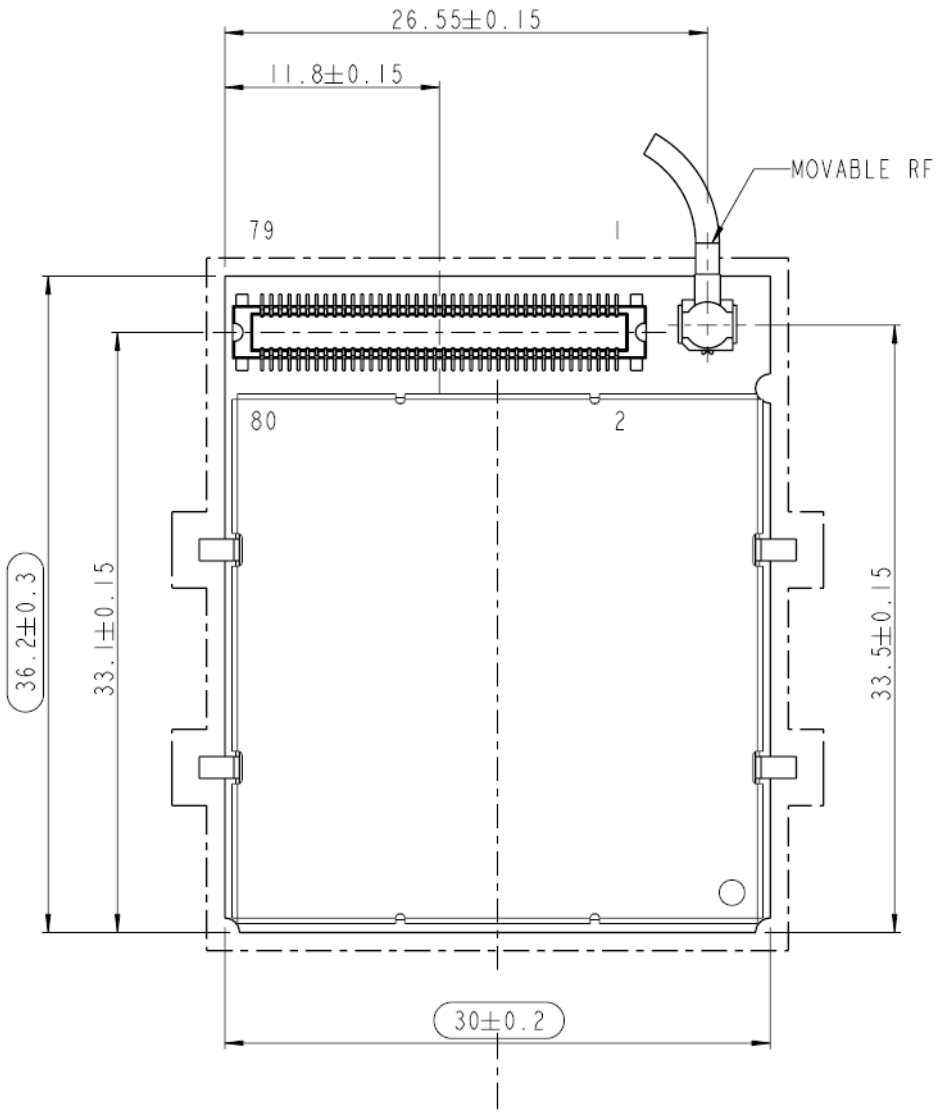
AT#ADC=1,2

The read value is expressed in mV.

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

13. Mounting the GC864-QUAD/PY on the Board

The position of the Molex board to board connector and the pin 1 are shown in the following picture.



NOTE:

The metal tabs present on GC864-QUAD/PY must be connected to GND.

This module could not be processed with a reflow.

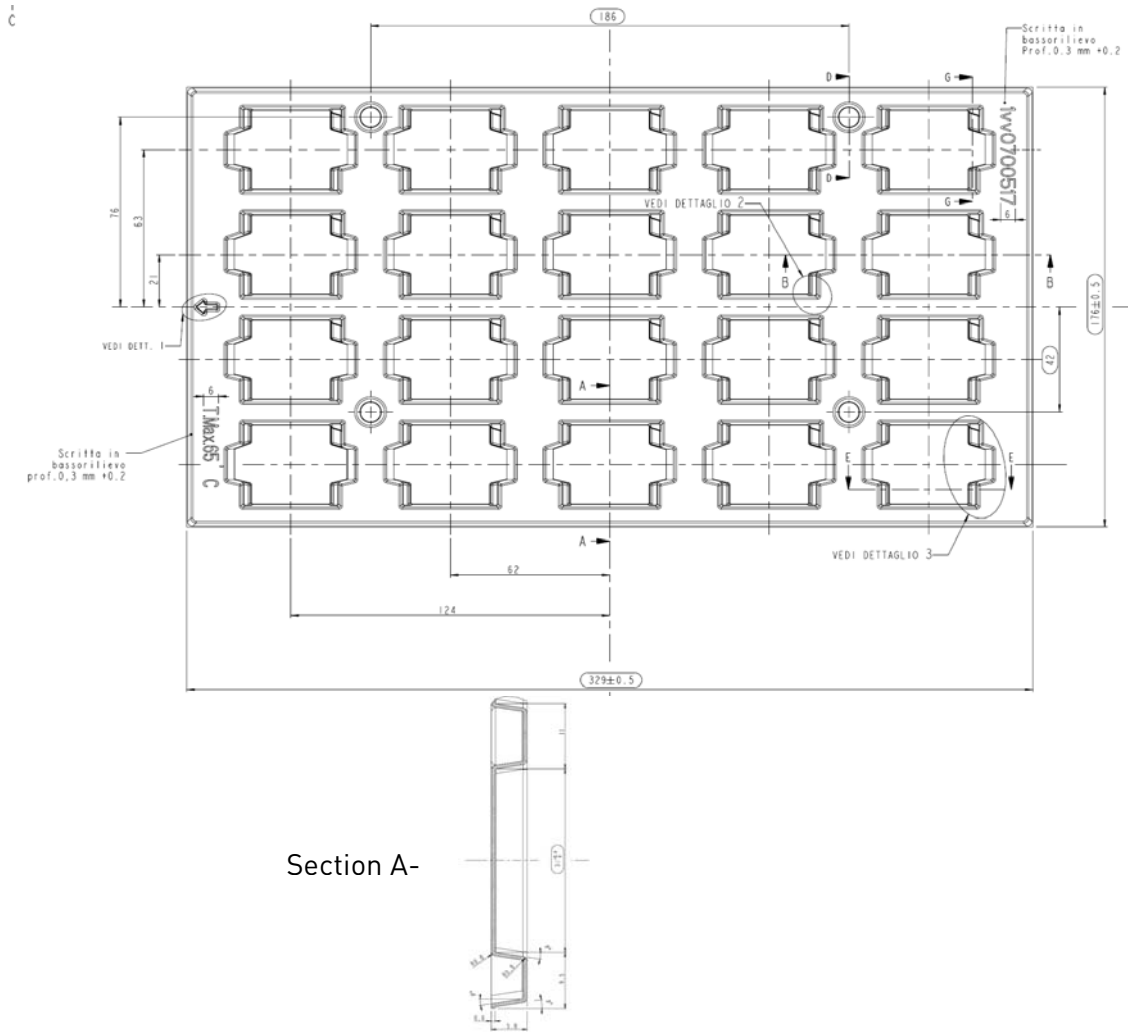
13.1.1. Debug of the GC864-QUAD/PY in Production

To test and debug the mounting of the GC864, we strongly recommend to foreseen test pads on the host PCB, in order to check the connection between the GC864-QUAD/PY itself and the application and to test the performance of the module connecting it with an external computer. Depending by the customer application, these pads include, but are not limited to the following signals:

- TXD
- RXD
- ON/OFF
- RESET
- GND
- VBATT
- TX_TRACE
- RX_TRACE
- PWRMON

14. Packing System

The Telit GC864-QUAD and GC864-PY are packaged on trays of 20 pieces each.



The size of the tray is: 329 x 176mm.

WARNING:

These trays can withstand at the maximum temperature of 65° C.

15. Conformity Assessment Issues

The Telit GC864 has been assessed in order to essential requirements of the R&TTE Directive Equipment & Telecommunications Terminal demonstrate the conformity against the harmonized final involvement of a Notified Body.

CE 0168

If the module is installed in conformance to the Telit installation manuals, no further evaluation under **Article 3.2** of the R&TTE Directive and do not require further involvement of a R&TTE Directive Notified Body for the final product.

In all other cases, or if the manufacturer of the final product is in doubt, then the equipment integrating the radio module must be assessed against **Article 3.2** of the R&TTE Directive.

In all cases the assessment of the final product must be made against the Essential requirements of the R&TTE Directive **Articles 3.1(a)** and **(b)**, Safety and EMC respectively, and any relevant Article 3.3 requirements.

This Product Description, the Hardware User Guide and Software User Guide contain all the information you may need for developing a product meeting the R&TTE Directive.

Furthermore the GC864 module is FCC Approved as module to be installed in other devices. This device is to be used only for fixed and mobile applications. If the final product after integration is intended for portable use, a new application and FCC is required.

The GC864 is conforming to the following US Directives:

- Use of RF Spectrum. Standards: FCC 47 Part 24 (GSM 1900)
- EMC (Electromagnetic Compatibility). Standards: FCC47 Part 15

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

To meet the FCC's RF exposure rules and regulations:

- The system antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all the persons and must not be co-located or operating in conjunction with any other antenna or transmitter.
- The system antenna(s) used for this module must not exceed 1.4dBi (850MHz) and 3.0dBi (1900MHz) for mobile and fixed or mobile operating configurations.
- Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and to have their complete product tested and approved for FCC compliance.

16. SAFETY RECOMMENDATIONS

NOTE:

Read this section carefully to ensure the safe operation.

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the zfollowing areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc
- Where there is risk of explosion such as gasoline stations, oil refineries, etc

It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations.

The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force.

Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation EN 50360.

The European Community provides some Directives for the electronic equipments introduced on the market. All the relevant information are available on the European Community website:

http://europa.eu.int/comm/enterprise/rtte/dir99-5.htm

The text of the Directive 99/05 regarding telecommunication equipments is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://europa.eu.int/comm/enterprise/electr_equipment/index_en.htm