

CE910-DUAL Hardware User Guide

1w0301010 Rev .0 – 2012-07-10



APPLICABILITY TABLE

PRODUCT
CE910-DUAL



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Contents

1. Introduction	8
1.1. Scope	8
1.2. Audience	8
1.3. Contact Information, Support	8
1.4. Document Organization	9
1.5. Text Conventions	10
1.6. Related Documents	10
2. General Product Description	11
2.1. Overview	11
2.2. Product Specifications	12
2.3. RoHS Compliance	13
3. CE910-DUAL Module Connections	14
3.1. Pin-Out	14
3.1.1 LGA Pads Layout	19
4. Hardware Commands	20
4.1. Turning on the CE910-DUAL module	20
4.1.1 Initialization and Activation State	20
4.2. Turning off the CE910-DUAL module	22
4.2.1 Shutdown by Software Command	23
4.2.2 Hardware Shutdown	23
4.3. Hardware Unconditional Shutdown	24
4.4. Summary of Turning ON and OFF the Module	25
5. Power Supply	26
5.1. Power Supply Requirements	26
5.2. General Design Rules	27
5.2.1 Electrical Design Guidelines	27
5.2.2 + 5V Input Source Power Supply Design Guidelines	27
5.2.3 +12V Input Source Power Supply Design Guidelines	28
5.2.4 Battery Source Power Supply Design Guidelines	29
5.2.5 Thermal Design Guidelines	29



- 5.2.6. Power Supply PCB layout Guidelines 30
- 6. Antenna..... 32**
 - 6.1. CDMA Antenna Requirements..... 32
 - 6.2. CDMA antenna – PCB line Guidelines 33
 - 6.3. CDMA Antenna installation Guidelines..... 34
- 7. USB Port..... 35**
- 8. Serial Port..... 36**
 - 8.1. Modem Serial Port 1 36
 - 8.2. RS232 Level Translation 39
- 9. Audio Section Overview 41**
 - 9.1. MIC connection 42
 - 9.2. LIN-IN connection..... 43
 - 9.3. EAR connection 44
- 10. General Purpose I/O..... 45**
 - 10.1. Logic Level Specification 46
 - 10.2. Using a GPIO Pad as Input..... 47
 - 10.3. Using a GPIO Pad as Output 47
 - 10.4. Using the Temperature Monitor Function 48
 - 10.4.1. Short Description..... 48
 - 10.5. Indication of Network Service Availability..... 48
 - 10.6. RTC Bypass Output..... 49
 - 10.7. VAUX/PWRMON Power Output..... 49
- 11. ADC section 50**
 - 11.1. Description 50
 - 11.2. Using ADC Converter..... 50
- 12. Mounting the Module on your Board..... 51**
 - 12.1. General 51
 - 12.2. Module Finishing & Dimensions 51
 - 12.3. Recommended foot print for the application..... 52



- 12.4. Stencil 53
- 12.5. PCB Pad Design..... 53
- 12.6. Recommendations for PCB Pad Dimensions (mm)..... 53
- 12.7. Solder Paste 55
 - 12.7.1. Solder Reflow 55
- 12.8. Debug in production 56
- 13. Packing System 57**
 - 13.1. Tray Drawing 57
 - 13.2. Moisture Sensibility..... 57
- 14. Application Design Guide 58**
 - 14.1. Download and Debug Port..... 58
- 15. Conformity Assessment Issues (Problèmes d'évaluation de conformité) 59
- 16. Safety Recommendations..... 62
- 17. Document History..... 63



1. Introduction

1.1. Scope

The aim of this document is the description of typical hardware solutions useful for developing a product with the Telit CE910-DUAL module.

1.2. Audience

This document is intended for Telit customers who are about to implement their applications using our CE910-DUAL modules.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

<http://www.telit.com/en/products/technical-support-center/contact.php>

For detailed information about where to buy the Telit modules or for recommendations on accessories and components visit:

<http://www.telit.com>

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Please keep us informed of comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.



1.4. Document Organization

This document contains the following chapters:

Chapter 1: “Introduction” provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: “General Product Description” gives an overview of the features of the product.

Chapter 3: “CE910-DUAL Module Connections” deals with the pin out configuration and layout.

Chapter 4: “Hardware Commands” How to operate the module via hardware.

Chapter 5: “Power supply” Power supply requirements and general design rules.

Chapter 6: “Antenna” The antenna connection and board layout design are the most important parts in the full product design.

Chapter 7: “USB Port” The USB port on the Telit CE910-DUAL is the core of the interface between the module and OEM hardware.

Chapter 8: “Serial ports” Refers to the serial ports of the Telit CE910-DUAL.

Chapter 9: “Audio Section overview” Refers to the audio blocks of the Base Band Chip of the CE910-DUAL Telit Module.

Chapter 10: “General Purpose I/O” How the general purpose I/O pads can be configured.

Chapter 11: “ADC section” Deals with this one kind of converter.

Chapter 12: “Mounting the CE910-DUAL on the application board” Mechanical dimensions and recommendations on how to mount the module on the user’s board.

Chapter 13: “Packing System” Deals with packing system.

Chapter 14: “Application Design Guide” Deals with the design of host system for download or upgrade.

Chapter 15: “Conformity Assessment Issues” provides some fundamental hints about the conformity assessment that the final application might need.

Chapter 16: “Safety Recommendation” provides some safety recommendations that must be followed by the customer in the design of the application that makes use of the Telit CE910-DUAL.

Chapter 17: “Document History” provides document revision history of the Telit CE910-DUAL.



1.5. Text Conventions



Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.



Caution or Warning – Alerts the user to important points about integrating the module. If these points are not followed, the module and end user equipment may fail or malfunction.



Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- CE910-DUAL Software User Guide, 1v0301011
- CE910-DUAL AT Commands Reference Guide, 80399ST10111A
- Telit EVK2 User Guide, 1v0300704



2. General Product Description

2.1. Overview

The aim of this document is the description of typical hardware solutions useful for developing a product with the Telit CE910-DUAL module.

In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace all hardware solutions and products that may be designed. The solutions to be avoided must be considered as mandatory. While the suggested hardware configurations must not be considered mandatory, the information given must be used as a guide and a starting point for properly developing a product with the Telit CE910-DUAL module.



NOTE:

The integration of the CDMA 1xRTT module within a user application must be done according to the design rules described in this manual.

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2.2. Product Specifications

CE910-DUAL Specifications	
Air Interface	CDMA 1xRTT
Frequency Bands	800/1900MHz
Data Service	CDMA 1xRTT: 153.6 Kbps (full-duplex)
Max. RF out power	<ul style="list-style-type: none"> • CDMA BC0: Power class 3 (24.5dBm) for 1xRTT • CDMA BC1: Power class 2 (24.5dBm) for 1xRTT
Typical conducted sensitivity	<ul style="list-style-type: none"> • CDMA BC0: Better than -108dBm • CDMA BC1: Better than -107dBm
Device dimensions	28.2mm(L) x 28.2mm(W) x 2.4mm(T) : 2 shields * 2.05mm(T)(1 shield) version is coming soon
Weight	4.7g (2 shields)
Operational temperature	<ul style="list-style-type: none"> • -30 ~ +60°C: The module is fully functional(*) in the entire temperature range and fully meets the 3GPP2 specifications. • -30 ~ +85°C: The module is fully functional(*) in the entire temperature range. Behavior outside the range of -30 ~ +60°C might deviate from 3GPP2 specification. <p>(*)Functional: the module is able to make and receive voice calls, data calls, and SMS.</p>
Storage temperature	-40 ~ +85°C
Operating voltage	3.4 ~ 4.2V
IO voltage	1.8V
Interface	<ul style="list-style-type: none"> • 144 Land-Grid-Array interface • 10 general I/O ports maximum including multi-functional I/Os • State LED output • 1 A/D converter • Full RS232 CMOS UART: baud rate up to 4Mbps • Reserved two wires CMOS UART for debugging • USB 2.0: baud rate up to 12Mbps
Antenna	Primary antenna, 800/1900MHz



Audio	<ul style="list-style-type: none"> Analog audio interface (1 EAR/MIC)
Message	SMS (MO/MT)
Approvals	<ul style="list-style-type: none"> Regulatory: FCC, IC Carrier: Verizon, Sprint (TBD)

2.3. RoHS Compliance

As a part of Telit’s corporate policy of environmental protection, the CE910-DUAL complies with the RoHS (Restriction of Hazardous Substances) directive of the European Union (EU directive 2002/95/EG).



3. CE910-DUAL Module Connections

3.1. Pin-Out

Pin	Signal	I/O	Function	Internal Pull up	Type
USB HS 2.0 Communication Port					
B15	USB D+	I/O	USB differential Data(+)		
C15	USB D-	I/O	USB differential Data(+)		
A13	VBUS	I	Power sense for the internal USB transceiver		5V
Asynchronous UART – Prog. / data +HW Flow Control					
N15	C103/TXD	I	Serial data input from DTE		1.8V
M15	C104/RXD	O	Serial data output to DTE		1.8V
M14	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE		1.8V
L14	C105/RTS	I	Input for Request to send signal (RTS) from DTE		1.8V
P15	C106/CTS	O	Output for Clear to send signal (CTS) to DTE		1.8V
N14	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE		1.8V
P14	C107/DSR	O	Output for Data set ready signal (DSR) to DTE		1.8V
R14	C125/RING	O	Output for Ring indicator signal (RI) to DTE		1.8V
Asynchronous Auxiliary UART(Reserved)					
D15	Reserved	-	Reserved		
E15	Reserved	-	Reserved		
RUM Card Interface(Reserved)					
A3	Reserved	-	Reserved		
A4	Reserved	-	Reserved		
A5	Reserved	-	Reserved		
A6	Reserved	-	Reserved		
A7	Reserved	-	Reserved		
Digital Voice interface (Reserved)					
B9	Reserved	-	Reserved		
B6	Reserved	-	Reserved		
B7	Reserved	-	Reserved		
B8	Reserved	-	Reserved		
Analog Voice Interface					
B2	EAR+	AO	Earphone signal output, phase +		1.8V
B3	EAR-	AO	Earphone signal output, phase -		1.8V
B4	MIC+	AI	Microphone input, phase +		1.8V
B5	MIC-	AI	Microphone input, phase -		1.8V
SPI (Reserved)					
D15	Reserved	-	Reserved		
E15	Reserved	-	Reserved		
F15	Reserved	-	Reserved		
H14	Reserved	-	Reserved		
Digital IO					



Pin	Signal	I/O	Function	Internal Pull up	Type
C8	GPIO 01	I/O	GPIO 01 / STAT LED		1.8V
C9	GPIO 02	I/O	GPIO 02		1.8V
C10	GPIO 03	I/O	GPIO 03		1.8V
C11	GPIO 04	I/O	GPIO 04		1.8V
B14	GPIO 05	I/O	GPIO 05		1.8V
C12	GPIO 06	I/O	GPIO 06		1.8V
C13	GPIO 07	I/O	GPIO 07		1.8V
K15	GPIO 08	I/O	GPIO 08		1.8V
L15	GPIO 09	I/O	GPIO 09		1.8V
G15	GPIO 10	I/O	GPIO 10		1.8V
ADC Section					
B1	ADC_IN	AI	Analog/Digital converter input		Analog
RF Section					
K1	Antenna	I/O	CDMA Antenna (50Ohm)		RF
Miscellaneous Function					
P11	Reserved	-	Reserved		
R13	HW_SHUTDOWN*	I	Hardware unconditional shutdown		VBATT
R12	ON_OFF*	I	Input Command for Power ON/Software shutdown		1.8V
C14	VRTC	I	VRTC Backup Capacitor		Power
R11	VAUX/PWRMON	O	Supply Output for external accessories / Power ON Monitor		1.8V
Power Supply					
M1	VBATT	-	Main Power Supply (Baseband)		Power
M2	VBATT	-	Main Power Supply (Baseband)		Power
N1	VBATT_PA	-	Main Power Supply (PAM)		Power
N2	VBATT_PA	-	Main Power Supply (PAM)		Power
P1	VBATT_PA	-	Main Power Supply (PAM)		Power
P2	VBATT_PA	-	Main Power Supply (PAM)		Power
E1	GND	-	Ground		
G1	GND	-	Ground		
H1	GND	-	Ground		
J1	GND	-	Ground		
L1	GND	-	Ground		
A2	GND	-	Ground		
E2	GND	-	Ground		
F2	GND	-	Ground		
G2	GND	-	Ground		
H2	GND	-	Ground		
J2	GND	-	Ground		
K2	GND	-	Ground		
L2	GND	-	Ground		
R2	GND	-	Ground		
M3	GND	-	Ground		
N3	GND	-	Ground		
P3	GND	-	Ground		



Pin	Signal	I/O	Function	Internal Pull up	Type
R3	GND	-	Ground		
D4	GND	-	Ground		
M4	GND	-	Ground		
N4	GND	-	Ground		
P4	GND	-	Ground		
R4	GND	-	Ground		
N5	GND	-	Ground		
P5	GND	-	Ground		
R5	GND	-	Ground		
N6	GND	-	Ground		
P6	GND	-	Ground		
R6	GND	-	Ground		
P8	GND	-	Ground		
R8	GND		Ground		
P9	GND	-	Ground		
P10	GND	-	Ground		
R10	GND	-	Ground		
M12	GND	-	Ground		
B13	GND	-	Ground		
P13	GND	-	Ground		
E14	GND	-	Ground		
Reserved					
C1	Reserved	-	Reserved		
D1	Reserved	-	Reserved		
F1	Reserved	-	Reserved		
C2	Reserved	-	Reserved		
D2	Reserved	-	Reserved		
C3	Reserved	-	Reserved		
D3	Reserved	-	Reserved		
E3	Reserved	-	Reserved		
F3	Reserved	-	Reserved		
G3	Reserved	-	Reserved		
H3	Reserved	-	Reserved		
J3	Reserved	-	Reserved		
K3	Reserved	-	Reserved		
L3	Reserved	-	Reserved		
C4	Reserved	-	Reserved		
C5	Reserved	-	Reserved		
C6	Reserved	-	Reserved		
C7	Reserved	-	Reserved		
N7	Reserved	-	Reserved		
P7	Reserved	-	Reserved		
A8	Reserved	-	Reserved		
N8	Reserved	-	Reserved		
A9	Reserved	-	Reserved		



Pin	Signal	I/O	Function	Internal Pull up	Type
N9	Reserved	-	Reserved		
R7	Reserved	-	Reserved		
R9	Reserved	-	Reserved		
A10	Reserved	-	Reserved		
B10	Reserved	-	Reserved		
B11	Reserved	-	Reserved		
N10	Reserved	-	Reserved		
A11	Reserved	-	Reserved		
N11	Reserved	-	Reserved		
A12	Reserved	-	Reserved		
B12	Reserved	-	Reserved		
D12	Reserved	-	Reserved		
N12	Reserved	-	Reserved		
P12	Reserved	-	Reserved		
D13	Reserved	-	Reserved		
E13	Reserved	-	Reserved		
F13	Reserved	-	Reserved		
G13	Reserved	-	Reserved		
H13	Reserved	-	Reserved		
J13	Reserved	-	Reserved		
K13	Reserved	-	Reserved		
L13	Reserved	-	Reserved		
M13	Reserved	-	Reserved		
N13	Reserved	-	Reserved		
A14	Reserved	-	Reserved		
D14	Reserved	-	Reserved		
F14	Reserved	-	Reserved		
G14	Reserved	-	Reserved		
J14	Reserved	-	Reserved		
K14	Reserved	-	Reserved		
H15	Reserved	-	Reserved		
J15	Reserved	-	Reserved		



WARNING:

Reserved pins must not be connected.





NOTE:

Almost all pins not in use must be left disconnected. The only exceptions are the following pins:

PAD	Signal
M1,M2,N1,N2,P1,P2	VBATT&VBATT_PA
E1,G1,H1,J1,L1,A2,E2,F2,G2,H2,J2,K2,L2,R2,M3,N3,P3,R3,D4,M4,N4,P4,R4,N5,P5,R5,N6,P6,R6,P8,R8,P9,P10,R10,M12,B13,P13,E14	GND
R12	ON/OFF*
R13	HW_SHUTDOWN*
B15	USB_D+
C15	USB_D-
A13	VBUS
N15	C103/TXD
M15	C104/RXD
L14	C105/RTS
P15	C106/CTS
D15	TXD_AUX
E15	RXD_AUX
K1	Antenna

RTS must be connected to the GND (on the module side) if flow control is not used.

The above pins are also necessary to debug the application incorporating the module.



3.1.1 LGA Pads Layout

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
1		ADC_IN1	RES	RES	GND	RES	GND	GND	GND	ANTENNA	GND	VBATT	VBATT_PA	VBATT_PA	
2	GND	EAR+	RES	RES	GND	GND	GND	GND	GND	GND	GND	VBATT	VBATT_PA	VBATT_PA	GND
3	RES	EAR-	RES	RES	RES	RES	RES	RES	RES	RES	RES	GND	GND	GND	GND
4	RES	MIC+	RES	GND								GND	GND	GND	GND
5	RES	MIC-	RES										GND	GND	GND
6	RES	RES	RES										GND	GND	GND
7	RES	RES	RES										RES	RES	RES
8	RES	RES	GPIO_01 / STAT_LED										RES	GND	GND
9	RES	RES	GPIO_02										RES	GND	RES
10	RES	RES	GPIO_03										RES	GND	GND
11	RES	RES	GPIO_04										RES	RES	VALX/PWRM ON
12	RES	RES	GPIO_06	RES								GND	RES	RES	ON_OFF*
13	USB_VUSB	GND	GPIO_07	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	GND	HW_SHUTO OWN*
14	RES	GPIO_05	VRTC	RES	GND	RES	RES	RES	RES	RES	C105/RTS	C108/DTR	C109/DCD	C107/DSR	C125/RING
15	USB_D+	USB_D-	RES	RES	RES	RES	GPIO_10	RES	RES	GPIO_08	GPIO_09	C104/RXD	C103/TXD	C106/CTS	

Top View



NOTE:

The pin defined as **RES** must be considered RESERVED and not connected on any pin in the application. The related area on the application has to be kept empty.



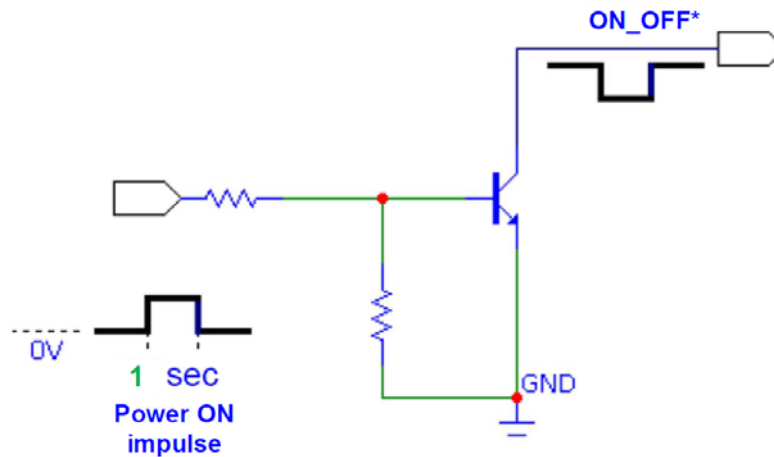
4. Hardware Commands

4.1. Turning on the CE910-DUAL module

To turn on the CE910-DUAL, the pad ON_OFF* must be tied low for at least 1 second and then released.

The maximum current that can be drained from the ON_OFF* pad is 0.1 mA.

A simple circuit to power on the module is illustrated below:

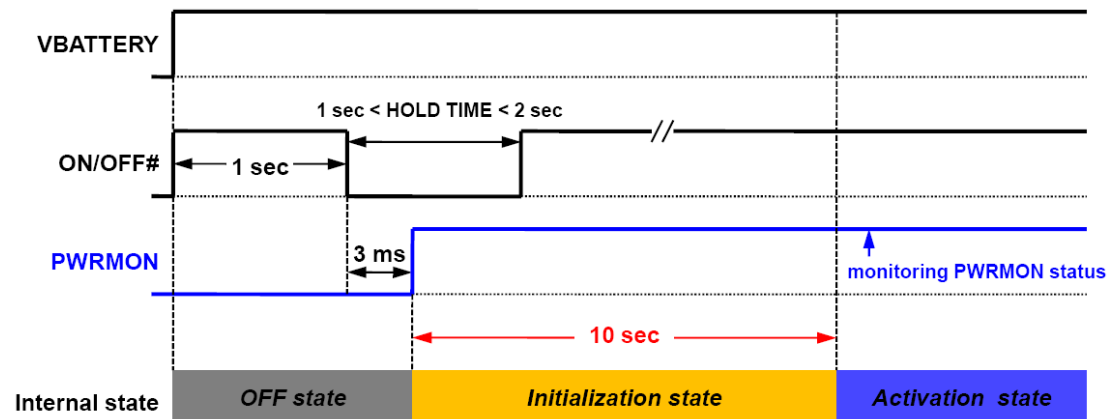


4.1.1. Initialization and Activation State

Upon turning on CE910-DUAL module, the CE910-DUAL module is not active yet because the boot sequence of CE910-DUAL is still executing internally. It takes about 10 seconds to complete the initialization of the module internally.

For this reason, it would be useless to try to access CE910-DUAL during the Initialization state as below. The CE910-DUAL module needs at least 10 seconds after the PWRMON goes High to become operational by reaching the activation state.





During the *Initialization state*, any kind of AT-command is not available. DTE must wait for the *Activation state* to communicate with CE910-DUAL.

To check if the CE910-DUAL has powered on, the hardware line VAUX/PWRMON must be monitored. When VAUX/PWRMON goes high, the module has powered on.



NOTE:

Do not use any pull up resistor on the ON_OFF* line. It is pulled up internally. Using a pull up resistor may bring latch up problems on the CE910-DUAL power regulator and improper power on/off of the module. The line ON_OFF* must be connected only in open collector configuration.



NOTE:

In this document all the lines are inverted. Active low signals are labeled with a name that ends with "*" or with a bar over the name.



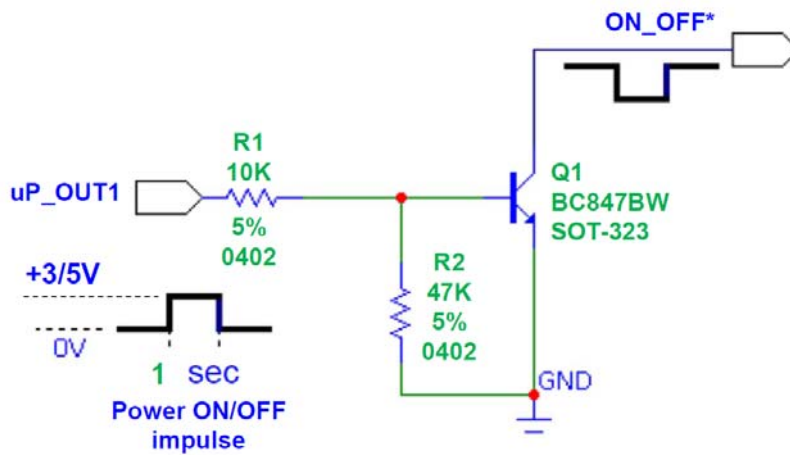
NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CE910-DUAL module when the module is powered OFF or during an ON/OFF transition.

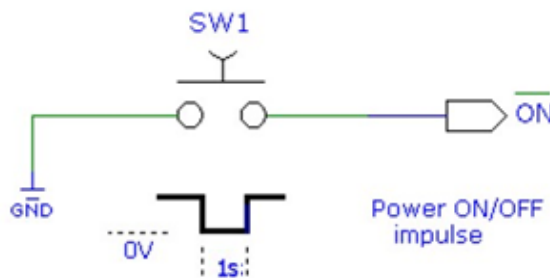
For example:

1. To drive the ON_OFF* pad with a totem pole output of a +3/5 V microcontroller (uP_OUT1):





2. To drive the ON_OFF* pad directly with an ON/OFF button:



4.2. Turning off the CE910-DUAL module

Turning off the device can be done in two ways:

- By software command (see CE910-DUAL Software User Guide)
- By hardware shutdown

When the device is shut down by software command or by hardware shutdown, it issues a detach request to the network that informs the network that the device will no longer be reachable.



NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CE910-DUAL when the module is powered OFF or during an ON/OFF transition.



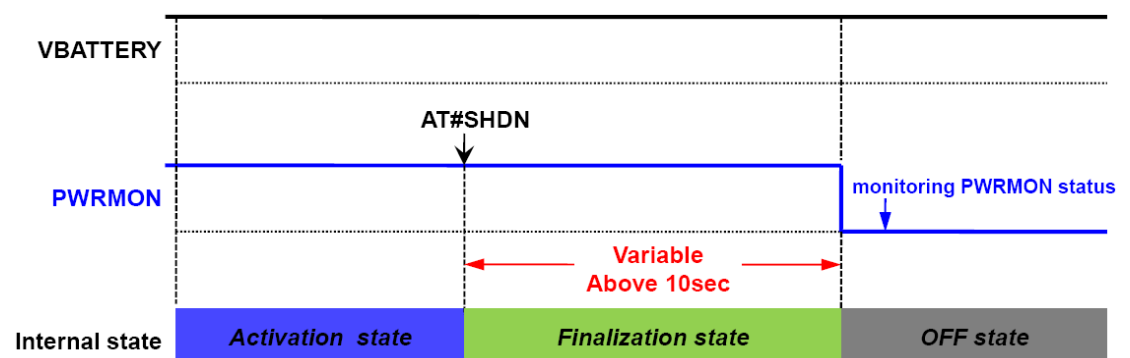
4.2.1. Shutdown by Software Command

The CE910-DUAL can be shut down by a software command.

When a shutdown command is sent, the CE910-DUAL goes into the finalization state and will shut down PWRMON at the end of this state.

The period of the finalization state can vary according to the state of the CE910-DUAL so it cannot be fixed definitely.

Normally it will be above 10 seconds after sending a shutdown command and DTE should monitor the status of VAUX/PWRMON to see the actual power off.



TIP:

To check if the device has powered off hardware line VAUX/PWRMON must be monitored. When VAUX/PWRMON goes low, the device has powered off.

4.2.2. Hardware Shutdown

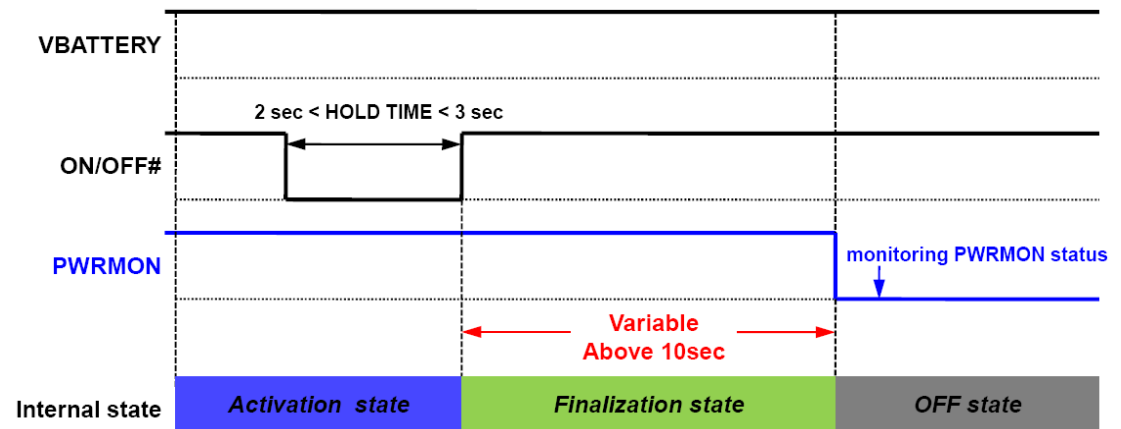
To turn OFF the CE910-DUAL the pad ON_OFF* must be tied low for at least 2 seconds and then released. The same circuitry and timing for the power on must be used.

When the hold time of ON_OFF* is above 2 seconds, the CE910-DUAL goes into the finalization state and will shut down VAUX/PWRMON at the end of this state.

The period of the finalization state can vary according to the state of the CE910-DUAL so it cannot be fixed definitely.

Normally it will be above 10 seconds after releasing ON_OFF* and DTE should monitor the status of PWRMON to see the actual power off.





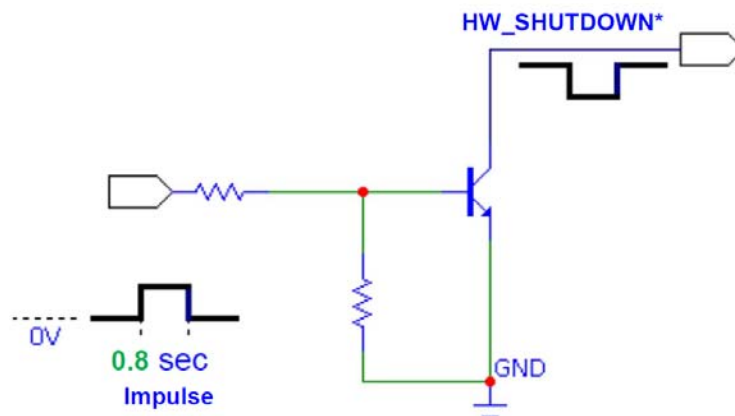
TIP:

To check if the device has powered off, hardware line VAUX/PWRMON must be monitored. When VAUX/PWRMON goes low, the device has powered off.

4.3. Hardware Unconditional Shutdown

To unconditionally shutdown the CE910-DUAL, the pad HW_SHUTDOWN* must be tied low for at least 800 milliseconds and then released.

A simple circuit to unconditionally shutdown the module is illustrated below:



NOTE:

Do not use any pull up resistor on the HW_SHUTDOWN* line or any totem pole digital output. Using a pull up resistor may bring latch up problems on the CE910-DUAL power regulator and result in improper functioning of the module. The line HW_SHUTDOWN* must be connected only in open collector configuration.



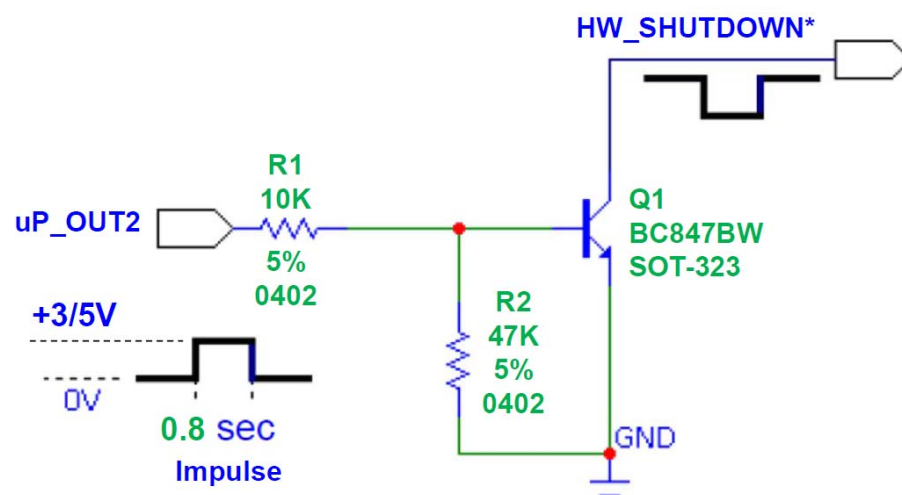


TIP:

The unconditional hardware Shutdown must always be implemented on the boards and the software must use it only as an emergency exit procedure.

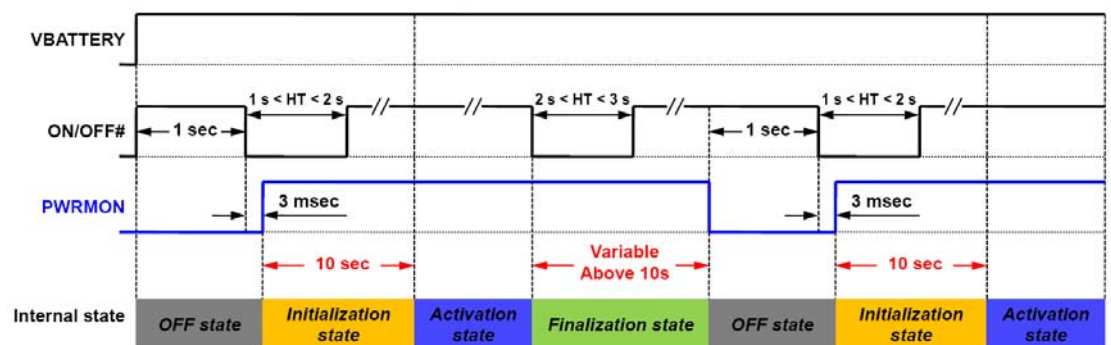
For example:

To drive the HW_SHUTDOWN* pad with a totem pole output of a +3/5 V microcontroller (uP_OUT2):



4.4. Summary of Turning ON and OFF the Module

The chart below describes the overall sequences for turning the module ON and OFF.



5. Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product's overall performance. Read carefully the requirements and the guidelines that follow for a proper design.

5.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfill the following requirements:

Power Supply	
Nominal Supply Voltage	3.8V
Max Supply Voltage	4.2V
Supply Voltage Range	3.4V ~ 4.2V

Current Consumption		
Mode	Average (mA)	Mode Description
Power off current (Typical)		140uA(*)
Standby mode		No call in progress (slot cycle index=2)
AT+CFUN=1	29	Normal mode; full functionality of the module
AT+CFUN=4	27	Disabled TX and RX; modules is not registered on the network
AT+CFUN=0 or AT+CFUN=5	3	Power saving; CFUN=0 module registered on the network and can receive voice call or an SMS; but it is not possible to send AT commands; module wakes up with an unsolicited code (call or SMS) or rising RTS line. CFUN=5 full functionality with power saving; Module registered on the network can receive incoming call sand SMS
Tx and Rx mode		A call in progress



Max Power Mode	750(TBD)	CDMA 1x call
----------------	----------	--------------

(*¹)The off current is the total supply current from the main battery with the XO regulator ON, 19.2MHz XO ON and others are OFF.

(*²) Standby current consumption depends on network configuration or module configuration.



NOTE:

The Operating Voltage Range **MUST** never be exceeded. Special care must be taken in order to fulfill min/max supply voltage requirement.



TIP:

The electrical design for the power supply should be made ensuring it will be capable of a peak current output of at least 1A.

5.2. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout

5.2.1. Electrical Design Guidelines

The electrical design of the power supply depends strongly on the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

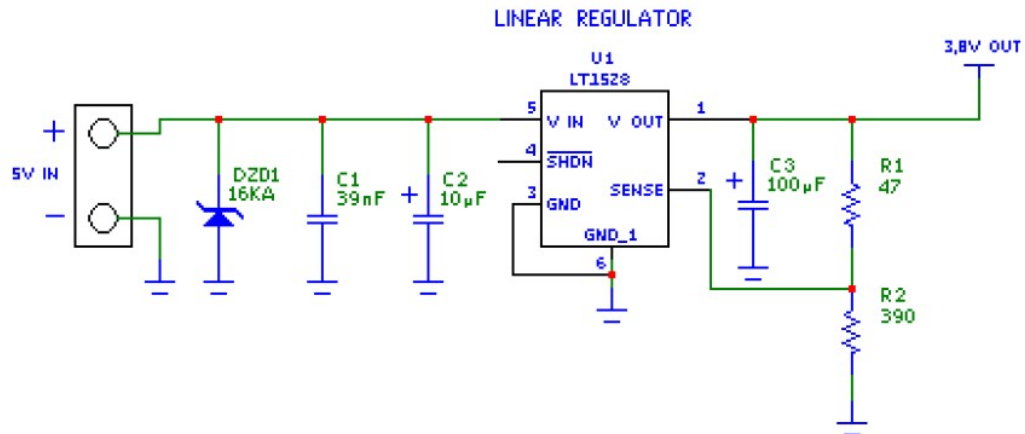
5.2.2. + 5V Input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there is not a big difference between the input source and the desired output so a linear regulator can be used. A switching power supply will not be suitable because of the low drop-out requirements.
- When using a linear regulator, a proper heat sink must be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the CE910-DUAL. A 100µF tantalum capacitor is usually suited.



- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode must be inserted close to the power input in order to save the CE910-DUAL from power polarity inversion.

An example of a linear regulator with 5V input:



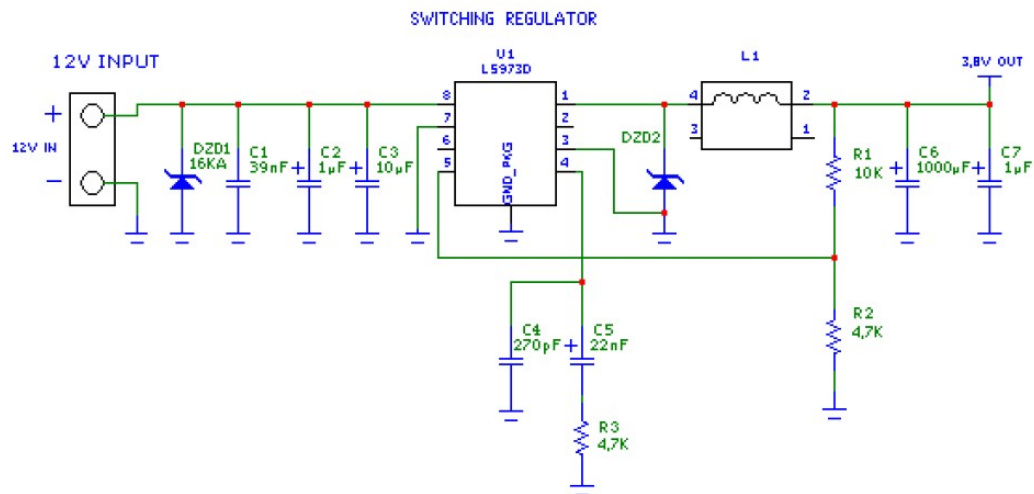
5.2.3. +12V Input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suitable and must not be used. A switching power supply would be preferable because of its better efficiency, especially with the 1A peak current load represented by CE910-DUAL.
- When using a switching regulator, a 500 kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case, the frequency and switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15.8V and this must be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks. A 100µF tantalum capacitor is usually suited for this.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For car applications a spike protection diode must be inserted close to the power input in order to clean the supply from spikes.



- A protection diode must be inserted close to the power input in order to save the CE910-DUAL from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is in the schematic below:



5.2.4. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V. A single 3.7V lithium-ion cell battery type is ideal to supply power to the Telit CE910-DUAL module.



WARNING:

The three battery cells (Ni/Cd or Ni/MH 3.6V nom. battery types or 4V PB types) **MUST NOT** be used directly because their maximum voltage can rise over the absolute maximum voltage for the CE910-DUAL and cause damage. **USE** only Li-Ion battery types.

- A bypass low (usually a 100uF tantalum) ESR capacitor with adequate capacity must be provided in order to cut the current absorption peaks.
- Make sure the low ESR capacitor (usually a tantalum) is rated at least 10V.
- A protection diode must be inserted close to the power input in order to protect the CE910-DUAL module from power polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 1A. The suggested battery capacity is from 500mAh to 1000mAh.

5.2.5. Thermal Design Guidelines

The thermal design for the power supply heat sink must be done with the following specifications:



Average current consumption during CDMA 1x @PWR level max : 750 mA



NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit via the network. The average current consumption hence varies significantly.

Considering the very low current during idle, especially if the Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

If we assume that the device stays in transmission for short periods of time (a few minutes) and then remains for quite a long time in idle (one hour), then the power supply always has time to cool down between the calls and the heat sink could be smaller than the calculated for 750mA maximum RMS current. There could even be a simple chip package (no heat sink).

Moreover in average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than 750 mA (usually around 300 mA).

For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating.

The heat generated by the CE910-DUAL must be taken into consideration during transmission at 24.5dBm max during calls. This generated heat will be mostly conducted to the ground plane under the CE910-DUAL. The application must be able to dissipate heat.

In the CDMA 1x mode, since CE910-DUAL emits RF signals continuously during transmission, special attention must be paid to how to dissipate the heat generated.

The current consumption will be up to about 750mA in CDMA 1x continuously at the maximum TX output power (24.5dBm). Thus, you must arrange the area on the application PCB must be as large as possible under CE910-DUAL.

The CE910-DUAL must be mounted on the large ground area of the application board and make many ground vias to dissipate the heat.

5.2.6. Power Supply PCB layout Guidelines

As seen in the electrical design guidelines, the power supply must have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct operation of the circuitry. A misplaced component can be useless or can even decrease the power supply performance.

- The bypass low ESR capacitor must be placed close to the Telit CE910-DUAL power input pads, or if the power supply is a switching type, the capacitor can be placed close to the inductor to cut the ripple if the PCB trace from the capacitor to CE910-DUAL is wide enough to ensure a drop-less connection even during the 1A current peaks.



- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 1A current peaks are absorbed. While a voltage drop of hundreds of mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If the application does not have an audio interface but only uses the data feature of the Telit CE910-DUAL, then this noise is not as disruptive and the power supply layout design can be more forgiving.
- The PCB traces to CE910-DUAL and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 1A current peaks are absorbed. This is a must for the same above-mentioned reasons. Try to keep this trace as short as possible.
- The PCB traces connecting the switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (usually 100-500 kHz).
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board must be done in a way to guarantee that the high current return paths in the ground plane are not overlapped with any noise sensitive circuitry such as the microphone amplifier/buffer or earphone amplifier.

The power supply input cables must be kept separate from noise sensitive lines such as microphone/earphone cables.



6. Antenna

The antenna connection and board layout design are the most important parts in the full product design and they strongly reflect on the product’s overall performance. Read carefully and follow the requirements and the guidelines for a proper design.

6.1. CDMA Antenna Requirements

The antenna for a Telit CE910-DUAL device must fulfill the following requirements:

CDMA Antenna Requirements	
Frequency range	Depending on the frequency band(s) provided by the network operator, the customer must use the most suitable antenna for that/those band(s)
Bandwidth	70 MHz in CDMA BC0 140 MHz in CDMA BC1
Gain	Gain < 5.12dBi in CDMA BC0 Gain < 6.12dBi in CDMA BC1
Impedance	50 Ohm
Input power	> 24.5dBm Average Power in CDMA
VSWR absolute max	≤ 5:1 (Limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (Limit to fulfill all regulatory requirement)

When using the Telit CE910-DUAL, since there’s no antenna connector on the module, the antenna must be connected to the CE910-DUAL antenna pad (K1) by means of a transmission line implemented in the PCB.

In the case that the antenna is not directly connected at the antenna pad of the CE910-DUAL, then a PCB line is required.



This transmission line shall fulfill the following requirements:

Antenna Line on PCB Requirements	
Characteristic Impedance	50Ohm
Max Attenuation	0.3dB
Coupling with other signals shall be avoided	
Cold End (Ground Plane) of antenna shall be equipotential to the CE910-DUAL ground pads	

Furthermore if the device is developed for the US and/or Canada market, it must comply with the FCC and/or IC approval requirements:

This device is to be used only for mobile and fixed application. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-Users must be provided with transmitter operation conditions for satisfying RF exposure compliance. OEM integrators must ensure that the end user has no manual instructions to remove or install the CE910-DUAL module. Antennas used for this OEM module must not exceed 5dBi gain for mobile and fixed operating configurations.

6.2. CDMA antenna – PCB line Guidelines

- Make sure that the transmission line’s characteristic impedance is 50ohm.
- Keep line on the PCB as short as possible since the antenna line loss shall be less than around 0.3dB.
- Line geometry should have uniform characteristics, constant cross section, avoid meanders and abrupt curves.
- Any kind of suitable geometry/structure can be used for implementing the printed transmission line afferent the antenna.
- If a Ground plane is required in line geometry, that plane has to be continuous and sufficiently extended so the geometry can be as similar as possible to the related canonical model.
- Keep, if possible, at least one layer of the PCB used only for the Ground plane; If possible, use this layer as reference Ground plane for the transmission line.
- It is wise to surround (on both sides) the PCB transmission line with Ground. Avoid having other signal tracks facing directly the antenna line track.
- Avoid crossing any un-shielded transmission line footprint with other tracks on different layers.
- The Ground surrounding the antenna line on PCB has to be strictly connected to the main Ground plane by means of via holes (once per 2mm at least) placed close to the ground edges facing line track.
- Place EM noisy devices as far as possible from CE910-DUAL antenna line.
- Keep the antenna line far away from the CE910-DUAL power supply lines.
- If EM noisy devices are present on the PCB hosting the CE910-DUAL, such as fast



switching ICs, take care of shielding them with a metal frame cover.

- If EM noisy devices are not present around the line use of geometries like Micro strip or Grounded Coplanar Waveguide are preferred since they typically ensure less attenuation when compared to a Strip line having same length.

6.3. CDMA Antenna installation Guidelines

- Install the antenna in a place covered by the CDMA signal.
- If the device antenna in the application is located greater then 20cm from the human body and there are no co-located transmitters then the Telit FCC/IC approvals can be re-used by the end product.
- Antenna shall not be installed inside metal cases.
- Antenna shall be installed also according to antenna manufacture instructions.



WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect CE910-DUAL or customer specific requirements from ESD event to Antenna port (K1).



7. USB Port

The CE910-DUAL module includes a Universal Serial Bus (USB) transceiver, which operates at USB Full-speed (12Mbits/sec).

It is compliant with the USB 2.0 specification and can be used for diagnostic monitoring, control and data transfers.

The table below describes the USB interface signals:

Pin	Signal	I/O	Function	Type
B15	USB_D+	I/O	USB differential Data(+)	
C15	USB_D-	I/O	USB differential Data(+)	
A13	VBUS	I	Power sense for the internal USB transceiver	5V

The USB_DPLUS and USB_DMINUS signals have a clock rate of 60MHz. The signal traces should be routed carefully. Trace lengths, number of vias and capacitive loading should be minimized. The impedance value should be as close as possible to 90 Ohms differential.



WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect CE910-DUAL or customer specific requirements from ESD event to USB lines (B15, C15 and A13).



8. Serial Port

The serial ports on the Telit CE910-DUAL are the interface between the module and OEM hardware.

At this moment 1 serial port is available on the module:

- Modem Serial Port 1 (Main)

Several configurations can be designed for the serial port on the OEM hardware.

The most common are:

- RS232 PC comport
- Microcontroller UART@1.8V(Universal Asynchronous Receiver Transmit)
- Microcontroller UART@5V or other voltages different from 1.8V

Depending on the type of serial port on the OEM hardware, a level translator circuit may be needed to make the system work.

Serial port 1 is a +1.8V UART with all the 7 RS232 signals.

The electrical characteristics of the serial port are explained in the following tables:

Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on non-power pin with respect to ground	-0.3	+2.3V

Operating Range - Interface levels

Parameter	Min	Max
Input high level	1.5V	2.1 V
Input low level	0V	0.35V
Output high level	1.35V	1.8V
Output low level	0V	0.45V

8.1. Modem Serial Port 1

Serial port 1 on the CE910-DUAL is a +1.8V UART with all 7 RS232 signals.



It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

Pin	Signal	I/O	Function	Type
N14	DCD - dcd_uart	O	Data Carrier Detect	B-PU, 1.8V
M15	RXD - Tx_uart	O	Transmit line *see Note	B-PU, 1.8V
N15	TXD - Rx_uart	I	Receive line *see Note	B-PD, 1.8V
M14	DTR - dtr_uart	I	Data Terminal Ready	B-PU, 1.8V
P14	DSR - dsr_uart	O	Data Set Ready	B-PD, 1.8V
L14	RTS - rts_uart	I	Request to Send	B-PD, 1.8V
P15	CTS - cts_uart	O	Clear to Send	B-PD, 1.8V
R14	RI - ri_uart	O	Ring Indicator	B-PU, 1.8V

The following table shows the typical input value of internal pull-up resistors for input lines and in all module states:

Signal / State	OFF	RESET	ON	Powersaving	Pull up tied to
TXD	unknown	Pd (21K ~ 210K)	Pd (21K ~ 210K)	Pd (21K ~ 210K)	
RTS	unknown	Pd (21K ~ 210K)	Pd (21K ~ 210K)	Pd (21K ~ 210K)	
CTS	unknown	Pu (39K ~ 390K)	Pu (39K ~ 390K)	Pu (39K ~ 390K)	1V8



NOTE:

For minimum implementation, only the TXD and RXD lines must be connected, the other lines can be left open provided a software flow control is implemented.



NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CE910-DUAL when the module is powered off or during an ON/OFF transition.



NOTE:

According to V.24, RX/TX signal names are referred to the application side. Therefore, on the CE910-DUAL side these signals are in the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ rx_uart) of the CE910-DUAL serial port and vice versa for RX.





NOTE:

High-speed UART supports up to 4Mbps. Please refer to the AT command User Guide in detail.



WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect CE910-DUAL or customer specific requirements from ESD event to UART port (M15, N15, P15 and L14).



8.2. RS232 Level Translation

In order to interface the Telit CE910-DUAL with a PC com port or a RS232 (EIA/TIA-232) application, a level translator is required. This level translator must:

- Invert the electrical signal in both directions
- Change the level from 0/1.8V to +/-15V

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.

The simplest way to translate the levels and invert the signal is by using a single chip level translator. There is a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).

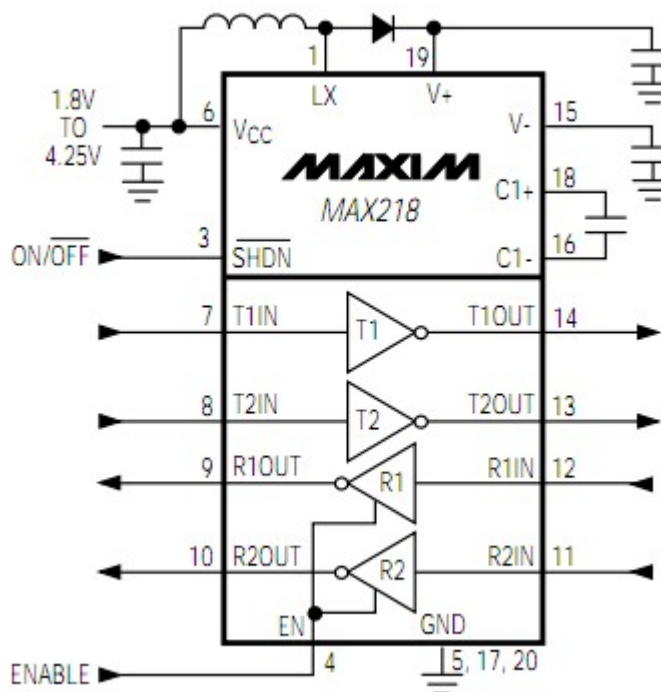
By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.

In order to translate the whole set of control lines of the UART you will need:

- 5 drivers
- 3 receivers

An example of RS232 level adaption circuitry could be accomplished using a MAXIM transceiver (MAX218).

In this case the chipset is capable of translating directly from 1.8V to the RS232 levels (Example on 4 signals only).

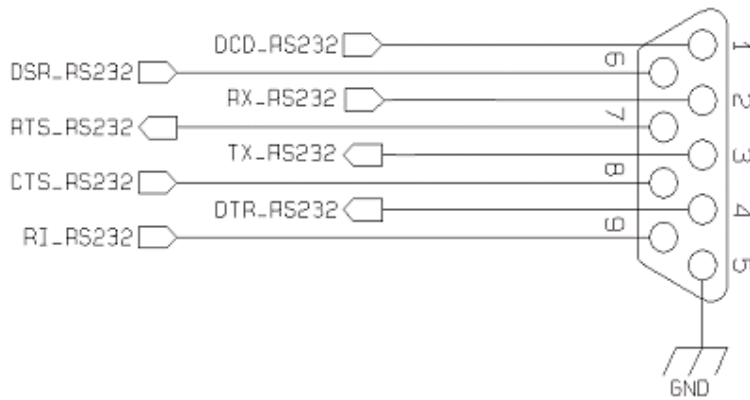




NOTE:

In this case the length of the lines on the application has to be taken into account to avoid problems in case of High-speed rates on RS232.

The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



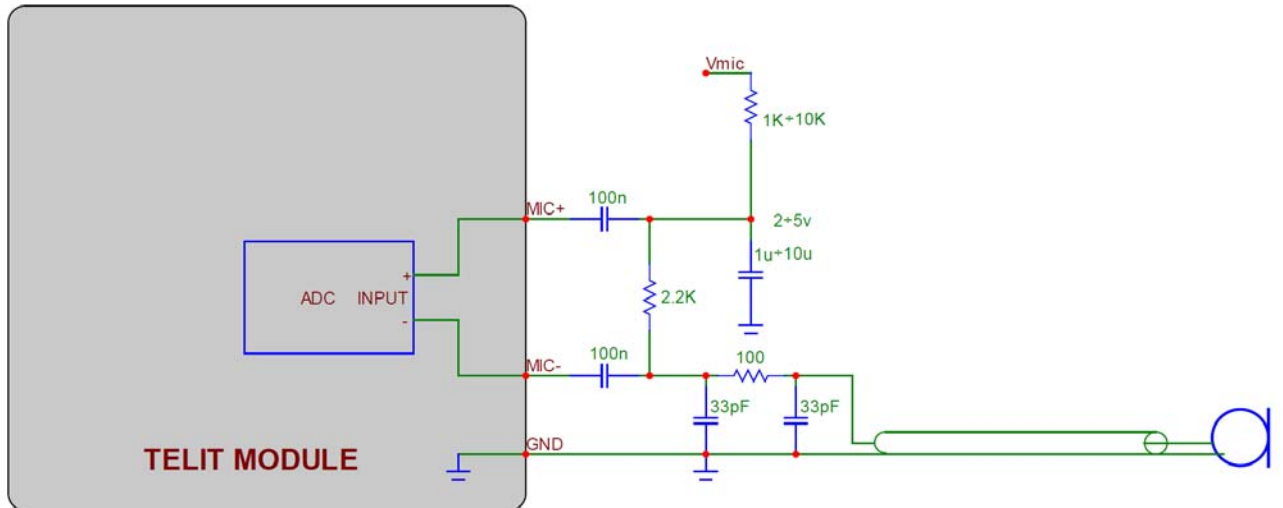
9. Audio Section Overview

The CE910-DUAL provides one differential input for audio to be transmitted(Uplink) and a balanced output for audio to be received(Downlink).

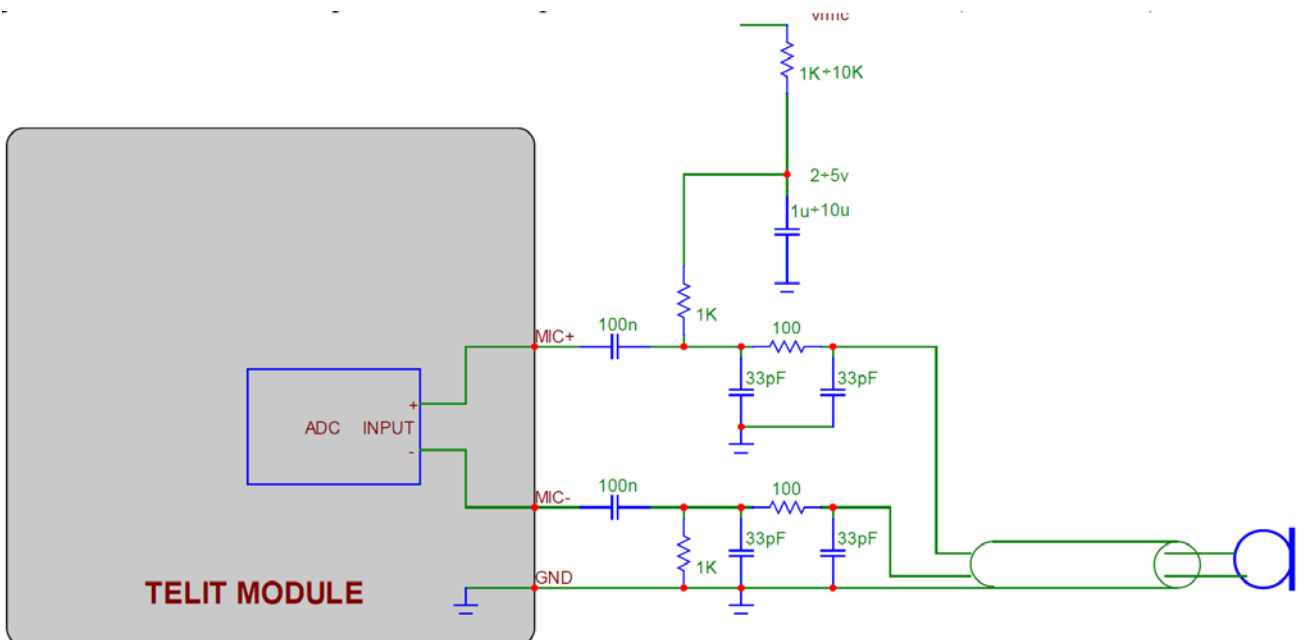
The bias for the microphone has to be as clean as possible; the first connection (single ended) is preferable since the Vmic noise and ground noise are fed into the input as common mode and then rejected. This sounds strange; usually the connection to use in order to reject the common mode is the balanced one. In this situation we have to recall that the microphone is a sound to current transducer, so the resistor is the current to tension transducer, so finally the resistor feeds the input in balanced way even if the configuration, from a microphone point of view, seems to be un-balanced.



9.1. MIC connection



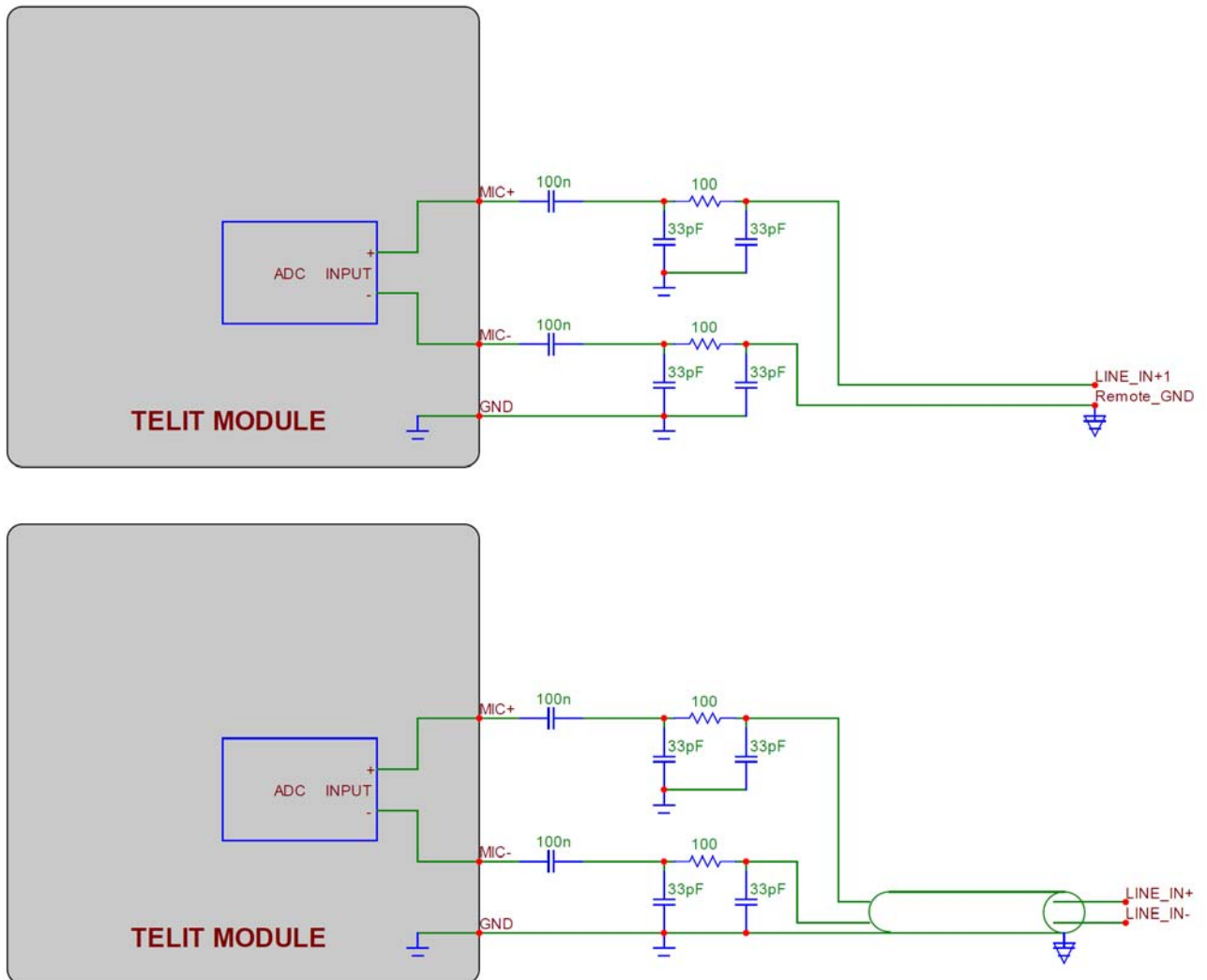
If a “balanced way” is anyway desired, much more care has to be taken to VMIC noise and ground noise; also the 33pF-100ohm-33pF RF-filter has to be doubled (one each wire).



TIP: Since the J-FET transistor inside the microphone acts as RF-detector-amplifier, ask vendor for a microphone with anti-EMI capacitor (usually a 33pF or a 10pF capacitor placed across the output terminals inside the case).



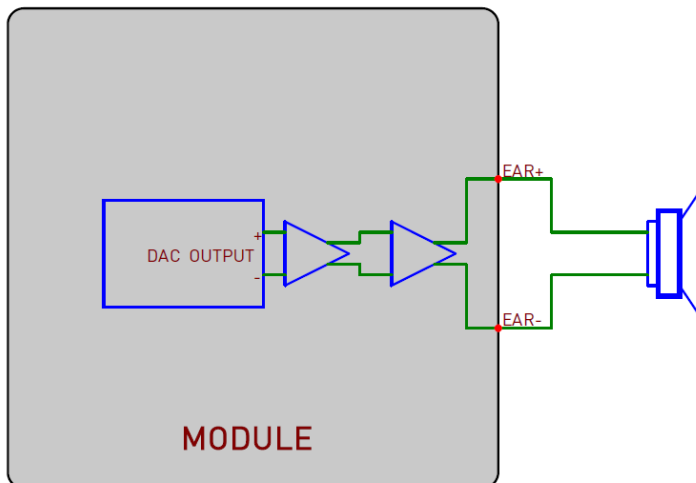
9.2. LIN-IN connection



If the audio source is not a mike but a different device, the following connections can be done. Place 100nF capacitor in series with both inputs, so the DC current is blocked. Place the 33pF-100Ohm-33pF RF-filter, in order to prevent some EMI field to get into the high impedance high gain MIC inputs. Since the input is differential, the common mode voltage noise between the two (different) grounds is rejected, provided that both AF_IN+ & AF_IN- are connected directly onto the source.



9.3. EAR connection



The audio output of the CE910-DUAL is balanced, this is helpful to double the level and to reject common mode (click and pop are common mode and therefore rejected). These outputs can drive directly a small loudspeaker with electrical impedance not lower than 320hm.



TIP: in order to get the maximum audio level at a given output voltage level (dBspl/Vrms), the following breaking through procedure can be used. Have the loudspeaker as close as you can to the listener (this simplify also the echo cancelling); choose the loudspeaker with the higher sensitivity (dBspl per W); choose loudspeakers with the impedance close to the limit in order to feed more power inside the transducer (it increases the W/Vrms ratio). If this were not enough, an external amplifier should be used.



10. General Purpose I/O

The general-purpose I/O pads can be configured to act in three different ways:

- Input
- Output
- Alternate function (internally controlled)

Input pads can only be read and report the digital value (high or low) present on the pad at the read time.

Output pads can only be written to set the value of the pad or queried.

An alternate function pad is internally controlled by the CE910-DUAL firmware and acts depending on the function implemented.

The following GPIOs are available on the CE910-DUAL.

Pin	Signal	I/O	Function	Drive Strength	Type
C8	GPIO_01	I/O	Configurable GPIO	2 mA	1.8V
C9	GPIO_02	I/O	Configurable GPIO	2 mA	1.8V
C10	GPIO_03	I/O	Configurable GPIO	2 mA	1.8V
C11	GPIO_04	I/O	Configurable GPIO	2 mA	1.8V
B14	GPIO_05	I/O	Configurable GPIO	2 mA	1.8V
C12	GPIO_06	I/O	Configurable GPIO	2 mA	1.8V
C13	GPIO_07	I/O	Configurable GPIO	2 mA	1.8V
K15	GPIO_08	I/O	Configurable GPIO	2 mA	1.8V
L15	GPIO_09	I/O	Configurable GPIO	2 mA	1.8V
G15	GPIO_10	I/O	Configurable GPIO	2 mA	1.8V



10.1. Logic Level Specification

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels.

The following table shows the logic level specifications used in the CE910-DUAL interface circuits:

Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) with respect to ground	-0.3V	2.3V

Operating Range - Interface levels (1.8V CMOS)

Parameter	Min	Max
Input high level	1.5V	2.1V
Input low level	0.0V	0.35V
Output high level	1.35V	1.8V
Output low level	0.0V	0.45V

Current characteristics

Parameter	Typical
Output Current	2mA
Input Current	30uA



10.2. Using a GPIO Pad as Input

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.

If the digital output of the device is connected with the GPIO input, the pad has interface levels different from the 1.8V CMOS. It can be buffered with an open collector transistor with a 4.7K Ω pull-up resistor to 1.8V.

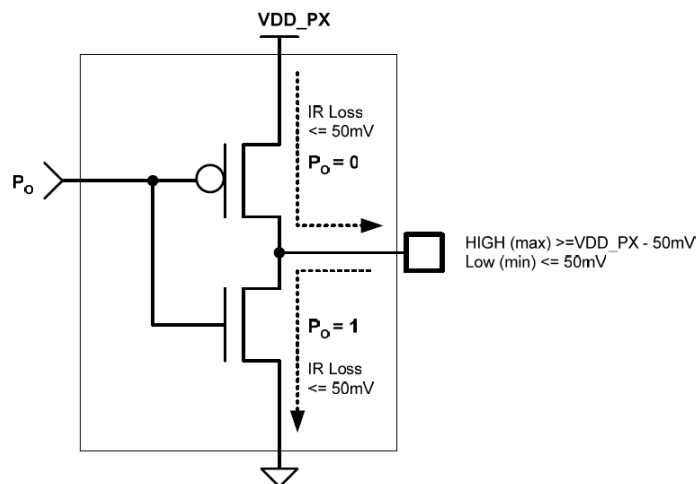


NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

10.3. Using a GPIO Pad as Output

The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.



output PAD equivalent circuit



10.4. Using the Temperature Monitor Function

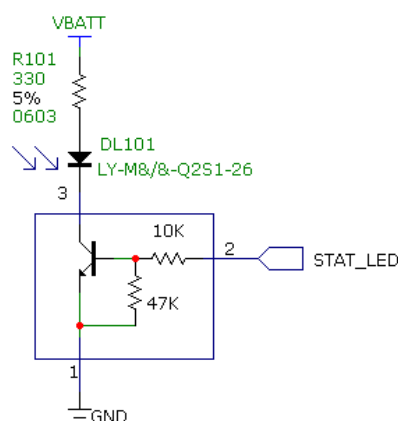
10.4.1. Short Description

The Temperature Monitor is a function of the module that permits control of its internal temperature and if properly set (see the #TEMPMON command on AT Interface guide) raises to High Logic level a GPIO when the maximum temperature is reached.

10.5. Indication of Network Service Availability

The STAT_LED pin status shows information on the network service availability and Call status. In the CE910-DUAL modules, the STAT_LED usually needs an external transistor to drive an external LED. Because of the above, the status indicated in the following table is reversed with respect to the pin status:

LED status	Device Status
Permanently off	Device off
Fast blinking (Period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (Period 3s, Ton 0,3s)	Registered full service
Permanently on	a call is active



10.6. RTC Bypass Output

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing only RTC to be active when all the other parts of the device are off. To this power output a backup capacitor can be added in order to increase the RTC autonomy during power off of the battery.



NOTE:

NO devices must be powered from this pin.

10.7. VAUX/PWRMON Power Output

A regulated power supply output is provided in order to supply small devices from the module. This output is active when the module is ON and goes OFF when the module is shut down. The operating range characteristics of the supply are:

Operating Range – VAUX/PWRMON power supply

Parameter	Min	Typical	Max
Output voltage	1.77V	1.8V	1.83V
Output current			200mA
Output bypass capacitor (Inside the module)		2.2μF	



11. ADC section

11.1. Description

The on board ADC is 12-bit converter. It is able to read a voltage level in the range of 0 ~ 1.2 volts applied on the ADC pin input and store and convert it into 12 bit word.

Parameter	Min	Max	Units
Input Voltage range	0	1.2	Volt
AD conversion	-	12	bits
Resolution	-	< 1	mV
Input Resistance	1		Mohm

The CE910-DUAL provides one Analog to Digital Converter.

The input lines are:

ADC_IN available on pin B1 and Pin 7 of PL102 on Interface Board (CS1467D)

11.2. Using ADC Converter

An AT command is available to use the ADC function.

The command is AT#ADC=1,2. The read value is expressed in mV

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.



12. Mounting the Module on your Board

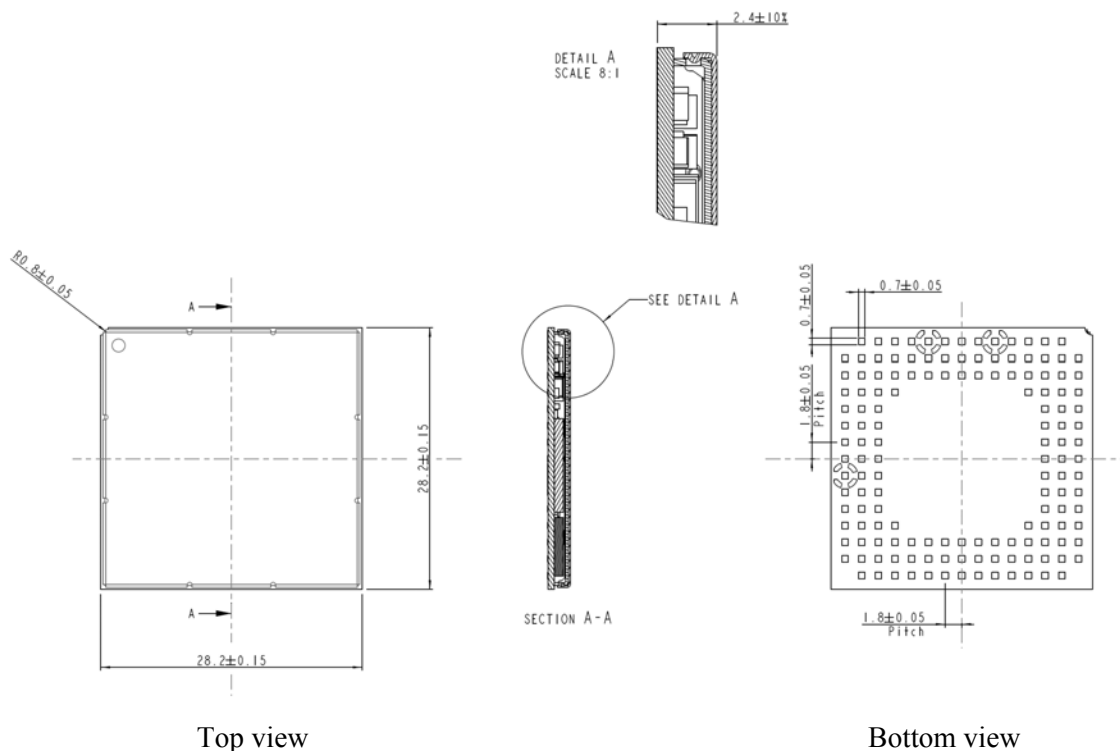
12.1. General

The CE910-DUAL has been designed in order to be compliant with a standard lead-free SMT process.

12.2. Module Finishing & Dimensions

The CE910-DUAL overall dimensions are:

- Length : 28.2 mm
- Width : 28.2 mm
- Thickness : 2.40* mm (2 shields)
- Weight : 4.7 g (2 shields)

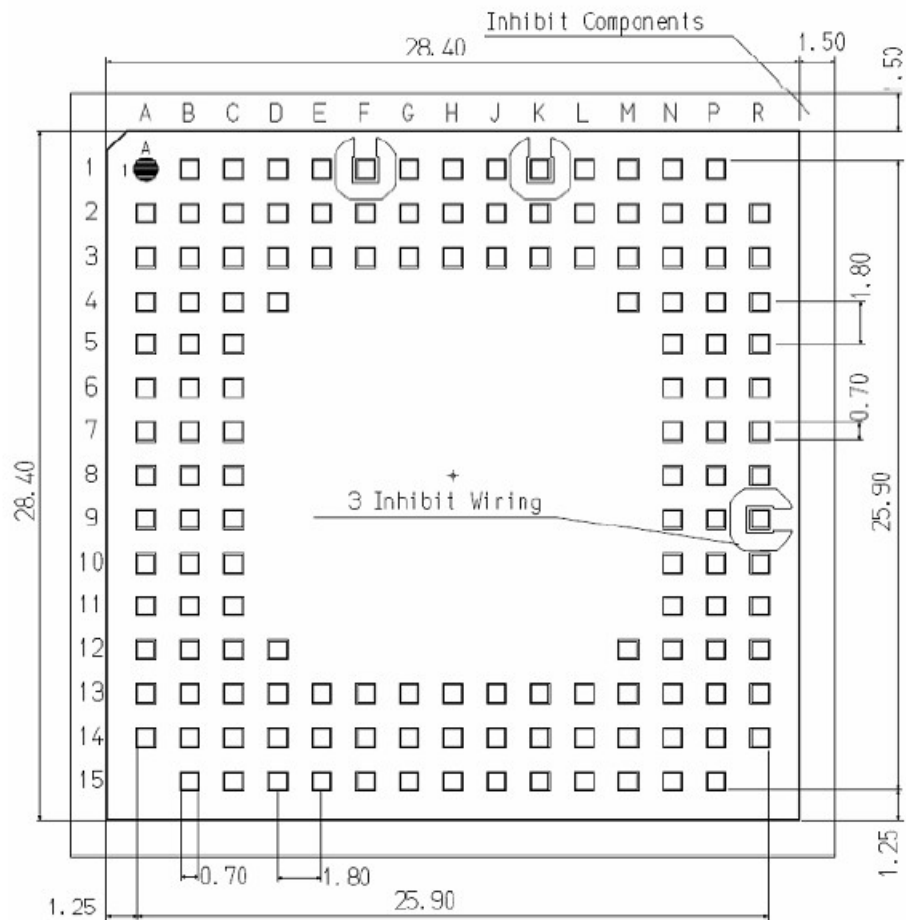


(Dimensions in mm)

* Thickness 2.05 mm(T) version(1 shield) is coming soon.



12.3. Recommended foot print for the application



144 pins

< Top View >

In order to easily rework the CE910-DUAL it is suggested to consider having a 1.5 mm placement inhibit area around the module on the application.

It is also suggested, as a common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.



NOTE:

In the customer application, the region under WIRING INHIBIT (see figure) must be clear from signal or ground paths.

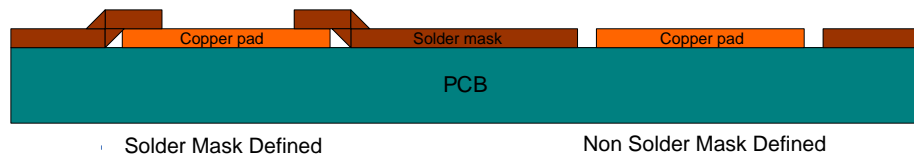


12.4. Stencil

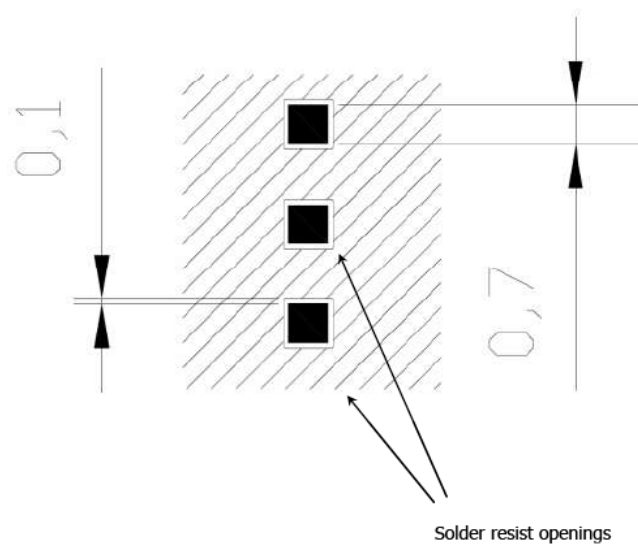
Stencil's apertures layout can be the same as the recommended footprint (1:1). A suggested thickness of stencil foil is less than 120 μm .

12.5. PCB Pad Design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.

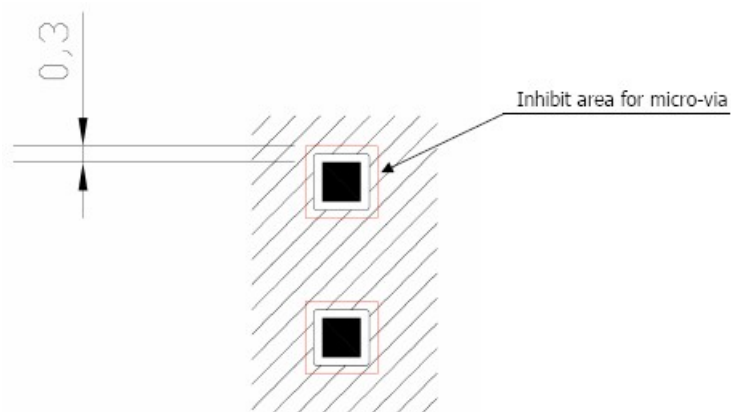


12.6. Recommendations for PCB Pad Dimensions (mm)



It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal as the pad itself (see following figure).





Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB Pad Surfaces:

Finish	Layer thickness (um)	Properties
Electro-less Ni / Immersion Au	3 ~ 7 / 0.05 ~ 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.



12.7. Solder Paste

Solder Paste	Lead free
	Sn/Ag/Cu

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

12.7.1. Solder Reflow

The following is the recommended solder reflow profile:

Profile stage	Description	Lead-free(High-Temp) condition limits
Preheat	Initial ramp	3 °C/sec max
Soak	Dry out and flux activation	135 to 175 °C 60 to 120 sec
Reflow	Time above solder paste melting point	40 to 90 sec
	SMT peak package body temperature	245 °C
Cool down	Cool rate-ramp to ambient	6 °C/sec max



NOTE:

All temperatures refer to topside of the package, measured on the package body surface.



WARNING:

The CE910-DUAL module withstands one reflow process only.



12.8. Debug in production

To test and debug the mounting of CE910-DUAL, we strongly recommend foreseeing test pads on the host PCB, in order to check the connection between the CE910-DUAL itself and the application and to test the performance of the module connecting it with an external computer. Depending on the customer application, these pads include, but are not limited to the following signals:

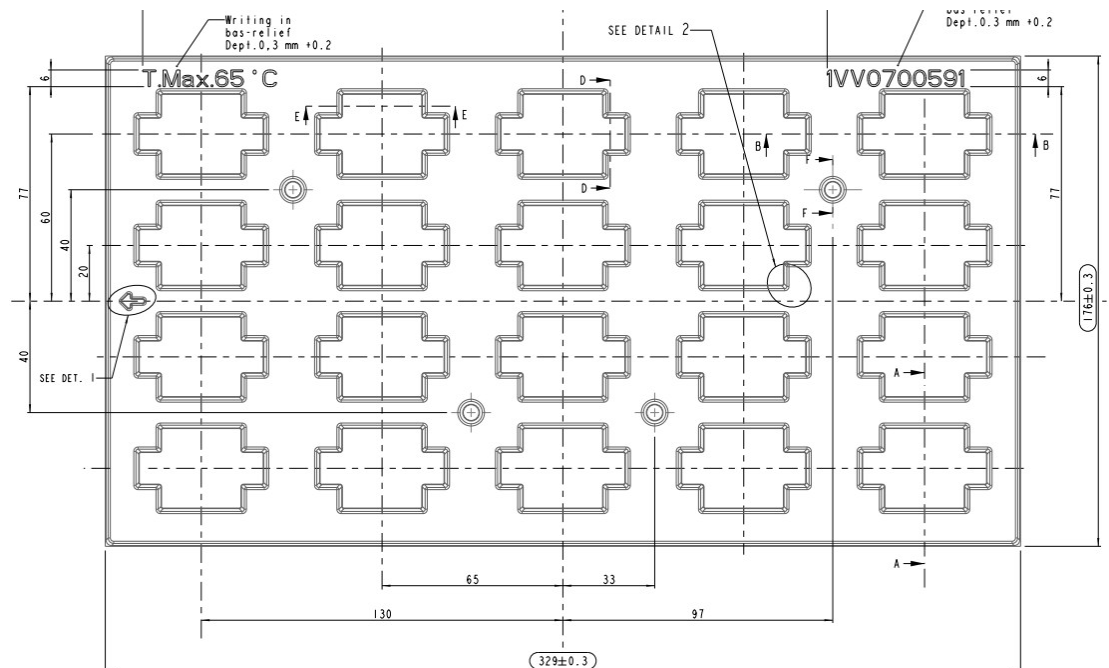
- TXD
- RXD
- ON/OFF
- RESET
- GND
- VBATT
- PWRMON



13. Packing System

The CE910-DUAL modules are packaged on trays of 20 pieces each. These trays can be used in SMT processes for pick & place handling.

13.1. Tray Drawing



(1VV0700591-0A)



WARNING:

These trays can withstand a maximum temperature of 65°C.

13.2. Moisture Sensibility

The CE910-DUAL is a Moisture Sensitive Device level 3, in accordance with standard IPC/JEDEC J-STD-020. Observe all of the requirements for using this kind of component.

Calculated shelf life in sealed bag: 4 months at <40°C and <90% relative humidity (RH).



14. Application Design Guide

14.1. Download and Debug Port

One of the following options should be chosen in the design of host system in order to download or upgrade the Telit's software and debug CE910-DUAL when CE910-DUAL is already mounted on a host system.

Users who use both of UART and USB interfaces to communicate CE910-DUAL

- Must implement a download method in a host system for upgrading CE910-DUAL when it's mounted.

Users who use USB interface only to communicate CE910-DUAL

- Must arrange UART port in a host system for debugging or upgrading CE910-DUAL when it's mounted.

Users who use UART interface only to communicate CE910-DUAL

- Must arrange USB port in a host system for debugging or upgrading CE910-DUAL when it's mounted.



15. Conformity Assessment Issues (Problèmes d'évaluation de conformité)

The CE910-DUAL is FCC/IC Approved as module to be installed in other devices. This device should be used only for fixed and mobile applications and if the final product after integration is intended for portable use, a new application and FCC is required.

Le CE910-DUAL est approuvé FCC/IC comme module à installer dans d'autres dispositifs. Ce dispositif doit être utilisé uniquement pour des applications fixes et mobiles et si le produit fini est prévu après intégration pour un usage portatif, une nouvelle application et la FCC est requise

The user is cautioned that this device should be used only as specified within this manual to meet RF exposure requirements.

L'utilisateur est averti que ce dispositif doit être utilisé uniquement comme spécifié dans ce manuel pour répondre aux normes d'exposition aux ondes rf.

Use of this device in a manner inconsistent with this manual could lead to excessive RF exposure conditions.

L'utilisation de ce dispositif en quelque sorte contradictoire avec ce manuel a pu mener aux états excessifs d'exposition de rf.

The CE910-DUAL is conforming to the following US Directives:

- Use of RF Spectrum. Standards: FCC47 Part 22&24
- EMC Standards: FCC47 Part 15

Le CE910-DUAL est conforme aux directives suivantes des USA

- Utilisation de spectre de rf. Normes : FCC47 partie 22&24
- Normes d'EMC : FCC47 partie 15

This device complies with Part 15 of the FCC Rules.

Ce dispositif est conforme à la partie 15 des règles FCC.

Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le fonctionnement est sujet aux deux conditions suivantes :

- (1) ce dispositif peut ne pas causer l'interférence nocive, et
- (2) ce dispositif doit accepter aucune interférence, y compris un interférence qui pourrait causer le fonctionnement non désiré du dispositif.



The user must refer to below information to meet the FCC/IC's RF exposure rules and regulations when they design:

Lors de la conception, l'utilisateur doit se référer à l'information ci-dessous pour remplir les conditions et réglementations FCC/IC' d'exposition aux ondes RF:

- The system antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all the persons and must not be co-located or operating in conjunction with any other antenna or transmitter.
Le système d'antenne utilisé pour cet émetteur doit être installé à une distance d'au moins de 20 cm de toute personne et ne doit pas être co-implanté ou opérer en même temps que n'importe quelle autre antenne ou émetteur.
- The system antenna(s) used for this module must not exceed 5.12dBi in CDMA BC0 and 6.12dBi in CDMA BC1 for mobile and fixed or mobile operating configurations.
Le système d'antenne utilisé pour ce module ne doit pas dépasser 5.12dBi en CDMA BC0 et 6.12dBi en CDMA BC1 pour des configurations mobiles et fixes ou des configurations opérant en mode mobile.
- Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.
Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and to have their complete product tested and approved for FCC compliance.
Les instructions d'installation de l'antenne ainsi que les conditions de fonctionnement de l'émetteur doivent être remis aux utilisateurs et aux installateurs conformément à la réglementation sur l'exposition aux ondes rf. Des fabricants des dispositifs mobiles, fixes ou portables incorporant ce module sont invités à clarifier toutes les questions de normalisation et à avoir leur produit complètement testé pour la mise en conformité FCC.
- CE910-DUAL is intended for the OEM integrator only.
CE910-DUAL est prévu pour l'intégrateur OEM seulement.
- The user is required to see the Grant of Equipment document for other restrictions.
L'utilisateur doit se référer au document « Grant of equipment » pour d'autres restrictions.
- CE910-DUAL must be operated and used with a locally approved access point.
CE910-DUAL doit être actionné et utilisé avec un point d'accès localement approuvé.
- The radio transmitter(IC ID: 5131A-CE910DUAL) has been approved by Industry Canada to operate with the antenna type listed in this manual with the maximum permissible gain and required antenna impedance for each antenna type indicated.
Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.
L'émetteur radio (identification d'IC : 5131A-CE910DUAL) a été approuvé par Industry Canada pour fonctionner avec le type d'antenne énuméré dans ce manuel

avec le gain autorisé maximum et l'impédance d'antenne exigée pour chaque type d'antenne indiqué. Les types d'antenne non inclus dans cette liste, ayant un gain supérieur au gain maximum indiqué pour ce type, sont strictement interdits pour un usage avec ce dispositif.

The following regulatory and safety notices must be published in documentation supplied to the end user of the product or system incorporating an adapter in compliance with local regulations.

- Host system including CE910-DUAL must be labeled with “Contains transmitter module with FCC ID: RI7CE910-DUAL and IC ID: 5131A-CE910DUAL”

Les notices de normalisation et de sécurité doivent se trouver dans la documentation fournie à l'utilisateur du produit ou du système incorporant un adaptateur conforme aux réglementations locales.

- Le système hôte comprenant CE910-DUAL doit être marqué avec « Contient un module émetteur avec IDENTIFICATION FCC : RI7CE910-DUAL et identification IC : 5131A-CE910DUAL »



16. Safety Recommendations

READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country's regulations and the specific environmental regulation.

Do not disassemble the product; any evidence of tampering will compromise the warranty validity. Follow the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to conform to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pads because electrostatic discharges may damage the product itself.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken with the external components of the module as well as of any project or installation issue because of the risk of disturbing the CDMA network or external devices or having impact on security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against SAR regulations.



17. Document History

Revision	Date	Changes
0	2012-07-10	Initial release

