

80pppSTzzzza Rev. 0 - 12-Nov-07



Making machines talk.



80pppSTzzzza Rev. 0, 12-Nov-07

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Notice

OEM integrators and installers are instructed that the phrase. This device contains transmitter FCC ID: RI7CC864-DUAL must be placed on the outside of the host.

	Warning: Exposure to Radio Frequency Radiation The radiated output
	power of this device is far below the FCC radio frequency exposure
	limits. Nevertheless, the device should be used in such a manner that
	the potential for human contact during normal operation is minimized.
<u>/!</u> \	In order to avoid the possibility of exceeding the FCC radio
~~	frequency exposure limits, human proximity to the antenna should
	not be less than 20cm during normal operation. The gain of the
	antenna for Cellular band must not exceed -2.000dBi.
	The gain of the antenna for PCS band must not exceed -3.00000dBi.



# 1. Overview

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit CC864-Dual module.

In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors are to be avoided. Obviously this document can not embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configuration shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with Telit CC864-Dual module. For further hardware details that may not be explained in this document.

## 1.1. General Specifications

Parameters	Descriptions		
External Access	Code Division Multiple Access		
CDMA Protocol	IS-95A/B, IS-98A, IS-126, IS-637A, IS-707, IS-2000		
Data Rate	153.6Kbps(Full-duplex)		
GPS	SGPS/Standalone		
Vocoder	EVRC, 13kQCELP		
Number of Channel	832 for Cellular, 1200 for PCS		
Operating Temperature	-30℃ ~ +80℃		

## 1.2. Receiver Specifications

Parameters	Descriptions
Frequency Range	869~894Mhz, 1930~1990Mhz
Sensitivity	Below -104dBm
Input Dynamic Range	-25dBm ~ -104dBm





## 1.3. Transmitter Specifications

Parameters	Descriptions			
Frequency Range	824~849Mhz, 1850~1910Mhz			
Power Class	Class $III$ for Cellular, Class $II$ for PCS			
Power Range	0.2W ~ 1.0W			
Nominal Power	0.27W(24.31dBm)			

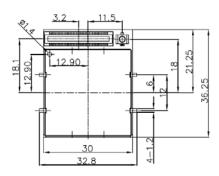
## 1.4. gpsOne Receiver Specifications

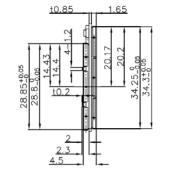
Parameters	Descriptions		
Frequency Range	L1, 1575.42Mhz		
C/A Code	1.023Mhz Chip Rate		
Receiver Sensitivity	-152dBm		

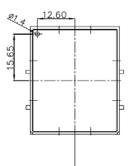
# 2. Mechanical Dimensions

The Telit CC864-Dual module overall dimensions are:

- Length : 36.25mm
- Width : 30mm
- Thickness : 4.8mm









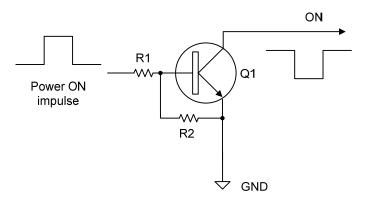
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# 3. Hardware Commands

## 3.1. Turning ON the CC864-Dual

To turn ON the CC864-DUAL the pad ON/OFF must be tied for at least 1 second and then released.



## 3.2. Turning OFF the CC864-Dual

The turning off of the device can be done in two ways:

- . by software command
- . by hardware shutdown

When the device is shut down by software command or by hardware shutdown, it issues to the network a detach request that informs the network that the device will not be reachable any more.

## 3.3. Hardware shutdown

To turn OFF the CC864-Dual the pad ON/OFF must be tied for at least 1 second and released. The same circuitry and timing for the power on shall be used. The device shuts down after the release of the ON/OFF pad.



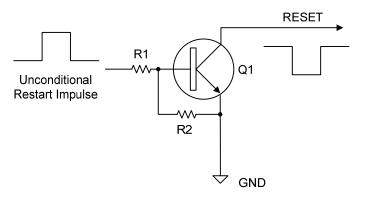
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## 3.4. Hardware RESET Reboot

To unconditionally Reboot the CC864-Dual, the pad RESET must be tied low for at least 200 milliseconds and the released.

A simple circuit to do it is :



# 4. Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performance, hence read carefully the requirements and the guidelines for a proper design.

## 4.1. Power Supply Requirements

- Nominal Supply Voltage : 3.8V
- Max Supply Voltage : 4.2V
- Supply voltage range : 3.6V ~ 4.2V
- Max Peak current consumption(impulsive) : 1A
- Max Average current consumption during CDMA transmission : 700mA
- Average current during Power saving(Sleep mode) : ≤ 2mA



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The current peaks can be as high as about 1A. Therefore the power supply has to be designed in order to withstand with these current peaks without big voltage drops; this means that both the electrical design and the board layout must be designed for this current flow. If the voltage goes under 3.3V, the module will be shut down automatically.

## 4.2. Electrical Design Rules

The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories :

- +5V input(typically PC internal regulator output)
- +12V input(typically automotive)
- Battery

### 4.2.1. +5V Input Source Power Supply Design Guidelines

The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.

When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.

A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the CC864-Dual, a 100µF tantalum capacitor is usually suited.

Make sure the low ESR capacitor on the power supply output(usually a tantalum one) is rated at least 10V.

A protection diode should be inserted close to the power input, in order to save the CC864-DUAL from power polarity inversion.

### 4.2.2. +12V Input Source Power Supply Design Guidelines

The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching



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power supply will be preferable because of its better efficiency with the 1A peak current load represented by the CC864-Dual.

When using a switching to the regulator, a 500k<sup>l</sup>/<sub>2</sub> or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.

For car PB battery the input voltage can rise up to 15.8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.

A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.

Make sure the low ESR capacitor on the power supply output(usually a tantalum one) is rated at least 10V.

For car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.

A protection diode should be inserted close to the power input, in order to save the CC864-Dual from power polarity inversion. This can be the same diode as for spike protection.

### 4.2.3. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V lithium-ion cell battery type is suited for supplying the power to the CC864-Dual module.

The three cells Ni/Cd or Ni/MH 3.6V Nom. Battery types or 4V PB types must not be used directly because their maximum voltage can rise over the absolute maximum voltage for the CC864-Dual and damage it.

A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100uF tantalum capacitor is usually suited.

A protection diode should be inserted close to the power input, in order to save the CC864-Dual from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversion when connecting the battery.



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# 4.3. Battery Charge control Circuitry Design Guideline

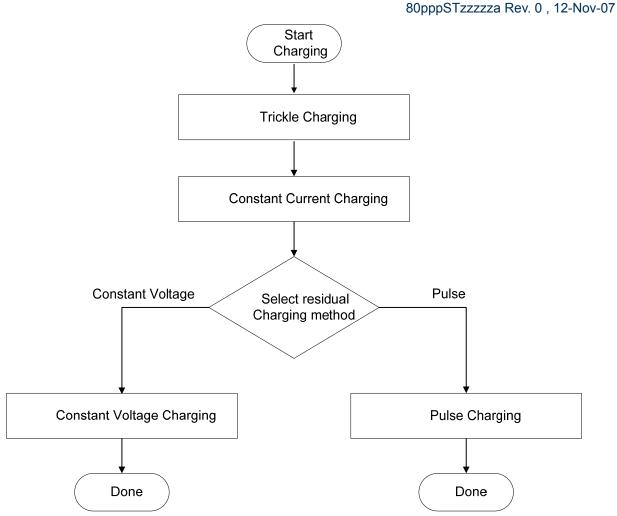
The CC864-Dual provides support circuitry for charging a lithium-ion battery, utilizing as many as four software-enabled charging techniques: trickle, constant current, constant voltage, and pulsed. Battery voltage, external supply voltage, and total detected current measurements are available to software through the analog multiplexer. This allows the software device to monitor charging parameters, make decisions, and control the charging process.

Charging begins with trickle charging, a mode that limits the current and avoids pulling VDD down. Once a minimum battery voltage is established using trickle charging, constant current charging is enabled via software to charge the battery quickly - this mode is sometimes called fast charging. Once the Li-ion battery approaches its target voltage (through constant current charging), the charge is completed using either constant voltage or pulse charging. Further discussion of all charging modes is provided in the sections identified within bellowed picture. The main battery charging sequence is



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### 4.3.1. Trickle charging

Trickle charging of the main battery, enabled through software control and powered from Vdd, is provided by the CC864-Dual. This mode is used to raise a severely depleted battery's voltage to a level sufficient to begin fast charging.

Fast charging with a high-current supply should not be attempted on a deeply discharged battery – the battery would draw excessive current, pull the Vdd voltage down, and possibly cause a handset malfunction or shutdown due to an under-voltage lockout condition. If the CC864-Dual implements current limiting, the excessive current would combine with the potentially large voltage drop across the pass transistor to generate unwanted heat within the device. To avoid these problems the CC864-Dual provides a constant, low-current charging mode - trickle charging. Trickle charging is enabled through software control and should be used until the main battery



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reaches its desired threshold, usually about 3.0V for Li-ion batteries. The threshold varies with battery type and application, so there is no predefined value implemented in the detection circuits. Software must terminate trickle charging based on battery voltage measurements and the battery type – there is not a preset termination threshold.

### 4.3.2. Constant current charging

The CC864-Dual supports constant current charging of the main battery. During constant current charging the battery is charged with a constant current(600mA). As the battery voltage rises and approaches its desired value(4.2V) the charging current begins to decrease. This is the end of constant current charging and the beginning of residual charging. The target value is set by SBI-programming to a value higher than the desired final voltage to overcome the battery internal ESR and achieve faster charging. Software monitors the voltage and takes the appropriate action to terminate the constant current charging mode. Charging continues with residual charging(either constant voltage or pulsed).

### 4.3.3. Constant voltage charging

Once constant current charging of a lithium-ion battery is finished, the charging continues using either constant voltage or pulsed techniques.

The constant voltage charging is very similar to its constant current mode. The battery voltage is constant(or nearly so) while the charging current decreases exponentially for the remaining charger process.

The end of constant voltage charging is typically detected by allowing voltage operation for a predetermined duration beyond crossing the VBATDET threshold in the charger IC(on the order of one-half to two hours). It is important to limit this predetermined duration – do not allow charging to continue indefinitely! Charging too long will damage the battery....consult battery manufacturers for specific recommendations.

### 4.3.4. Pulse charging

Pulse charging is implemented by switching the pass transistor in the charger IC on and off ; phone



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electronics should draw minimal current so the battery's open circuit voltage can be measured accurately during the off interval.

Pulse charging, compared to constant voltage charging, provides better voltage accuracy, reaches full charge more quickly, and dissipates less transistor power when switching from constant current charging. Pulse charging is enabled through software control, uses the same hardware as constant current or constant voltage charging, but repetitiously opens and closes the pass transistor to deliver current pulses to the battery.

As the battery charges it reaches the VBADET threshold, causing the internal charger IC counter  $T_ON$  to start. The pass transistor stays closed(and the battery continues charging) until the  $T_ON$  counter expires. Then the pass transistor is opened, charging stops, and another internal counter( $T_OFF$ ) is enabled. Without continued charging, the battery voltage may drop-if it drops too far, additional charging is needed. If it holds its voltage, it is fully charged and the charging process is terminated. This is one purpose of pulsed operation – to check and recheck the battery's open circuit voltage, confirming a full charger before terminating the process.

### 4.4. Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specification:

- Average current consumption during transmission at Max level : 700mA
- Average current consumption during transmission at Min level : 220mA
- Average current during Idle mode : 60mA
- Average current during sleep mode : 1mA
- Average current during hibernation mode : 275nA

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

If we assume that the device stays into transmission for short periods of time(let's say few minutes) and then remains for a quite long time in idle(let's say one hour), then the power supply has always the time to cool down between the calls and the heat sink could be smaller than the calculated one for 700mA maximum RMS current, or even could be the simple chip package(no heat sink) Moreover in the average network conditions the device is requested to transmit at a lower power



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level than the maximum and hence the current consumption will be less than 700mA. For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating. This generated heat will be mostly conducted to the ground plane under the CC864-DUAL, you must ensure that your application can dissipate it.

## 4.5. Power Supply PCB layout Guidelines

The Bypass low ESR capacitor must be placed close to the CC864-Dual power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the CC864-Dual is wide enough to ensure a dropless connection even during the 1A current peaks.

The protection diode must be placed close to the input connector where the power source is drained.

The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drop occur when the 1A current peaks are absorbed.

The PCB traces to the CC864-Dual and Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 1A current peaks are absorbed. Try to keep this traces as short as possible.

The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC(only for switching power supply). This is done in order to reduce the radiated field(noise) at the switching frequency(100~500kl/z usually)

The use of a good common ground plane is suggested.

The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.

The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.



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# 5. Antenna

The antenna connection and board layout are the most important part in the full product design and they strongly reflect on the product overall performance, hence read carefully the requirements and the guidelines for a proper design.

## 5.1. Antenna Requirements

Parameters	Descriptions			
Frequency range(CDMA)	Tx : 824₩z ~ 849, Rx : 869 ~ 894₩z			
Frequency range(PCS)	Tx : 1850Mz ~ 1910Mz, Rx : 1930Mz ~ 1990Mz			
Frequency range(GPS)	1575.42M±z			
Impedance	50Ω			
VSWR recommended	≤2			
Radiation pattern	Omni-directional			
Polarization	Vertical			

Furthermore if the device is developed for the US market and/or Canada market, it shall comply to the FCC and/or IC approval requirements:

## 5.2. Antenna Connector

The CC864-Dual module is equipped with a 50 Ohm RF connector from Murata, GSC type and P/N MM9329-2700RA1. The counterpart suitable is Murata MXTK92 type or MXTK88 type.

## 5.3. Antenna installation Guidelines

Install the antenna in a place covered by the CDMA signal

Antenna shall not be installed inside metal cases

Antenna shall be installed also according Antenna manufacturer instructions



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# 6. PINs allocation

The CC864-DUAL uses an 80 pin Molex p.n 53949-0878 male connector for the connections with the external applications. This connector matches the 54150-0878 model.

Dia	O'an al	1/0	E un altern	Internal	Tana			
Pin	Signal	I/O	Function		Туре			
	Power Supply							
1	VBATT	-	Main power supply		Power			
2	VBATT	-	Main power supply		Power			
3	VBATT	-	Main power supply		Power			
4	VBATT	-	Main power supply		Power			
5	GND	-	Ground		Power			
6	GND	-	Ground		Power			
7	GND	-	Ground		Power			
			Audio					
8	AXE	I	Handsfree switching	100kΩ	CMOS 2.8V			
9	EAR_HF+	AO	Handsfree ear output, phase+		Audio			
10	EAR_HF-	AO	Handsfree ear output, phase-		Audio			
11	EAR_MT+	AO	Handset earphone signal output, phase+		Audio			
12	EAR_MT-	AO	Handset earphone signal output, phase-		Audio			
13	MIC_HF+	AI	Handsfree microphone input ; phase+, nominal		Audio			
			level					
			3mVrms					
14	MIC_HF-	AI	Handsfree microphone input ; phase-, nominal		Audio			
			level					
			3mVrms					
15	MIC_MT+	AI	Handset microphone signal input ; phase+,		Audio			
			nominal level					
			50mVrms					
16	MIC_MT-	AI	Handset microphone signal input ; phase-,		Audio			
			nominal level 50mVrms					
		1	R-UIM Card Interface					
18	UIM_PWR	-	Power supply for the UIM		2.8V			



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UIM_RST	0	Reset		2.8V
				2.01
UIM_DATA	I/O	Data I/O		2.8V
UIM_IN	Ι	Presence(active low)	47kΩ	2.8V
UIM_CLK	0	Clock		2.8V
		QCOM Diagnostic Monitor		
RX_TRACE	Ι	RX Data for debug monitor		CMOS 2.8V
TX_TRACE	0	TX Data for debug monitor		CMOS 2.8V
		Prog. / Data + Hw Flow Control		·
C103/TXD	Ι	Serial data input (TXD) from DTE		CMOS 2.8V
C104/RXD	0	Serial data output to DTE		CMOS 2.8V
C107/DSR	0	Output for Data set ready signal (DSR) to DTE		CMOS 2.8V
C106/CTS	0	Output for Clear to send signal (CTS) to DTE		CMOS 2.8V
C108/DTR	Ι	Input for Data terminal ready signal (DTR) from		CMOS 2.8V
		DTE		
C125/RING	0	Output for Ring indicator signal (RI) to DTE		CMOS 2.8V
C105/RTS	Ι	Input for Request to send signal (RTS) from DTE		CMOS 2.8V
C109/DCD	0	Output for Data carrier detect signal (DCD) to		CMOS 2.8V
		DTE		
		liC		•
SCL	I/O	IIC Hardware interface		CMOS 2.8V
SDA	I/O	IIC Hardware interface		CMOS 2.8V
		USB		
USB_ID	Ι	USB_ID input	47kΩ	CMOS 2.8V
USB_VBUS	Al/A	USB_VBUS power supply		5V
	0			
USB_D+	I/O	USB Data(USB Internal Transceiver In/Output)		2.8V~3.6V
USB_D-	I/O	USB Data(USB Internal Transceiver In/Output)		2.8V~3.6V
		DAC and ADC		
ADC_IN1	AI	Analog/Digital converter input		A/D
ADC_IN2	AI	Analog/Digital converter input		A/D
ADC_IN3	AI	Analog/Digital converter input		A/D
DAC_OUT	AO	Digital/Analog converter output		D/A(PWM)
		РСМ		
PCM_CLOCK	I/O	Telit GPIO Configurable GPIO		CMOS 2.8V
	JIM_CLK     RX_TRACE     TX_TRACE     TX_TRACE     T03/TXD     C103/TXD     C103/TXD     C104/RXD     C107/DSR     C106/CTS     C108/DTR     C105/RTS     C109/DCD     SCL     SDA     JSB_ID     JSB_VBUS     JSB_D+     JSB_D-     ADC_IN1     ADC_IN2     ADC_OUT		JIM_CLK   O   Clock     QCOM Diagnostic Monitor     RX_TRACE   I   RX Data for debug monitor     Y_TRACE   O   TX Data for debug monitor     Prog. / Data + Hw Flow Control     2103/TXD   I   Serial data input (TXD) from DTE     2104/RXD   O   Serial data output to DTE     2104/RXD   O   Serial data output to DTE     2106/CTS   O   Output for Data set ready signal (DSR) to DTE     2108/DTR   I   Input for Clear to send signal (CTS) to DTE     2108/DTR   I   Input for Request to send signal (RI) to DTE     2109/DCD   O   Output for Request to send signal (RTS) from DTE     2109/DCD   O   Output for Data carrier detect signal (DCD) to DTE     2109/DCD   O   Output for Data carrier detect signal (DCD) to DTE     2109/DCD   O   Output for Data carrier detect signal (DCD) to DTE     2109/DCD   O   IIC Hardware interface     3DA   I/O   IIC Hardware interface     3DA   I/O   IIC Hardware interface     3DA   I/O   USB_ID input     JSB_DB_D   I   U	JIM_CLK   O   Clock     QCOM Diagnostic Monitor     RX_TRACE   I   RX Data for debug monitor     X_TRACE   O   TX Data for debug monitor     Prog. / Data + Hw Flow Control     Clock     Prog. / Data + Hw Flow Control     O     TX Data for debug monitor     Prog. / Data + Hw Flow Control     Clock     O     Serial data input (TXD) from DTE     Clock     O Output for Data set ready signal (DSR) to DTE     Clock     O Output for Data terminal ready signal (DTR) from DTE     Clos/CTS     O   Output for Request to send signal (RTS) from DTE     Clos/CTS     I   Input for Request to send signal (DCD) to DTE     Clos/RTS   I   Input for Request to send signal (DCD) to DTE     Clos/RTS   I   Input for Request to send signal (DCD) to DTE     Clos/RTS   I   Input for Request to send signal (DCD) to DTE     SCL   I/O   IIC Hardware interface     SDA   I/O



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	1	1	80pppSTzzz		0, 12-1100-07
63	TGPIO_10/PCM_T	I/O	Telit GPIO10 Configurable GPIO		CMOS 2.8V
	Х				
65	TGPIO_18/PCM_ RX	I/O	Telit GPIO18 Configurable GPIO		CMOS 2.8V
71	TGPIO_17/PCM_	I/O	Telit GPIO17 Configurable GPIO		CMOS 2.8V
	SYNC				011002.01
			Miscellaneous Functions		
45	STAT_LED	0	Status indicator led		CMOS 1.8V
46	GND	-	Ground		Ground
49	PWRMON	0	Power ON Monitor		CMOS 2.8V
50	VAUX1	-	Power output for external accessories (AT		2.85V/
			command driven)		150mA
51	CHARGE	AI	Charger input Li-Ion		Power
52	CHARGE	AI	Charger input Li-Ion		Power
53	ON/OFF*	I	Input command for switching power ON or OFF	47kΩ	Pull up to
			(toggle command). The pulse to be sent to the		VBTT
			CC864-DUAL must be equal or greater than 1		
			second.		
54	RESET*	Ι	Reset input		
55	VRTC				Power
			Telit GPIO		
56	TGPIO_19	I/O	Telit GPIO19 Configurable GPIO		CMOS 2.8V
57	TGPIO_11/VIBRA	I/O	Telit GPIO11 Configurable GPIO/Vibrator		CMOS 2.8V
	TOR				
58	TGPIO_20	I/O	Telit GPIO20 Configurable GPIO		CMOS 2.8V
59	TGPIO_04/CONV	I/O	Telit GPIO4 Configurable GPIO/Conversation		CMOS 2.8V
	ERSATION				
60	TGPIO_14	I/O	Telit GPIO14 Configurable GPIO		CMOS 2.8V
61	TGPIO_15	I/O	Telit GPIO15 Configurable GPIO		CMOS 2.8V
62	TGPIO_12/AUDIO	I/O	Telit GPIO12 Configurable GPIO/Audio Call		CMOS 2.8V
	CALL BUTTON		Button		
64	TGPIO_22	I/O	Telit GPIO22 Configurable GPIO		CMOS 1.8V
66	TGPIO_03/AUDIO MUTE	I/O	Telit GPIO03 Configurable GPIO/Audio Mute		CMOS 2.8V



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R_SAVING   mode     68   TGPIO_06/ALAR   I/O   Telit GPIO06 Configurable GPIO/Power wakeup   C     70   TGPIO_01   I/O   Telit GPIO01 Configurable GPIO   C     72   TGPIO_21   I/O   Telit GPIO21 Configurable GPIO   C     73   TGPIO_07/BUZZE   I/O   Telit GPIO07 Configurable GPIO/Buzzer   C     R   2   74   TGPIO_02   I/O   Telit GPIO16 Configurable GPIO   C     75   TGPIO_16   I/O   Telit GPIO16 Configurable GPIO   C   C     76   TGPIO_09   I/O   Telit GPIO16 Configurable GPIO   C   C     76   TGPIO_09   I/O   Telit GPIO16 Configurable GPIO   C   C     77   TGPIO_13/ACTIV   I/O   Telit GPIO13 Configurable GPIO/ACTIVE pin to   C     77   TGPIO_13/ACTIV   I/O   Telit GPIO13 Configurable GPIO/ACTIVE pin to   C     78   E   protect current leakage   C   C	, 12-INOV-07
68     TGPIO_06/ALAR M     I/O     Telit GPIO06 Configurable GPIO/Power wakeup     C       70     TGPIO_01     I/O     Telit GPIO01 Configurable GPIO     C       72     TGPIO_21     I/O     Telit GPIO21 Configurable GPIO     C       73     TGPIO_07/BUZZE     I/O     Telit GPIO07 Configurable GPIO/Buzzer     C       74     TGPIO_02     I/O     Telit GPIO02 Configurable GPIO     C       75     TGPIO_16     I/O     Telit GPIO09 Configurable GPIO     C       75     TGPIO_09     I/O     Telit GPIO09 Configurable GPIO     C       76     TGPIO_09     I/O     Telit GPIO13 Configurable GPIO     C       76     TGPIO_13/ACTIV     I/O     Telit GPIO13 Configurable GPIO/ACTIVE pin to protect current leakage     C       78     TGPIO_05/RFTX     I/O     Telit GPIO05 Configurable GPIO/Transmitter ON monitor     C       Reserved       17	CMOS 2.8V
M     Image: Model of the second sec	
70     TGPIO_01     I/O     Telit GPIO01 Configurable GPIO     C       72     TGPIO_21     I/O     Telit GPIO21 Configurable GPIO     C       73     TGPIO_07/BUZZE     I/O     Telit GPIO07 Configurable GPIO/Buzzer     C       74     TGPIO_02     I/O     Telit GPIO02 Configurable GPIO     C       74     TGPIO_02     I/O     Telit GPIO02 Configurable GPIO     C       75     TGPIO_16     I/O     Telit GPIO16 Configurable GPIO     C       76     TGPIO_09     I/O     Telit GPIO16 Configurable GPIO     C       76     TGPIO_13/ACTIV     I/O     Telit GPIO13 Configurable GPIO/ACTIVE pin to protect current leakage     C       78     TGPIO_05/RFTX     I/O     Telit GPIO05 Configurable GPIO/Transmitter ON monitor     C       17	CMOS 2.8V
TGPIO_21     I/O     Telit GPIO21 Configurable GPIO     C       73     TGPIO_07/BUZZE     I/O     Telit GPIO07 Configurable GPIO/Buzzer     2       74     TGPIO_02     I/O     Telit GPIO02 Configurable GPIO     C       75     TGPIO_16     I/O     Telit GPIO16 Configurable GPIO     C       76     TGPIO_09     I/O     Telit GPIO16 Configurable GPIO     C       76     TGPIO_09     I/O     Telit GPIO18 Configurable GPIO     C       77     TGPIO_13/ACTIV     I/O     Telit GPIO13 Configurable GPIO/ACTIVE pin to protect current leakage     C       78     TGPIO_05/RFTX     I/O     Telit GPIO05 Configurable GPIO/Transmitter ON monitor     C       Reserved       17	
73     TGPIO_07/BUZZE     I/O     Telit GPIO07 Configurable GPIO/Buzzer     2       74     TGPIO_02     I/O     Telit GPIO02 Configurable GPIO     0     0       75     TGPIO_16     I/O     Telit GPIO09 Configurable GPIO     0     0       76     TGPIO_09     I/O     Telit GPIO16 Configurable GPIO     0     0       77     TGPIO_16     I/O     Telit GPIO13 Configurable GPIO     0     0       77     TGPIO_13/ACTIV     I/O     Telit GPIO13 Configurable GPIO/ACTIVE pin to     0       78     TGPIO_05/RFTX     I/O     Telit GPIO05 Configurable GPIO/Transmitter ON     0       78     TGPIO_05/RFTX     I/O     Telit GPIO05 Configurable GPIO/Transmitter ON     0       74     TGPIO_05/RFTX     I/O     Telit GPIO05 Configurable GPIO/Transmitter ON     0       77     TGPIO_05/RFTX     I/O     Telit GPIO05 Configurable GPIO/Transmitter ON     0       74     TGPIO_05/RFTX     I/O     Telit GPIO/Transmitter ON     0       78     TGPIO_05/RFTX     I/O     Telit GPIO/Transmitter ON     0 <t< td=""><td>CMOS 2.8V</td></t<>	CMOS 2.8V
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74     TGPIO_02     I/O     Telit GPIO02 Configurable GPIO     C       75     TGPIO_16     I/O     Telit GPIO16 Configurable GPIO     C       76     TGPIO_09     I/O     Telit GPIO19 Configurable GPIO     C       77     TGPIO_13/ACTIV     I/O     Telit GPIO13 Configurable GPIO/ACTIVE pin to protect current leakage     C       78     TGPIO_05/RFTX     I/O     Telit GPIO05 Configurable GPIO/Transmitter ON monitor     C       Reserved       17	CMOS
TGPIO_16     I/O     Telit GPIO16 Configurable GPIO     C       76     TGPIO_09     I/O     Telit GPIO09 Configurable GPIO     C       77     TGPIO_13/ACTIV     I/O     Telit GPIO13 Configurable GPIO/ACTIVE pin to protect current leakage     C       78     TGPIO_05/RFTX     I/O     Telit GPIO05 Configurable GPIO/Transmitter ON monitor     C       Reserved       17	2.8V(PWM)
76   TGPIO_09   I/O   Telit GPIO09 Configurable GPIO   C     77   TGPIO_13/ACTIV   I/O   Telit GPIO13 Configurable GPIO/ACTIVE pin to   C     78   TGPIO_05/RFTX   I/O   Telit GPIO05 Configurable GPIO/Transmitter ON   C     78   TGPIO_05/RFTX   I/O   Telit GPIO05 Configurable GPIO/Transmitter ON   C     79   TGPIO_05/RFTX   I/O   Telit GPIO05 Configurable GPIO/Transmitter ON   C     78   TGPIO_05/RFTX   I/O   Telit GPIO05 Configurable GPIO/Transmitter ON   C     71   MON   MON   MON   MON   C     79   17   I/O   I/O   I/O   I/O     70   17   I/O   I/O   I/O   I/O     741   I/O   I/O   I/O   I/O   I/O     72   I/O   I/O   I/O   I/O   I/O     741   I/O   I/O   I/O   I/O   I/O     741   I/O   I/O   I/O   I/O   I/O     741   I/O   I/O   I/O   I/O   I/O     1	CMOS 2.8V
77   TGPIO_13/ACTIV   I/O   Telit GPIO13 Configurable GPIO/ACTIVE pin to   0     78   TGPIO_05/RFTX   I/O   Telit GPIO05 Configurable GPIO/Transmitter ON   0     78   TGPIO_05/RFTX   I/O   Telit GPIO05 Configurable GPIO/Transmitter ON   0     79   TGPIO_05/RFTX   I/O   Telit GPIO05 Configurable GPIO/Transmitter ON   0     79   TGPIO_05/RFTX   I/O   Telit GPIO05 Configurable GPIO/Transmitter ON   0     70   MON   Nonitor   10   10     71   10   10   10   10     71   10   10   10   10     72   10   10   10   10     741   10   10   10   10     72   10   10   10   10     73   10   10   10   10     741   10   10   10   10   10     74   10   10   10   10   10	CMOS 2.8V
E protect current leakage   78 TGPIO_05/RFTX I/O   MON Telit GPIO05 Configurable GPIO/Transmitter ON monitor C   Reserved   17 10   41 10 10   42 10 10	CMOS 2.8V
78   TGPIO_05/RFTX   I/O   Telit GPIO05 Configurable GPIO/Transmitter ON monitor   C     Reserved     17	CMOS 2.8V
MON     monitor       Reserved     17       17     1       41     1       42     1	
Reserved     17     17     17     17     17     17     17     17     17     17     17     17     17     10     <	CMOS 2.8V
17    41    42	
41 42	
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43	
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47	
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# 7. Interface Description

This chapter covers information required to convert the CC864-Dual into a subscriber unit application.

And this chapter include :

- UART1 : RS232 level translation for AT command
- R-UIM card holder
- USB
- IIC BUS Interface
- ADC/DAC signals
- General Purpose I/O

## 7.1. UART1(RS232 level translation)

The serial port on the CC864-DUAL is the core of the interface between the module and Host hardware.

Depending from the type of serial port on the Host hardware, a level translator circuit may be needed to make the system work. The only configuration that doesn't need a level translation is the 2.8V UART.

There are two UART port on the CC864-Dual. It differs from the PC RS232 in the signal polarity(RS232 is reversed) and levels. The levels for the CC864-Dual UART are the CMOS levels:

Absolute maximum ratings – Not functional

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.75V
Input voltage on analog pins when on	-0.3V	+3.0V

#### Operating Range – Interface levels(2.8V CMOS)

Level	Min	Max	
Input high level VIH	1.85V	3.15V	



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Input low level	VIL	-0.3V	0.9V
Output high level	VOH	2.4V	2.85V
Output low level	VOL	0.0V	0.45V

UART1 is used for interfacing between the CC864-Dual and Host. The CC864-Dual and its host transmit data or AT-command through RS-232 signal line.

The signals of the CC864-Dual serial port are:

RS232 Pin Nr	Signal	PIN Number	Name	Usage	
1	DCD-	32	Data Carrier Detect	Output from the CC864-Dual that	
	dcd_uart			indicates the carrier presence	
2	RXD-tx_uart	26	Transmit line	Output transmit line of CC864-Dual UART	
3	TXD-rx_uart	25	Receive line	Input receive of the CC864-Dual UART	
4	DTR-dtr_uart	29	Data Terminal Ready	Input to the CC864-Dual that control the DTE READY condition	
5	GND	5,6,7	Ground	Ground	
6	DSR-dsr_uart	27	Data Set Ready	Output from the CC864-Dual that indicates the module is ready	
7	RTS-rts_uart	31	Request to Send	Input to the CC864-Dual that controls the Hardware flow control	
8	CTS-cts_uart	28	Clear to Send	Output from the CC864-Dual that controls the Hardware flow control	
9	RI-ri_uart	30	Ring Indicator	Output from the CC864-Dual that indicates the incoming call condition	

In order to interface the CC864-Dual with a PC com port or a RS232(EIA/TIA-232) application a level translator is required. This level translator must

invert the electrical signal in both directions

change the level from 0/3V to 15/-15V

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accepts signals with lower levels on the RS232 side(EIA/TIA-562), allowing for a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.



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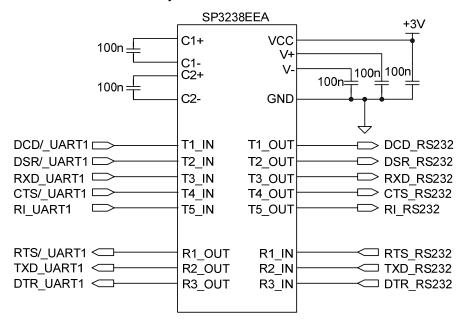


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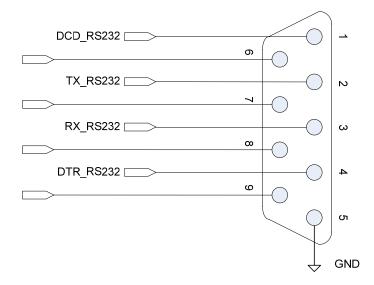
By convention the driver is the level translator from the 0-3V UART level to the RS232 level, while the receiver is the translator from RS232 level to 0-3V UART.

In order to translate the whole set of control lines of the UART you will need: 5 driver and 3 receiver

An example of level translation circuitry of this kind is :



The RS232 serial port lines are usually connected to a DB9 connector with the following layout :



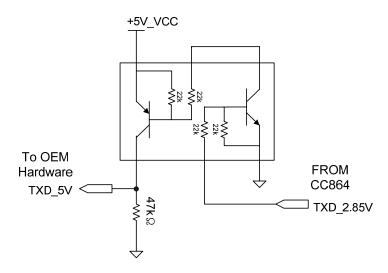


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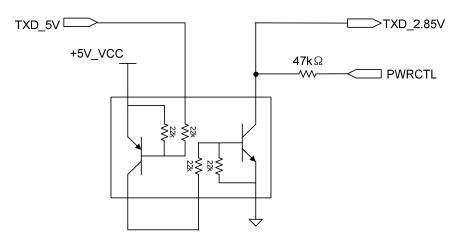


### 7.1.1. 5V UART level translation

If the Host application uses a microcontroller with a serial port(UART) that works at a voltage different from 2.8~3V, then a circuitry has to be provided to adapt the different levels of the two sets of signals. As for the RS232 translation there are a multiple of single chip translators, but since the translation requires very few components, then also a discrete design can be suited. For example a possible inexpensive translator circuit for a 5V driver can be:



And for a 5V receiver:



### 7.2. R-UIM Holder



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The Removable User Identify Module(R-UIM) is a smart card for CDMA cellular applications. R-UIM provides personal authentication information which allows the mobile station or handset to be connected with the network. The R-UIM card enables handset independence for the user. The R-UIM card can be inserted into any CDMA R-UIM equipped handset, allowing the user to receiver or make calls and receive other subscribed services from any R-UIM equipped handset.

### 7.2.1. R-UIM Design Guidelines

Aim of this section is to give basic design guide lines to integrate a R-UIM holder in applications that uses

Pin NO.	Signal Name	Signal Description	Direction
18	VREG_UIM_PWR_2.85V	Power supply	$CC864\text{-}Dual \to R\text{-}UIM$
19	UIM_RST	Reset signal	$CC864\text{-}Dual \to R\text{-}UIM$
20	UIM_DATA	Serial data	CC864-Dual $\leftrightarrow$ R-UIM
21	UIM_IN	NC	
22	UIM_CLK	Clock	$CC864\text{-}Dual \to R\text{-}UIM$

## 7.3. USB Port

The CC864-Dual includes a universal serial bus(USB) transceiver. This transceiver operates at USB low-speed(1.5Mbits/sec) and USB full-speed(12Mbits/sec). It is complaint with USB 2.0 specification. It can be used for diagnostic monitoring purpose.

Pin Number	Signal	Usage
35	USB_ID	Analog input used to sense whether a peripheral device is connected, and determine the peripheral type, a host or a slave
48	USB_VBUS	Power supply for the internal USB transceiver. This pin is configured as an analog input or and analog output depending upon the type of peripheral device connected.
79	USB_D+	Plus(+) line of the differential, bi-directional USB signal to/from the



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		peripheral device
80 USB D-	Minus(+) line of the differential, bi-directional USB signal to/from the	
00	036_0-	peripheral device

### 7.4. IIC Bus Interface

I2C is a two-wire bus for inter-IC communication that supports any IC fabrication process(NMOS, CMOS, bipolar, etc). Two wires(or lines), serial data(SDA) and serial clock(SCL), carry information between the connected devices. Each device is recognized by a unique address(whether it's a microcontroller, memory, LCD driver, stereo DAC, or keyboard interface) and can operate as either a transmitter or receiver, depending on the device function.

Pin No	Name	Description	
33	SCL	Serial BUS Clock	
34	SDA	Serial BUS Data	

## 7.5. ADC/DAC signals

Analog measurement output or sensor output(Battery voltage, temperature etc) can be connected to ADC pin. Then it change analog value to digital.

DAC pin drive out PWM signal and control external component. And you need additional RC filter to change PWM signal to analog signal.

Pin No	Name	Description	Direction
37	ADC_IN1	Analog/Digital converter	$\rightarrow$ CC864-Dual
		input	
38	ADC_IN2	Analog/Digital converter	$\rightarrow$ CC864-Dual
		input	
39	ADC_IN3	Analog/Digital converter	$\rightarrow$ CC864-Dual
		input	
40	DAC_OUT	Digital/Analog converter	← CC864-Dual
		input	





## 7.6. General Purpose I/O

The general purpose I/O pads can be configured to act in three different ways:

- input : Input pads can only be read and report the digital value(high or low) present on the pad at the read time
- output : output pads can only be written or queried and set the value of the pad output
- alternate function(internally controlled) : an alternate function pad is internally controlled by the CC864-Dual firmware and acts depending on the function implemented.

Din	Signal	I/O	Function	Tuno	Default	On_OFF	Alternative
Pin	Signal	10	Function	Туре	state	state	Function
70	TGPIO_01	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	
74	TGPIO_02	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	JDR
66	TGPIO_03	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	AUDIO MUTE
59	TGPIO_04	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	CONVERSATION
78	TGPIO_05	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	RFTXMON
68	TGPIO_06	I/O	Gonfigurable GPIO	CMOS2.8V	Input		ALARM
73	TGPIO_07	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	BUZZER
67	TGPIO_08	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	POWER_SAVING
76	TGPIO_09	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	
63	TGPIO_10	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	PCM_TX
57	TGPIO_11	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	VIBRATOR
62	TGPIO_12	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	CALL_KEY
77	TGPIO_13	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	ACTIVE
60	TGPIO_14	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	
61	TGPIO_15	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	
75	TGPIO_16	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	
71	TGPIO_17	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	PCM_SYNC
65	TGPIO_18	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	PCM_RX
56	TGPIO_19	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	
58	TGPIO_20	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	



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72	TGPIO_21	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	
64	TGPIO_22	I/O	Gonfigurable GPIO	CMOS2.8V	Input	Low	

### 7.6.1. Logic level specifications

Where not specifically stated, all the interface circuits work at 2.8V CMOS logic levels. The following tables shows the logic level specifications used in the CC864-Dual interface circuits :

#### Absolute maximum ratings – Not functional

Parameter	Min	Max
Input level on any digital pin when	-0.3V	+3.75V
on		
Input voltage on analog pins when	-0.3V	+3.0V
on		

#### Operating Range – Interface levels(2.8V CMOS)

Level	Min	Max
Input high level VIH	1.85V	3.15V
Input low level VIL	-0.3V	0.9V
Output high level VOH	2.4V	2.85V
Output low level VOL	0.0V	0.45V

#### For 1.8V

#### Operating Range – Interface levels(1.8V CMOS)

Level	Min	Max
Input high level	1.6V	2.1V
Input low level	-0.3V	0.63V
Output high level	1.35V	1.8V
Output low level	0.0V	0.35V

### 7.6.2. Using a GPIO pad as Input



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The GPIO pads, when used as input, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 2.8V CMOS levels of the GPIO

### 7.6.3. Using a GPIO pad as Output

The GPIO pads, when used as outputs, can drive 2.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

### 7.6.4. TGPIO\_03/AUDIOMUTE

This pin can be used to mute audio. It is always desirable to have a mute control on the amplifier, in order to turn it off while the device is not sending signal to the output, in this matter the amplifier background noise which may be audible during idle condition is cut off.

### 7.6.5. TGPIO\_04/CONVERSATION

This signal can be used as the audio amplifier enable control signal when the modem uses the audio amplifier on its receiver speaker output layer. It will reduce current consumption because it can activate the amplifier only when there is voice data.

### 7.6.6. TGPIO\_05/RFTXMON

This pin will be changed to High state when CC864-DUAL is transmitting state.



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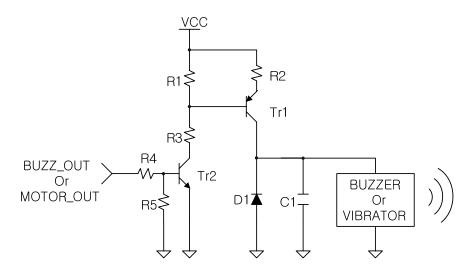
### 7.6.7. TGPIO\_06/ALARM

This pin, when configured as Alarm Output, is controlled by the CC864-Dual module and will rise when the alarm starts and fall after the issue of a dedicated AT command.

This output can be used to power up the CC864-Dual controlling microcontroller or application at the alarm time, giving you the possibility to program a timely system wake-up to achieve some periodic actions and completely turn off either the application and the CC864-Dual during sleep periods, dramatically reducing the sleep consumption to few  $\mu$ A. In battery powered devices this feature will greatly improve the autonomy of the device.

### 7.6.8. TGPIO\_07/BUZZER

This pin, when configured as Buzzer Output, is controlled by the CC864-Dual module and will drive with appropriate square waves a Buzzer driver. This permits to your application to easily implement Buzzer feature with ringing tones or melody played at the call incoming, tone playing on SMS incoming or simply playing a tone or melody when needed by your application. The example is :



### 7.6.9. TGPIO\_08/POWER\_SAVING

The Host gives this signal to the CC864-Dual, it makes the CC864-Dual turn to be power saving



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mode. This signal is Low enable. When the CC864-Dual enters into power saving mode, every active items include UART port will be off. So current consumption is considerably reduced.

And the CC864-Dual monitors the TXD line state of UART1. If the state will be changed Low state, the CC864-Dual will turn to be power saving mode automatically.

The application developer must keep in mind that this signal and TXD line state of UART1 perform same function. So if one of the both becomes Low state , the CC864-Dual will turn to be power saving mode.

### 7.6.10. TGPIO\_11/VIBRATOR

When configured as VIBRATOR output, this pin is controlled by the CC864-Dual module and will drive with appropriate square waves. Refer the Buzzer circuitry.

### 7.6.11. TGPIO\_12/CALL\_KEY

When Earjack is inserted, this pin is used to connect outgoing call or response incoming call.

### 7.6.12. TGPIO\_13/ACTIVE

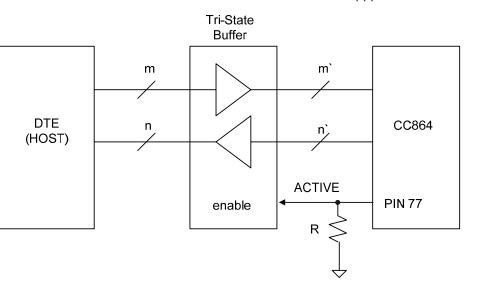
This signal is used as an enable signal to control the buffer between CC864-Dual and the host. When reset procedure and boot sequence are done successfully, CC864-Dual drives ACTIVE signal to be High state. And its output is Low state when CC864-Dual is power off. So a pull-down resistor is needed to be clear its state.

Most of the signals(except ON/OFF, RESET, STAT\_LED) between CC864-Dual and host must use a buffer. It prevents leakage currents flow from Host that is power-on stated to CC864-Dual that is power-off stated. Leakage current could cause CC864-Dual to reset failure.



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# 8. Audio Section

The CC864-DUAL module provides two different audio blocks; both in transmit(Uplink) and in receive(Downlink) direction:

"MT lines" should be used for handset function,

"HF lines" is suited for hands-free function or earphone function.

These two blocks can be active only one at a time, selected by AXE hardware line or by AT command.

The audio characteristics are equivalent in transmit blocks, but are different in the receive ones and this should be kept in mind when designing.

## 8.1. Differential Audio Interface design

You can use the MIC\_MT+, MIC\_MT-, EAR\_MT+, EAR\_MT-.

### 8.1.1. General Design Rules



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There are several configuration for the audio paths, but the most difference is between balanced and unbalanced microphone configuration.

It is highly recommended to keep the whole microphone path balanced even if this means having 2wires connecting the microphone instead of one needed in the unbalanced case. The balanced circuitry is more suited because of its good common mode noise rejection.

Keep the microphone traces on the PCB and wires as short as possible.

If your application requires an unbalanced microphone, then keep the lines on the PCB balanced and "unbalance" the path close to the microphone wire connector if possible.

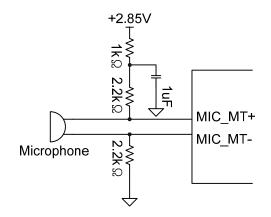
Make sure that the microphone traces in the PCB don't cross or run parallel to noisy traces(especially the power line).

If possible put all around to the microphone lines a ground trace connected to the ground plane by several vias. This is done in order to simulate a shielded trace on the PCB.

The CC864-DUAL provides two audio paths in receive section. Only one of the paths can be active at a time, selectable by AXE hardware line or by AT command.

#### 8.1.2. Microphone design

You need an additional external bias circuitry. The example is :



### 8.2. Receiver design

The EAR\_MT+, EAR\_MT- are the differential line-out drivers. You can drive directly a 16Ω earpiece

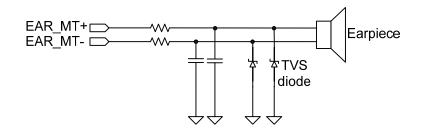


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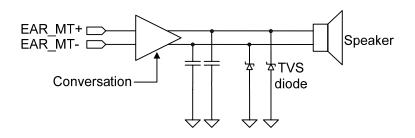
80pppSTzzzza Rev. 0, 12-Nov-07

and don't need an external audio amplifier circuitry. This solution is often the most cost effective, reducing the components count to a minimum. The example is :



## 8.3. Speaker design

The EAR\_MT+, EAR\_MT- are the differential line-out drivers. You can drive a  $8\Omega$  speaker with an external audio amplifier. This solution is can be used when high audio power is needed. The example is :



# 8.4. Single-ended Audio Interface design (Handfree or earphone design)

You can use the MIC\_HF+, MIC\_HF-, EAR\_HF+, EAR\_HF-.

Additional MIC\_HF+ bias circuitry, AUDIO\_AUX circuitry, AUDIO\_CALL\_BUTTON circuitry are needed.

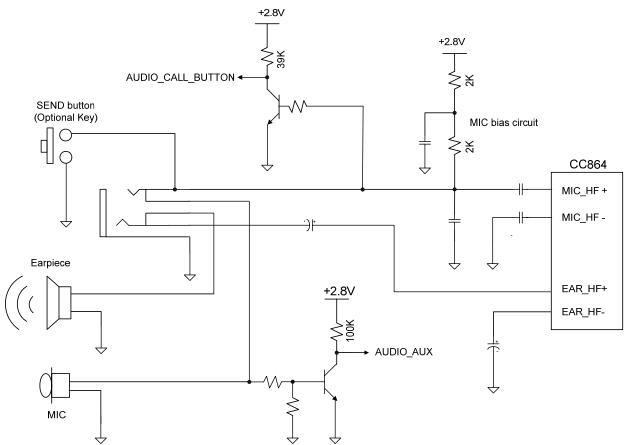
AUDIO\_AUX will be used to notify if earphone is inserted or not. AUDIO\_CALL\_BUTTON will be used to send outgoing call or to receive incoming call. The example is :



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## 8.5. Car kit speakerphone design

If you want to design carkit speakerphone with PCM signals, you must need an external codec and an external audio amplifier. When PCM signals connected, the default state of PCM\_RX signal is high state. CC864-DUAL monitor this signal and change audio path to PCM signals.

### 8.6. PCM Interface

The CC864-Dual PCM interface can be used in two modes : 1) auxiliary PCM(the default) running at 128kHz; or 2) primary PCM running at 2.048Mhz.

The auxiliary PCM interface enables communication with an external CODEC to support hands-



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free application. Linear,  $\mu$ -law, and A-law CODECs are supported by the auxiliary PCM interface. The auxiliary CODEC port operates with standard long-sync timing and a 128kHz clock. Most  $\mu$ -law and A-law CODECs are support the 128kHz AUX\_PCM\_CLK bit clock.

The auxiliary CODEC port also supports 2.048Mhz PCM data and sync timing for linear, µ-law, and A-law CODECs that match the sync timing – this is called the primary PCM interface(or just PCM interface). PCM interface can be configured and controlled by either direct register access through the CODEC\_CTL register, or by the aDSP CODEC configuration command. Using the CODEC configuration command is the preferred method.

Pin Number	Name	I/O	Description	Level
36	PCM_CLOCK	I/O	PCM_CLOCK	CMOS 2.8V
63	TGPIO_10/PCM_TX	I/O	TGPIO10 Configurable GPIO/PCM_TX	CMOS 2.8V
65	TGPIO_18/PCM_RX	I/O	TGPIO18 Configurable GPIO/PCM_RX	CMOS 2.8V
71	TGPIO_17/PCM_SYNC	I/O	TGPIO17 Configurable GPIO/PCM_SYNC	CMOS 2.8V

# 9. Miscellaneous signals

## 9.1. VAUX1

A regulated power supply output is provided in order to supply small devices from module. This output is active when the module is ON and goes off when module is shut down. The operating range characteristics of the supply are:

Operating Range – Vout power supply

Parameters	Min	Тур	Max
Output voltage	2.75V	2.85V	2.95V
Output current			100mA



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Output bypass		2.2uF	
capacitor			

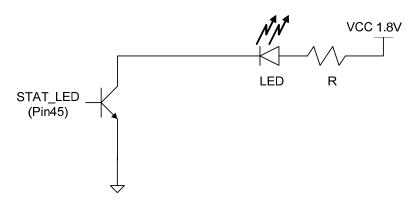
Care must be taken to avoid latch-up on the CC864-Dual and the use of this output line to power electronic devices shall be considered with care, especially for devices that generate spikes and noise such as level translators, digital ICs or microcontroller, failure in any of these condition can severely compromise the CC864-Dual functionality.

## 9.2. VRTC

This pin is used to supply power to RTC(Real Time Clock) Module when CC864-Dual is off state. RTC module can power up CC864-Dual at alarm time. Refer the "TGPIO\_06/ALARM" part. Connect Super capacitor at this pin. Super capacitor is charged when CC864-Dual is on and it supply power to the RTC Module when CC864-Dual is off.

### 9.3. STAT\_LED

This pin is a open collector output signal. It can be synchronized by Slot Cycle Index to make the LED blinking. Turn On time is 50ms. If the modem is in no service area, the modem turns off the LED. The LED is blinking in idle mode, and keeps Turn On in traffic mode.





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## 9.4. PWRMON

Its function is similar to ACTIVE. If the reset procedure or boot sequence is finished successfully, PWRMON will be changed to High state.

## 9.5. AUDIO\_AUX

This pin can be used for Handfree(earphone detection) switching. If the earphone is inserted to the earjack connector, CC864-Dual will change the audio path to MIC\_HF± and EAR\_HF± from MIC\_MT± and EAR\_MT±.





# 10. Safety Recommendations

#### READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas :

Where it can interface with other electronic devices in environments such as hospitals, airports, air crafts, etc

Where there is risk of explosion such as gasoline, oil refineries, etc

It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations.

The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the R-UIM card, checking carefully the instruction for its use. Do not insert or remove the R-UIM when the product is in power saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue. Should there be any doubt, please refer to the technical documentation and the regulation in force.

Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interface with other electronic devices and has to quarantine a minimum distance from the body(20Cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.



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# 11. Reference

- QSC6055<sup>™</sup>, QSC6065<sup>™</sup>, QSC6075<sup>™</sup> and QSC6085<sup>™</sup> Single Chip<sup>™</sup> Device Specification 80-VC881-1
- QSC6055<sup>™</sup>, QSC6065<sup>™</sup>, QSC6075<sup>™</sup> and QSC6085<sup>™</sup> Qualcomm Single Chip<sup>™</sup> User Guide 80-VC881-3

# 12. Document Change Log

Revision	Date	Changes
Draft #0	12-Nov-07	Draft



## **FCC Compliance Information**

This device complies with Part 15 of FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received. Including interference that may cause undesired operation.