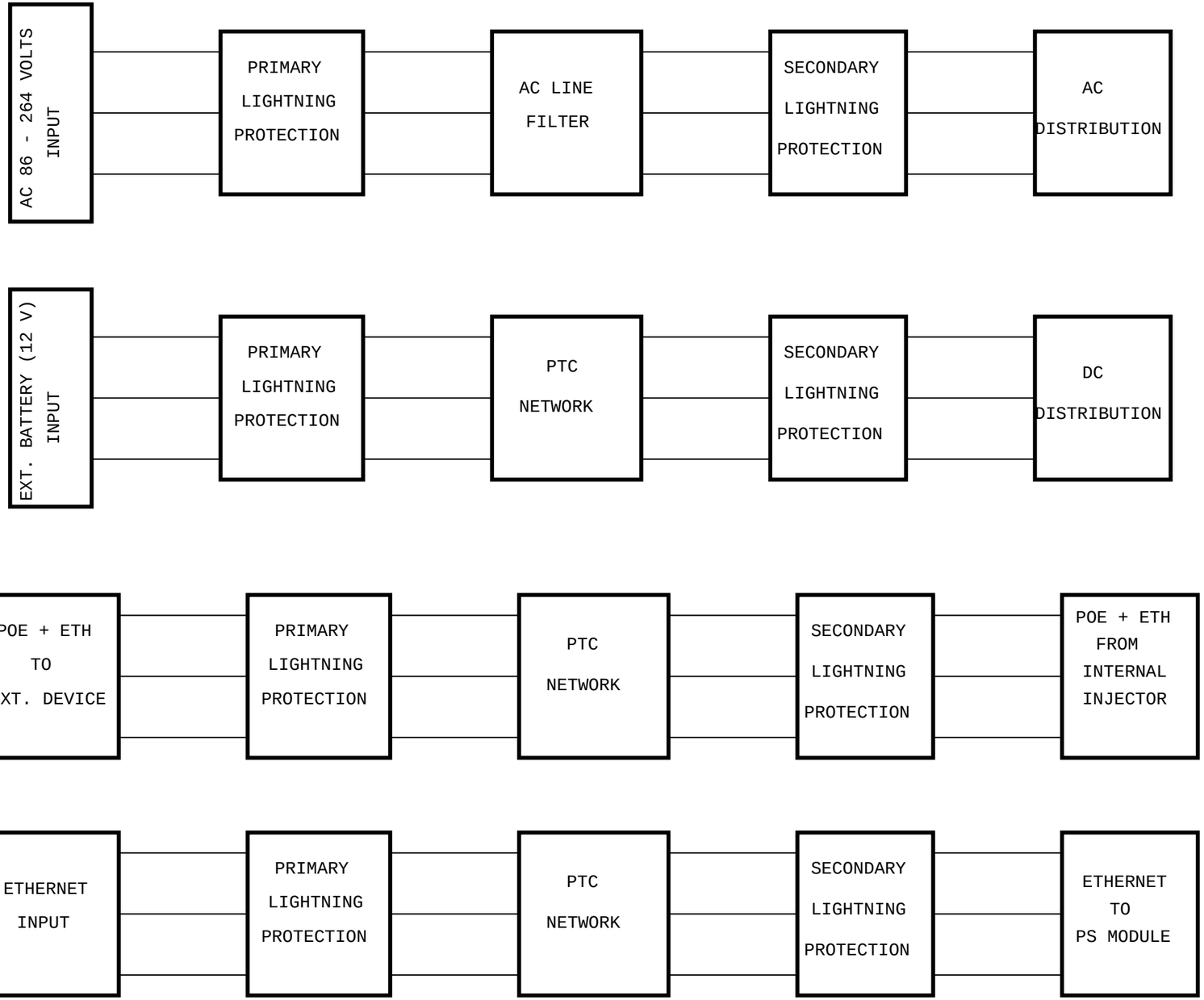

NOTES:

10/6/04 600-0103-01 Rev. A - Initial Release

12/2/04 600-0103-02 Rev. A - Artwork Change Only - Corrected AC Line Spacing

01.01 Sheet index & block diagram

PCB1

PCB
610-0103-02

Thursday, December 02, 2004
16:07:30 GMT

STRIX SYSTEMS, INC.
26610 AGOURA RD. SUITE 110
CALABASAS, CA 91302

Title: SCHEMATIC, LIGHTNING PROTECTION MODULE

Size	Document Number	Rev
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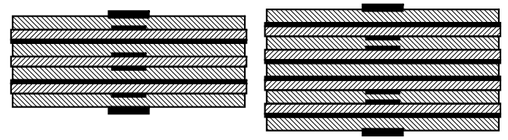
Date: Sheet 1 of 4

NOTES. Unless otherwise stated on this schematic:

1. All resistor values are in ohms.
2. All resistors are 0603 package, 1/16th Watt, 1% tolerance.
3. All resistor networks are 1/16th Watt, 2% or 5% tolerance, EXB-38V (3.2mm x 1.6mm) package.
4. All capacitor values are in microfarads.
5. All non-polarized capacitors are 10V (or greater) working, 10% tolerance, 0603 package.
6. All polarized capacitors are 6V (or greater) working, 20% tolerance, A-Case (3.2mm x 1.6mm).
7. All polarized capacitors are to face the same way (may be at rightangles, but with consistent polarity).
8. Pin numbers on polarized capacitors do not necessarily indicate polarity.
9. Nets with names containing CLK are to be routed first, using 3W rule (see illustration), avoiding outer layers. They must be adjacent to an unbroken (non-split) part of a power or ground plane. No PPs on stubs to be placed on CLK nets.
10. Series damping resistors/networks are to be placed close to the chip as drawn (driving end).
11. Layout is to allow socketing of programmable parts as noted.
12. "TP" indicates a physical Test Point (Harwin H3442-01). "PP" indicates a pad-only Probe Point (0.035" square, on 0.050" centers).
13. Testability: All nets except CLK lines are to have at least a PP Probe Point on the solder side, a probeable via, or a through-hole lead. Power and Ground nets to be accessible via multiple probe points. CLK lines should use existing vias for test wherever possible.
14. Silk-screen is to show numbers of at least the corner pins of all connectors, on both sides of the board.
15. Silk-screen is to show every tenth pin of fine pitch devices with a dash mark.
16. Silk-screen is to show as many row/column designators of BGA packages as possible.
17. Silk-screen is to show ground test points as "GND" instead of a TP reference designator.
18. Silk-screen is to show a reference designator for all devices except Probe Points (PPs).
19. Check final silk-screen for missing text due to masking by other layers
20. Values and part numbers are shown for reference only. See separate Bill of Materials.
21. Cut back power planes at edge of board at least 0.025" more than ground plane, more if possible.
22. Do not run any traces outside power plane cutback.
23. After final placement, renumber reference designators to facilitate assembly (Left to right, top to bottom, solder side starts at high-number). Check for anomalous auto-numbering.
24. Limit all trace lengths that are over 1 inch to twice their Manhattan Length.
25. Place a "Keep Out" area beneath all clock oscillators and clock drivers, on all layers.
26. No thieving to be added to this design.
27. In general, resistors or resistor networks may share power/ground vias with other resistors or with capacitors. Capacitors should not share power/ground vias with other capacitors.
28. Nets with names containing VCC33_, VCC20_, GND_ etc. are local power/ground traces and should be at least 0.015" wide. See schematic for more specific Instructions.
29. Nets with names containing DRV are series resistor drivers and must be shorter than 1"
30. All balls on BGAs are to have a breakout (via) regardless of whether the ball is used or not.
31. Manufacturer logo and other information to be in silk screen only.
32. Absolutely no changes/additions to gerbers within board outline permitted.

Layer stack is T.B.D.

GROUND Layer should use 2 Oz. Copper



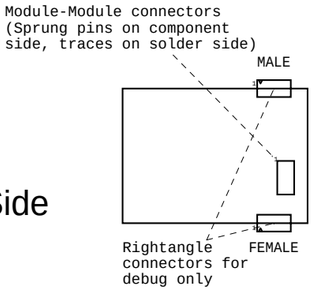
Approx. 0.007" core & prepreg Approx. 0.006" core & prepreg

Not to scale

Board thickness = 0.062"

Location of inter-module connectors (See pg. 03.02)

View from Component Side



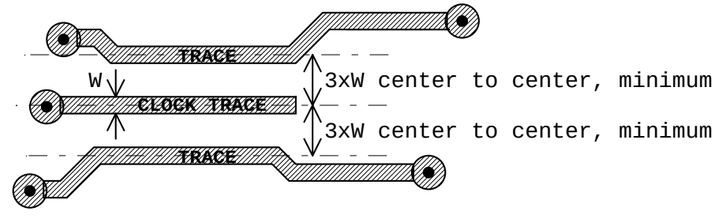


Illustration of "3W rule" for clocks

01.02 Notes

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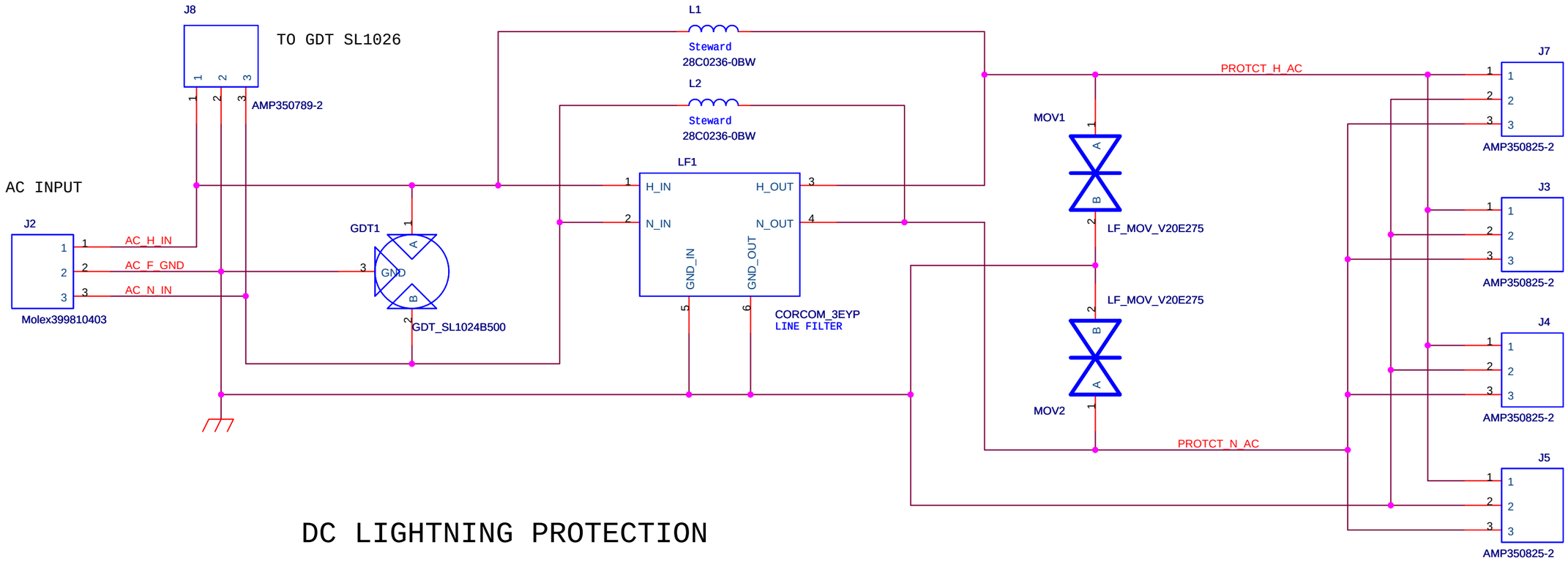
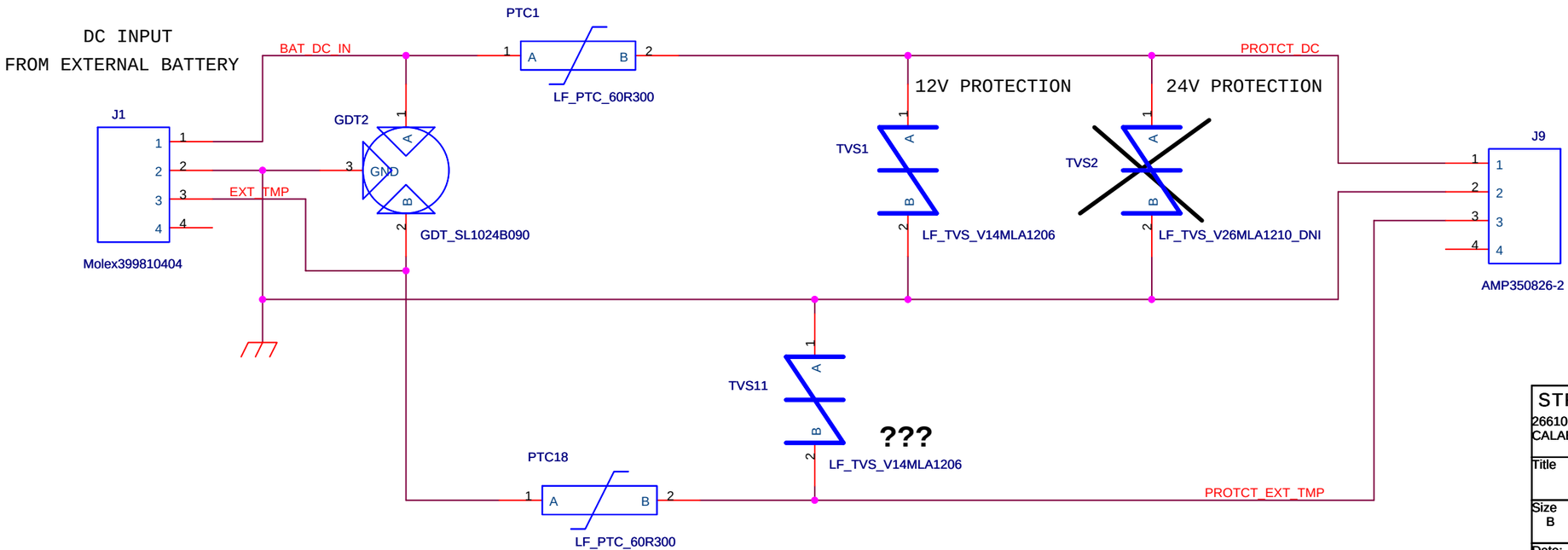
AC LIGHTNING PROTECTION



DC LIGHTNING PROTECTION



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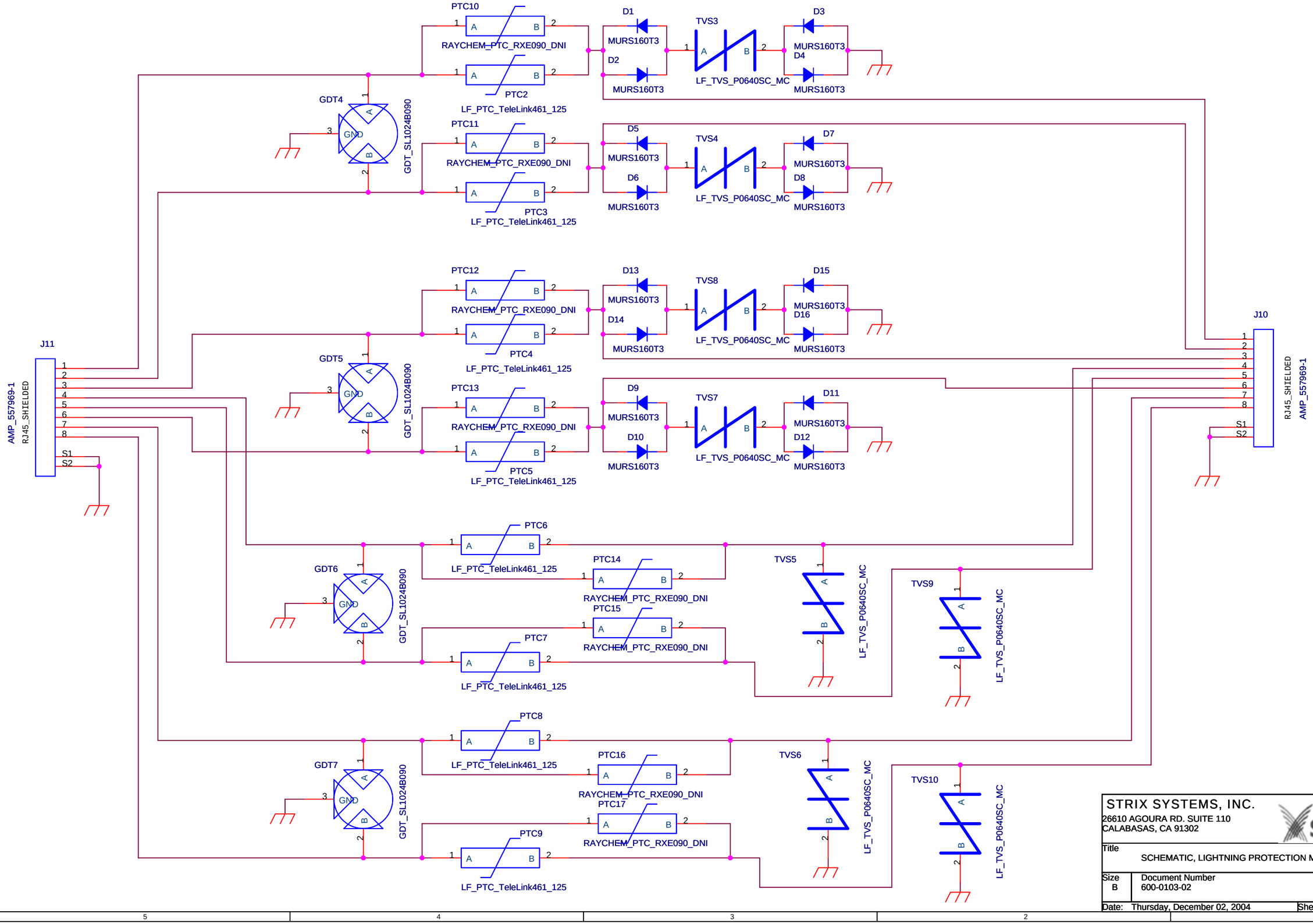

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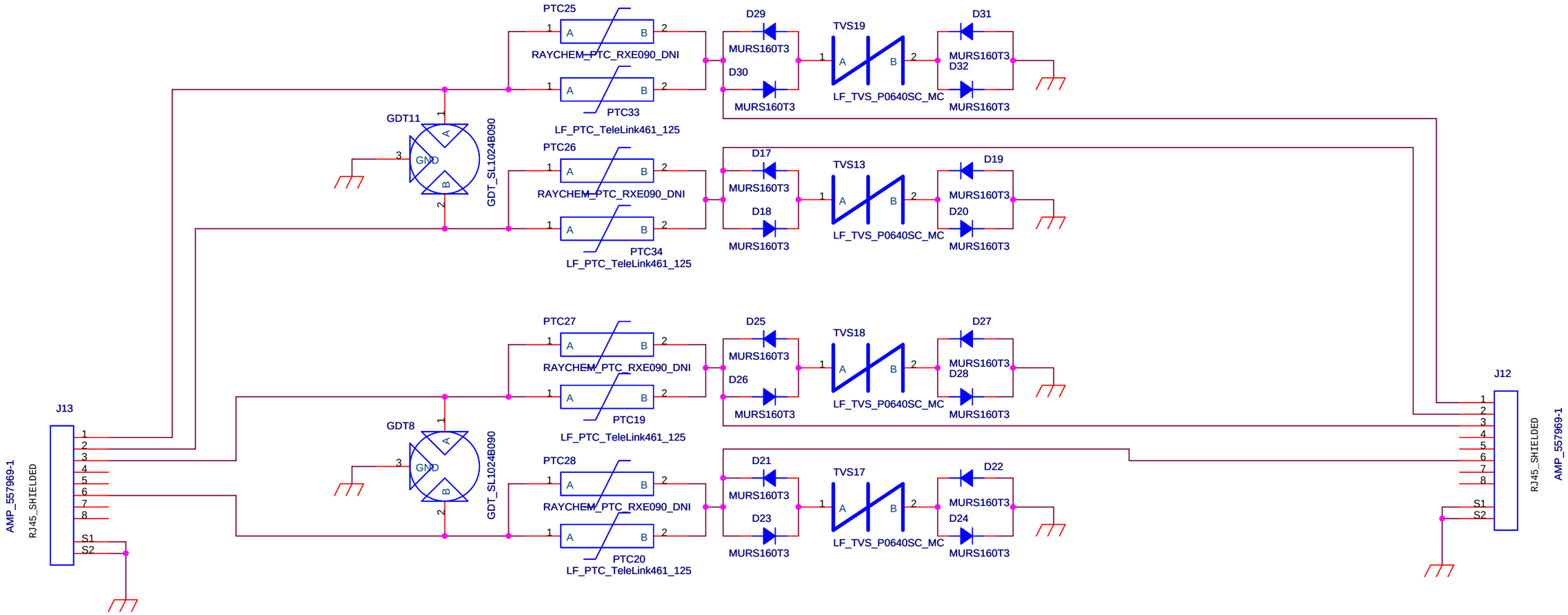

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