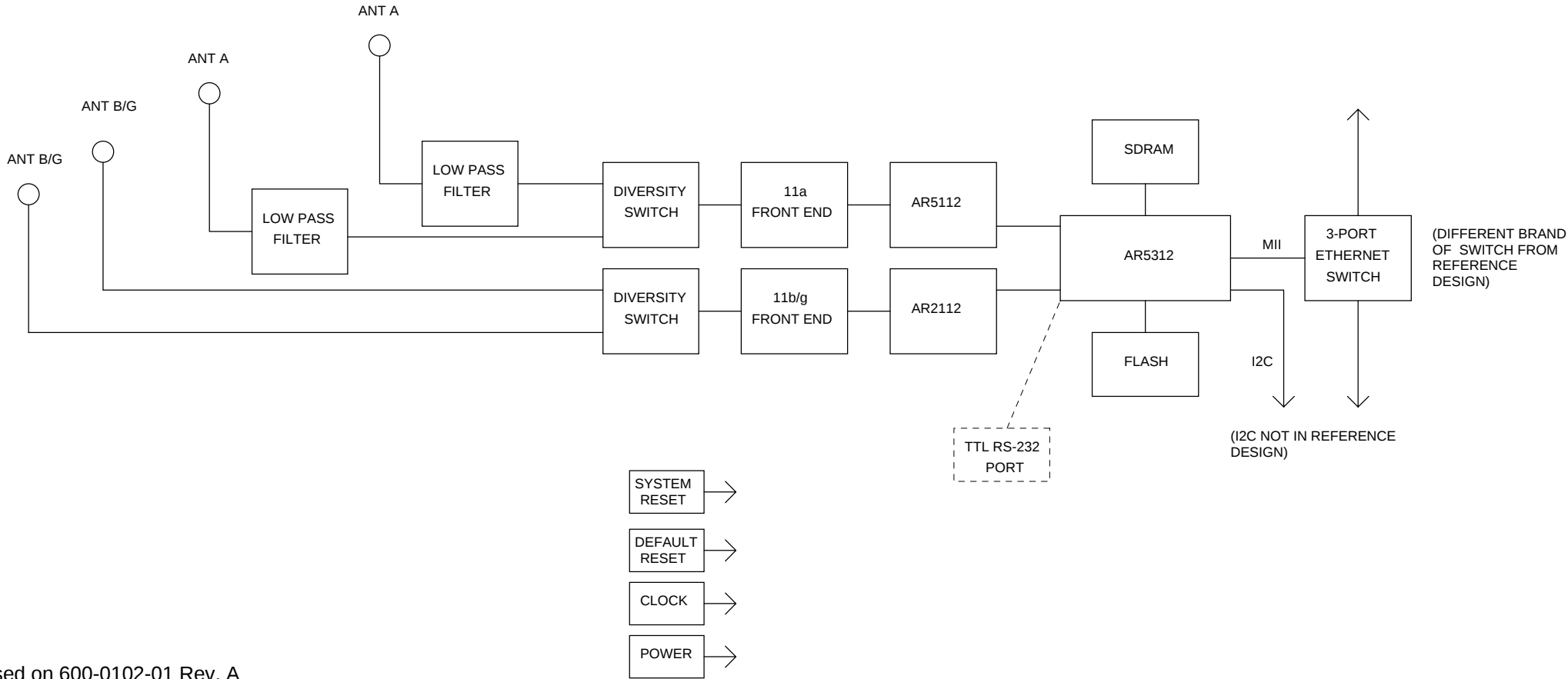


SHEET INDEX

- 01.01 Sheet index & block diag.
- 01.02 Notes
- 02.01 Atheros Rev. Info
- 02.02 Memory_Reset_GPIOs_RS232
- 02.03 Radio_Interfaces
- 02.04 AR5112_11a
- 02.05 AR5112_11g
- 02.06 11a_RF_Front_End
- 02.07 11g_RF_Front_End
- 02.08 PowerPins_Vin
- 02.09 Misc
- 03.01 Ethernet to processor
- 03.02 Ethernet to outside
- 04.01 Reset circuit, I2C
- 04.03 Power regulators
- 05.01 Ethernet Switch Power
- 07.01 RF interconnect



600-0102-02 History

- Rev A: Proto release based on 600-0102-01 Rev. A
- Artwork change only.
- Improved the matching of the A Radio RF lines to the connectors.
- Improved silk screen markings.

600-0102-01 History

- Rev A: Proto release based on 600-0026-01 Rev.8
- Changed RF output to 2x 802.11A and 2x 802.11B/G
- Added System Reset in addition to Default Reset
- Modified intra board connectors

600-0036-01 History

- Rev A: Proto release based on 600-0026-01 Rev.8
- Added side RF connector and removed I2C Mux.
- GPIO2 routes radio output to Int. or Ext RF connector

600-0026-01 History

- Rev 8: Added GPIO to control MS bit of FLASH file system
- Pin swaps on GPIO and SDRAM data resistor packs
- Rev 7: Hooked up GPIOs to I2C controller reset and INT.
- Rev 6: Changed 2-cap/1-pad scheme in front end. Memory size changes
- Rev 5: Corrected duplicate reference designators
- Rev 4: Update to AP30-046 (Cap. DNIs and value change. See sheet 02.01)
- Smaller xtal package for Kendin. Spacer added to serial port connector.
- Rev 3: Corrected BGA reference designator
- Changed misc. LEDs to surface mount
- Separate transistor drivers for LEDs
- GPIO changes
- Rev 2: Updated to Atheros AP30-044
- Rev 1: Made from 0014 Rev 18 schematic plus Atheros AP30-042
- Changed bias tee values

01.01 Sheet index & block diagram

Wednesday, February 16, 2005
14:40:08 GMT

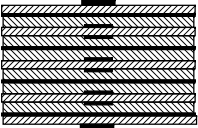
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Size C	Document Number 600-0102-02	Rev A
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NOTES. Unless otherwise stated on this schematic:

1. All resistor values are in ohms.
2. All resistors are 0603 package, 1/16th Watt, 1% tolerance.
3. All resistor networks are 1/16th Watt, 2% or 5% tolerance, EXB-38V (3.2mm x 1.6mm) package.
4. All capacitor values are in microfarads.
5. All non-polarized capacitors are 10V (or greater) working, 10% tolerance, 0603 package.
6. All polarized capacitors are 6V (or greater) working, 20% tolerance, A-Case (3.2mm x 1.6mm).
7. All polarized capacitors are to face the same way (may be at rightangles, but with consistent polarity).
8. Pin numbers on polarized capacitors do not necessarilly indicate polarity.
9. Nets with names containing CLK are to be routed first, using 3W rule (see illustration), avoiding outer layers. They must be adjacent to an unbroken (non-split) part of a power or ground plane. No PPs on stubs to be placed on CLK nets.
10. Series damping resistors/networks are to be placed close to the chip as drawn (driving end).
11. Layout is to allow socketing of programmable parts as noted.
12. "TP" indicates a physical Test Point (Harwin H3442-01). "PP" indicates a pad-only Probe Point (0.035" square, on 0.050" centers).
13. Testability: All nets except CLK lines are to have at least a PP Probe Point on the solder side, a probeable via, or a through-hole lead. Power and Ground nets to be accessible via multiple probe points. CLK lines should use existing vias for test wherever possible.
14. Silk-screen is to show numbers of at least the corner pins of all connectors, on both sides of the board.
15. Silk-screen is to show every tenth pin of fine pitch devices with a dash mark.
16. Silk-screen is to show as many row/column designators of BGA packages as possible.
17. Silk-screen is to show ground test points as "GND" instead of a TP reference designator.
18. Silk-screen is to show a reference designator for all devices except Probe Points (PPs).
19. Check final silk-screen for missing text due to masking by other layers
20. Values and part numbers are shown for reference only. See separate Bill of Materials.
21. Cut back power planes at edge of board at least 0.025" more than ground plane, more if possible.
22. Do not run any traces outside power plane cutback.
23. After final placement, renumber reference designators to facilitate assembly (Left to right, top to bottom, solder side starts at high-number). Check for anomalous auto-numbering.
24. Limit all trace lengths that are over 1 inch to twice their Manhattan Length.
25. Place a "Keep Out" area beneath all clock oscillators and clock drivers, on all layers.
26. No thieving to be added to this design.
27. In general, resistors or resistor networks may share power/ground vias with other resistors or with capacitors. Capacitors should not share power/ground vias with other capacitors.
28. Nets with names containing VCC33_, VCC20_, GND_ etc. are local power/ground traces and should be at least 0.015" wide.
29. Nets with names containing DRV are series resistor drivers and must be shorter than 1"
30. All balls on BGAs are to have a breakout (via) regardless of whether the ball is used or not.
31. Vendor identification on bare board to be in silkscreen only, not in copper
32. No changes to be made by board vendor to copper withing board outline without written authorization

Layer stack - TBD



Approx. 0.004" core & prepreg

Not to scale

Board thickness = 0.062"

Location of inter-module connectors

View from Component Side

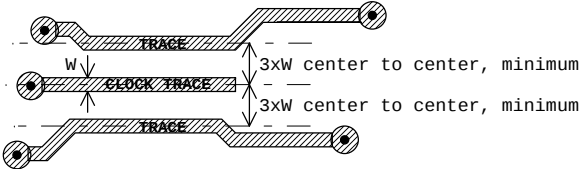
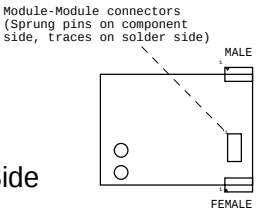


Illustration of "3W rule" for clocks

01.02 Notes

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Recent 0014 history:
Rev 18: Added RF filter
Rev 17+: Made diversity connectors DNI
Rev 17: Released to BOM.COM
Reduced RF/GPIO isolation cap to 2200pF
Rev. 16 Added back cut-off section
Rev 15: Released to BOM.COM
Changed Red LED resistor to 35.7 ohms
Added miniature TTL-RS232 socket

THESE UPDATES "MANUALLY"
PERFORMED ON 600-0026-01

DATE	REVISION NUMBER	INITIALS	DESCRIPTION
	245-01172-010		INTERNAL RELEASE
3/31/03	245-01172-020	EA	INITIAL CUSTOMER RELEASE
4/7/03	245-01172-021	EA	Update F3 to LFB215G37SG8A185, F4 to HHM-1562B, F8 to DEA205425BT-2028A4, F12 to HHM-1517, F13 to DEA252400BT-2030A1, R64 to 100 1%, R128 to 100 1%, D2 and D4 to no stuff, R138 to 750 1%, R140 to 10k 1%, D1 and D3 to SMS7621-079 for 020 board build.
4/16/03	245-01172-030	EA	Changed WLAN LED to two single color LEDs to fit the AP21 form factor. R99 to 1pF, L22 to 3.3nH, L20 to 4.3nH, L18 to 1.8nH, L16 to 1.8nH, L15 to 1.6nH, R80 to 350, R85 to 200, C196 to 2.4pF, C66, C88, C94 to 2.2pF. Added, R151-R154. ADDED R155, R156, R157.
5/25/03	245-01172-040	EA	Changed L11 to C284 0.5pF cap; L4 to 3.3nH; C101and L12 to no stuff; U3 pin 14 to 3.3V_A_11a; L11, C111, C112 to 0.5pF caps; SDRAM series Rs and R65 and R66 to 56 Ohm; R87, R88 to 150 Ohm; R100, R102 to R; C149 and C168 to 30pF, 1%; C46, C47, C187, C207 to C, C146 to 1.8pF; C196 to 2.7pF; L26 to 3.9nH. Deleted L13 and C121. Added VR for clock oscillator ckt, C285, C286, C287, C291, C292, R158, R159, R160, R161, R162, C293, C297, L35, L36, second antenna connector pair. Connected VR6 to 2.5V.
5/27/03	245-01172-041	EA	Changed L8 and L9 to 1.8nH; R78 to 1.21k, 1%; R157 to 10k, 1%; R115 to R. Fixed comment for AR2312 from U4 to U10.
6/3/03	245-01172-042	EA	Changed R94 to R; R87, R88 to 100, 1%; C284 to 0 Ohm; R128 to 249, 1%; R64 to 158, 1%; C168 to 15pF; C149 to 4pF; R67 to 6.19k, 1%; R78 to 10k, 1%; R83, C297 to 100pF; R77 to 133, 1%; Q6 to MMBT5179; C142, C293, C295 to 0.1uF; C141 to 100pF; R160 to 68; C294 to 4.7uF; C296 to 2.2uF; U9 to AR2112; S1, S2 to MASWSS0094; F5, F7 to LDG0UQD-3060C. Changes reflect loading of the extenal oscillator circuit.
6/27/03	245-01172-043	EA	Changed C35, C51, C141, C142, C287, C293, C294, C295, C296 to C; R67, R77 to R; L17 to L; Q6 to Q; VR7 to no stuff; C71, C77 to 10uF; C282 to 22uF; C149, C168 to 10pF; C46 to 1.2pF; R78 to 1M Ohm; R83 to 0; C297 to 0 Ohm; L4 to 1.8nH; J2 to P64-13Z-0AG9.
7/24/03	245-01172-044	EA	Changed (to use Murata filter) L15, L18, L22 to 0 Ohm; L16 and L20 to L; F10 to LFB2H2G45SG7A204. Changed (to improve spurs) C279 to 22uF. Changed U7 to MT48LC4M32B2TG-7.
8/19/03	245-01172-045	EA	Changed C187, C207, C283 to C; C279 to 33uF Tantalum.
9/18/03	245-01172-046	HB	Consolidate the manufacturer, No Design Changes.

AP30 - AR5002AP BASED,
CONCURRENT 802.11a and 802.11b/g,
WIRELESS ROUTER

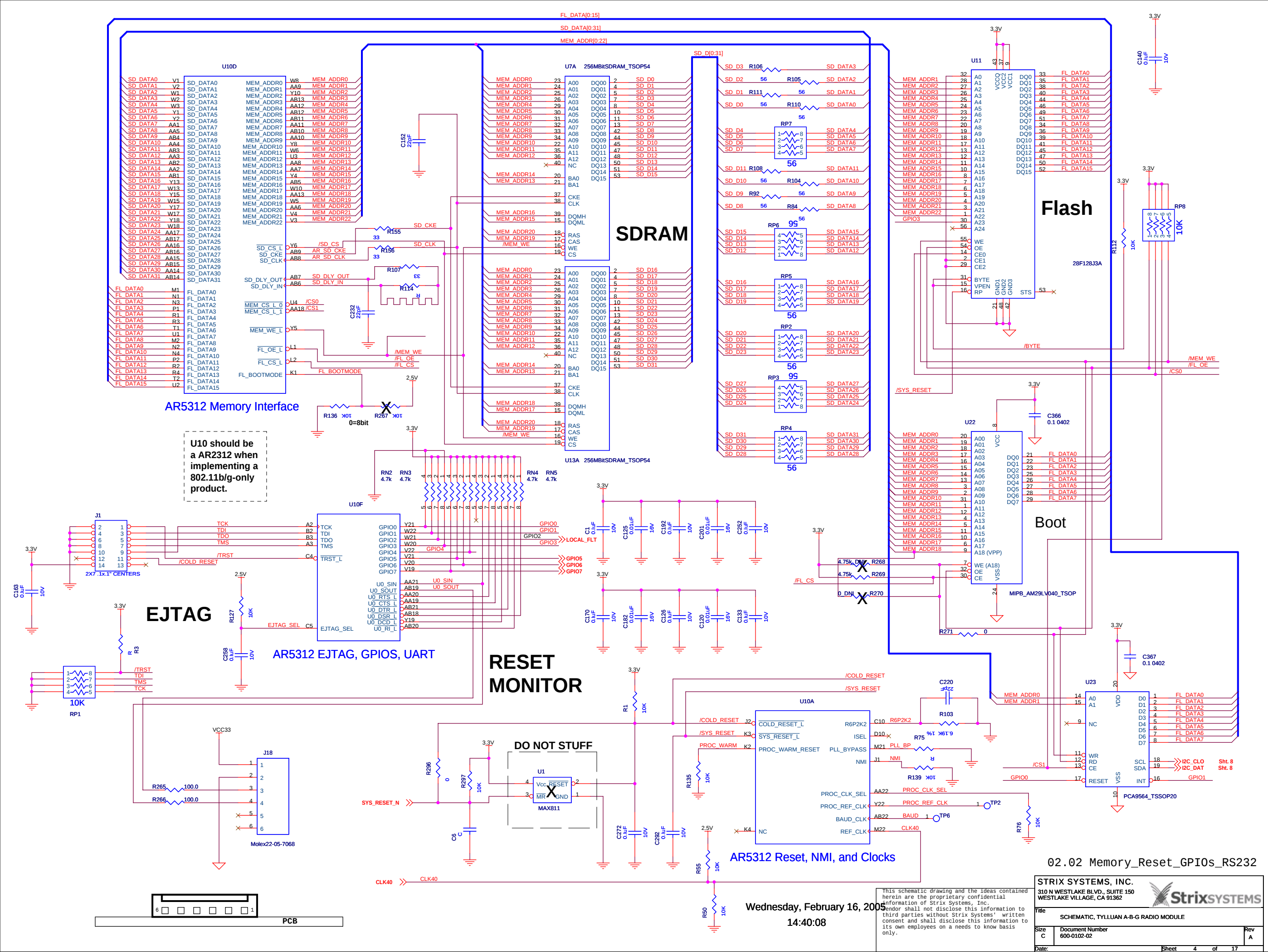
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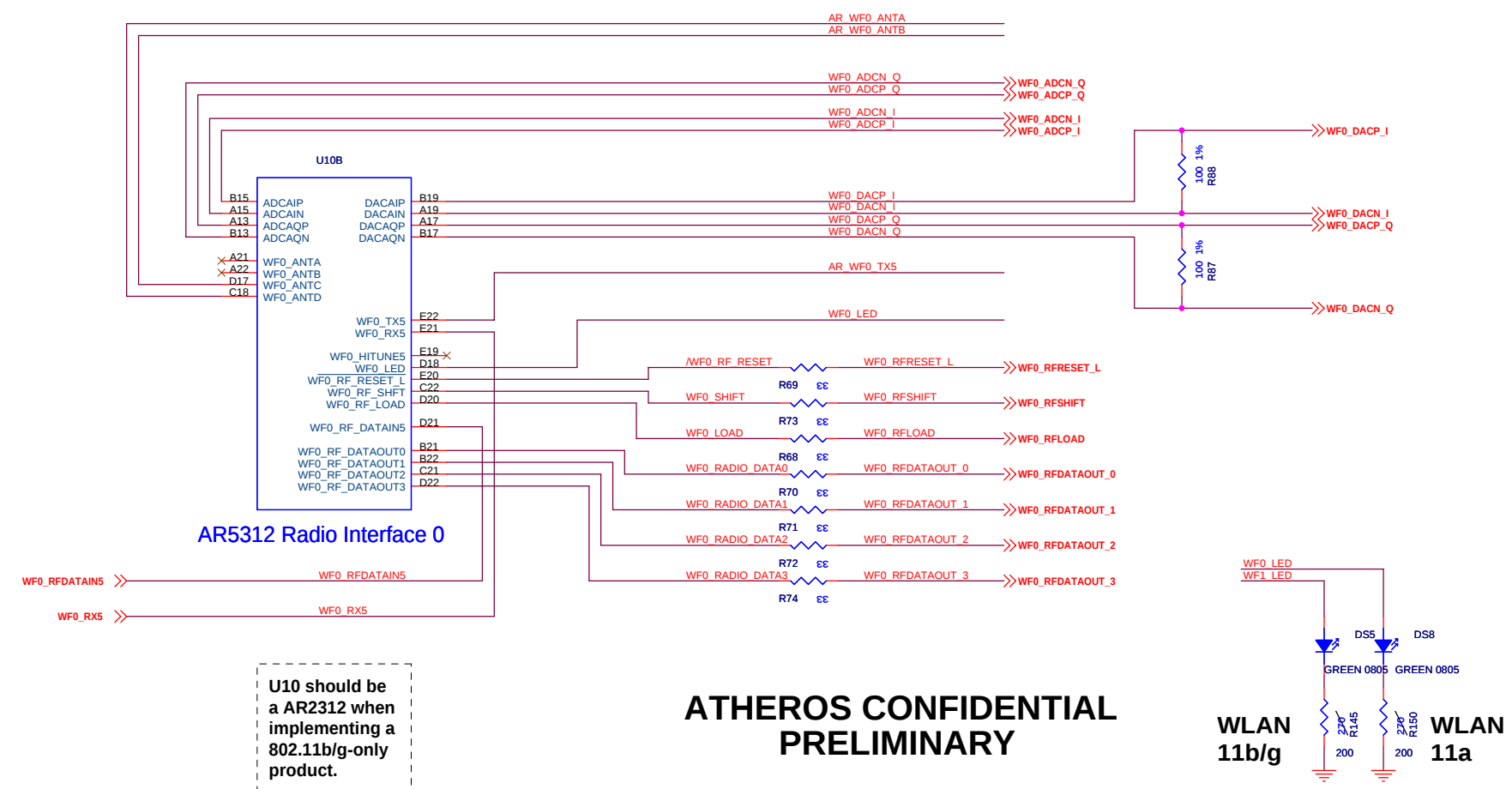
02.01 Rev. Info

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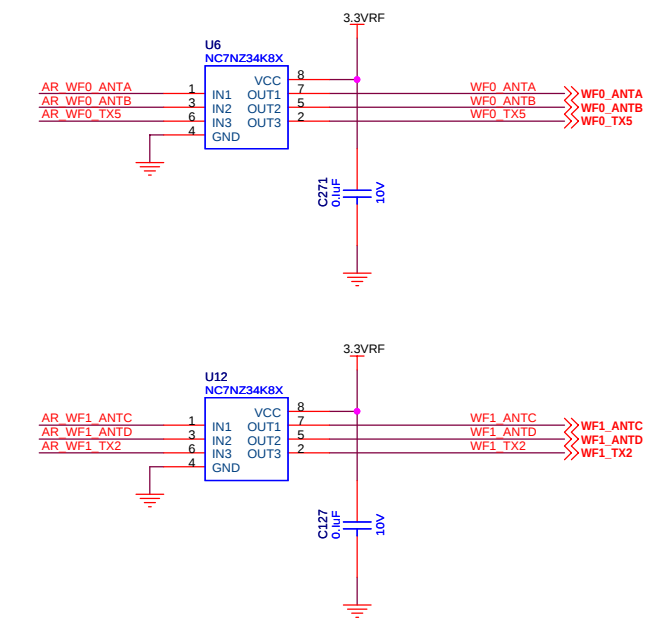
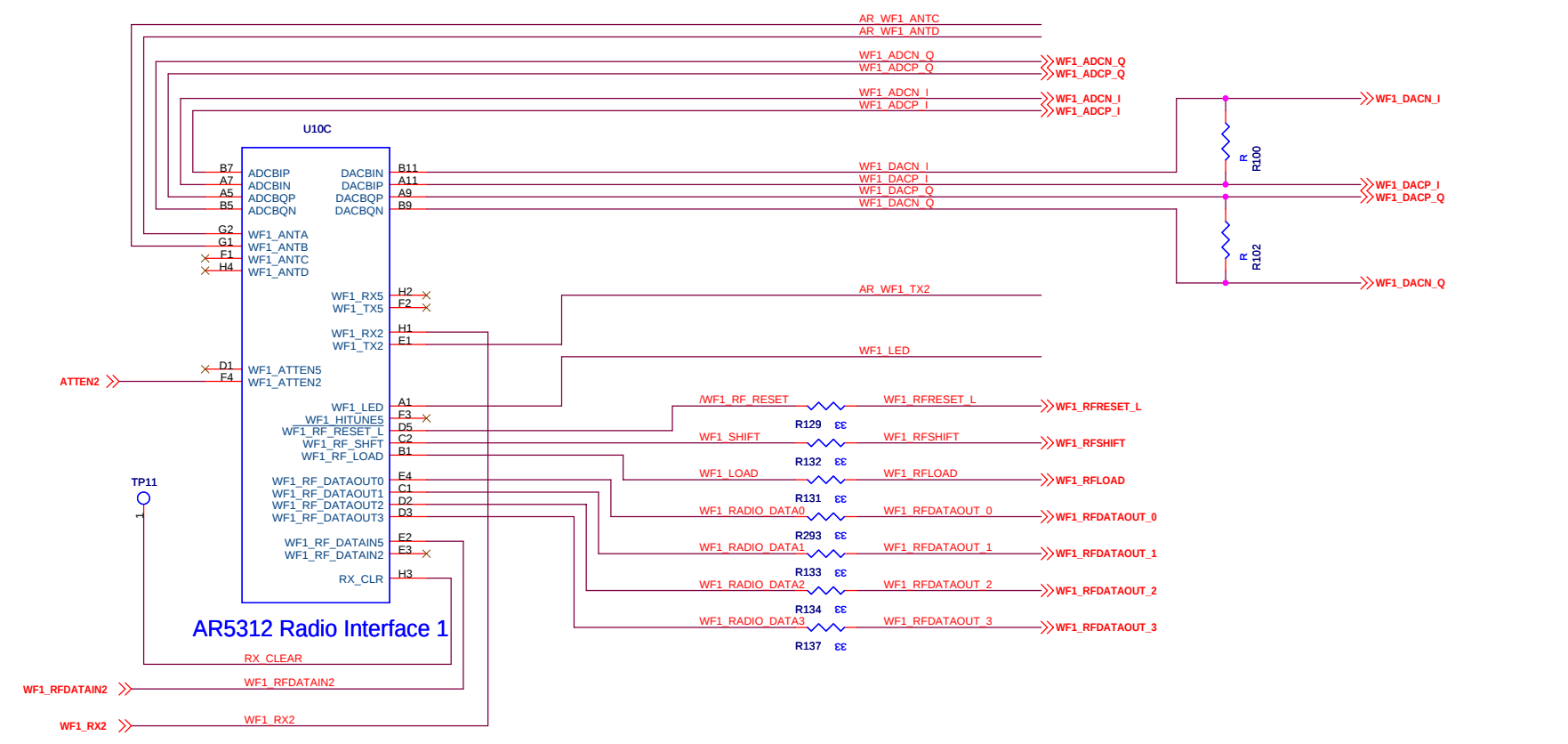
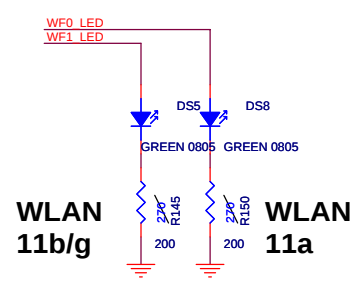
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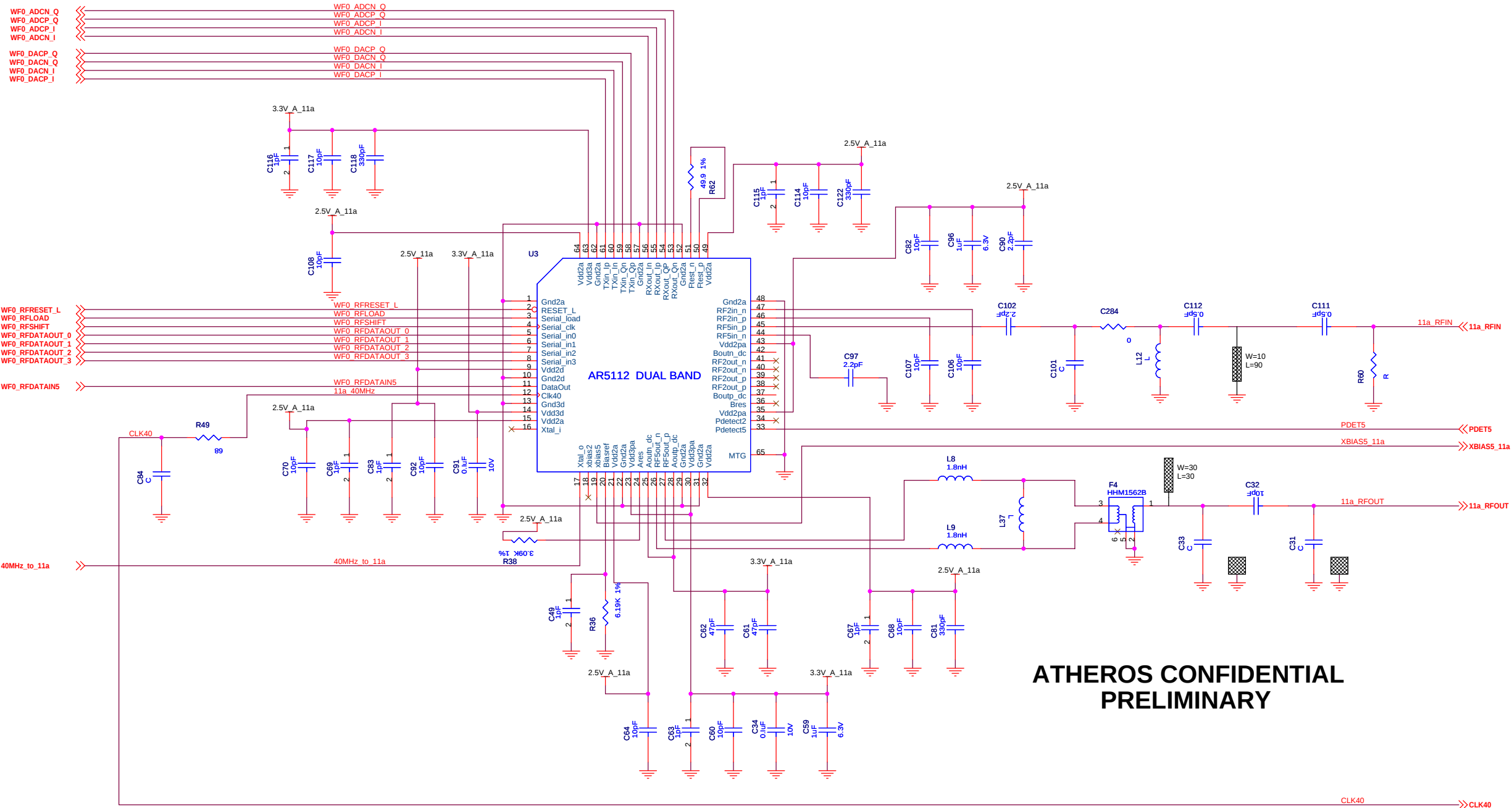
02.03 Radio_Interfaces

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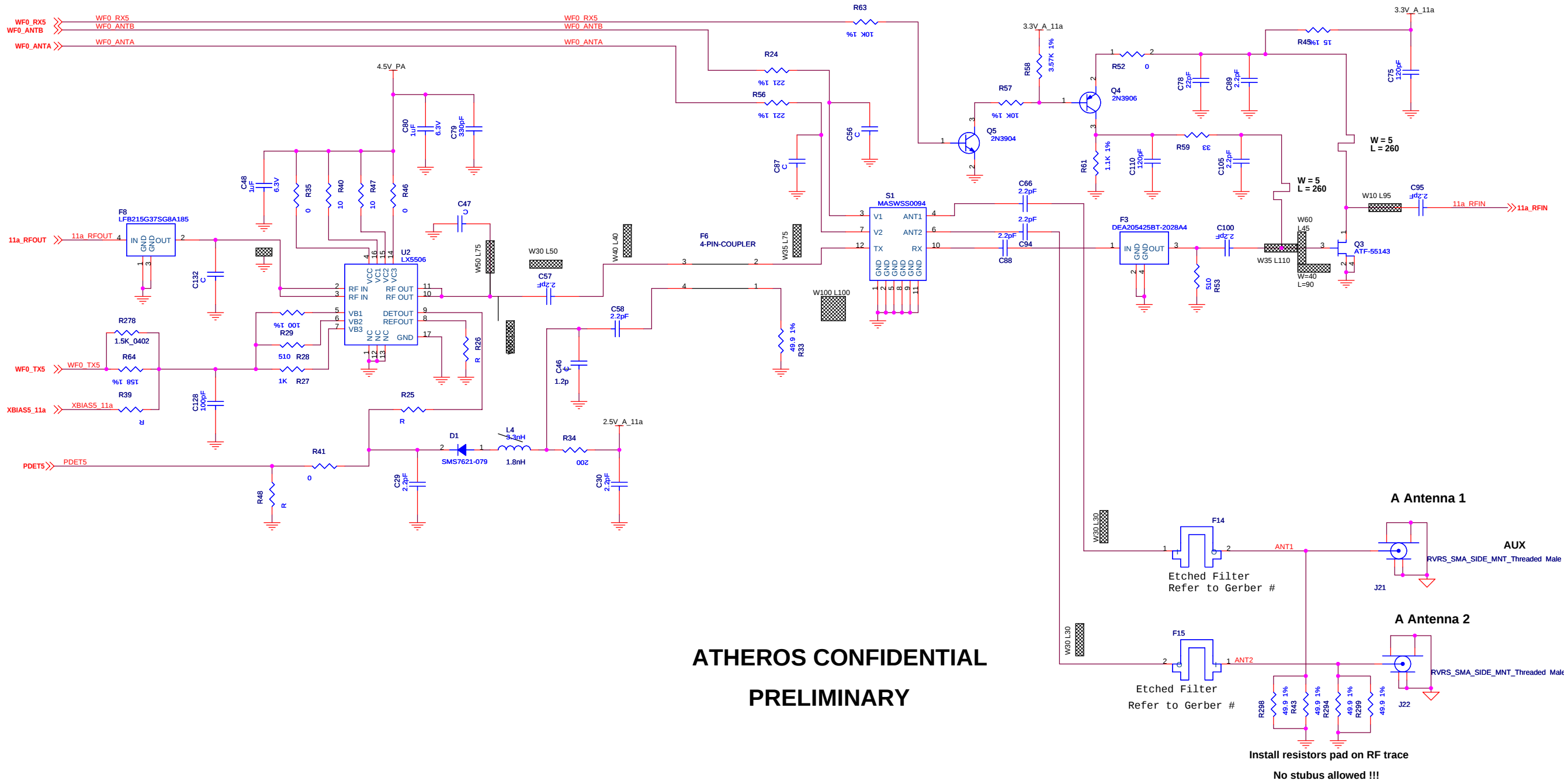




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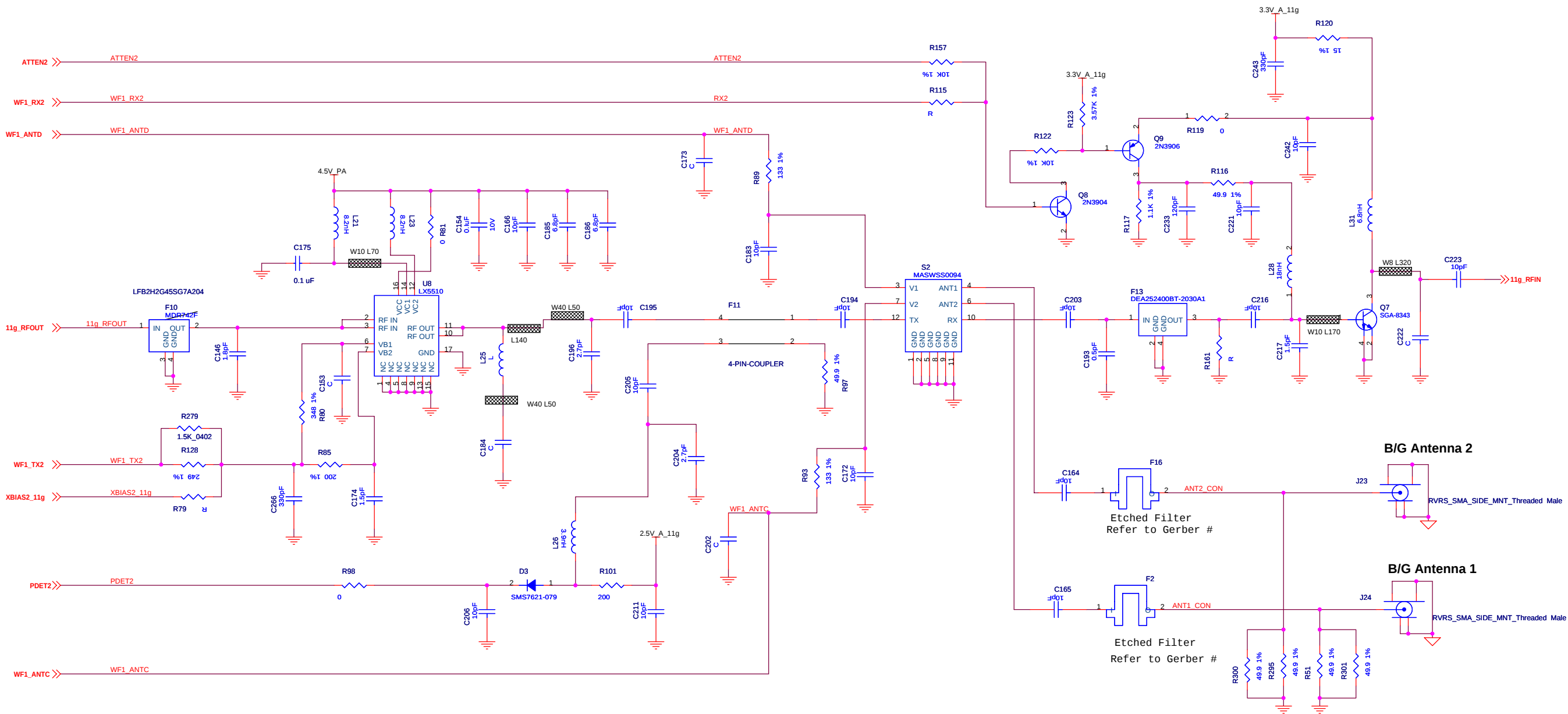
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02.06 11a_RF_Front_End

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Install resistors pad on RF trace

No stubs allowed !!!

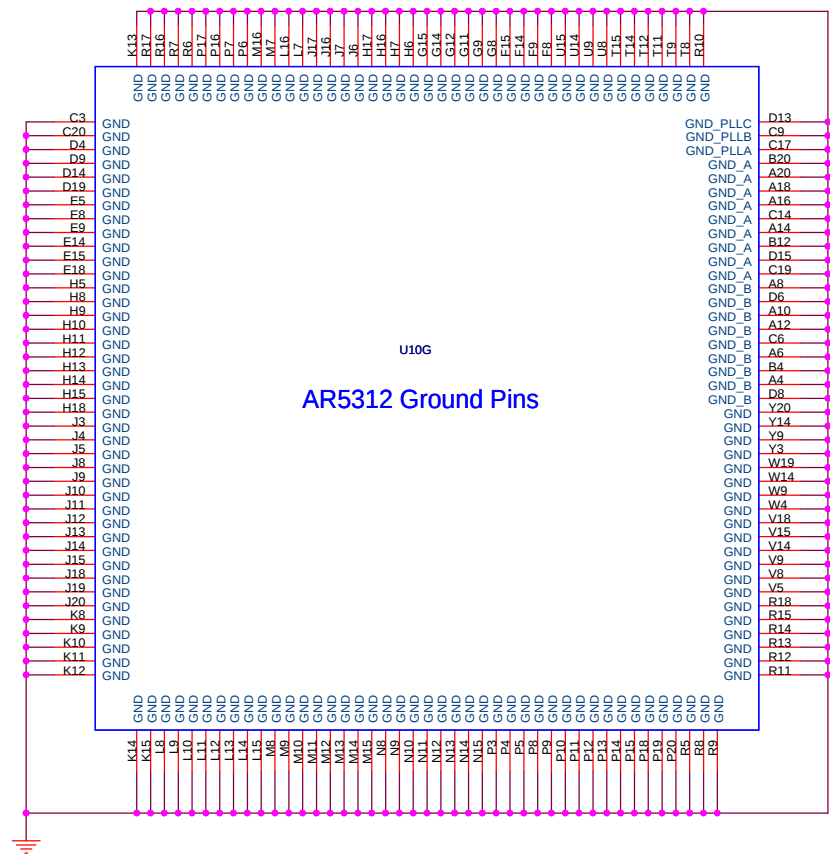
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02.07 11g_RF_Front_End

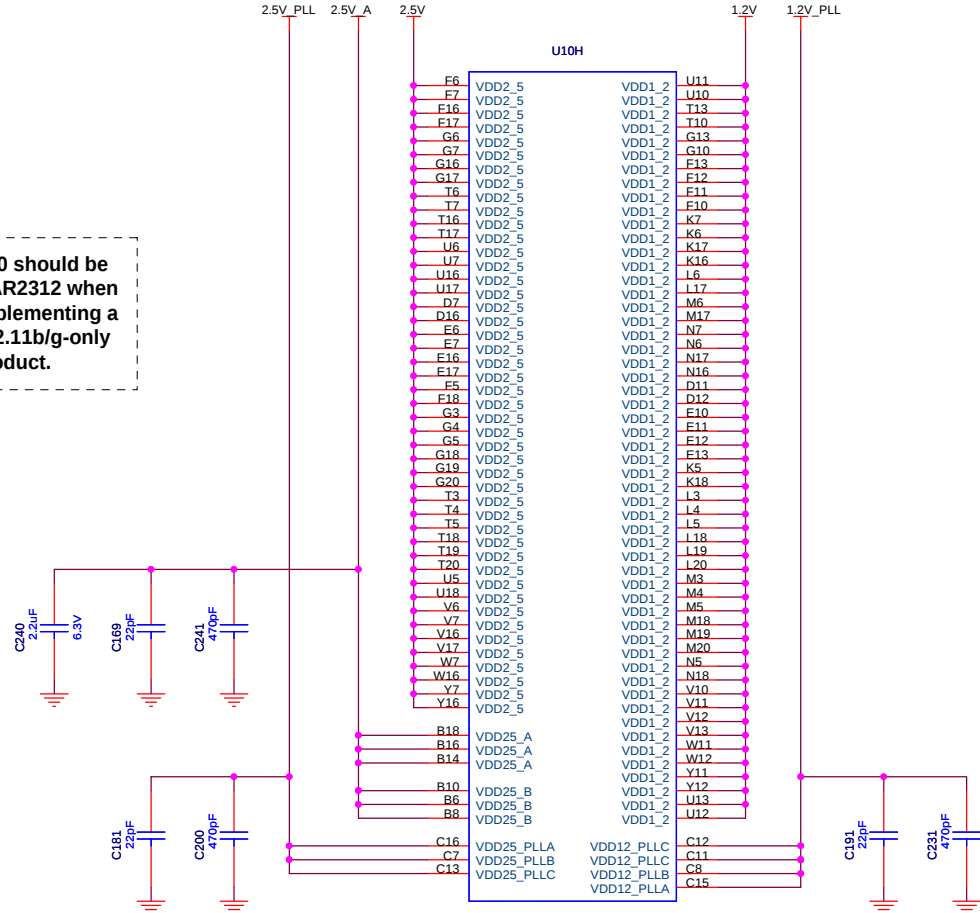
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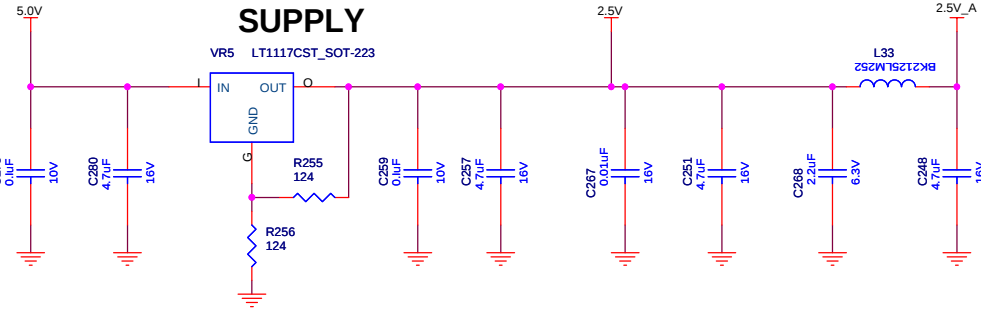


U10 should be a AR2312 when implementing a 802.11b/g-only product.

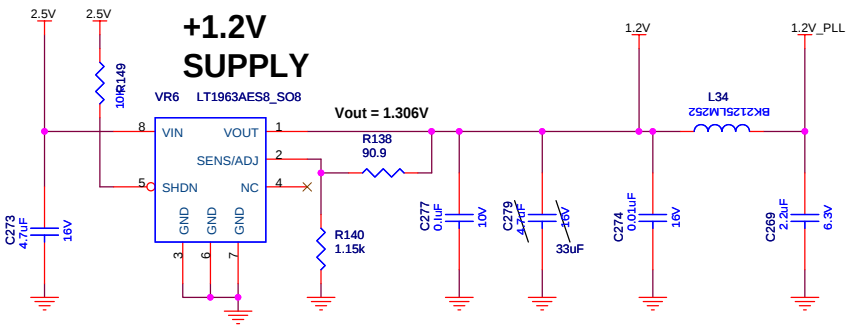


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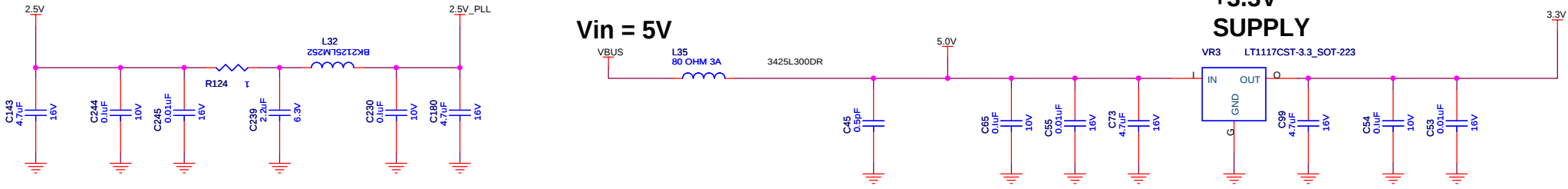
+2.5V
SUPPLY



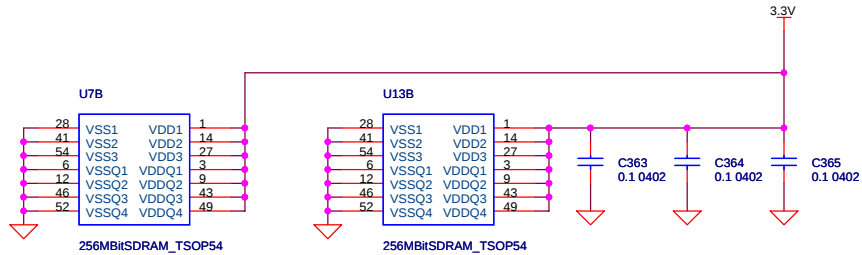
+1.2V
SUPPLY



+3.3V
SUPPLY



Vin = 5V



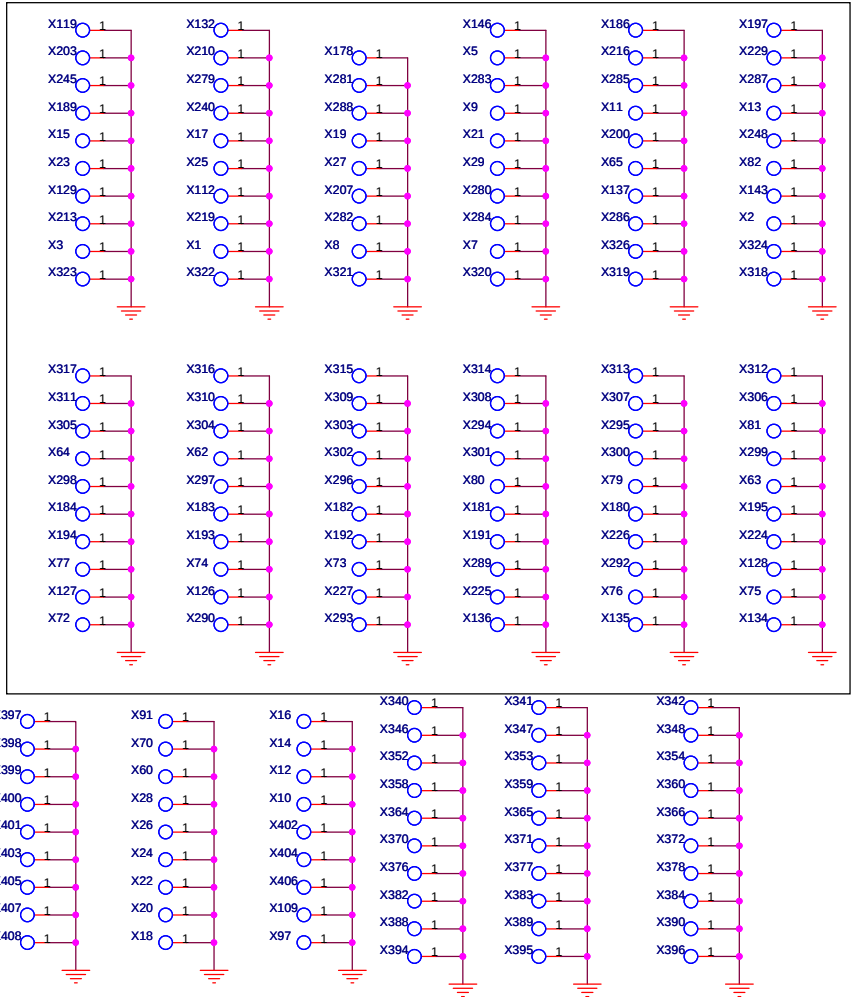
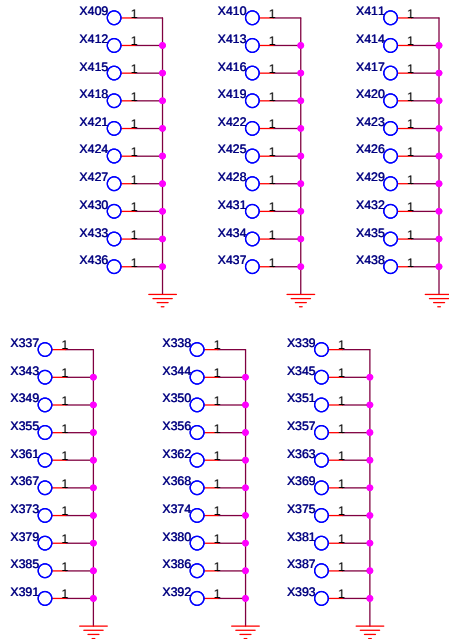
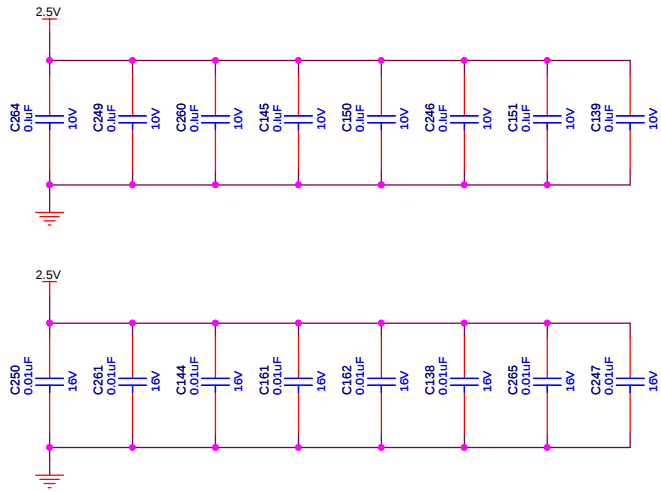
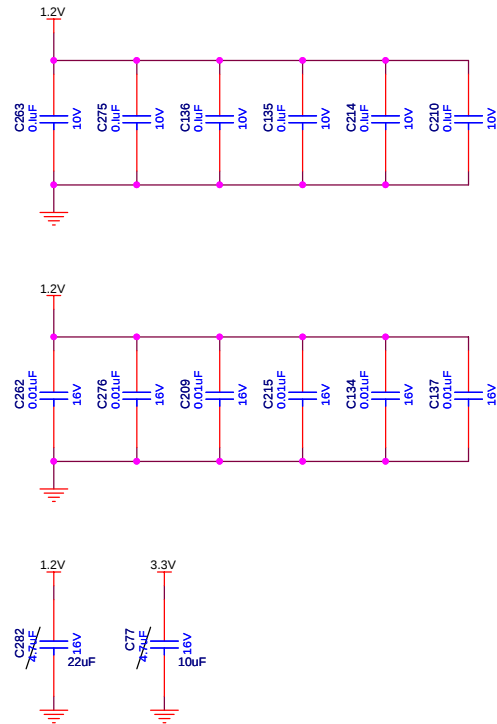
02.08 PowerPins_Vin

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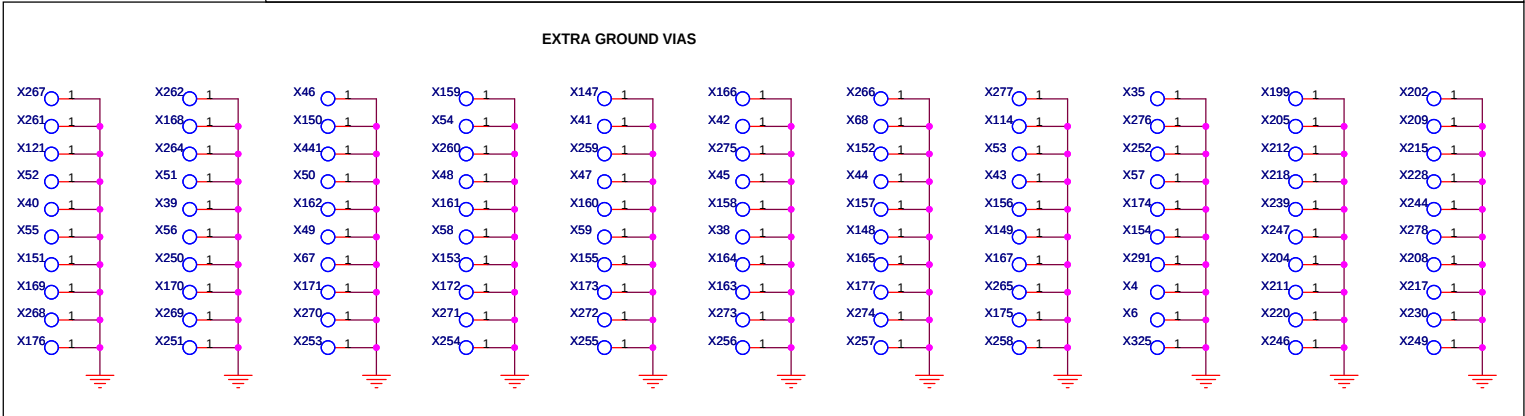
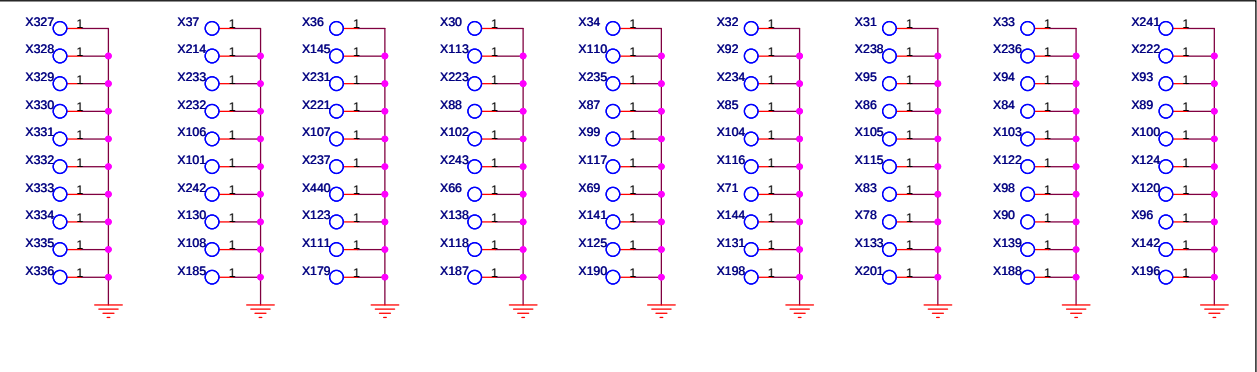
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02.09 Misc

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SCHEMATIC, TYLLUAN A-B-G RADIO MODULE

Size
C

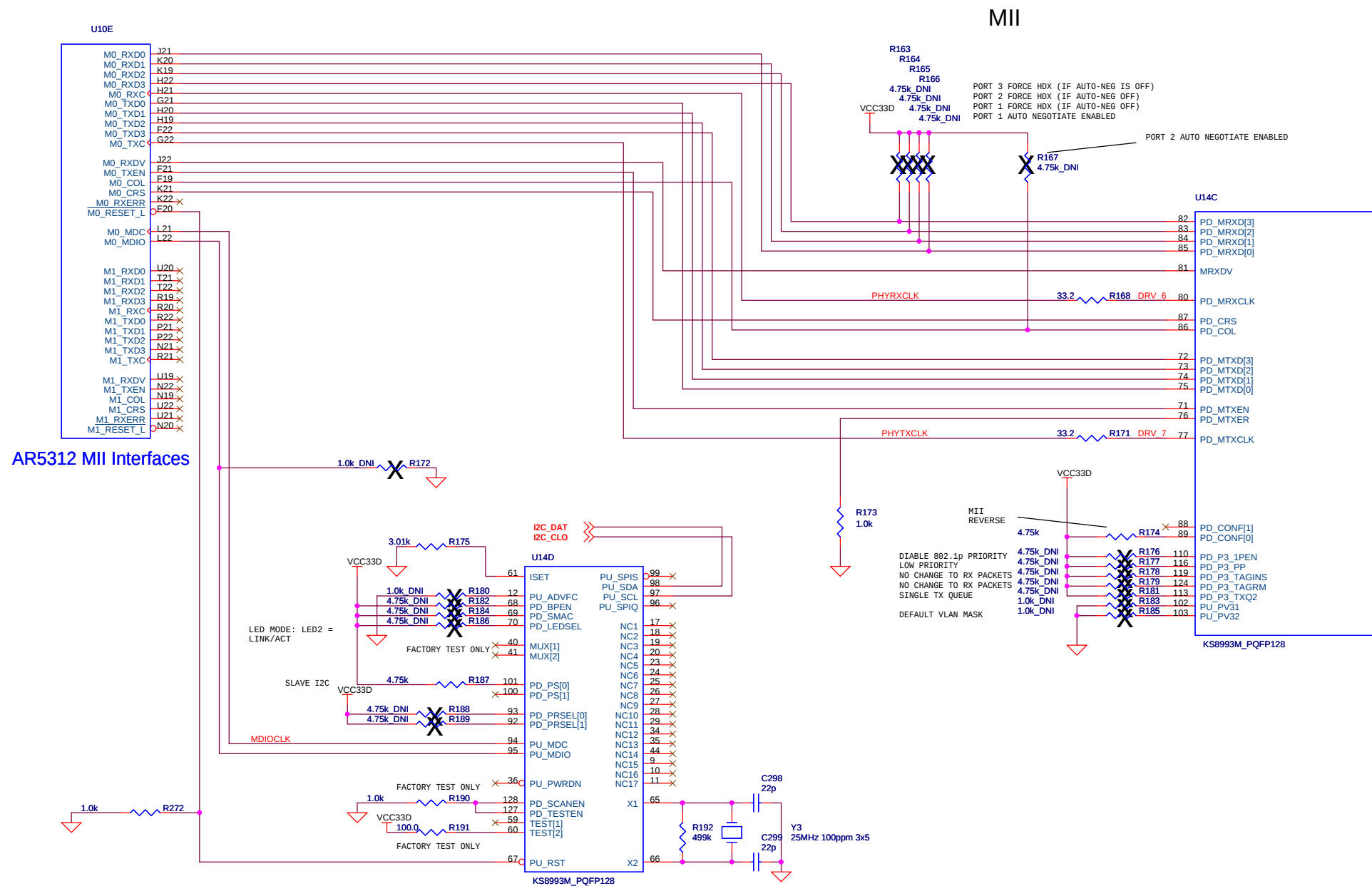
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600-0102-02

Rev
A

Date: _____

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11

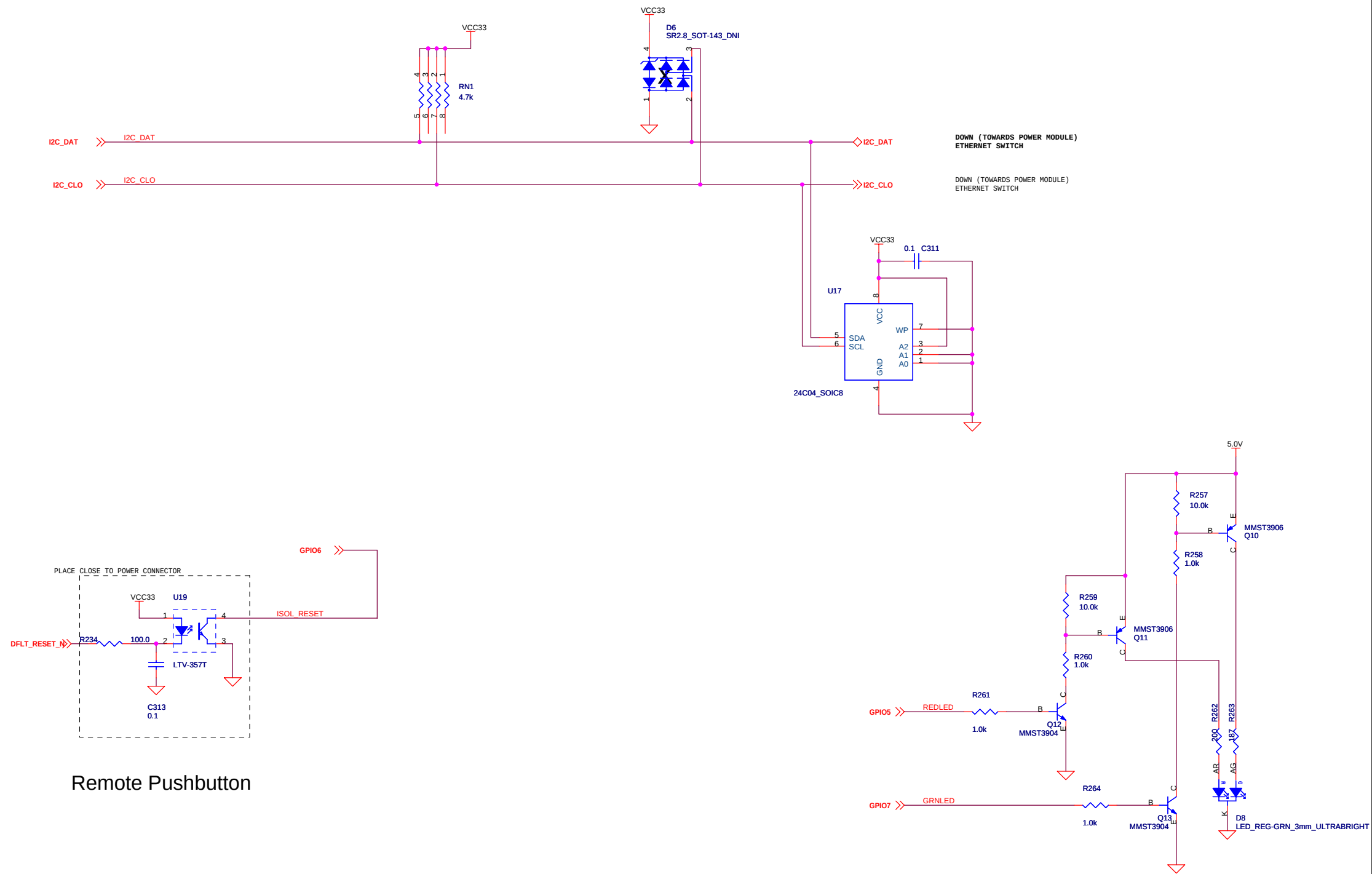
of
17



03.01 Ethernet to processor

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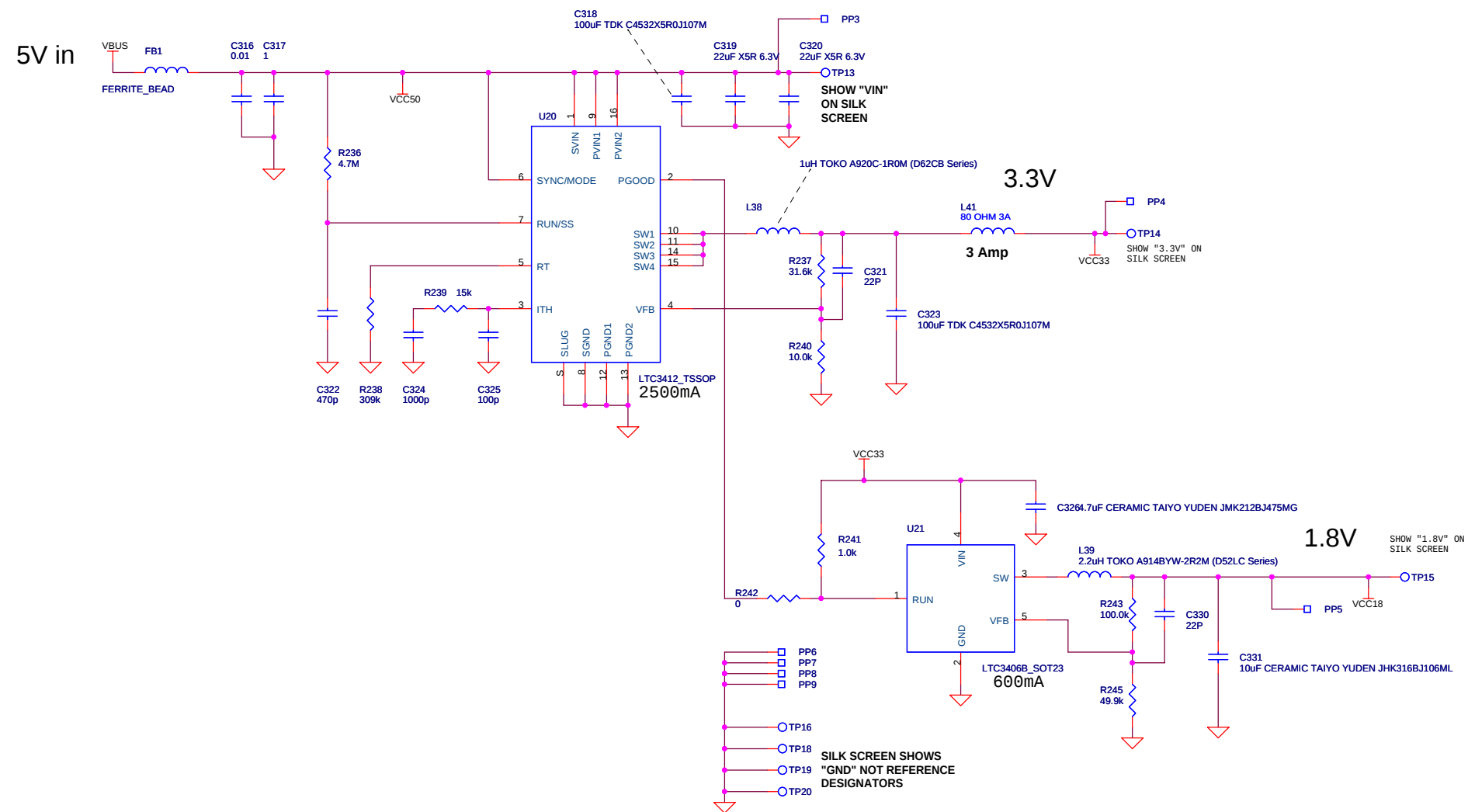
Remote Pushbutton

04.01 Reset circuit, I2C Multiplexer

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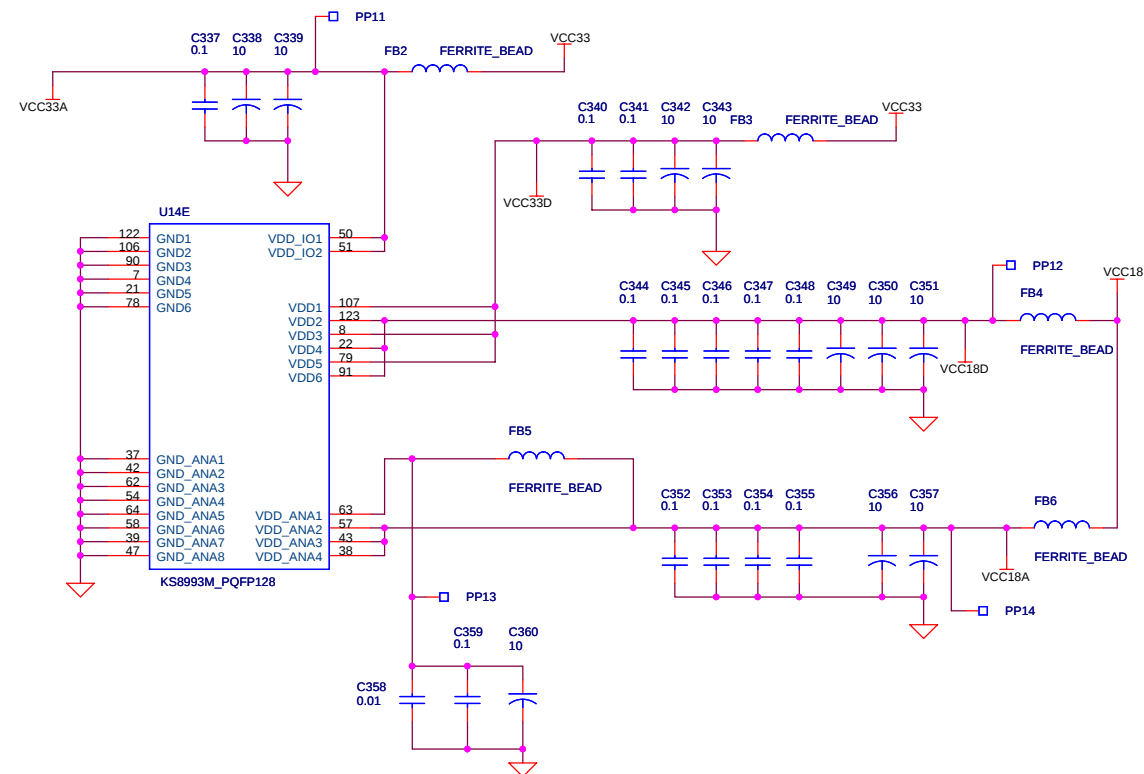


04.03 Power regulators

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Size: C	Document Number: 600-0102-02	Rev: A
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05.01 Ethernet Switch Power

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07.01 RF interconnect

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