Qualcomm Technologies, Inc.

QCA9377-7 Dual-band 1x1 802.11ac + Bluetooth 5.0

Device Specification (Non-NDA/QDN)

80-YK433-1 Rev. A

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Revision history

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1 Introduction

1.1 Documentation overview

This document contains the technical information for QCA9377-3 and is organized as follows:

Chapter 1	Gives a high-level, functional description of the device; lists the device features; and defines marking conventions, terms, and acronyms used throughout this document.
Chapter 2	Defines the device pin assignments.
Chapter 3	Defines the device electrical characteristics, including absolute maximum ratings and recommended operating conditions.
Chapter 4	Provides integrated circuit (IC) mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.
Chapter 5	Describes carrier, storage and handling information.
Chapter 6	Presents procedures and specifications for mounting.
Chapter 7	Presents reliability data, including a definition of the qualification samples and a summary of qualification test results.

1.2 QCA9377 device description

The QCA9377-7 is a single-die wireless local area network (WLAN) and Bluetooth combination solution to support 1 × 1 IEEE 802.11a/b/g/n/ac WLAN standards and Bluetooth 5.0 + HS, enabling seamless integration of WLAN/Bluetooth and low-energy technology.

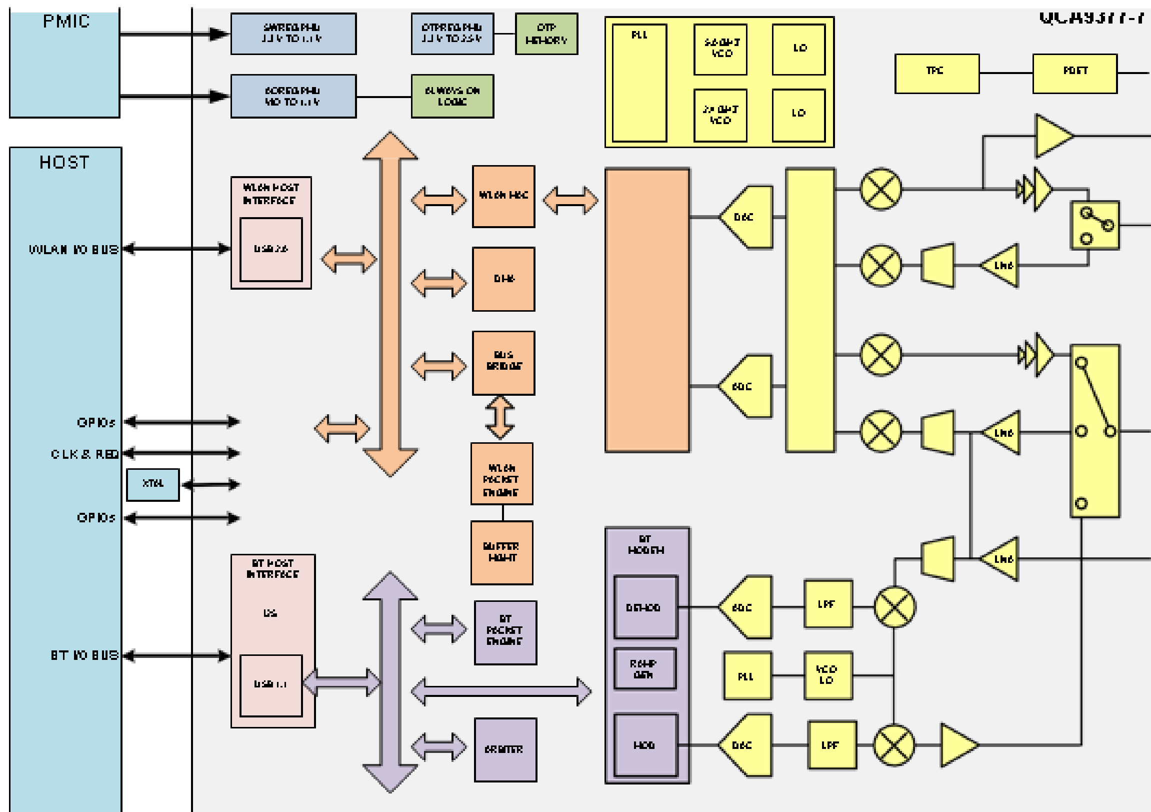

Figure 1-1 QCA9377-7 functional block diagram

1.3 Product features

- QCA9377-7: Supports low-power USB 2.0 interfaces for WLAN and a USB 1.1 interface for Bluetooth
- Provides a highly integrated WLAN system-on-chip (SoC) for 5 GHz 802.11ac, or 2.4 GHz/5 GHz 802.11n WLAN applications
- Supports Bluetooth 5.0, Qualcomm® Bluetooth Low Energy, and ANT+ and backward compatibility with Bluetooth 1.x and Bluetooth 2.x + Enhanced Data Rate
- Supports a single-ended radio frequency (RF) port for cleaner and lower cost design
- Supports 20 MHz/40 MHz at 2.4 GHz and supports 20 MHz, 40 MHz, or 80 MHz at 5 GHz
- Supports multiuser multiple-input multiple-output (MIMO)
- Supports Bluetooth-WLAN coexistence and internal stacked module-LTE (ISM-LTE) coexistence
- Operates on one 3.3 V power supply and an I/O supply of 1.8 V or 3.3 V. Both WLAN and Bluetooth power management use advanced power-saving techniques, such as:
  - Gating clocks to idle or inactive blocks
  - Voltage scaling to specific blocks in certain states
  - Fast start and settling circuits to reduce Tx

- Active duty cycles
- Processor frequency scaling
- Other techniques to optimize power consumption across all operating states
  - Includes additional features, such as:
    - Low-density parity check (LDPC)
    - 1.5 kB of on-chip, one-time programmable (OTP) memory to eliminate the need for an external flash and to further reduce the external component count and bill of materials (BOM) cost
  - Provides a 48 MHz reference clock
  - Supports Bluetooth for class 1 and class 2 power-level transmissions without requiring an external PA
  - Available in a low-profile 4.34 mm × 5.48 mm WLNSP package with 0.4 mm pitch

Uses an internal power amplifier (PA) and an internal low-noise amplifier (LNA) to support the datasheet specifications. Can support an external PA and an external LNA with central logic.

1.4 Terms and acronyms

Table 1-1 Terms and acronyms

Term	Definition
ADC	Analog-to-digital converter
AFR	Average failure rate
BLE	Qualcomm® Bluetooth Low Energy
BOM	Bill of materials
BT	Bluetooth
CDM	Charged device model
CMOS	Complementary metal-oxide semiconductor
CTS	Clear to send
DAC	Digital-to-analog converter
ESD	Electrostatic discharge
GPIO	General-purpose input/output
HBM	Human body movement
IC	Integrated circuit
I2C	Inter-integrated circuit
I/O	Input/output
ISM	Internal stacked module
LDPC	Low-density parity check
LNA	Low-noise amplifier
LO	Local oscillator
LTE	Long-term evolution
MIMO	Multiple-input multiple-output
MRT	Moisture resistance test

Term	Definition
MSL	Moisture-sensitivity level (for PCBs)
MTTF	Mean time to failure
OTP	One-time programmable
PA	Power amplifier
PCIe	Personal computer interface express
PLL	Phase locked loop
PMU	Performance monitoring unit
QTI	Qualcomm Technologies, Inc.
RF	Radio frequency
RH	Relative humidity
RoHS	Restriction of Hazardous Substances
RTS	Request to send
RxD	Receive diversity
SDIO	Secure digital input/output
SMT	Surface mount technology
SoC	System-on-chip
SPI	Serial peripheral interface
TPC	Temperature compensation circuit
Tx	Transmit
TxD	Transmit diversity
UART	Universal asynchronous receiver/transmitter
USB	Universal serial bus
VCO	Voltage-controlled oscillator
Vdd	Handset supply voltage
WLAN	Wireless local area network
WLNSP	Wafer-level nanoscale package

1.5 Special marks

Table 1-2 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, SDC1_DATA[7:4] indicates a range that is 4 bits in length. DATA[7:0] refers to all eight DATA pins.
_L	A suffix of _L indicates an active low signal. For example, RESIN_L.
0x00000	Hexadecimal numbers are identified with an x in the number (for example, 0x0000). All numbers are decimal (base 10), unless otherwise specified. Nonobvious binary numbers have the term binary enclosed in parentheses at the end of the number. For example, 0011 (binary).

2 Pin definitions

The QCA9377 device is available in the 115-pin wafer-level nanoscale package (WLNSP) that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 package details.

Figure 2-1 shows a high-level view of the pin assignments.

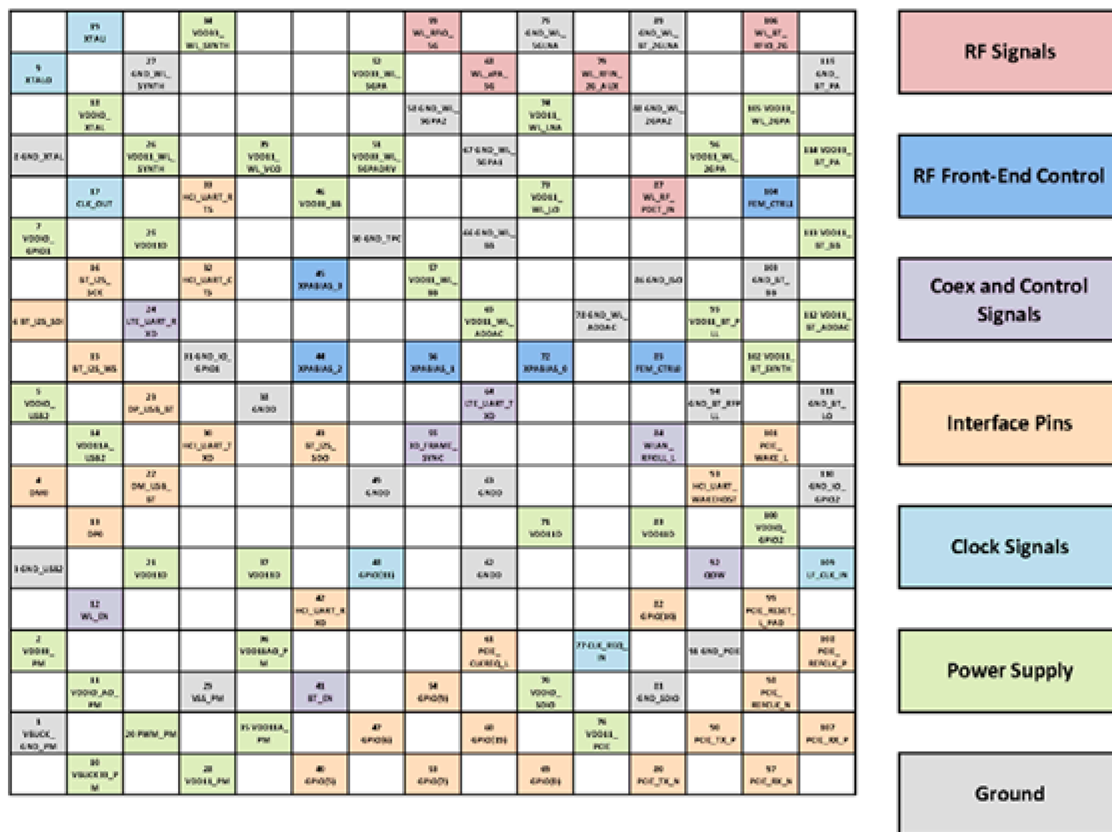

Figure 2-1 QCA9377 pin assignments (top view)

Table 2-1 QCA9377-7 IC pin assignments in numeric order and corresponding location

Ball pad number	Ball pad name QCA9377-7	Ball pad center (x-coordinate) (mm)	Ball pad center (y-coordinate) (mm)	Pad size diameter (mm)
1	VBUCK_GND_PM	1.981	-2.264	0.25
2	VDD33_PM	1.981	-1.698	0.25
3	GND_USB2	1.981	-1.132	0.25

Ball pad number	Ball pad name QCA9377-7	Ball pad center (x-coordinate) (mm)	Ball pad center (y-coordinate) (mm)	Pad size diameter (mm)
4	DM0	1.981	-0.566	0.25
5	VDDIO_USB2	1.981	0	0.25
6	GPIO(25)	1.981	0.566	0.25
7	VDDIO_GPIO1	1.981	1.132	0.25
8	GND_XTAL	1.981	1.698	0.25
9	XTALO	1.981	2.264	0.25
10	VBUCK33_PM	1.698	-2.547	0.25
11	VDDIO_AO_PM	1.698	-1.981	0.25
12	WL_EN	1.698	-1.415	0.25
13	DP0	1.698	-0.849	0.25
14	VDD11A_USB2	1.698	-0.283	0.25
15	GPIO(27)	1.698	0.283	0.25
16	GPIO(28)	1.698	0.849	0.25
17	CLK_OUT	1.698	1.415	0.25
18	VDDIO_XTAL	1.698	1.981	0.25
19	XTALI	1.698	2.547	0.25
20	PWM_PM	1.415	-2.264	0.25
21	VDD11D	1.415	-1.132	0.25
22	DM_USB_BT	1.415	-0.566	0.25
23	DP_USB_BT	1.415	0	0.25
24	LTE_UART_RXD	1.415	0.566	0.25
25	VDD11D	1.415	1.132	0.25
26	VDD11_WL_SYNTH	1.415	1.698	0.25
27	GND_WL_SYNTH	1.415	2.264	0.25
28	VDD11_PM	1.132	-2.547	0.25
29	VSS_PM	1.132	-1.981	0.25
30	GPIO(29)	1.132	-0.283	0.25
31	GND_IO_GPIO1	1.132	0.283	0.25
32	GPIO(31)	1.132	0.849	0.25
33	GPIO(32)	1.132	1.415	0.25
34	VDD33_WL_SYNTH	1.132	2.547	0.25
35	VDD11A_PM	0.849	-2.264	0.25
36	VDD11AO_PM	0.849	-1.698	0.25
37	VDD11D	0.849	-1.132	0.25
38	GNDD	0.849	0	0.25
39	VDD11_WL_VCO	0.849	1.698	0.25
40	GPIO(5)	0.566	-2.547	0.25
41	BT_EN	0.566	-1.981	0.25
42	GPIO(30)	0.566	-1.415	0.25
43	GPIO(26)	0.566	-0.283	0.25

Ball pad number	Ball pad name QCA9377-7	Ball pad center (x-coordinate) (mm)	Ball pad center (y-coordinate) (mm)	Pad size diameter (mm)
44	XPABIAS_2	0.566	0.283	0.25
45	XPABIAS_3	0.566	0.849	0.25
46	VDD33_BB	0.566	1.415	0.25
47	GPIO(6)	0.283	-2.264	0.25
48	GPIO(11)	0.283	-1.132	0.25
49	GNDD	0.283	-0.566	0.25
50	GND_TPC	0.283	1.132	0.25
51	VDD33_WL_5GPADRV	0.283	1.698	0.25
52	VDD33_WL_5GPA	0.283	2.264	0.25
53	GPIO(7)	0	-2.547	0.25
54	GPIO(9)	0	-1.981	0.25
55	3D_FRAME_SYNC	0	-0.283	0.25
56	XPABIAS_1	0	0.283	0.25
57	VDD11_WL_BB	0	0.849	0.25
58	GND_WL_5GPA2	0	1.981	0.25
59	WL_RFIO_5G	0	2.547	0.25
60	GPIO(8)	-0.283	-2.264	0.25
61	GPIO(19)	-0.283	-1.698	0.25
62	GNDD	-0.283	-1.132	0.25
63	GNDD	-0.283	-0.566	0.25
64	LTE_UART_TXD	-0.283	0	0.25
65	VDD11_WL_ADDAC	-0.283	0.566	0.25
66	GND_WL_BB	-0.283	1.132	0.25
67	GND_WL_5GPA1	-0.283	1.698	0.25
68	WL_xPA_5G	-0.283	2.264	0.25
69	GPIO(0)	-0.566	-2.547	0.25
70	VDDIO_SDIO	-0.566	-1.981	0.25
71	VDD11D	-0.566	-0.849	0.25
72	XPABIAS_0	-0.566	0.283	0.25
73	VDD11_WL_LO	-0.566	1.415	0.25
74	VDD11_WL_LNA	-0.566	1.981	0.25
75	GND_WL_5GLNA	-0.566	2.547	0.25
76	VDD11_PCIE	-0.849	-2.264	0.25
77	CLK_REQ_IN	-0.849	-1.698	0.25
78	GND_WL_ADDAC	-0.849	0.566	0.25
79	WL_RFIN_2G_AUX	-0.849	2.264	0.25
80	NC	-1.132	-2.547	0.25
81	GND_SDIO	-1.132	-1.981	0.25
82	GPIO(10)	-1.132	-1.415	0.25
83	VDD11D	-1.132	-0.849	0.25

Ball pad number	Ball pad name QCA9377-7	Ball pad center (x-coordinate) (mm)	Ball pad center (y-coordinate) (mm)	Pad size diameter (mm)
84	WLAN_RFKILL_L	-1.132	-0.283	0.25
85	FEM_CTRL0	-1.132	0.283	0.25
86	GND_ISO	-1.132	0.849	0.25
87	WL_RF_PDET_IN	-1.132	1.415	0.25
88	GND_WL_2GPA2	-1.132	1.981	0.25
89	GND_WL_BT_2GLNA	-1.132	2.547	0.25
90	NC	-1.415	-2.264	0.25
91	GND_PCIE	-1.415	-1.698	0.25
92	GPIO(35)	-1.415	-1.132	0.25
93	GPIO(24)	-1.415	-0.566	0.25
94	GND_BT_RFPLL	-1.415	0	0.25
95	VDD11_BT_PLL	-1.415	0.566	0.25
96	VDD11_WL_2GPA	-1.415	1.698	0.25
97	NC	-1.698	-2.547	0.25
98	NC	-1.698	-1.981	0.25
99	PCIE_RESET_L_PAD	-1.698	-1.415	0.25
100	VDDIO_GPIO2	-1.698	-0.849	0.25
101	GPIO(18)	-1.698	-0.283	0.25
102	VDD11_BT_SYNTH	-1.698	0.283	0.25
103	GND_BT_BB	-1.698	0.849	0.25
104	FEM_CTRL1	-1.698	1.415	0.25
105	VDD33_WL_2GPA	-1.698	1.981	0.25
106	WL_BT_RFIO_2G	-1.698	2.547	0.25
107	NC	-1.981	-2.264	0.25
108	NC	-1.981	-1.698	0.25
109	LF_CLK_IN	-1.981	-1.132	0.25
110	GND_IO_GPIO2	-1.981	-0.566	0.25
111	GND_BT_LO	-1.981	0	0.25
112	VDD11_BT_ADDAC	-1.981	0.566	0.25
113	VDD11_BT_BB	-1.981	1.132	0.25
114	VDD33_BT_PA	-1.981	1.698	0.25
115	GND_BT_PA	-1.981	2.264	0.25

2.1 I/O parameter definitions

This section contains a package pinout and a listing of the signal descriptions.

Table 2-2 Signal name/type abbreviations

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with complementary metal-oxide semiconductor (CMOS) input
DI	Digital input (CMOS)
DO	Digital output signal
OD	A digital output signal with open drain
GND	Ground
NC	No connection should be made to this pin
P	Voltage supply
Pad pull details for digital I/Os	
PU	Input signals with weak internal pull-up, to prevent signals from floating when left open
PD	Input signals with weak internal pull-down, to prevent signals from floating when left open

Table 2-3 Pin descriptions (QCA9377-7)

Pin	QCA9377-7	VDDIO or pad voltage	I/O	Description
BT USB 1.1 interface				
22	DM_USB_BT	VDDIO_USB2	AI,AO	QCA9377-5/-7: Bluetooth USB 1.1 differential pair
23	DP_USB_BT	VDDIO_USB2	AI,AO	
GPIO and NC				
32	GPIO[31]	VDDIO_GPIO1	DI	QCA9377-3: UART clear to send (CTS) signal
33	GPIO[32]	VDDIO_GPIO1	DO	QCA9377-3: UART request to send (RTS) signal
42	GPIO[30]	VDDIO_GPIO1	DI	QCA9377-3: UART receive diversity (RxD) signal
30	GPIO[29]	VDDIO_GPIO1	DO	QCA9377-3: UART transmit diversity (TXD) signal
93	GPIO[24]	VDDIO_GPIO2	OD	Bluetooth wakeup host. Active high
6	GPIO[25]	VDDIO_GPIO1	OD	Bluetooth PCM_IN signal
15	GPIO[27]	VDDIO_GPIO1	B	Bluetooth PCM_SYNC signal
16	GPIO[28]	VDDIO_GPIO1	PD	Bluetooth PCM_CLK signal
43	GPIO[26]	VDDIO_GPIO1	DO	Bluetooth PCM_OUT signal
Clock signals				
109	LF_CLK_IN	VDDIO_GPIO2	PD	External low-power 32.768 kHz clock input
48	GPIO[11]	VDDIO_GPIO1	DO	Clock request output

Pin	QCA9377-7	VDDIO or pad voltage	I/O	Description
77	CLK_REQ_IN	VDDIO_AO	PD	Clock request input: If chip is powered up, and CLK_REQ_IN is asserted (high), the chip can supply the crystal clock to the external chip. If only CLK_REQ_IN is asserted, and WLAN_EN or BT_EN is not enabled, the chip remains in a HOST_OFF state, to expect low power
18	VDDIO_XTAL	1.8 V or 3.3 V	P	Voltage supply for crystal
9	XTALO	1.1 V	–	External crystal output
19	XTALI	1.1 V	–	External crystal input
8	GND_XTAL	–	GND	Ground to VDDIO_XTAL
GPIO and NC				
54	GPIO[9]	VDDIO_SDIO	OD	GPIO[9] This pin can be configured to serial peripheral interface/inter-integrated circuit (SPI/I2C) bus interface: ▪ SPI_SI/I2C_SDA, open drain ▪ QCA9377-3: SDIO clock signal
69	GPIO[0]	VDDIO_SDIO	DI	GPIO[0] QCA9377-3: SDIO CMD line signal
60	GPIO[8]	VDDIO_SDIO	B	GPIO[8] QCA9377-3: SDIO data bus D0
53	GPIO[7]	VDDIO_SDIO	B	GPIO[7] QCA9377-3: SDIO data bus D1
47	GPIO[6]	VDDIO_SDIO	B	GPIO[6] This pin is a bootstrap signal. It must keep high for normal operation during power-on reset. QCA9377-3: SDIO data bus D2
40	GPIO[5]	VDDIO_SDIO	B	GPIO[5] QCA9377-3: SDIO data bus D3
82	GPIO[10]	VDDIO_SDIO	DO	GPIO[10] This pin can be configured for I2C bus interface. I2C_SO QCA9377-3: SDIO interrupt signal
70	VDDIO_SDIO	1.8 V or 3.3 V	P	Voltage supply for SDIO
81	GND_SDIO	–	GND	Ground for VDDIO_SDIO
99	PCIE_RESET_L_PAD	VDDIO_GPIO2	PD	QCA9377-5: PCIe reset with weak pull-down
101	GPIO[18]	VDDIO_GPIO2	OD	QCA9377-5: Request to service a function-initiated wake event. An external pull-up resistor to VDDIO_GPIO2 is required
61	GPIO[19]	VDDIO_AO	OD	QCA9377-5: Reference to clock request. An external pull-up resistor to VDDIO_AO is required
98	NC	1.1 V	AI	QCA9377-5: Differential reference clock (100 MHz)
108	NC	1.1 V	AI	

Pin	QCA9377-7	VDDIO or pad voltage	I/O	Description
97	NC	1.1 V	AI	QCA9377-5: Differential receive
107	NC	1.1 V	AI	
80	NC	1.1 V	AO	QCA9377-5: Differential transmit
90	NC	1.1 V	AO	
76	GND	1.1 V	P	Voltage supply for PCIe
91	GND_PCIE	–	GND	QCA9377-5: Ground for VDD11_PCIE
WLAN USB 2.0 interface				
4	DM0	VDDIO_USB2	AI,AO	QCA9377-7: WLAN USB 2.0 Differential pair
13	DP0	VDDIO_USB2	AI,AO	
Coexistence and control signals				
84	WLAN_RFKILL_L	VDDIO_GPIO2	PU	Turn off WLAN RF analog and front end. Active low
92	GPIO(35)	VDDIO_GPIO2	OD	This signal can be used to enable external wireless charging of a universal asynchronous receiver/transmitter (UART) circuit
24	LTE_UART_RXD	VDDIO_GPIO1	PU	LTE coexistence signal. LTE_UART_RXD or LTE_FS
55	3D_FRAME_SYNC	VDDIO_GPIO1	PD	Frame sync signal from TV to sync with 3D glass through Bluetooth
64	LTE_UART_TXD	VDDIO_GPIO1	DO	LTE coexistence signal. LTE_UART_TXD or LTE_PRI
12	WL_EN	VDDIO_AO	PD	WLAN enable. Active high
41	BT_EN	VDDIO_AO	PD	Bluetooth enable. Active high
RF chain				
59	WL_RFIO_5G	RF	AI,AO	WLAN 5 GHz RF I/O port. **Note**: If an external PA is used, this pin can be configured for RF input only.
68	WL_xPA_5G	RF	AO	5 GHz PA output, if external PA is used
79	WL_RFIN_2G_AUX	RF	AI	WLAN 2.4 GHz Rx port for 2G-only option
87	WL_RF_PDET_IN	RF	AI	WLAN Tx power detector input (2.4 GHz and 5 GHz)
106	WL_BT_RFIO_2G	RF	AI,AO	WLAN 2.4 GHz and Bluetooth RF I/O port
RF front-end control				
85	FEM_CTRL0	3.3 V	DO	Programmable by switch table, normally, if external LNA is used
104	FEM_CTRL1	3.3 V	DO	Programmable by switch table, normally, if external LNA is used
72	XPABIAS_0	3.3 V	AO	XPABIAS_0: PA enable for optional external PA
56	XPABIAS_1	3.3 V	AO	XPABIAS_1: PA enable for optional external PA

Pin	QCA9377-7	VDDIO or pad voltage	I/O	Description
44	XPABIAS_2	3.3 V	AO	XPABIAS_2: PA enable for optional 2 external PA
45	XPABIAS_3	3.3 V	AO	XPABIAS_3: PA enable for optional external PA
SWREG: 3.3 V to 1.1 V				
28	VDD11_PM	1.1 V	P	1.1 V voltage feedback to SWREG PMU
35	VDD11A_PM	1.1 V	P	Analog 1.1 V power supply output. This pin is connected from the SWREG_FB and gated from internal sleep control logic. The analog 1.1 V can be turned off during the sleep mode for lowest power consumption
10	VBUCK33_PM	3.3 V	P	SWREG voltage input
1	VBUCK_GND_PM	–	GND	Ground for internal 1.1 V regulator
29	VSS_PM	–	GND	Ground for internal 1.1 V regulator
20	PWM_PM	–	–	SWREG performance monitoring unit (PMU) output
PMU: VDDIO PMU				
11	VDDIO_AO_PM	1.8 V or 3.3 V	P	Always-on I/O supply for power management and real-time clock. This supply must be present if any other supply is present
36	VDD11AO_PM	1.1 V	P	1.1 V power output from AOREG PMU to supply internal always-on logics. Individual power supply
PMU: OTPREG25				
2	VDD33_PM	3.3 V	P	3.3 V input voltage for 2.5 V OTP regulator
Individual power supply				
46	VDD33_BB	3.3 V	P	3.3 V supply for internal analog baseband
114	VDD33_BT_PA	3.3 V	P	3.3 V supply for Bluetooth PA
105	VDD33_WL_2GPA	3.3 V	P	3.3 V supply for internal 2 GHz PA
52	VDD33_WL_5GPA	3.3 V	P	3.3 V supply for internal 5 GHz PA
51	VDD33_WL_5GPADRV	3.3 V	P	3.3 V supply for internal 5 GHz PA drive
34	VDD33_WL_SYNTH	3.3 V	P	3.3 V supply for internal synthesizer
5	VDDIO_USB2	3.3 V	P	3.3 V supply for USB, shared by Bluetooth/WLAN USB
7	VDDIO_GPIO1	1.8 V or 3.3 V	P	Voltage supply
100	VDDIO_GPIO2	1.8 V or 3.3 V	P	Voltage supply
112	VDD11_BT_ADDAC	1.1 V	P	1.1 V supply for Bluetooth ADC and DAC
113	VDD11_BT_BB	1.1 V	P	1.1 V supply for Bluetooth baseband
95	VDD11_BT_PLL	1.1 V	P	1.1 V supply for Bluetooth phase locked loop (PLL)
102	VDD11_BT_SYNTH	1.1 V	P	1.1 V supply for Bluetooth synthesizer
96	VDD11_WL_2GPA	1.1 V	P	1.1 V supply for 2 GHz PA
65	VDD11_WL_ADDAC	1.1 V	P	1.1 V supply for WLAN analog-to-digital converter (ADC) and digital-to-analog (DAC)

Pin	QCA9377-7	VDDIO or pad voltage	I/O	Description
57	VDD11_WL_BB	1.1 V	P	1.1 V supply for WLAN baseband
74	VDD11_WL_LNA	1.1 V	P	1.1 V supply for LNA
73	VDD11_WL_LO	1.1 V	P	1.1 V supply for local oscillator (LO)
26	VDD11_WL_SYNTH	1.1 V	P	1.1 V supply for WLAN synthesizer
39	VDD11_WL_VCO	1.1 V	P	1.1 V supply for WLAN voltage-controlled oscillator (VCO)
14	VDD11A_USB2	1.1 V	P	1.1 V supply for analog USB
21	VDD11D	1.1 V	P	1.1 V supply for digital
25	VDD11D	1.1 V	P	1.1 V supply for digital
37	VDD11D	1.1 V	P	1.1 V supply for digital
71	VDD11D	1.1 V	P	1.1 V supply for digital
83	VDD11D	1.1 V	P	1.1 V supply for digital
103	GND_BT_BB	–	GND	Ground for VDD11_BT_BB
111	GND_BT_LO	–	GND	Ground for VDD11_BT_SYNTH
115	GND_BT_PA	–	GND	Ground for VDD33_BT_PA
94	GND_BT_RFPLL	–	GND	Ground for WLAN PLL
31	GND_IO_GPIO1	–	GND	Ground for VDDIO_GPIO1
110	GND_IO_GPIO2	–	GND	Ground for VDDIO_GPIO2
86	GND_ISO	–	GND	Ground. Requires a GND via on this pin
50	GND_TPC	–	GND	Ground for temperature compensation circuit (TPC)
3	GND_USB2	–	GND	Ground for VDD11A_USB2
88	GND_WL_2GPA2	–	GND	Ground for VDD33_WL_2GPA
75	GND_WL_5GLNA	–	GND	Ground for VDD33_WL_LNA
67	GND_WL_5GPA1	–	GND	Ground for VDD33_WL_5GPA
58	GND_WL_5GPA2	–	GND	Ground for VDD33_WL_5GPA
78	GND_WL_ADDAC	–	GND	Ground for VDD11_WL_ADDAC
66	GND_WL_BB	–	GND	Ground for VDD11_WL_BB
89	GND_WL_BT_2GLNA	–	GND	Ground for VDD11_WL_LNA
27	GND_WL_SYNTH	–	GND	Ground for VDD11_WL_SYNTH
38	GNDD	–	GND	Ground for 1.1 V digital logic
49	GNDD	–	GND	Ground for 1.1 V digital logic
62	GNDD	–	GND	Ground for 1.1 V digital logic
63	GNDD	–	GND	Ground for 1.1 V digital logic

3 Electrical characteristics

3.1 Absolute maximum ratings

Table 3-1 summarizes the absolute maximum ratings, and Table 3-2 lists the recommended operating conditions for the QCA9377. Absolute maximum ratings are those values beyond which damage to the device can occur.

Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

NOTE: The maximum rating for signals follows the supply domain of the signals.

Table 3-1 Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VBUCK33_PM	SWREG supply input	-0.3	3.65	V
VDD11_PM	1.1 V voltage	-0.3	1.32	V
VDDIO_	Voltage supply	-0.3	4.0	V
VDD33_	3.3 V supply	-0.3	4.0	V
VDD11_	1.1 V supply	-0.3	1.32	V
VDD11D	1.1 V supply for digital	-0.3	1.32	V
RF_{IN}	Maximum RF input (reference to 50 Ω input)	–	+10	dBm
T_{STORE}	Storage temperature	-45	-45 to 135	˚C
ESD	Electrostatic discharge tolerance	2000	–	V
3.3 V I/O VIH MAX	Maximum digital I/O input voltage for 3.3 V I/O supply	–	VDD + 0.3	V
1.8 V I/O VIH MAX	Maximum digital I/O input voltage for 1.8 V I/O supply	–	VDD + 0.2	V
VIH MIN	Minimum digital I/O input voltage for 1.8 V or 3.3 V I/O supply	-0.3	–	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD33_	3.3 V supply	3.135	3.3	3.465	V
VBUCK33_PM	1.1 V switcher supply from internal 1.1 V PMU	3.135	3.3	3.465	V
VDD11_PM	1.1 V voltage from internal 1.1 V PMU	1.045	1.1	1.155	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDIO_	Voltage supply	1.71	1.8 or 3.3	3.46	V
VDD11_	1.1 V supply from internal 1.1 V PMU	1.045	1.1	1.155	V
VDD11D	1.1 V supply for digital from internal 1.1 V PMU	1.045	1.1	1.155	V
T_{OP}	For QCA9377-7 device variant	-40	–	85	°C
T_{CASE}	Case temperature	0	–	115	˚C
P_{siJT}	Junction to the top center of the package thermal resistance	–	–	0.5	˚C/W

3.3 Power sequencing

The QCA9377 device requires the following powerup sequence:

1. VDDIO_AO_PM and VDDIO_XTAL are tied to first I/O rail available.
2. VDDIO_SDIO/GPIO1/GPIO2 (1.8 V or 3.3 V).
3. All 3.3.
4. V rails.

To power down the device, the following sequence is required:

1. All 3.3 V rails.
2. VDDIO_SDIO/GPIO1/GPIO2 (1.8 V or 3.3 V).
3. VDDIO_AO_.
4. PM and VDDIO_XTAL.

NOTE: The following can be tied together:

- VDDIO_SDIO, VDDIO_GPIO1, and VDDIO_GPIO2
- VDDIO_AO_PM
- VDDIO_XTAL, and VDDIO_SDIO, VDDIO_GPIO1, and VDDIO_GPIO2

NOTE: For a timing diagram, see *QCA9377 Design Guidelines/Training Slides*.

3.4 Digital logic characteristics

Table 3-3 General DC electrical characteristics (for VDDIO=3.3 V I/O operation)

Symbol	Parameter	Comments	Min.	Typ.	Max.	Unit
VIH	High-level input voltage	–	0.7x VDDIO	–	VDDIO + 0.3	V
VIL	Low-level input voltage	–	-0.3	–	0.3 x VDDIO	V
VSHYS	Schmitt hysteresis	–	–	1.8 V IO: 375 3.3 V IO: 645	–	mV

Symbol	Parameter	Comments	Min.	Typ.	Max.	Unit
IIL	Input low leakage current	VIN = 0 V Supply = VIO max	-5.0	–	5.0	µA
RPULL	Input pull resistor	Up or down	–	1.8 V IO: 120 3.3 V IO: 70	–	kΩ
VOH	High-level output voltage	–	0.9 x VDDIO	–	VDDIO	V
VOL	Low-level output voltage	–	0	–	0.1 x VDDIO	V
IOH	High-level output current	–	3	–	–	mA
IOL	Low-level output current	–	–	–	-11	mA
CIN	Input capacitance	–	–	–	3	pF

4 Mechanical information

4.1 Device physical dimensions

The QCA9377 device is available in the 4.34 mm × 5.48 mm × 0.57 mm, 115-pin package that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package and by the ball pattern when viewed from below.

Figure 4-1 shows the QCA9377 device mechanical dimensions, top and bottom views.

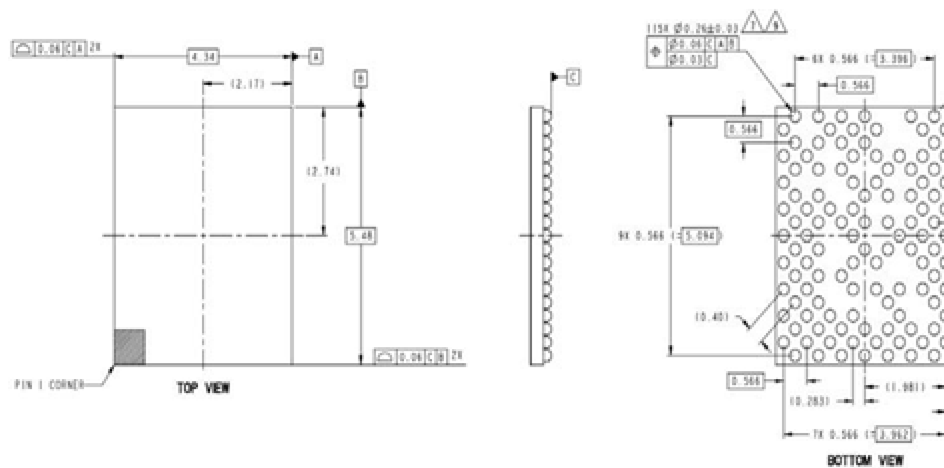

Figure 4-1 QCA9377 mechanical dimensions, top and bottom views

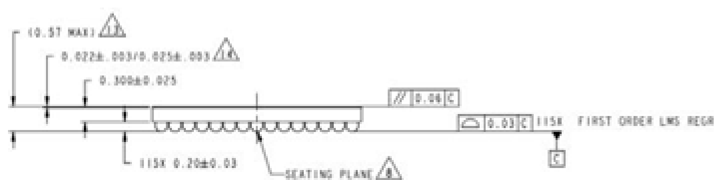

Figure 4-2 QCA9377 package mechanical dimensions height and seating plane

4.2 WLNSP part marking

This device can be ordered using the identification code shown in Section 4.3.

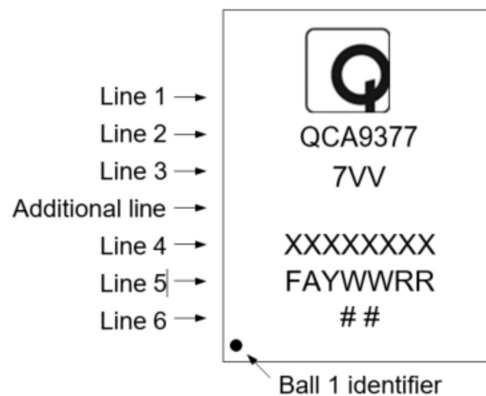

Figure 4-3 Package marking layout (QCA9377-7)

Table 4-1 Package marking identifiers

Line	Marking	Description
1	Q	Qualcomm name or logo
2	QCA9377	Qualcomm Technologies, Inc., product name
3	7VV	Configuration code + feature code
Additional line	–	Blank
4	XXXXXXXX	XXXXXXXX = Wafer lot number
5	FAYWWRR	F = Source of supply code for wafer fab locations F = N: Fabrication = UMC A = Source of supply code for assembly site code A = Y: Fabrication = Amkor, Taiwan A = K: Fabrication = SPIL, Taiwan Y = single/last-digit of year WW = Two-digit work week of current year RR = product revision
6	##	Two-digit wafer number

4.3 Device ordering information

Device ID code ►	AAA-AAAA	— P	— CCC	DDDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product revision	Source code	Feature code
Example ►	QCA9377	— 7	— 115	WLNSP	— TR or MT	— 03	— 0	—

'CCC' is not a fixed length; it depends on the # of pins in the package.

Package type varies in the # of characters.

Feature code (BB) may not be included when identifying older devices.

Figure 4-4 Device identification code

Table 4-2 Device types and configuration codes

Device type	Sample type	Product configuration code (P)	Product revision (RR)	Hardware version	Comments
QCA9377-7	ES1	7	00	v1.0.0	Wi-Fi, USB, Bluetooth, USB
	ES2		02	v1.0.2	
	CS		03	v1.1	

Table 4-3 lists the device identification codes by hardware version and chip variant.

Table 4-3 Device ordering code by chip variant

Chip variant	Hardware version	Device identification code
QCA9377-7	V1.1	QCA-9377-7-115WLNSP-TR-03-0
		QCA-9377-7-115WLNSP-SR-03-0
		QCA-9377-7-115WLNSP-HR-03-0

The P and RR values are more completely defined in Section 4.2.

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. The moisture-sensitivity level (MSL) of a package indicates its ability to withstand exposure after the package is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating. A low MSL device can be exposed on the factory floor longer than a high MSL device.

Table 4-4 MSL rating summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% relative humidity (RH); QCA9377 rating
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

Qualcomm Technologies, Inc. (QTI) follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The QCA9377 devices are classified as MSL1. The qualification temperature is 250ºC***. This qualification temperature (250°C) should not be confused with the peak temperature within the recommended solder reflow profile.

During device qualification, QTI follows the latest revision IPC/JEDEC J-STD-020 standard to determine the MSL of the IC.

Devices that qualify as MSL1 are deemed not moisture sensitive.

All other devices MSL2 through MSL6 are deemed to be moisture sensitive.

Moisture sensitive devices are dry-baked and dry-packed in accordance with IPC/JEDEC JSTD-033.

To ensure proper surface mount technology (SMT) assembly, procedures must follow the MSL and maximum reflow temperature specified on the shipping bag labels or barcode labels accompanying all QCA9377 IC shipments.

4.5 Thermal characteristics

Table 4-5 Device thermal resistance

Parameter	Parameter description	Comments	Typ.	Unit
θ_{JA}	Thermal resistance, J-to-A	Junction-to-ambient (still air)*	26.0	CW
* Junction-to-ambient thermal resistance (θ_{JAa}) is calculated with ambient temperature = 70°.				

5 Carrier, storage, and handling information

5.1 Tape and reel information

All QTI carrier tape systems conform to EIA-481 standards. A simplified sketch of the QCA9377-7 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.

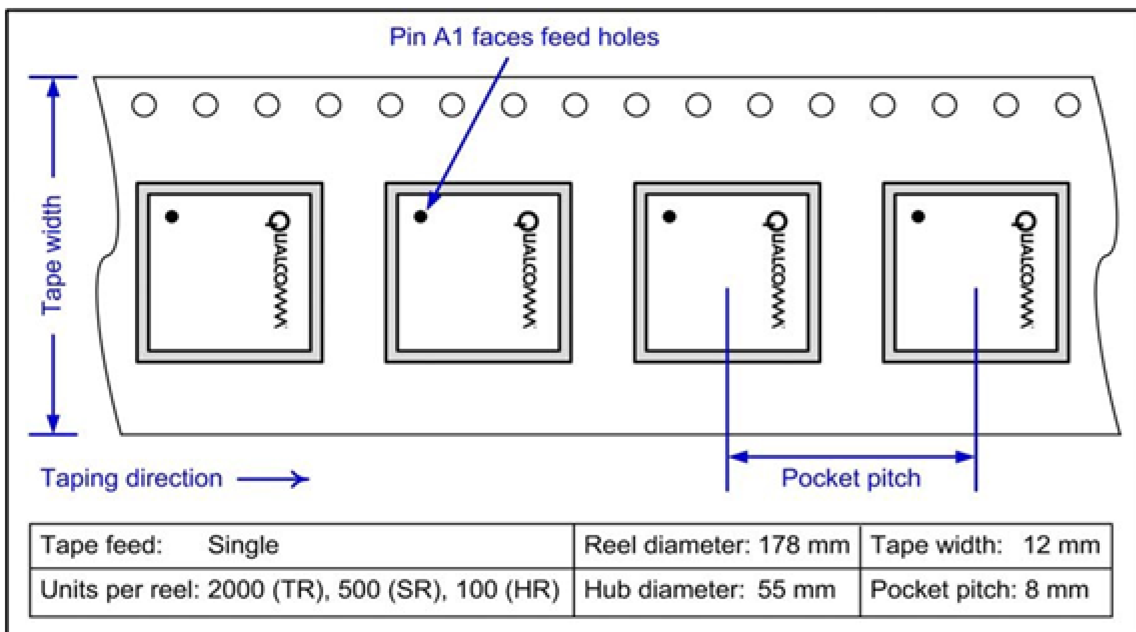

Figure 5-1 Carrier tape drawing with part orientation

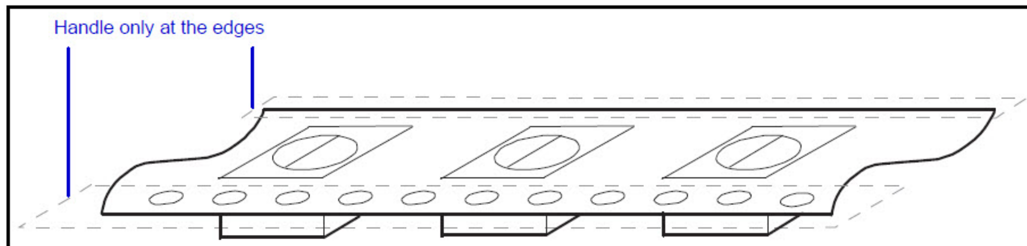

Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

QCA9377 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling is described in Section 5.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

Wafer-level packages, including this device, should not be baked.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential.

CAUTION: If this discharge path is through a semiconductor device, destructive damage could result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

See Chapter 7 for the QCA 9377-7 ESD ratings.

5.4 Barcode label and packing for shipment

See *IC Products Packing Method* (80-VK055-1) for all packing-related information, including barcode label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device is lead-free and Restriction of Hazardous Substances (RoHS)-compliant. Its SnAgCu solder balls use SAC405 composition.

6.2 SMT parameters

For recommendations on SMT process development, see *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE: Click the following link to download *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products. The daisy-chain interconnect drawing shows how packages should be attached to a characterization PCB. All SMT development described in Section 6.2 can be performed using daisy-chain packages. A bias can be applied, and solder-joint resistance can be monitored.

NOTE: Click the following link to download *Daisy Chain Interconnect, 115 WLNSP, 4.34×5.48mm, Superset* (DS90-Y8108-1) from the Qualcomm CreatePoint support website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/0901003981cc8934

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

7 Part reliability

7.1 Reliability qualifications summary

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
Average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-A Use condition: Temperature: 65°C, core voltage: 1.2 V Total samples from three different wafer lots	3x77	0F/231 AFR=25 FITs
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	3x77	40.4
ESD – Human-body movement (HBM) rating JESD22-A114-F Total samples from one wafer lot	1x3	Pass ±2000 V, all pins
ESD – Charged device model (CDM) rating JESD22-C101-D Total samples from one wafer lot	1x3	Pass ±400 V, all pins
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA; temperature: 85°C Total samples from one wafer lot	1x6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × Vdd max per device specification; temperature: 85°C Total samples from one wafer lot	1x6	Pass

Table 7-2 Package reliability results

Tests, standards, and conditions	SPIL	ATT	Result
Moisture resistance test (MRT): MSL1; J-STD-020/JESD22-A113-F Reflow at 260°C +0/-5°C, Total samples from three different assembly lots	3x231	3x231	Both pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8 to 10 minutes Cycle rate: 2 cycles per hour Preconditioning: JESD22-A113-F MSL1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	3x77	3x77	Both pass

Tests, standards, and conditions	SPIL	ATT	Result
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	3x77	3x77	Both pass
Biased highly accelerated stress test: JESD22-A110 110°C/85% RH and 264 hours duration Preconditioning: JESD22-A113-F MSL1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	3x77	3x77	Both pass
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots	3x77	3x77	Both pass
Physical dimensions: JESD22-B100-A Case outline drawing: Qualcomm internal document Total samples from one assembly lot at each SAT	1x15	1x15	Both pass
Solder ball shear JESD22-B117 After 10X reflow cycles; 260°C +0/-5°C	1x15	1x15	Both pass

7.2 Qualification sample description

Device number: QCA9377

Package type: WLP 115B

Package body size: 4.32 mm × 5.46 mm × 0.566 mm

Fab process: 40 nm LP CMOS

Fab location: UMC Taiwan

Assembly location: SPIL & ATT