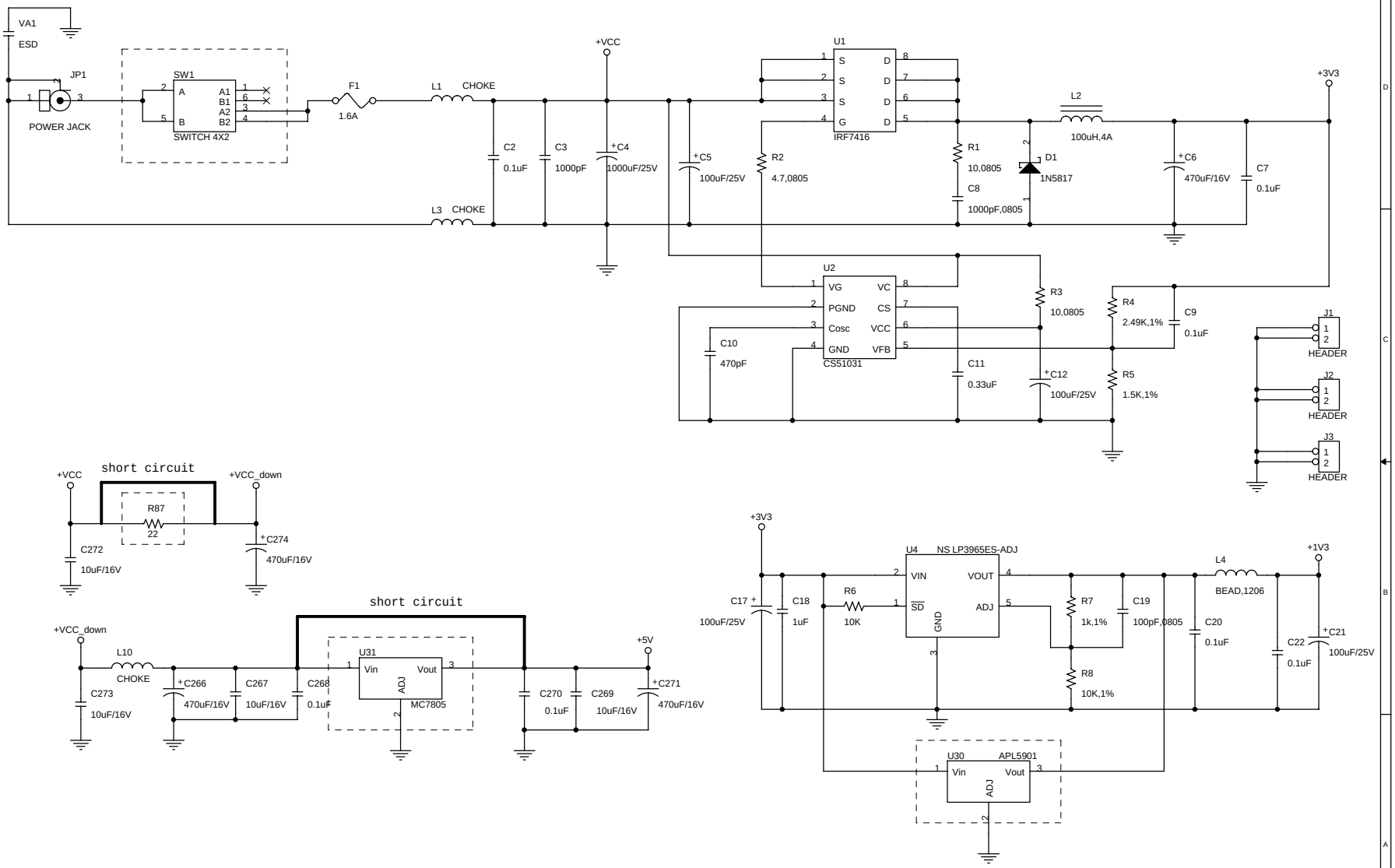
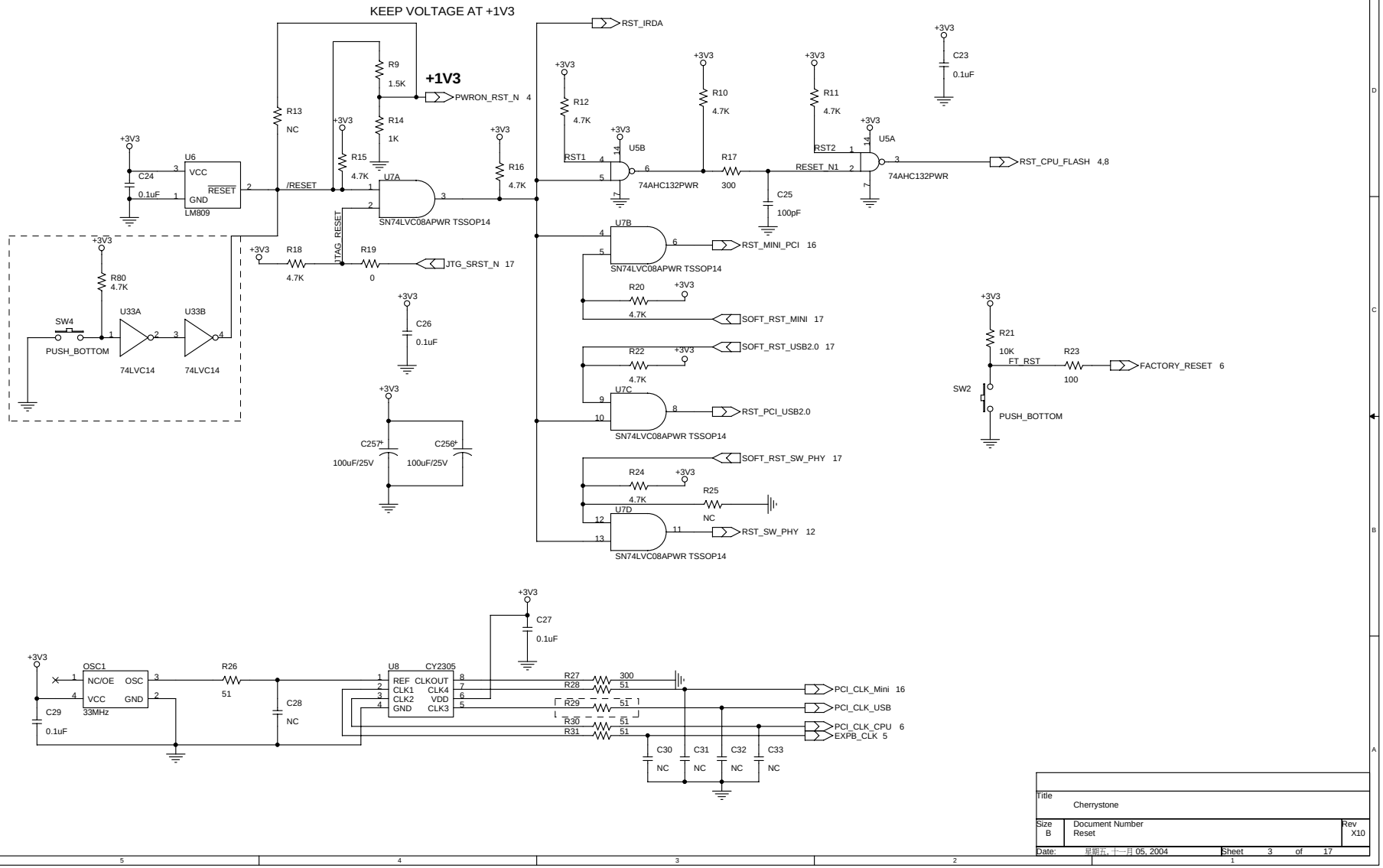


Title	Cherrystone	
Size: Custom	Document Number: POWER	Rev: X10
Date: 星期五, 十一月 05, 2004	Sheet 2 of 17	



Title	Cherrystone	
Size B	Document Number Reset	Rev X10
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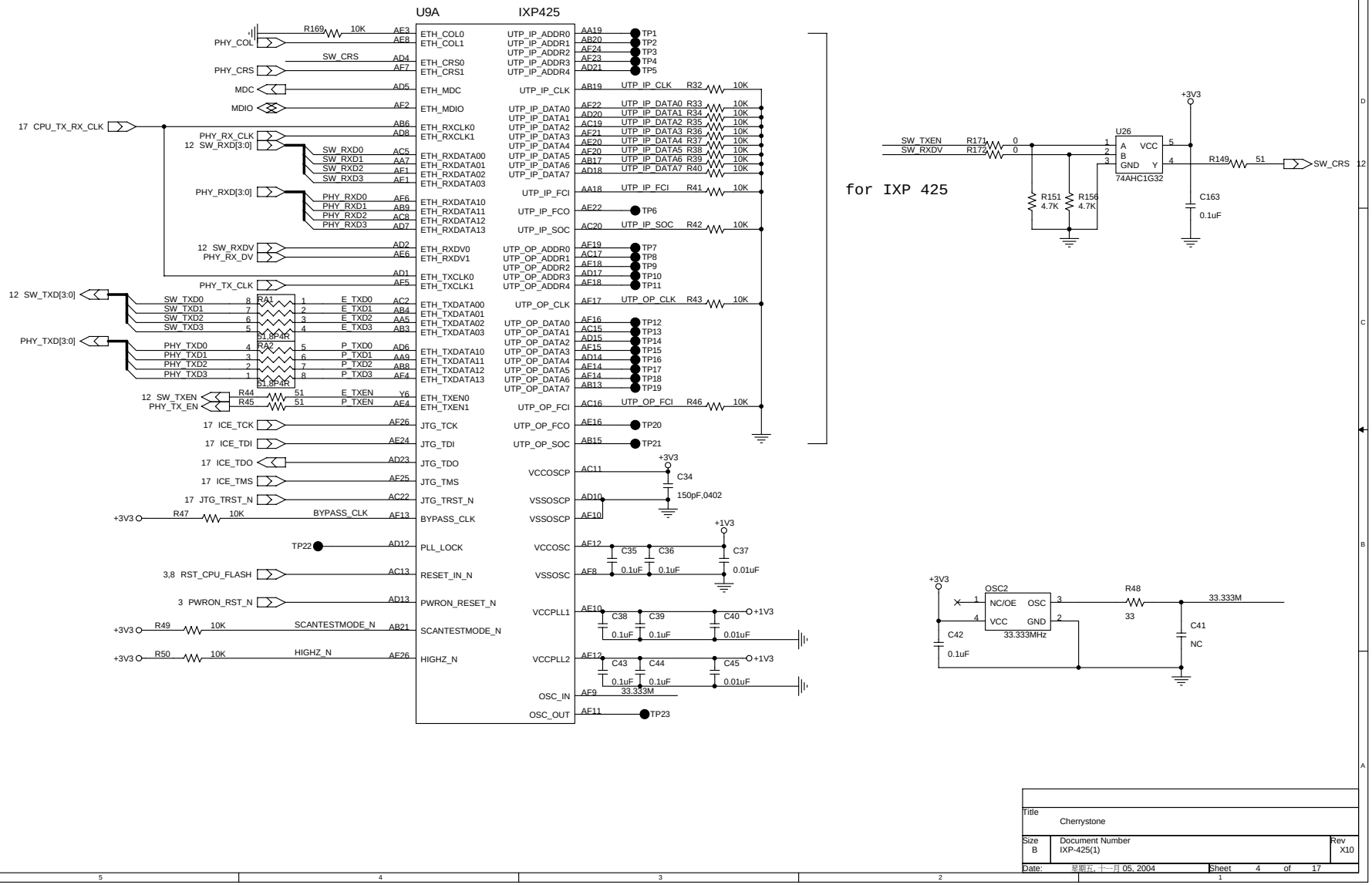
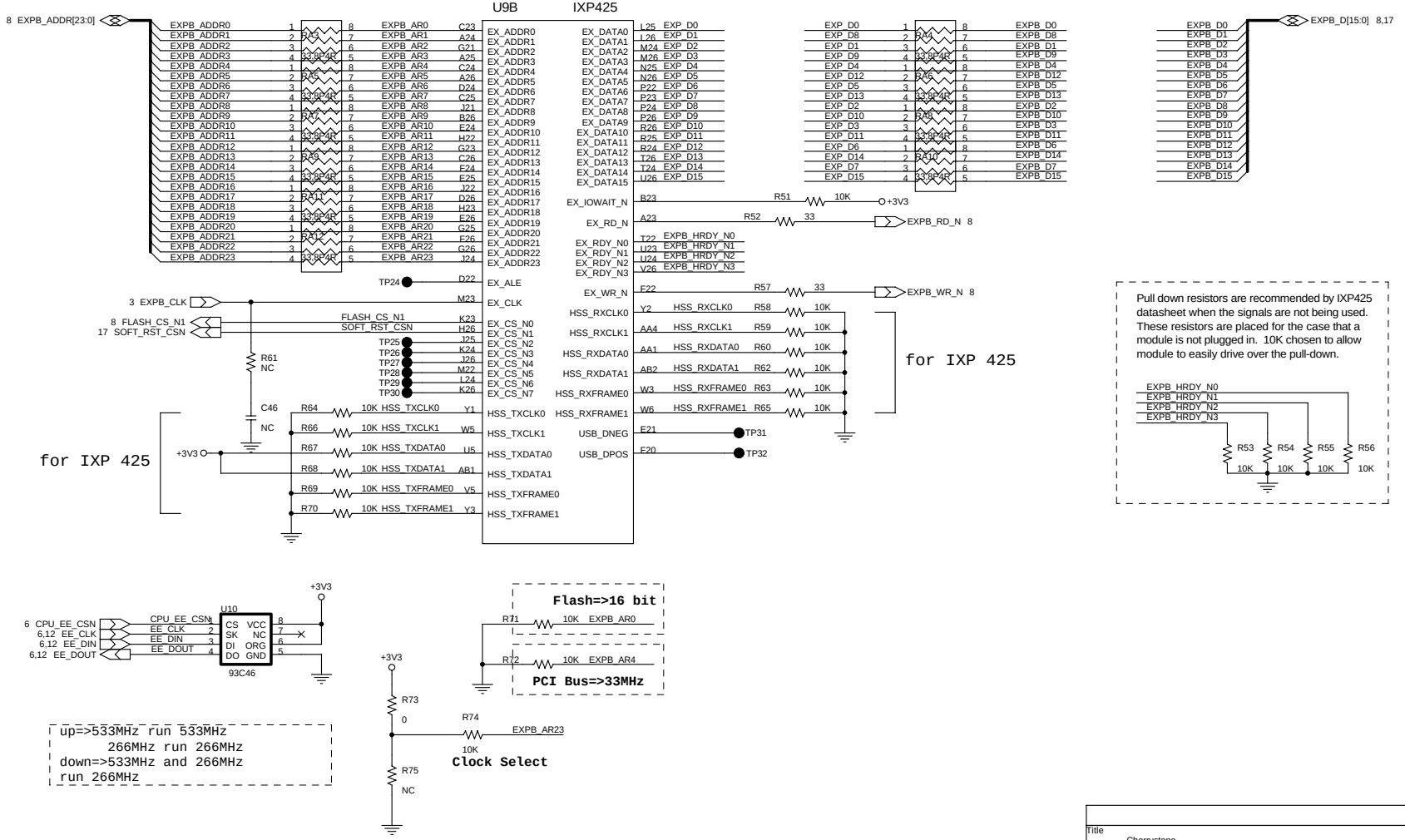
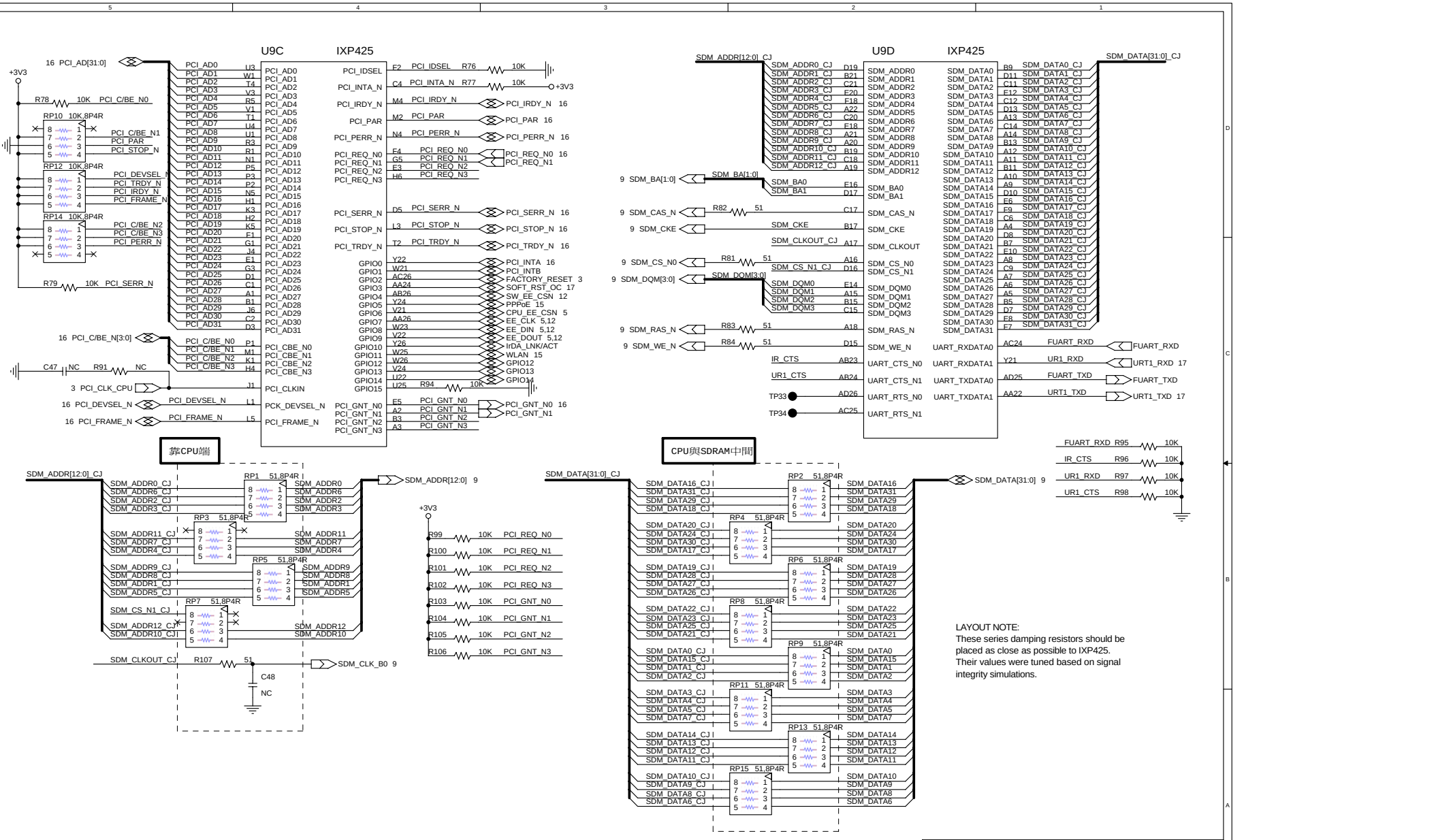


for IXP 425

Title: Cherrystone		
Size: B	Document Number: IXP-425(1)	Rev: X10
Date: 星期五, 十一月 05, 2004	Sheet 4 of 17	



Title	Cherrystone	
Size B	Document Number IXP-425(2)	Rev X10
Date: 星期五, 十一月 05, 2004	Sheet 5 of 17	


U9C IXP425
U9D IXP425
靠CPU端
CPU與SDRAM中間
LAYOUT NOTE:
These series damping resistors should be placed as close as possible to IXP425. Their values were tuned based on signal integrity simulations.
Title
Cherrystone
Size Custom
Document Number IXP-425(3)
Rev X10
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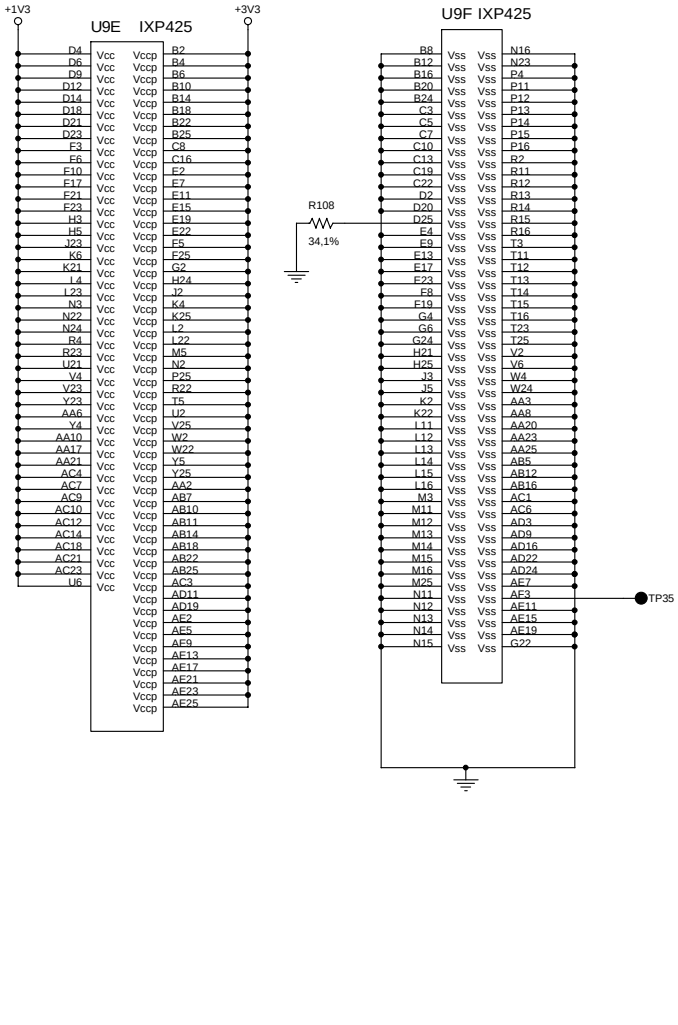
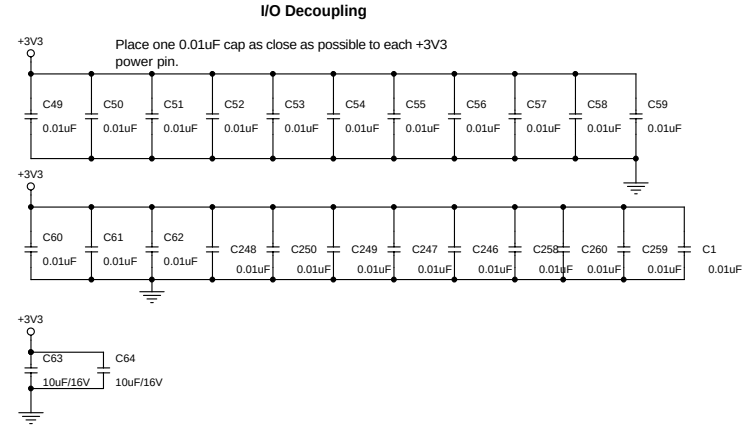
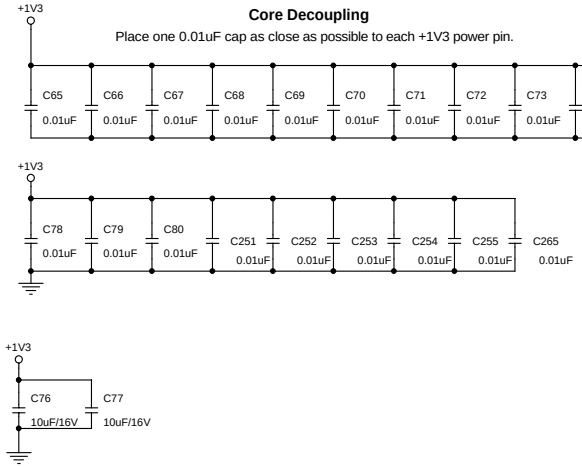
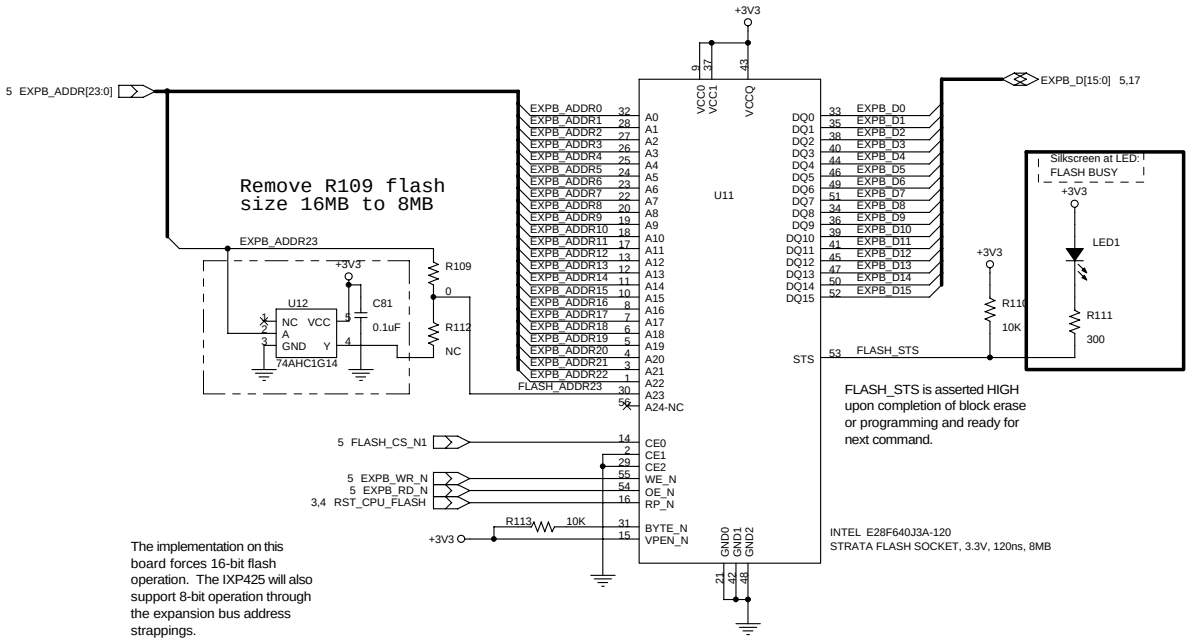






Title	Cherrystone	
Size B	Document Number IXP-425(4)	Rev X10
Date: 星期五, 十一月 05, 2004	Sheet 7 of 17	



Title	Cherrystone	
Size B	Document Number FLASH	Rev X10
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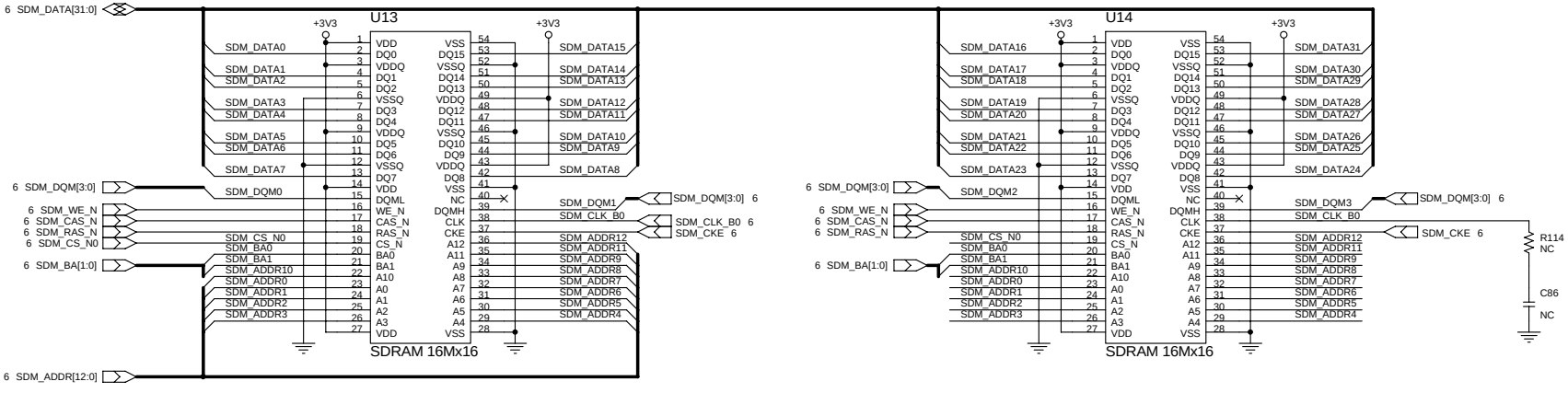

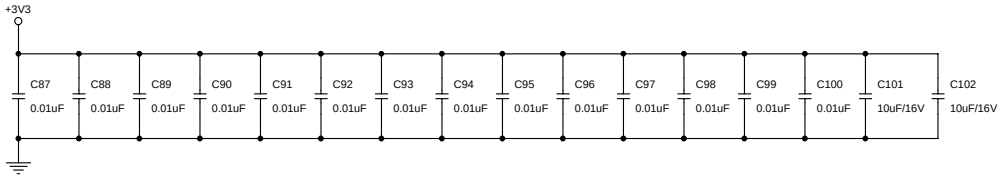

Title: Cherrystone		
Size: B	Document Number: SDRAM	Rev: X10
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Note : 1.pin63 : default enable flow control (1)
2.pin107 : default enable back pressure (1)
3.pin109 : default enable auto negotiation (1)

+3V3 R154 4.7K EE_CLK (1) Auto MDIX
R179 4.7K EE_DIN (0) Single color mode

U23 ADM6996L

+1V8 +3V3

C159 10uF/16V C156 C225 C226 C227 0.1uF

C232 10uF/16V C235 C228 C229 C231 C230 C234 C233 0.1uF

4 SW_TXD[3:0] SW_TXD3 SW_TXD2 SW_TXD1

15 P0_SPD 15 P1_SPD 15 P2_SPD 15 P3_SPD R155 R157 R160 R161 150

4 SW_RXD[3:0] RA13 SW_RXD3 SW_RXD2 SW_RXD1 SW_RXD0 51,8P4R

15 P0_L/A 15 P1_L/A 15 P2_L/A 15 P3_L/A R173 R174 R175 R176 150

4 SW_RXDV 17 SW_TX_RX_CLK

4 SW_TXD0 4 SW_CRS SW_TXD0 R165 4.7K R164 4.7K

4 SW_TXEN

TXP0 TXN0 RXP0 RXN0
TXP1 TXN1 RXP1 RXN1 P0_TXP P0_TXN P0_RXP P0_RXN
TXP2 TXN2 RXP2 RXN2 P1_TXP P1_TXN P1_RXP P1_RXN
TXP3 TXN3 RXP3 RXN3 P2_TXP P2_TXN P2_RXP P2_RXN
TXP4 TXN4 RXP4 RXN4 P3_TXP P3_TXN P3_RXP P3_RXN

+3V3 C164 10uF/16V C166 0.1uF

CONTROL Q1 2SB1386 C168 0.1uF

+1V8 C179 0.1uF C169 0.01uF C180 10uF/16V

3 RST_SW_PHY 17 SW_25MHz C150 NC R150 NC C183 0.1uF CONTROL R148 1.13K,1%

EE_DIN SW_EE_CSN EE_CLK EE_DOUT

+3V3 C185 0.1uF C186 0.01uF

+1V8 C177 0.1uF C184 0.01uF

+3V3 C151 10uF/16V C152 C153 C154 C155 0.1uF

+1V8 C171 10uF/16V C172 C173 C174 C175 C176 C160 C161 C162 0.1uF

14 P0_RXP R180 49.9 C157 0.1uF
14 P0_RXN R181 49.9
14 P0_TXP R182 49.9 C158 0.1uF
14 P0_TXN R183 49.9
14 P1_RXP R184 49.9 C165 0.1uF
14 P1_RXN R185 49.9
14 P1_TXP R186 49.9 C167 0.1uF
14 P1_TXN R187 49.9
14 P2_RXP R188 49.9 C170 0.1uF
14 P2_RXN R189 49.9
14 P2_TXP R190 49.9 C178 0.1uF
14 P2_TXN R191 49.9
14 P3_RXP R192 49.9 C181 0.1uF
14 P3_RXN R193 49.9
14 P3_TXP R194 49.9 C182 0.1uF
14 P3_TXN R195 49.9

+3V3

6 SW_EE_CSN SW_EE_CSN
5,6 EE_CLK EE_CLK
5,6 EE_DIN EE_DIN
5,6 EE_DOUT EE_DOUT

U22 93C66 CS SK DI DO VCC NC ORG GND

Title	Cherrystone		
Size	Document Number		Rev
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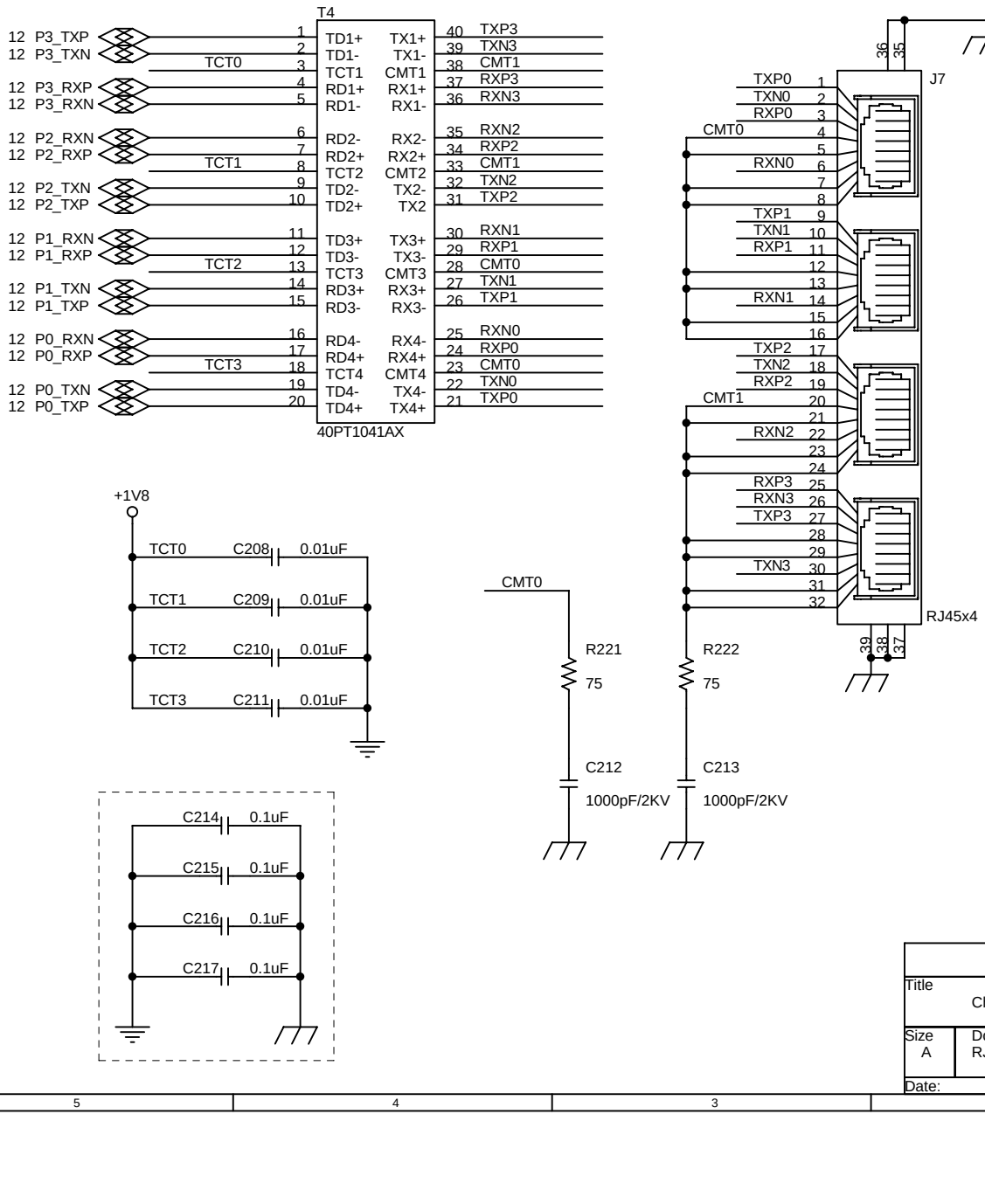
LAN



Title: Cherrystone		
Size: A	Document Number: RJ-45	Rev: X10
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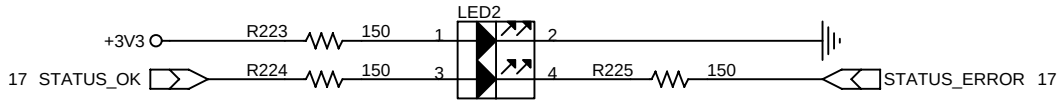
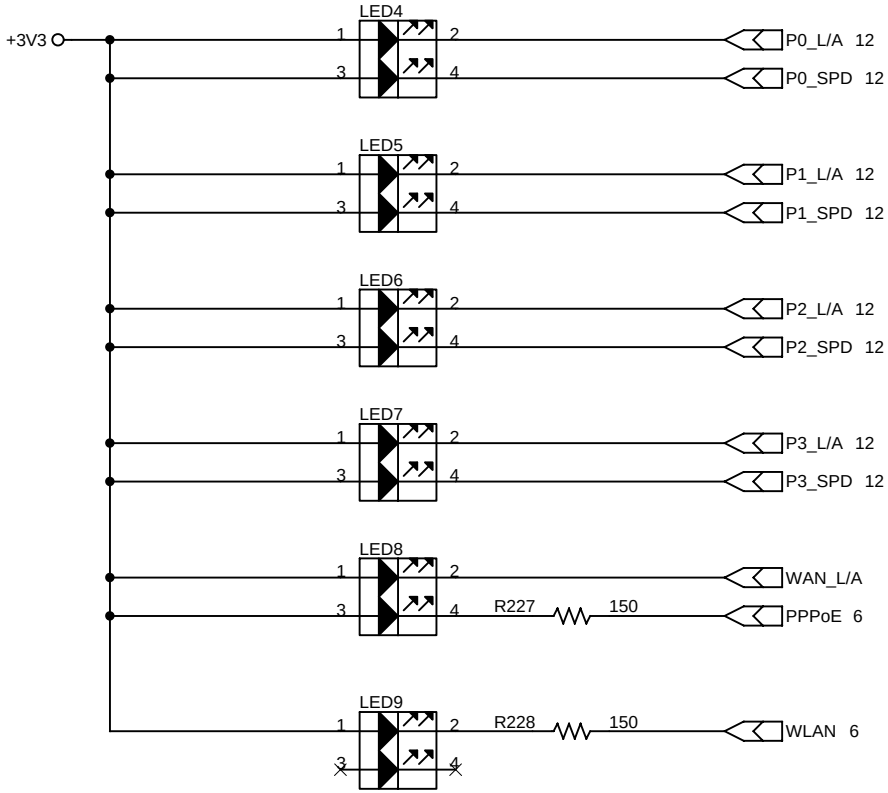


OK : Green
Error : Yellow and Blinking



Title: Cherrystone		
Size: A	Document Number: LED	Rev: X10
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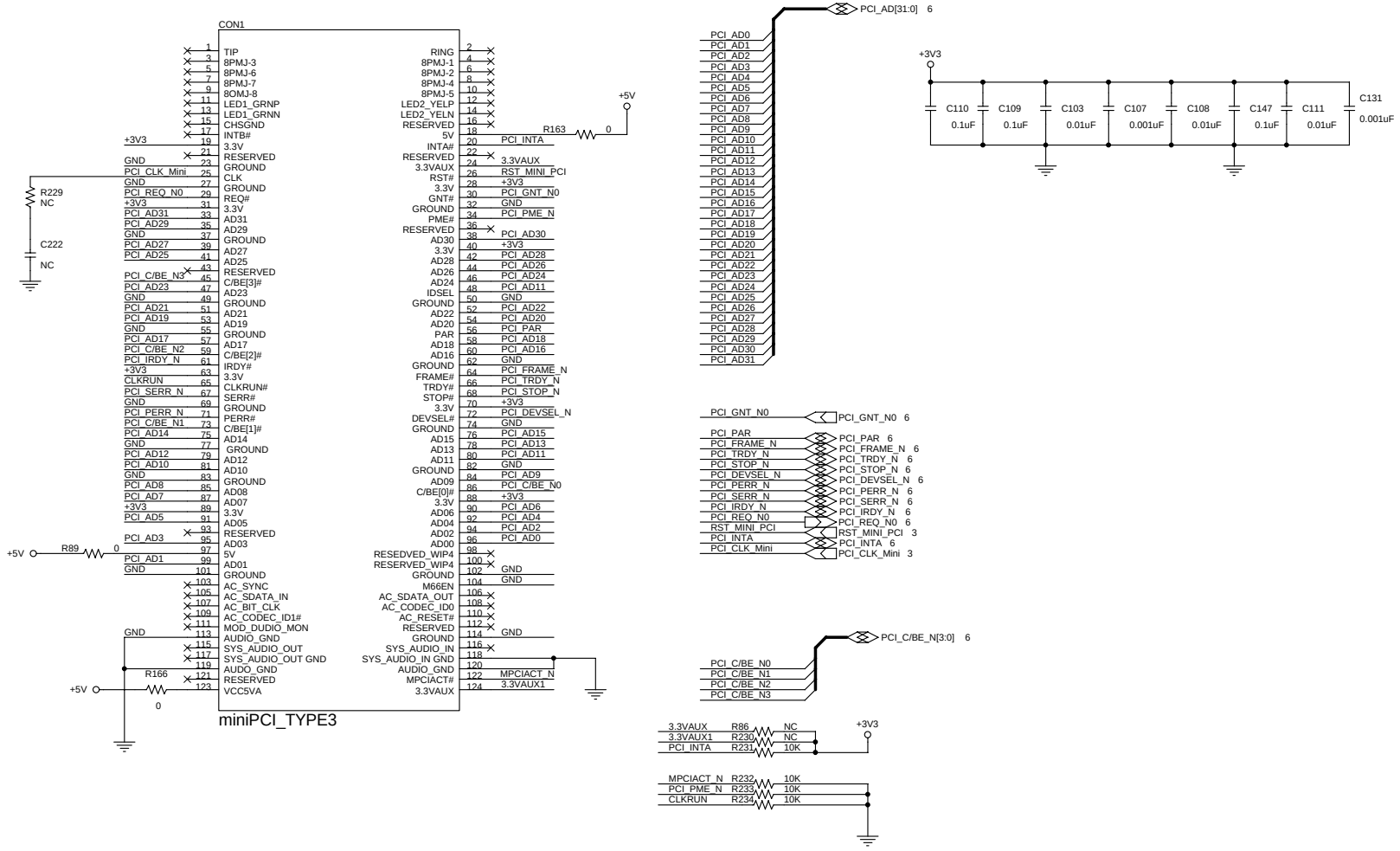

Title	Cherrystone	
Size B	Document Number Mini-PCI	Rev x10
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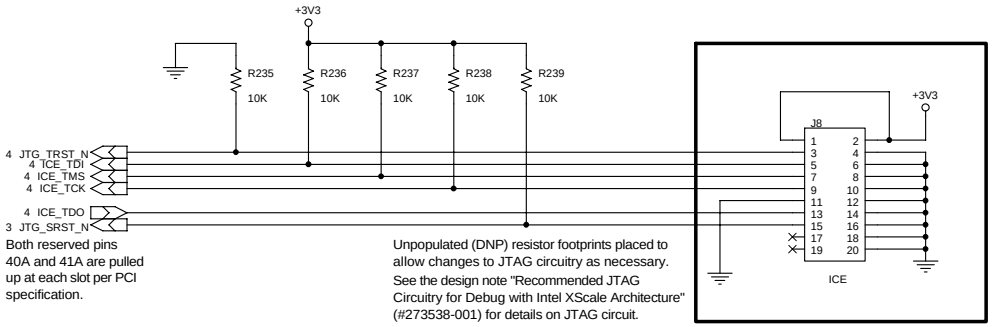
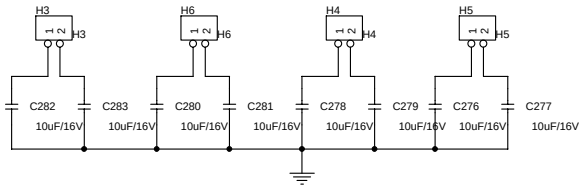
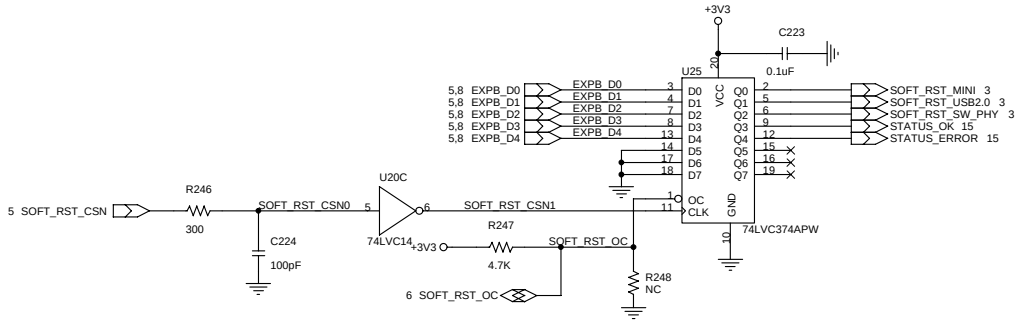
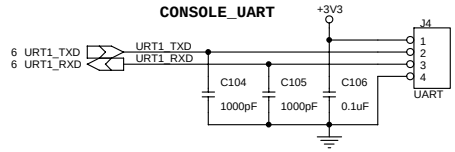


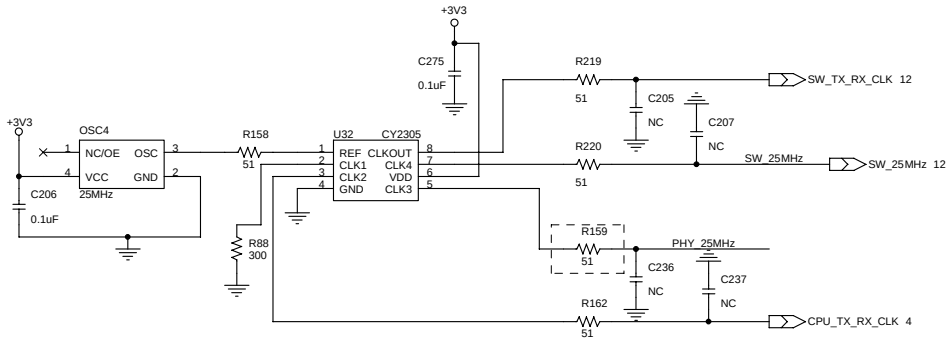
Both reserved pins 40A and 41A are pulled up at each slot per PCI specification.

Unpopulated (DNP) resistor footprints placed to allow changes to JTAG circuitry as necessary. See the design note "Recommended JTAG Circuitry for Debug with Intel XScale Architecture" (#273538-001) for details on JTAG circuit.









Title	Cherrystone	
Size B	Document Number Other	Rev X10
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