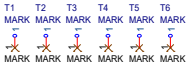
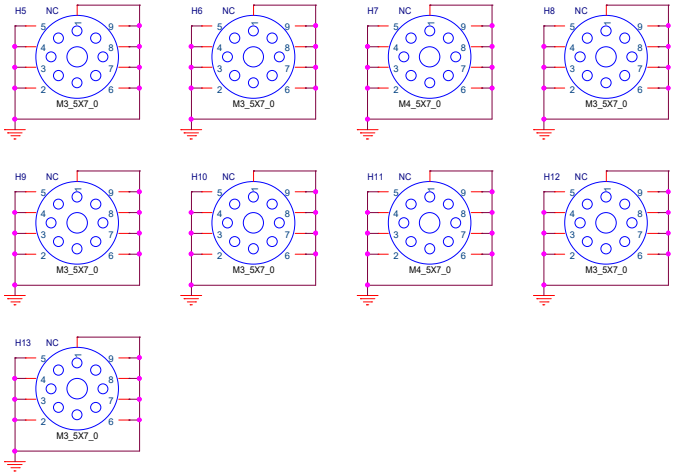
PCB MARK & LABEL

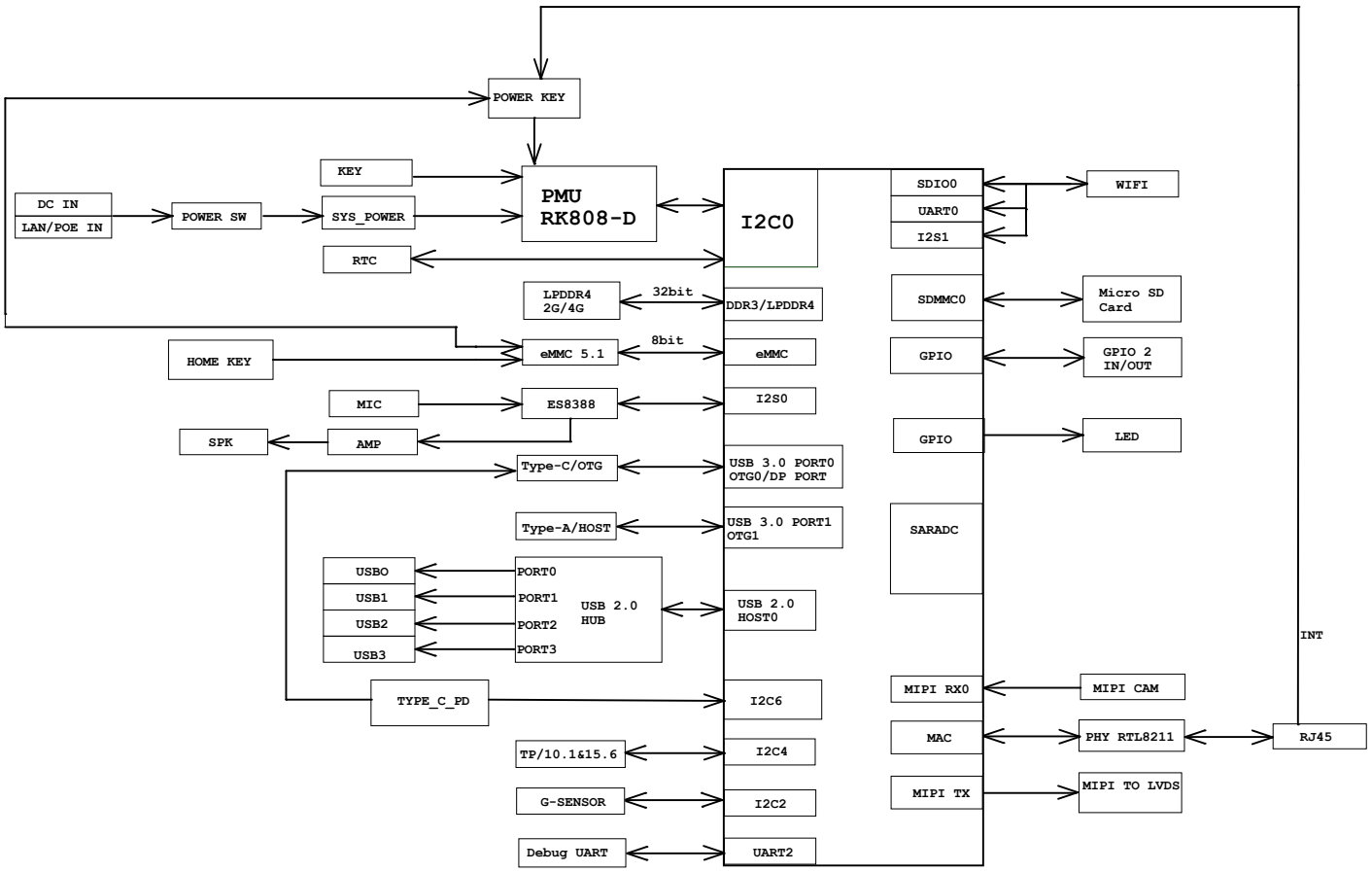
Heat Sink	
Optical Marks	
Label Outline	
Silkcreen	PCB Name & Version ELO3399 (E472673) ELO3399 ENG Version A20xxx A20xxx SMT DIP ROHS
Mounting Hole	

SIGNWAY			
Project:	E472878		
File:	01.Msc		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	ZhangboB,Yangyin	Sheet	1 of 32

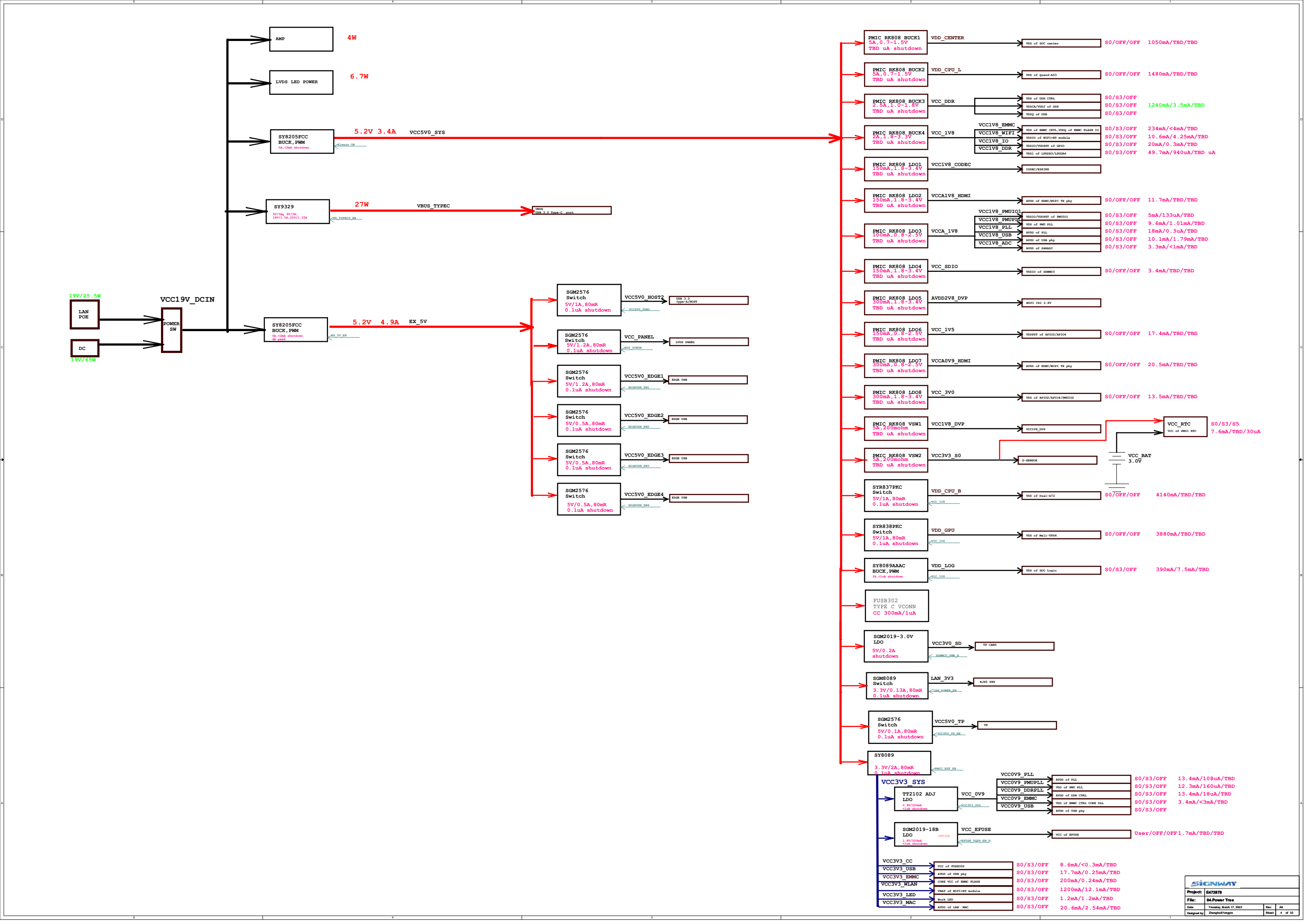
Change List

Version	Date	Author	Change Note	Approved
V0.1	April 24, 2020	Zhangbo&Yangyin	First edition.	Zhouchangliang

Project:	E472878		
File:	02.Change List		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	2 of 32



SIGNWAY	
Project:	E472878
File:	03.Block Diagram
Date:	Thursday, March 17, 2022
Rev:	A0
Designed by:	ZhangboShangyin
Sheet:	3 of 32

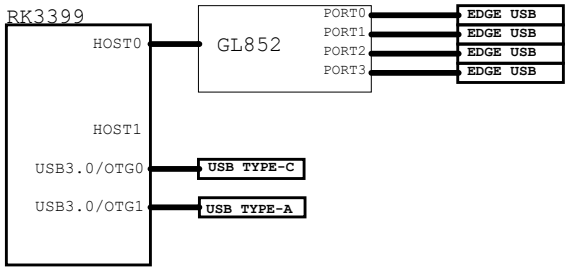


19V/25.5W
LAN POE
DC
19V/65W
POWER SW
VCC19V_DCIN
AMP
4W
LVDS LED POWER
6.7W
SY8205FCC BUCK,PWM
5.2V 3.4A
VCC5V0_SYS
SY9329
27W
VBUS_TYPEC
SY8205FCC BUCK,PWM
5.2V 4.9A
EX_5V
SGM2576 Switch 5V/1A,80mR 0.1uA shutdown
VCC5V0_HOST2
SGM2576 Switch 5V/1.2A,80mR 0.1uA shutdown
VCC_PANEL
SGM2576 Switch 5V/1.2A,80mR 0.1uA shutdown
VCC5V0_EDGE1
SGM2576 Switch 5V/0.5A,80mR 0.1uA shutdown
VCC5V0_EDGE2
SGM2576 Switch 5V/0.5A,80mR 0.1uA shutdown
VCC5V0_EDGE3
SGM2576 Switch 5V/0.5A,80mR 0.1uA shutdown
VCC5V0_EDGE4
PMIC RK808 BUCK1 5A,0.7-1.5V TBD uA shutdown
VDD_CENTER
S0/OFF/OFF 1050mA/TBD/TBD
PMIC RK808 BUCK2 5A,0.7-1.5V TBD uA shutdown
VDD_CPU_L
S0/OFF/OFF 1480mA/TBD/TBD
PMIC RK808 BUCK3 2.5A,1.0-1.8V TBD uA shutdown
VCC_DDR
S0/S3/OFF
S0/S3/OFF 1240mA/3.5mA/TBD
S0/S3/OFF
PMIC RK808 BUCK4 2A,1.8-3.3V TBD uA shutdown
VCC_1V8
VCC1V8_EMMC
VCC1V8_WIFI
VCC1V8_IO
VCC1V8_DDR
S0/S3/OFF 234mA/<4mA/TBD
S0/S3/OFF 10.6mA/4.25mA/TBD
S0/S3/OFF 20mA/0.3mA/TBD
S0/S3/OFF 49.7mA/940uA/TBD uA
PMIC RK808 LDO1 150mA,1.8-3.4V TBD uA shutdown
VCC1V8_CODEC
PMIC RK808 LDO2 150mA,1.8-3.4V TBD uA shutdown
VCCA1V8_HDMI
S0/OFF/OFF 11.7mA/TBD/TBD
PMIC RK808 LDO3 100mA,0.8-2.5V TBD uA shutdown
VCCA_1V8
VCC1V8_PMUIO
VCC1V8_PLL
VCC1V8_USB
VCC1V8_ADC
S0/S3/OFF 5mA/133uA/TBD
S0/S3/OFF 9.6mA/1.01mA/TBD
S0/S3/OFF 18mA/0.3uA/TBD
S0/S3/OFF 10.1mA/1.79mA/TBD
S0/S3/OFF 3.3mA/<1mA/TBD
PMIC RK808 LDO4 150mA,1.8-3.4V TBD uA shutdown
VCC_SDIO
S0/OFF/OFF 3.4mA/TBD/TBD
PMIC RK808 LDO5 300mA,1.8-3.4V TBD uA shutdown
AVDD2V8_DVP
PMIC RK808 LDO6 150mA,0.8-2.5V TBD uA shutdown
VCC_1V5
S0/OFF/OFF 17.4mA/TBD/TBD
PMIC RK808 LDO7 300mA,0.8-2.5V TBD uA shutdown
VCCA0V9_HDMI
S0/OFF/OFF 20.5mA/TBD/TBD
PMIC RK808 LDO8 300mA,1.8-3.4V TBD uA shutdown
VCC_3V0
S0/OFF/OFF 13.5mA/TBD/TBD
PMIC RK808 VSW1 5A,200mohm TBD uA shutdown
VCC1V8_DVP
VCC_RTC
S0/S3/S5 7.6mA/TBD/30uA
PMIC RK808 VSW2 5A,200mohm TBD uA shutdown
VCC3V3_S0
VCC_BAT 3.0V
SYR837PKC Switch 5V/1A,80mR 0.1uA shutdown
VDD_CPU_B
S0/OFF/OFF 4140mA/TBD/TBD
SYR838PKC Switch 5V/1A,80mR 0.1uA shutdown
VDD_GPU
S0/OFF/OFF 3860mA/TBD/TBD
SY8089AAAC BUCK,PWM
VDD_LOG
S0/S3/OFF 390mA/7.5mA/TBD
FUSB302 TYPE C VCONN CC 300mA/1uA
SGM2019-3.0V LDO 5V/0.2A shutdown
VCC3V0_SD
SGM8089 Switch 3.3V/0.13A,80mR 0.1uA shutdown
LAN_3V3
SGM2576 Switch 5V/0.1A,80mR 0.1uA shutdown
VCC5V0_TP
SY8089 3.3V/2A,80mR 0.1uA shutdown
VCC3V3_SYS
TT2102 ADJ LDO
VCC_0V9
VCC0V9_PLL
VCC0V9_PMUPLL
VCC0V9_DDRPLL
VCC0V9_EMMC
VCC0V9_USB
S0/S3/OFF 13.4mA/108uA/TBD
S0/S3/OFF 12.3mA/160uA/TBD
S0/S3/OFF 13.4mA/18uA/TBD
S0/S3/OFF 3.4mA/<3mA/TBD
S0/S3/OFF
SGM2019-18B LDO
VCC_EFUSE
User/OFF/OFF 1.7mA/TBD/TBD
VCC3V3_CC
VCC3V3_USB
VCC3V3_EMMC
VCC3V3_WLAN
VCC3V3_LED
VCC3V3_MAC
S0/S3/OFF 8.6mA/<0.3mA/TBD
S0/S3/OFF 17.7mA/0.25mA/TBD
S0/S3/OFF 200mA/0.24mA/TBD
S0/S3/OFF 1200mA/12.1mA/TBD
S0/S3/OFF 1.2mA/1.2mA/TBD
S0/S3/OFF 20.6mA/2.54mA/TBD
SIGNWAY
Project:
File: 04.Power Tree

I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_3V0	Rockchip RK808	0x1b	PMIC	100kHz,400KHz
					SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
					PT7C4337	0xd0,0xd1	RTC	100kHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5	I2C1_SDA_1V8 I2C1_SCL_1V8	VCC_1V8	ES8388/1.8V	0x10,0x11	Audio codec	100kHz
					FUSB302MPX/1.8V	0x44,0x46	USB-TypeC Mux	100kHz
					GL852	0X2C	USB HUB	100kHz
					TC358775XBG	0x1E,0x1F	LVDS Tx	100kHz
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2	I2C2_SDA_1V8 I2C2_SCL_1V8	VCC_1V8	MMA8452Q/1.8V	0x1D,0x1E	G-SENSOR	100kHz,400KHz,
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C3_SDA I2C3_SCL	VCC_3V0	TP/3.3V	TBD	TP TOUCH	100kHz,400KHz,3.4MHz
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C4_SDA I2C4_SCL	VCC_3V0	SW201/3.0V	0xA0 0xE0	EEPROM	10kHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	MAC USE					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2	I2C6_SDA_1V8 I2C6_SCL_1V8	VCC_1V8	SY9329	0XE2	PD	20kHz
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2	I2C7_SDA_1V8 I2C7_SCL_1V8	VCC_1V8	MIPI_CSI /1.8V			100kHz

USB MAP

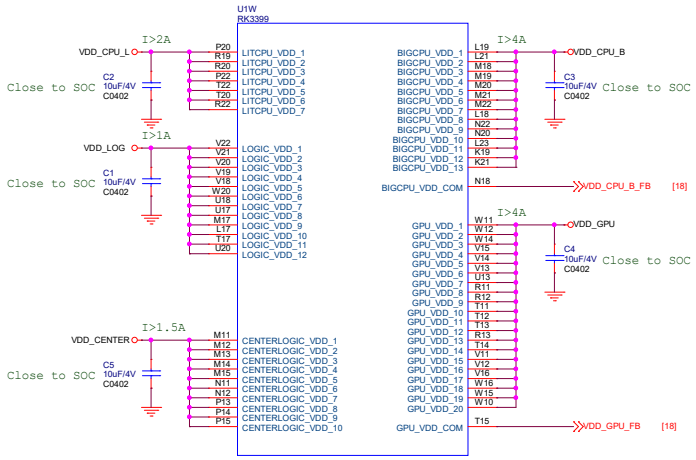


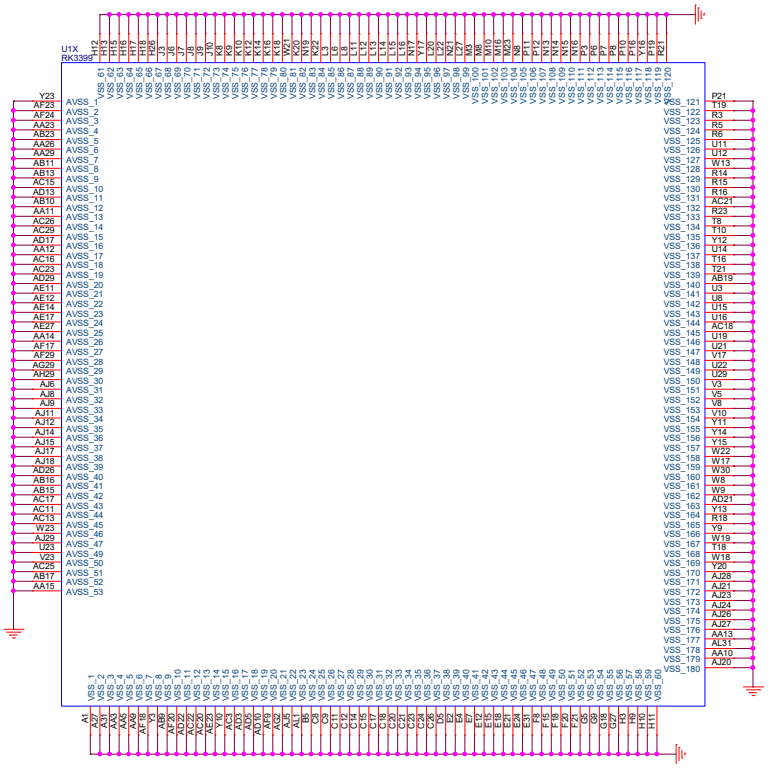
SIGNWAY			
Project:	E472878		
File:	05.I2C&USB Map		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	5 of 32

Power Domain Map

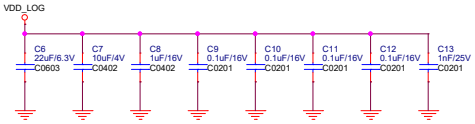
Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuio1_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLDO3
Part E	PMUIO2/PART E	pmu1830_gpio1abcd	3.0V	VCC_1V5	RK808-D Buck4 RK808-D VLDO6
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_LAN	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V	VCC_1V8	RK808-D VLDO3
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLDO6 RK808-D VLDO8
Part J	APIO5/PART J	audio_gpio3d_gpio4a	VCC1V8_CODEC	VCC1V8_CODEC	RK808-D VLDO1
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCC_SDIO	RK808-D VLDO4

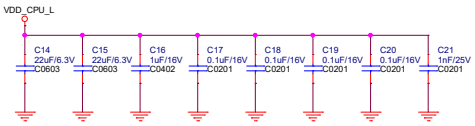
SIGNWAY			
Project:	E472878		
File:	06.Power Domain Map		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	6 of 32

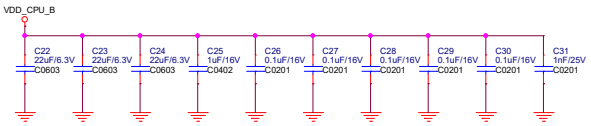


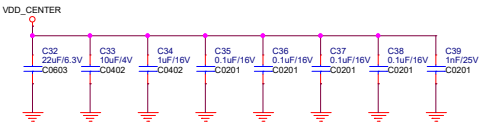


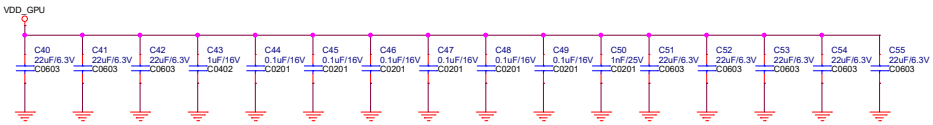
Note:Power filter CAP please place back of SOC or close to SOC



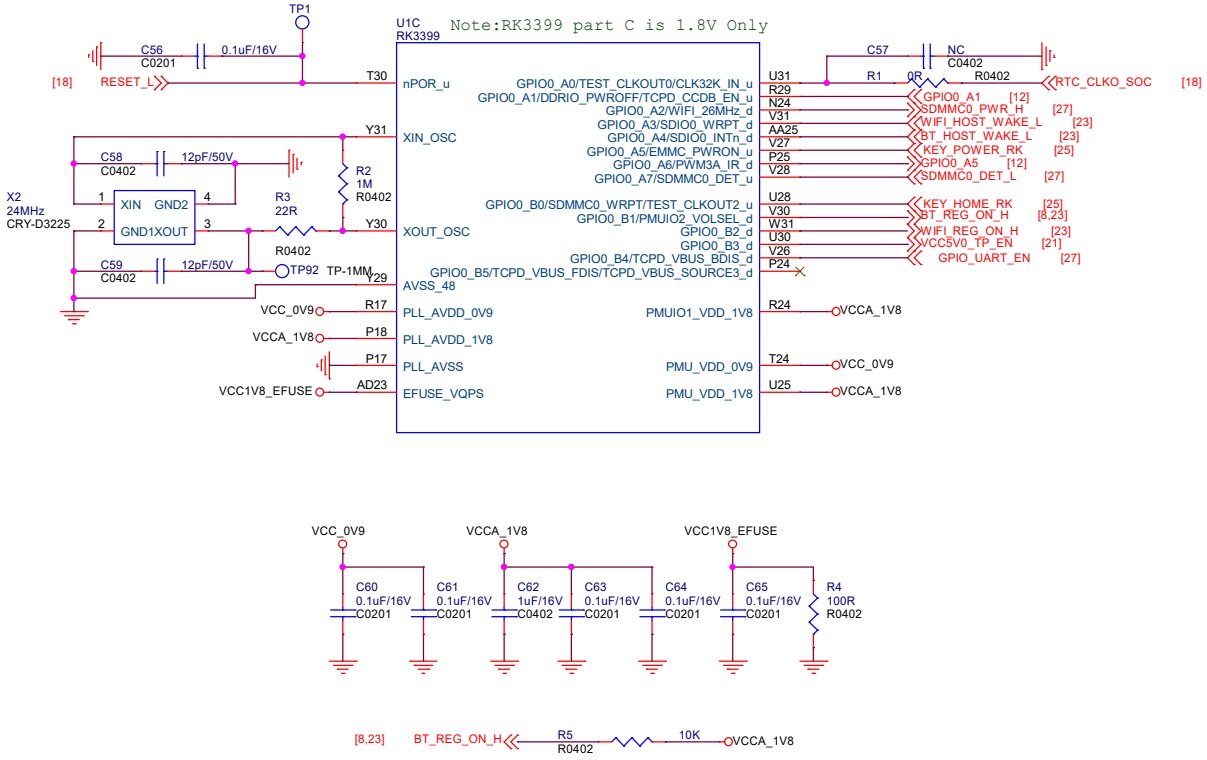




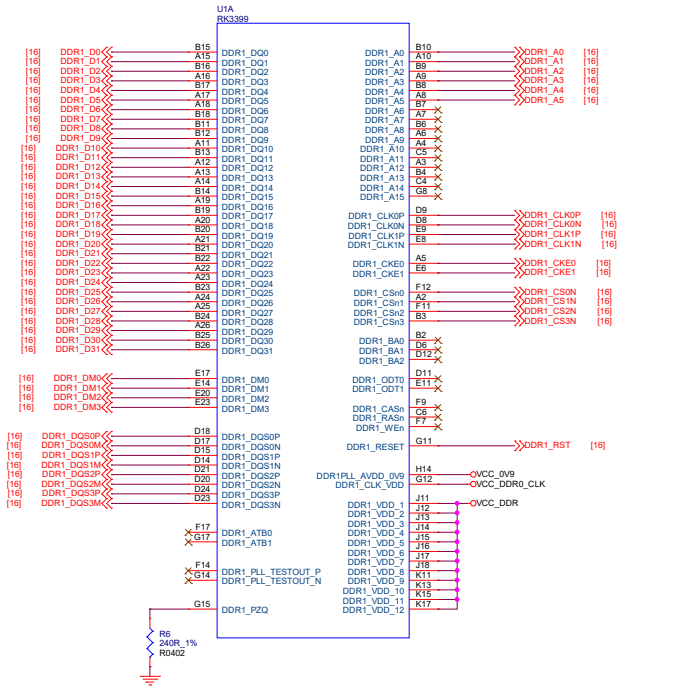


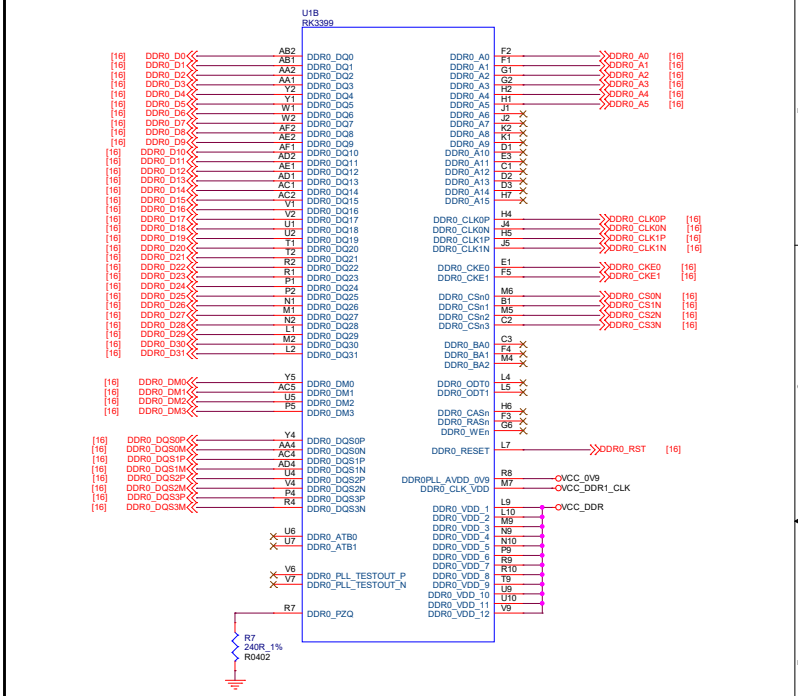


SIGNWAY	
Project:	E472878
File:	07.RK3399 Power
Date:	Thursday, March 17, 2022
Rev:	A0
Designed by:	Zhangbo&Yangyin
Sheet:	7 of 32



Project:	E472878
File:	08.RK3399 PMU Controler
Date: Thursday, March 17, 2022	Rev: A0
Designed by: Zhangbo&Yangyin	Sheet: 8 of 32





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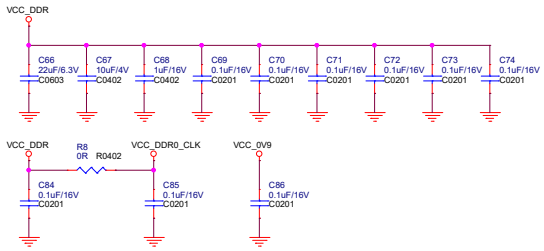

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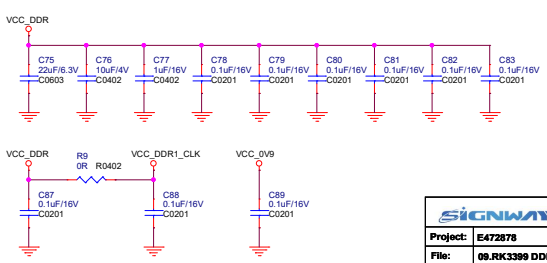
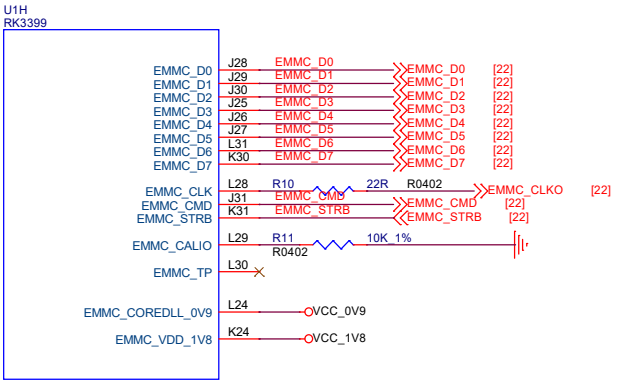
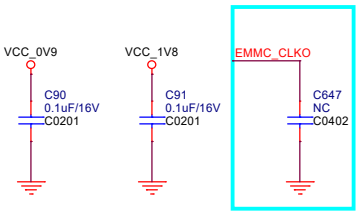


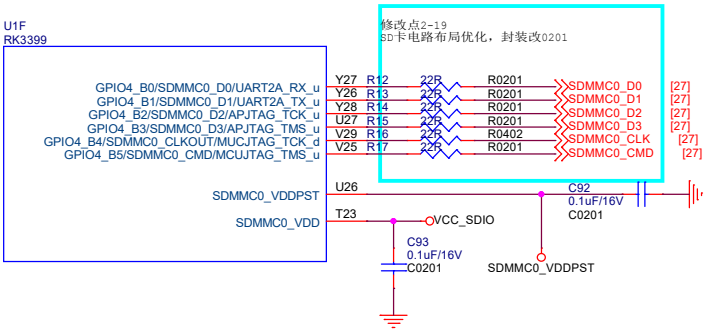
SIGNWAY	
Project:	E472878
File:	09.RK3399 DDR Controler
Date:	Thursday, March 17, 2022
Rev:	A0
Designed by:	Zhanglbo&Yangyin
Sheet:	9 of 32



EMMC design rule:
1.Data[0:7], CMD and STRB signals routing parallel as a group, the skew between each other must be less than 100mils;
2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
3.Max trace length < 3.93 inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;
6.R11 close to SOC;

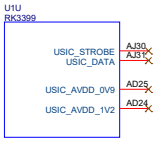


修改点2-27
EMMC_CLK增加滤波电容，EMI认证200M频率超。靠近R10 放置

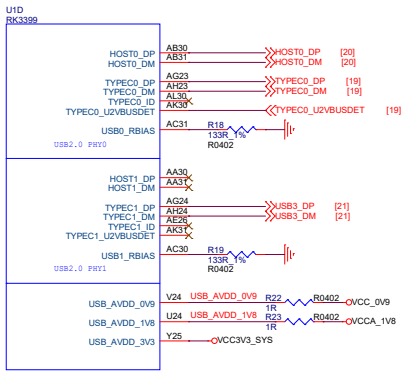


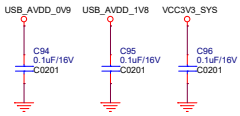
SDMMC design rule:
1.Data[0:7] and CMD signals routing parallel as a group, the skew between each other must be less than 100mils;
2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
3.Max trace length < 3.93 inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;

SIGNWAY			
Project:	E472878		
File:	10.RK3399 Flash&SDMMC Controler		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	10 of 32



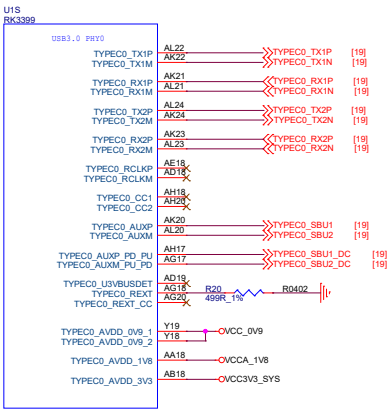
USB2.0

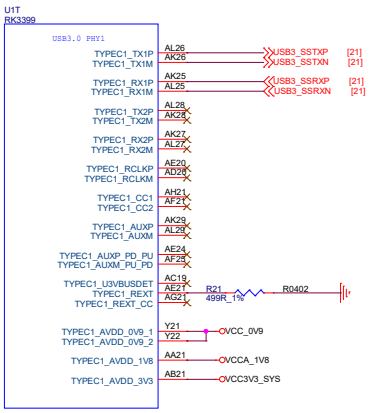


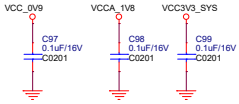


USB2.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals
follows the 3W rule;

USB3.0



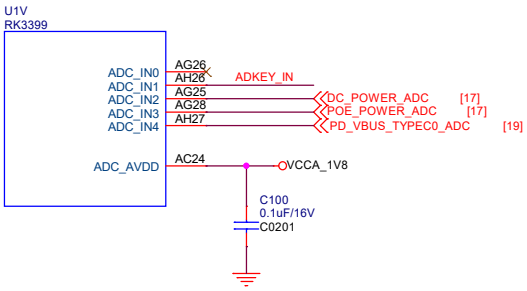


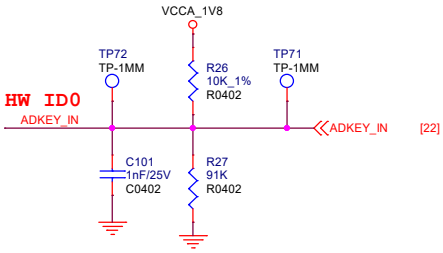


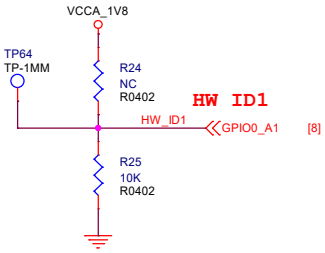
USB3.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between TX and
RX < 1.6 ns;
3.Max trace length < 6 inchs;
4.Max allowed via < 4;
5.Trace impedance 90ohm+/-10%;
6.The distance between other signals
follows the 3W rule;

DP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals
follows the 3W rule;

SIGNWAY	
Project:	E472878
File:	11.RK3399 USB/USIC Controler
Date:	Thursday, March 17, 2022
Rev:	A0
Designed by:	ZhangBoaYangyin
Sheet:	11 of 32



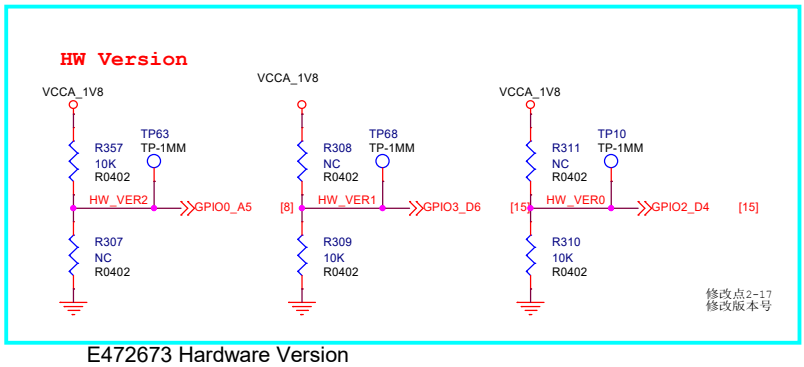




RK3399 project hardware ID definiton

ADC1 Function1: Hold on ZERO when AC plug in cold boot, enter Flash Image Mode.
ADC1 Function2: Secondary defininiton of product hardware ID.
GPIO0_A1: Main definiton of of product hardware ID.

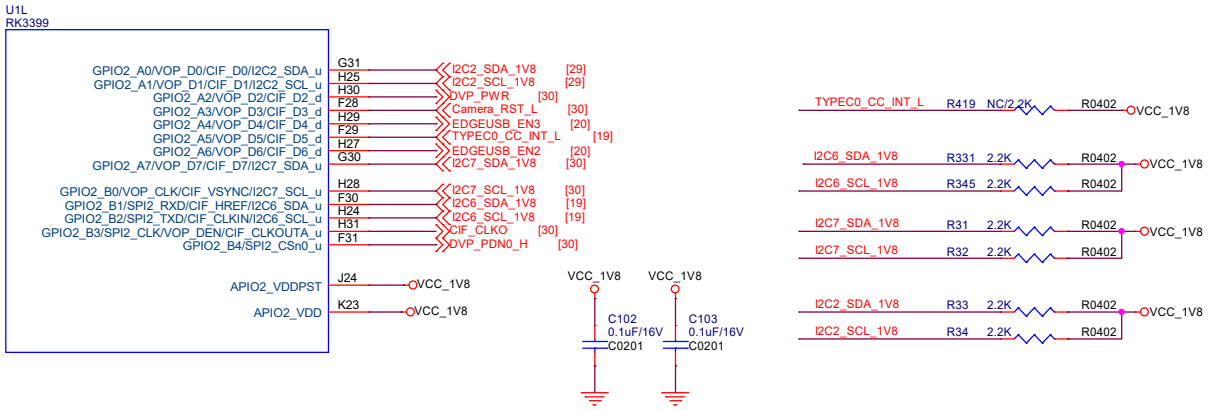
Seq.	GPIO0_A1	R27	ADC	HW ID	Date
01.	Low	NC	1.800V	E472673(15.6)	March 02, 2020
02.	Low	91K	1.622V	E472828(21.5)	
03.	Low	39K	1.433V	E473060(10.1)	
04.	Low	22K	1.238V	E473261(BACKPACK)	
05.	Low	13K	1.017V	E679524(USB-c)	
06.	Low	9.1K	0.858V	TBD	
07.	Low	6.2K	0.689V	TBD	
08.	Low	3.9K	0.505V	TBD	
09.	High	NC	1.800V	TBD	
10.	High	91K	1.622V	TBD	
11.	High	39K	1.433V	TBD	
12.	High	22K	1.238V	TBD	
13.	High	13K	1.017V	TBD	
14.	High	9.1K	0.858V	TBD	
15.	High	6.2K	0.689V	TBD	
16.	High	3.9K	0.505V	TBD	

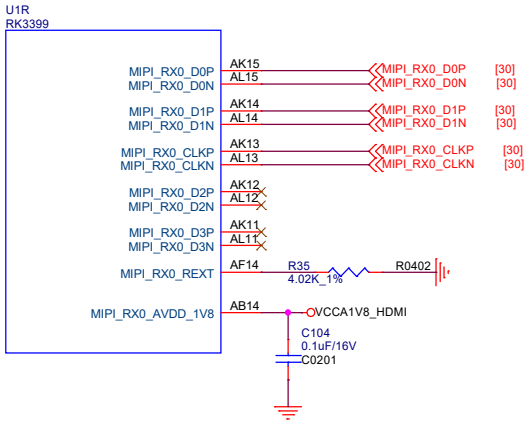


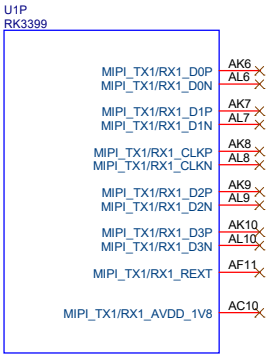
E472673 Hardware Version

Seq.	GPIO0_A5	GPIO3_D6	GPIO2_D4	HW Version	Date
01.	0	0	0	V1(EVT)	March 26, 2020
02.	0	0	1	V2	TBD
03.	0	1	0	V3	TBD
04.	0	1	1	V4	TBD
05.	1	0	0	V5	20210816
06.	1	0	1	V6	TBD
07.	1	1	0	V7	TBD
08.	1	1	1	V8	TBD

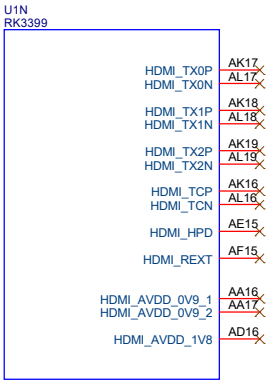
SIGNWAY			
Project:	E472878		
File:	12.RK3399 SARADC/Key		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	12 of 32



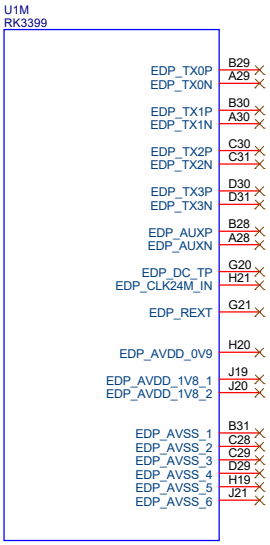




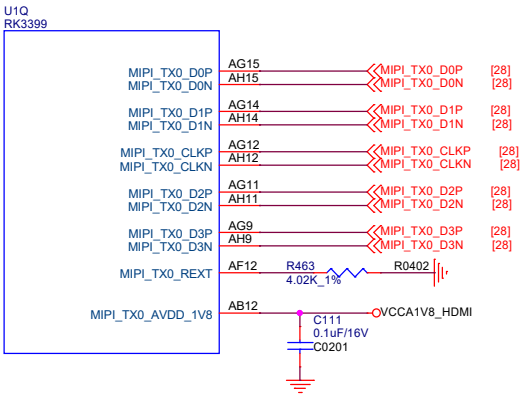
SIGNWAY	
Project:	E472878
File:	13.RK3399 DVP Interface
Date: Thursday, March 17, 2022	Rev: A0
Designed by: Zhangbo&Yangyin	Sheet: 13 of 32



HDMI design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between clk and data < 80 ps;
3.Max trace length < 9.8 inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;



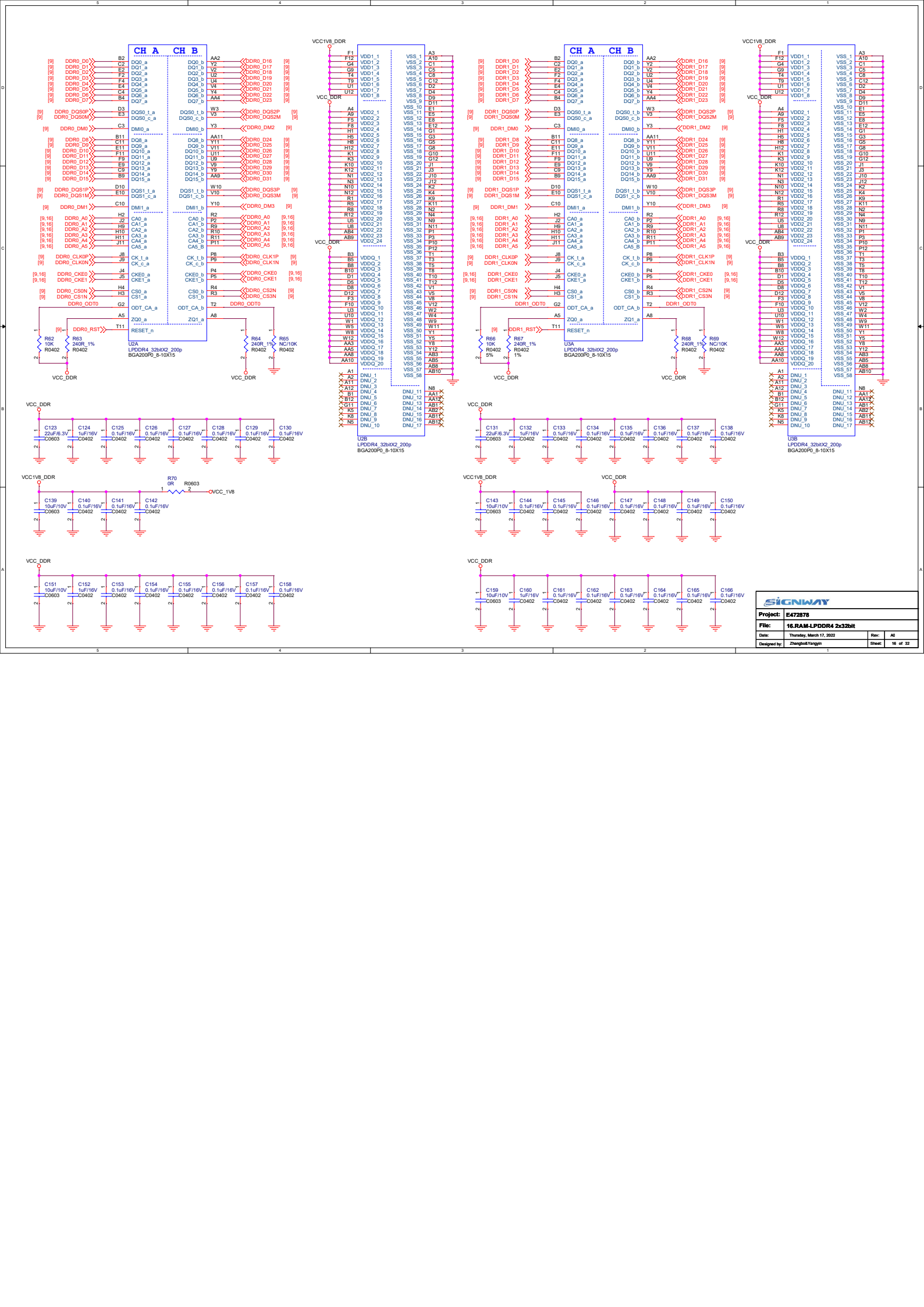
eDP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals
follows the 3W rule;



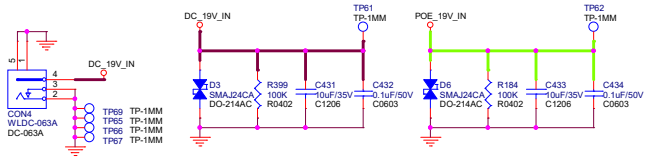
MIPI design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2 inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

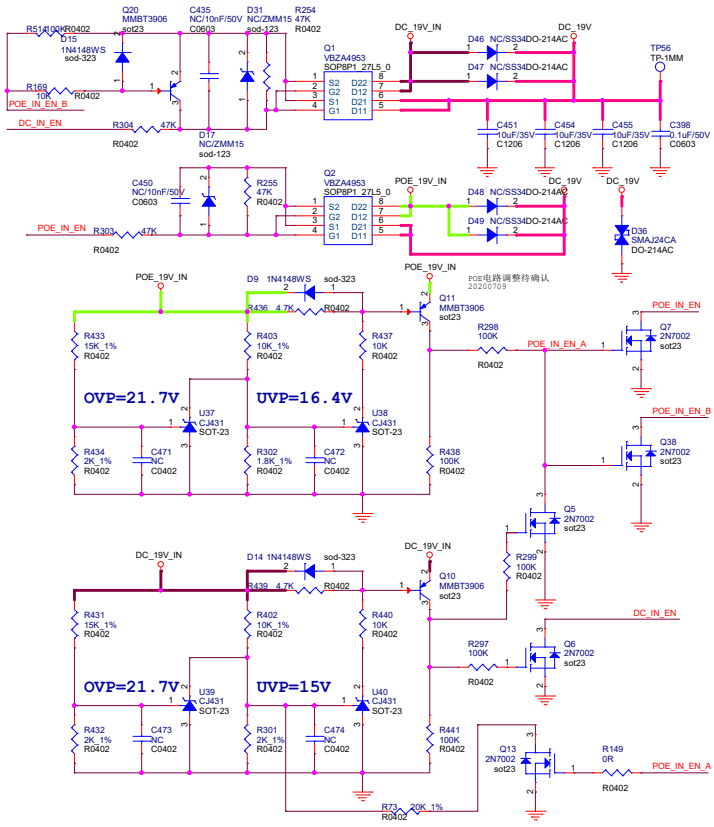
SIGNWAY			
Project:	E472878		
File:	14.RK3399 Display Interface		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	14 of 32

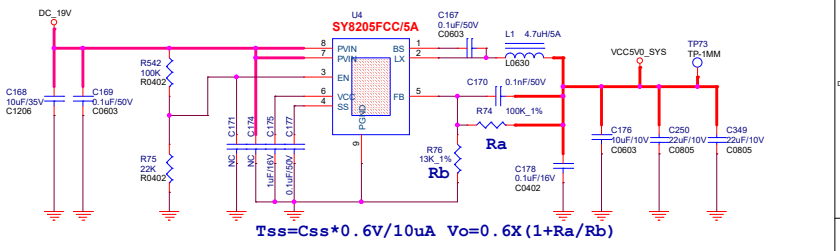
U1I
RK3399
Note:RK3399 part I is 3.3V only
修改点2-25
电阻靠近3399放置
GPIO3_A0/MAC_TXD2/SPI4_RXD_d
GPIO3_A1/MAC_TXD3/SPI4_TXD_d
GPIO3_A2/MAC_RXD2/SPI4_CLK_u
GPIO3_A3/MAC_RXD3/SPI4_CSn0_u
GPIO3_A4/MAC_TXD0/SPI0_RXD_d
GPIO3_A5/MAC_TXD1/SPI0_TXD_d
GPIO3_A6/MAC_RXD0/SPI0_CLK_u
GPIO3_A7/MAC_RXD1/SPI0_CSn0_u
GPIO3_B0/MAC_MDC/SPI0_CSn1_u
GPIO3_B1/MAC_RXDV_d
GPIO3_B2/MAC_RXER/I2C5_SDA_u
GPIO3_B3/MAC_CLK/I2C5_SCL_u
GPIO3_B4/MAC_TXEN/UART1_RX_u
GPIO3_B5/MAC_MDIO/UART1_TX_u
GPIO3_B6/MAC_RXCLK/UART3_RX_u
GPIO3_B7/MAC_CRS/CIF_CLKOUTB/UART3_TX_u
GPIO3_C0/MAC_COL/UART3_CTSn/SPDIF_TX_u
GPIO3_C1/MAC_TXCLK/UART3_RTSn_u
APIO1_VDDPST
APIO1_VDD
MAC_TXD2
MAC_TXD3
MAC_TXD0
MAC_TXD1
MAC_TXEN
MAC_TXCLK
MAC_CLK
PHY_TXD2
PHY_TXD3
MAC_RXD2
MAC_RXD3
PHY_TXD0
PHY_TXD1
MAC_RXD0
MAC_RXD1
MAC_MDC
MAC_RXDV
GPIO1_TP
PHY_TXEN
MAC_MDIO
MAC_RXCLK
PHY_RST
PHY_TXCLK
C113 120R C0402
VCC3V3_S0
L67 FB_60R_0603 L0603
VCC3V3_LAN
VCC_1V8
C114 0.1uF/16V C0201
C115 0.1uF/16V C0201
R46 4.7K R0402
R47 4.7K R0402
R48 4.7K R0402
R49 4.7K R0402
R50 1.5K R0402
VCC3V3_LAN
U1E
RK3399
Note:RK3399 part E is 1.8V/3.0V mode
PART E 3V
GPIO1_A0/ISP0_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD_VBUS_SINK_EN_d
GPIO1_A1/ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CC0_VCONN_EN_d
GPIO1_A2/ISP0_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCPD_CC1_VCONN_EN_d
GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT_d
GPIO1_A4/ISP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG_d
GPIO1_A5/AP PWROFF_d
GPIO1_A6/TSADC_INT_z
GPIO1_A7/SPI1_RXD/UART4_RX_u
GPIO1_B0/SPI1_TXD/UART4_TX_u
GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK_u
GPIO1_B2/SPI1_CSn0/PMCU_JTAG_TMS_u
GPIO1_B3/I2C4_SDA_u
GPIO1_B4/I2C4_SCL_u
GPIO1_B5_d
GPIO1_B6/PWM3B_IR_d
GPIO1_B7/SPI3_RXD/I2C0_SDA_u
GPIO1_C0/SPI3_TXD/I2C0_SCL_u
GPIO1_C1/SPI3_CLK_d
GPIO1_C2/SPI3_CSn0_u
GPIO1_C3/PWM2_d
GPIO1_C4/I2C8_SDA_u
GPIO1_C5/I2C8_SCL_u
GPIO1_C6/TCPD_VBUS_SOURCE0_d
GPIO1_C7/TCPD_VBUS_SOURCE1_d
GPIO1_D0/TCPD_VBUS_SOURCE2_d
DFTJTAG_TMS_u
DFTJTAG_TRSTn_d
PMUIO2_VDDPST
PMUIO2_VDD
EDP_ONOFF
TP_RST
TP_INT
HUB_RST1
PD_TYPEC0_EN
PMIC_SLEEP_H
OTP_OUT_H
ID1_3V0
ID2_3V0
ID3_3V0
ID4_3V0
I2C4_SDA
I2C4_SCL
EX_5V_EN
GPI2_SLEEP_H
I2C_SDA_PMIC
I2C_SCL_PMIC
CPU_B_SLEEP_H
LED_STATE
LOG_DVS_PWM
EDP_POWDN
PMIC_INT_L
GPIO1_3V0
GPIO2_3V0
PD_INT
VCC_1V5
VCC_3V0
I2C_SDA_PMIC
I2C_SCL_PMIC
F62 NC/TESD05CB ESD0402NP
F63 NC/TESD05CB ESD0402NP
修改点2-29
TP卡空气就电8kV不过，底部I2C信号添加ESD保护
PD_INT R515 2.2K R0402
TP_RST R512 2.2K R0402
TP_INT R513 2.2K R0402
VCC_3V0
1.8V Only: VDDPST=VDDIO=1.8V
3.3V Only: VDDPST=1.8V,VDDIO=3.3V
other: 3.0V mode:VDDPST=1.5V,VDDIO=3.0V; 1.8V mode:VDDPST=1.8V,VDDIO=1.8V
C116 0.1uF/16V C0201
C117 0.1uF/16V C0201
I2C_SDA_PMIC R51 2.2K R0402
I2C_SCL_PMIC R52 2.2K R0402
I2C4_SDA R53 2.2K R0402
I2C4_SCL R54 2.2K R0402
U1G
RK3399
Note:RK3399 part G is 1.8V only
GPIO2_C0/UART0_RX_u
GPIO2_C1/UART0_TX_u
GPIO2_C2/UART0_CTSn_u
GPIO2_C3/UART0_RTSn_u
GPIO2_C4/SDIO0_D0/SPI5_RXD_u
GPIO2_C5/SDIO0_D1/SPI5_TXD_u
GPIO2_C6/SDIO0_D2/SPI5_CLK_u
GPIO2_C7/SDIO0_D3/SPI5_CSn0_u
GPIO2_D0/SDIO0_CMD_u
GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1_u
GPIO2_D2/SDIO0_DETN/PCIE_CLKREQn_u
GPIO2_D3/SDIO0_PWREN_d
GPIO2_D4/SDIO0_BKPWR_d
APIO3_VDD_1V8
UART0_RXD
UART0_TXD
UART0_CTS
UART0_RTS
SDIO0_D0
SDIO0_D1
SDIO0_D2
SDIO0_D3
SDIO0_CMD
SDIO0_CLK
GSENSOR_INT_L_1V8
BT_WAKE_L
GPIO2_D4
SDIO design rule:
1.Data[0:7] and CMD signals routing parallel as a group, the skew between each other must be less than 100mils;
2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
3.Max trace length < 3.93 inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;
C118 0.1uF/16V C0201
R502 10K R0402
GSENSOR_INT_L_1V8
U1K
RK3399
Note:RK3399 part K is 1.8V/3.0V mode
GPIO4_C0/I2C3_SDA/UART2B_RX_u
GPIO4_C1/I2C3_SCL/UART2B_TX_u
GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM_d
GPIO4_C3/UART2C_RX_u
GPIO4_C4/UART2C_TX_u
GPIO4_C5/SPDIF_TX_d
GPIO4_C6/PWM1_d
GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG_u
GPIO4_D0/PCIE_CLKREQnB_u
GPIO4_D1/DP_HOTPLUG_d
GPIO4_D2_d
GPIO4_D3_d
GPIO4_D4_d
GPIO4_D5_d
GPIO4_D6_d
APIO4_VDDPST
APIO4_VDD
I2C3_SDA
I2C3_SCL
MIPI_PWM
UART2DBG_RX
UART2DBG_TX
AMP_MUTE
VLED
WLED
GPIO3_3V0_EN
POE_DET_OUT
BFUSE_VOPS_EN_H
EDGEUSB_EN4
EDGEUSB_EN1
CAMERA_AF_EN
UART2DBG_RX R55 22R R0402
UART2DBG_TX R56 22R R0402
CON99 NC/CON3P2.0 CON3P2_0-1X3H-DIP
F1 TESD05CB esd0402
F2 TESD05CB esd0402
I2C3_SDA R59 2.2K R0402
I2C3_SCL R60 2.2K R0402
POE_DET_OUT R548 2.2K R0402
VCC_3V0
R61 10K R0402
C121 0.1uF/16V C0201
C122 0.1uF/16V C0201
U1J
RK3399
Note:RK3399 part J is 1.8V/3.0V mode
PART J 1.8V
GPIO3_D0/I2S0_SCLK_d
GPIO3_D1/I2S0_LRCK_RX_d
GPIO3_D2/I2S0_LRCK_TX_d
GPIO3_D3/I2S0_SDI0_d
GPIO3_D4/I2S0_SDI1SDO3_d
GPIO3_D5/I2S0_SDI2SDO2_d
GPIO3_D6/I2S0_SDI3SDO1_d
GPIO3_D7/I2S0_SDO0_d
GPIO4_A0/I2S_CLK_d
GPIO4_A1/I2C1_SDA_u
GPIO4_A2/I2C1_SCL_u
GPIO4_A3/I2S1_SCLK_d
GPIO4_A4/I2S1_LRCK_RX_d
GPIO4_A5/I2S1_LRCK_TX_d
GPIO4_A6/I2S1_SDI0_d
GPIO4_A7/I2S1_SDO0_d
APIO5_VDDPST
APIO5_VDD
I2S0_SCLK
I2S0_LRCK_RX
I2S0_LRCK_TX
I2S0_SDI0
RESX_1V8
GPIO3_D6
I2S0_SDO0
I2S_MCLK
I2C1_SDA_1V8
I2C1_SCL_1V8
I2S1_SCLK
I2S1_LRCK_RX
VCC5V0_USB1
I2S1_SDI0
I2S1_SDO0
I2C1_SDA_1V8 R57 2.2K R0402
I2C1_SCL_1V8 R58 2.2K R0402
VCC1V8_CODEC
C119 0.1uF/16V C0201
C120 0.1uF/16V C0201
SIGNWAY
Project: E472878
File: 15.RK3399 GPIO
Date: Thursday, March 17, 2022
Rev: A0
Designed by: ZhangboliYangjin
Sheet: 15 of 32

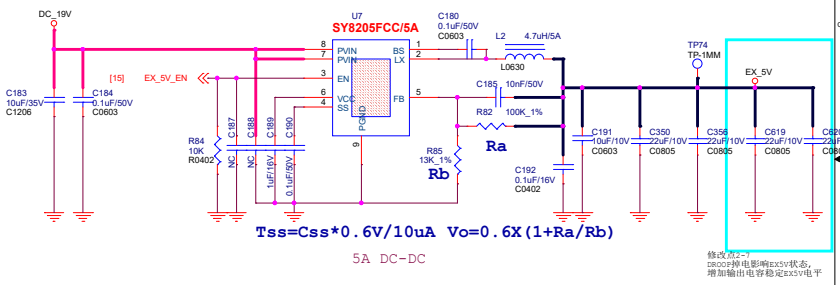

CH A
CH B
U2A
LPDDR4_32bitX2_200p
BGA200P0_8-10X15
U2B
LPDDR4_32bitX2_200p
BGA200P0_8-10X15
U3A
LPDDR4_32bitX2_200p
BGA200P0_8-10X15
U3B
LPDDR4_32bitX2_200p
BGA200P0_8-10X15
VCC1V8_DDR
VCC_DDR
VCC_1V8
DDR0_RST
DDR1_RST
DDR0_ODT0
DDR1_ODT0
R62 10K R0402
R63 240R_1% R0402
R64 240R_1% R0402
R65 NC/10K R0402
R66 10K R0402 5%
R67 240R_1% R0402 1%
R68 240R_1% R0402
R69 NC/10K R0402
R70 0R R0603
C123 22uF/6.3V C0603
C124 1uF/16V C0402
C125 0.1uF/16V C0402
C126 0.1uF/16V C0402
C127 0.1uF/16V C0402
C128 0.1uF/16V C0402
C129 0.1uF/16V C0402
C130 0.1uF/16V C0402
C131 22uF/6.3V C0603
C132 1uF/16V C0402
C133 0.1uF/16V C0402
C134 0.1uF/16V C0402
C135 0.1uF/16V C0402
C136 0.1uF/16V C0402
C137 0.1uF/16V C0402
C138 0.1uF/16V C0402
C139 10uF/10V C0603
C140 0.1uF/16V C0402
C141 0.1uF/16V C0402
C142 0.1uF/16V C0402
C143 10uF/10V C0603
C144 0.1uF/16V C0402
C145 0.1uF/16V C0402
C146 0.1uF/16V C0402
C147 0.1uF/16V C0402
C148 0.1uF/16V C0402
C149 0.1uF/16V C0402
C150 0.1uF/16V C0402
C151 10uF/10V C0603
C152 1uF/16V C0402
C153 0.1uF/16V C0402
C154 0.1uF/16V C0402
C155 0.1uF/16V C0402
C156 0.1uF/16V C0402
C157 0.1uF/16V C0402
C158 0.1uF/16V C0402
C159 10uF/10V C0603
C160 1uF/16V C0402
C161 0.1uF/16V C0402
C162 0.1uF/16V C0402
C163 0.1uF/16V C0402
C164 0.1uF/16V C0402
C165 0.1uF/16V C0402
C166 0.1uF/16V C0402
SIGNWAY
Project: E472878
File: 16.RAM-LPDDR4 2x32bit
Date: Thursday, March 17, 2022
Rev: A0
Designed by: Zhanglbo&Yangyin
Sheet: 16 of 32

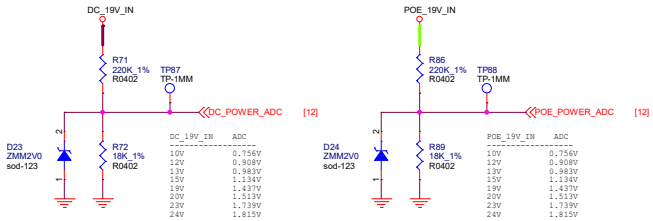
DC IN&SYSTEM Power



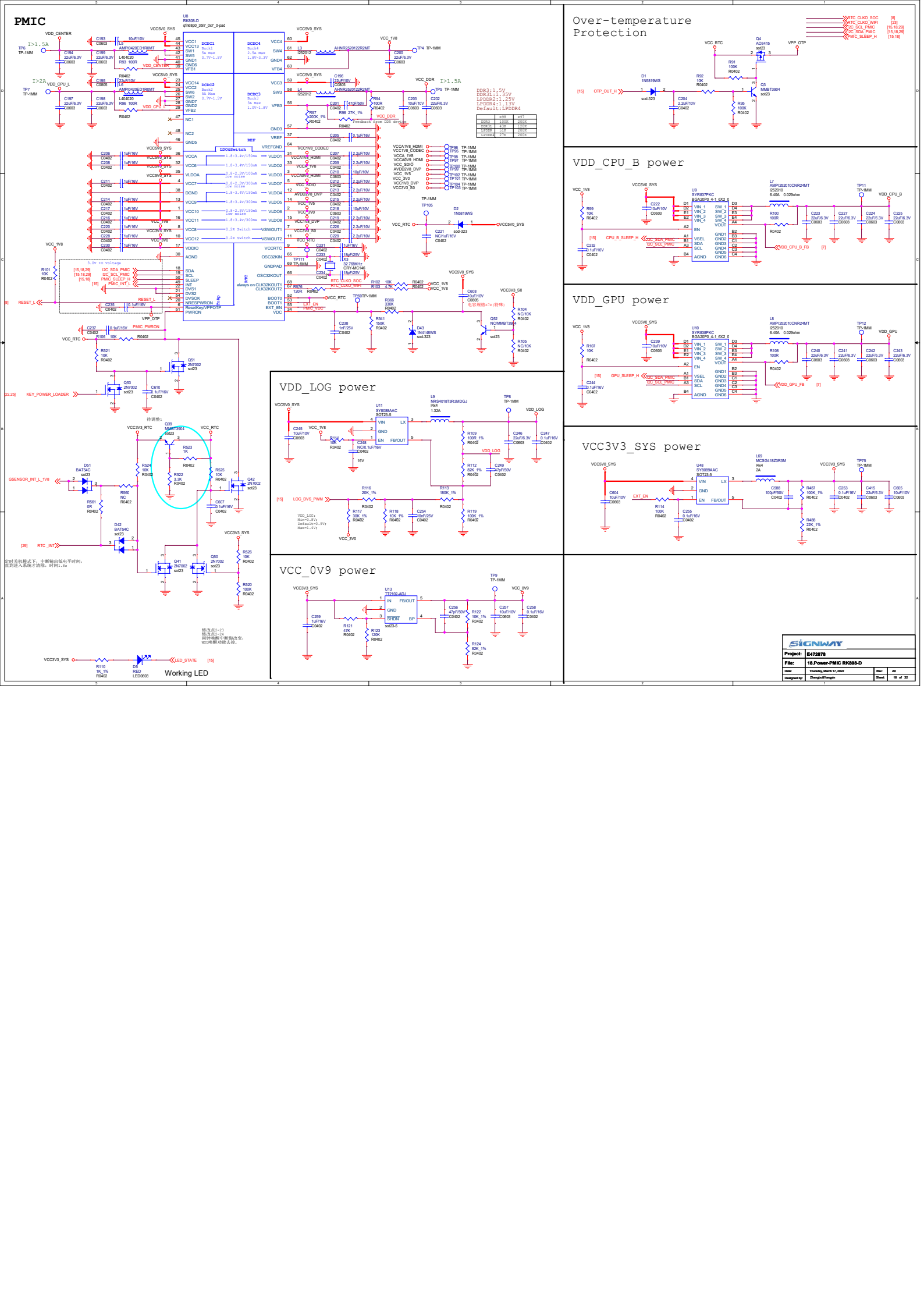




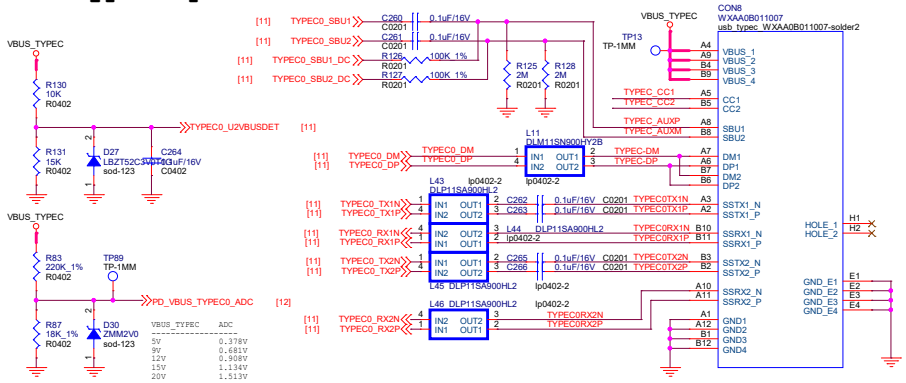




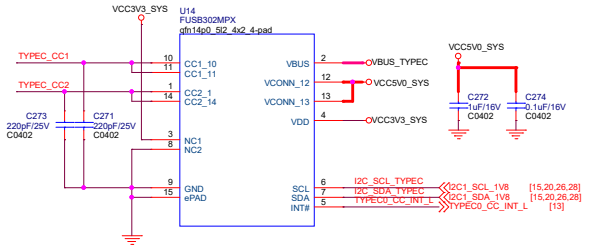
SIGNWAY	
Project:	E472878
File:	17.Power-DC IN&POWER SW
Date:	Tuesday, March 22, 2022
Rev:	A0
Designed by:	Zhanglbo&Yangyin
Sheet:	17 of 32


PMIC
U8
RK808-D
qfn68p0_3S7_0x7_0-pad
DCDC1
DCDC2
DCDC3
DCDC4
LDO&Switch
REF
I>1.5A
I>2A
VDD_CENTER
VDD_CPU_L
VCC5V0_SYS
VCC_1V8
VCC_DDR
VCC_RTC
VPP_OTP
PMIC_PWRON
RESET_L
KEY_POWER_LOADER
VDD_LOG
VDD_LOG power
VCC_0V9 power
Over-temperature Protection
VDD_CPU_B power
VDD_GPU power
VCC3V3_SYS power
Working LED
DDR3:1.5V
DDR3L:1.35V
LPDDR2:1.25V
LPDDR4:1.13V
Default:LPDDR4
Feedback from DDR device
待调整:
修改点2-23
修改点2-24
两种唤醒中断固改变,
vcc电源功能去除,
实时关机模式下，中断输出低电平时间，
直到进入系统才清除，时间1.ms
Project: E472878
File: 18.Power-PMIC RK808-D
Designed by: ZhangkaiXiangyin
Sheet 18 of 32

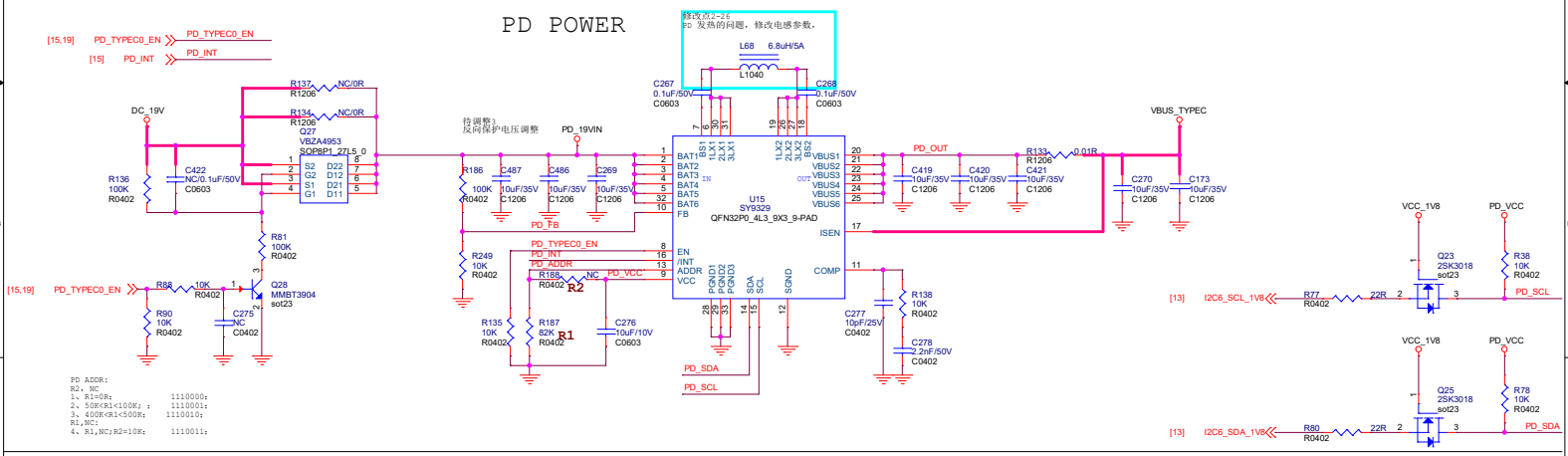
USB Type-C port



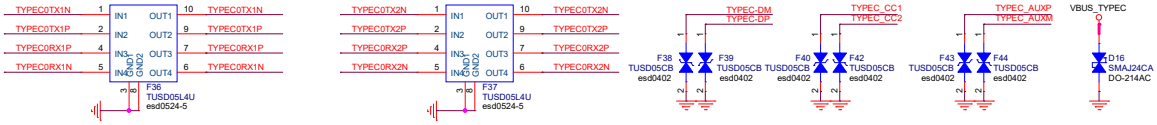
CC CTRL



PD POWER



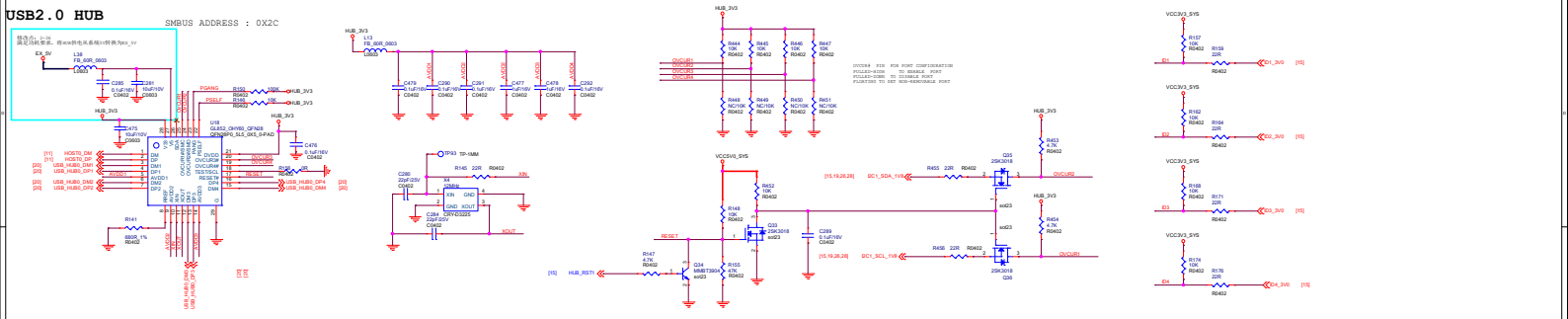
ESD



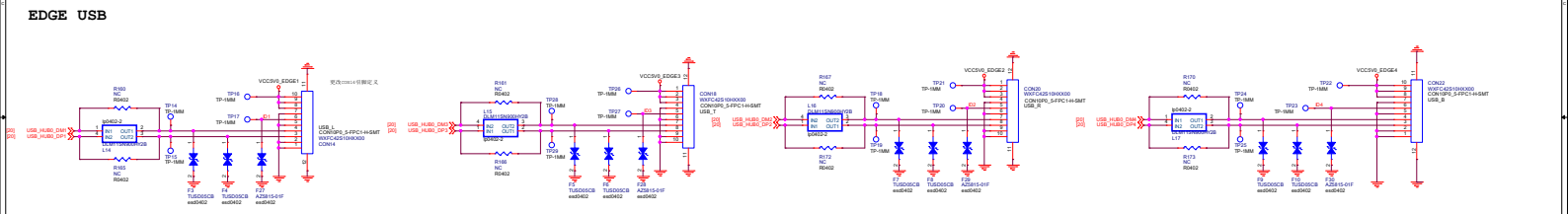
Project:	E472878
File:	19.TYPE-C
Date:	Thursday, March 17, 2022
Rev:	A0
Designed by:	Zhanglbo&Yangyin
Sheet:	19 of 32

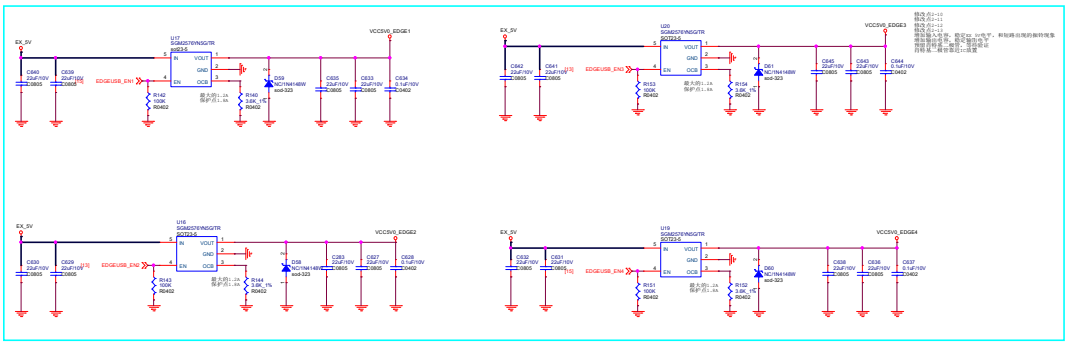
USB2.0 HUB

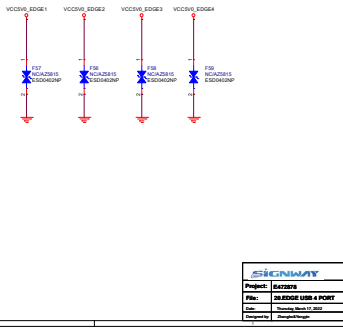
SMBUS ADDRESS : 0X2C



EDGE USB

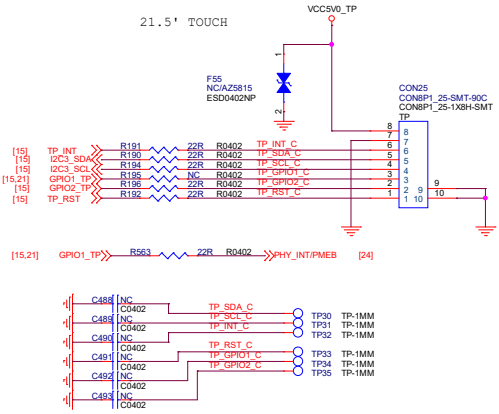




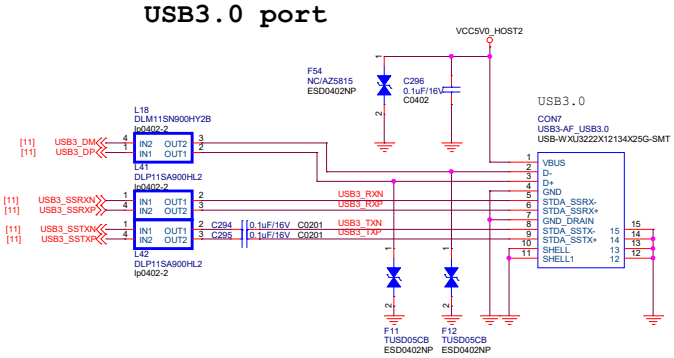


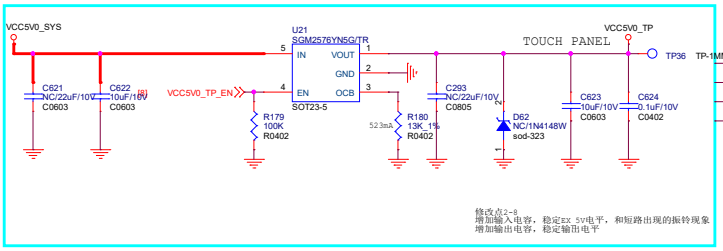
Project:	E472978
File:	39.EDGE USB 4 PORT
Date:	Thursday, March 17, 2022
Rev:	A0
Designed by:	ZhangHuiYongjie
Sheet:	39 of 39

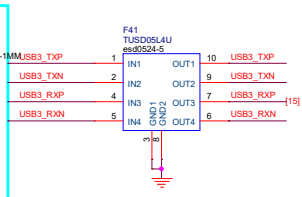
Touch Panel

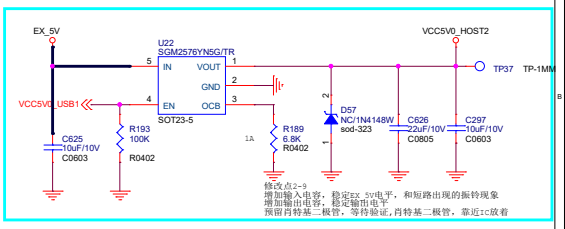


USB3.0 port



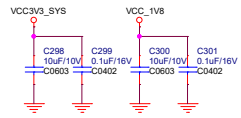






SIGNWAY	
Project:	E472878
File:	21.USB 3.0HOST &TP
Date:	Thursday, March 17, 2022
Rev:	A0
Designed by:	Zhangbo&Yangyin
Sheet:	21 of 32

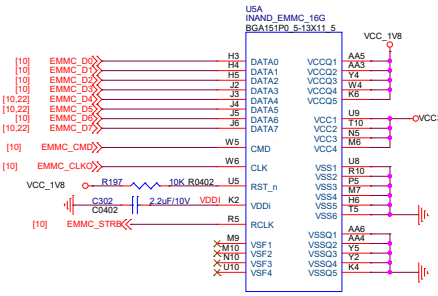
eMMC FLASH

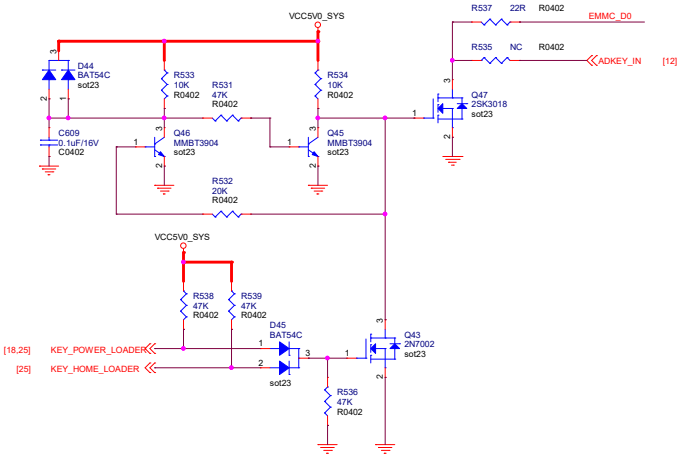


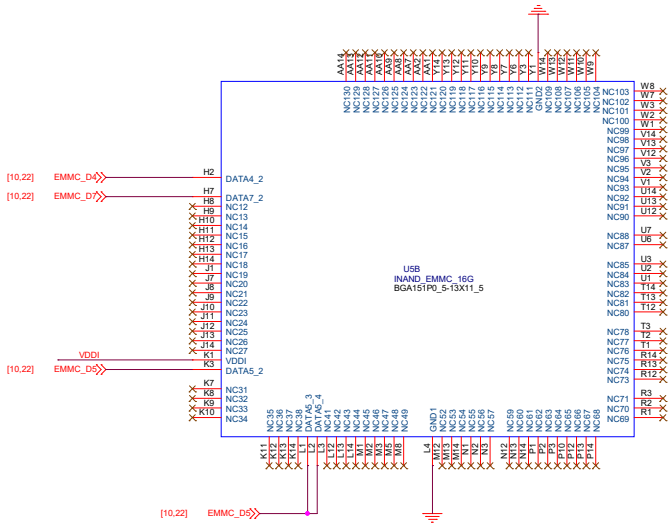
Note:All the Power filter capacitors should be placed close to the power pins of eMMC

Note:
Reserve TestPoint for firmware update.
If EMMC_CLKO=0V at power-on reset,
then system will enter into Maskrom mode.

EMMC_D0 TP2 TP-1MM
TP3 TP-1MM



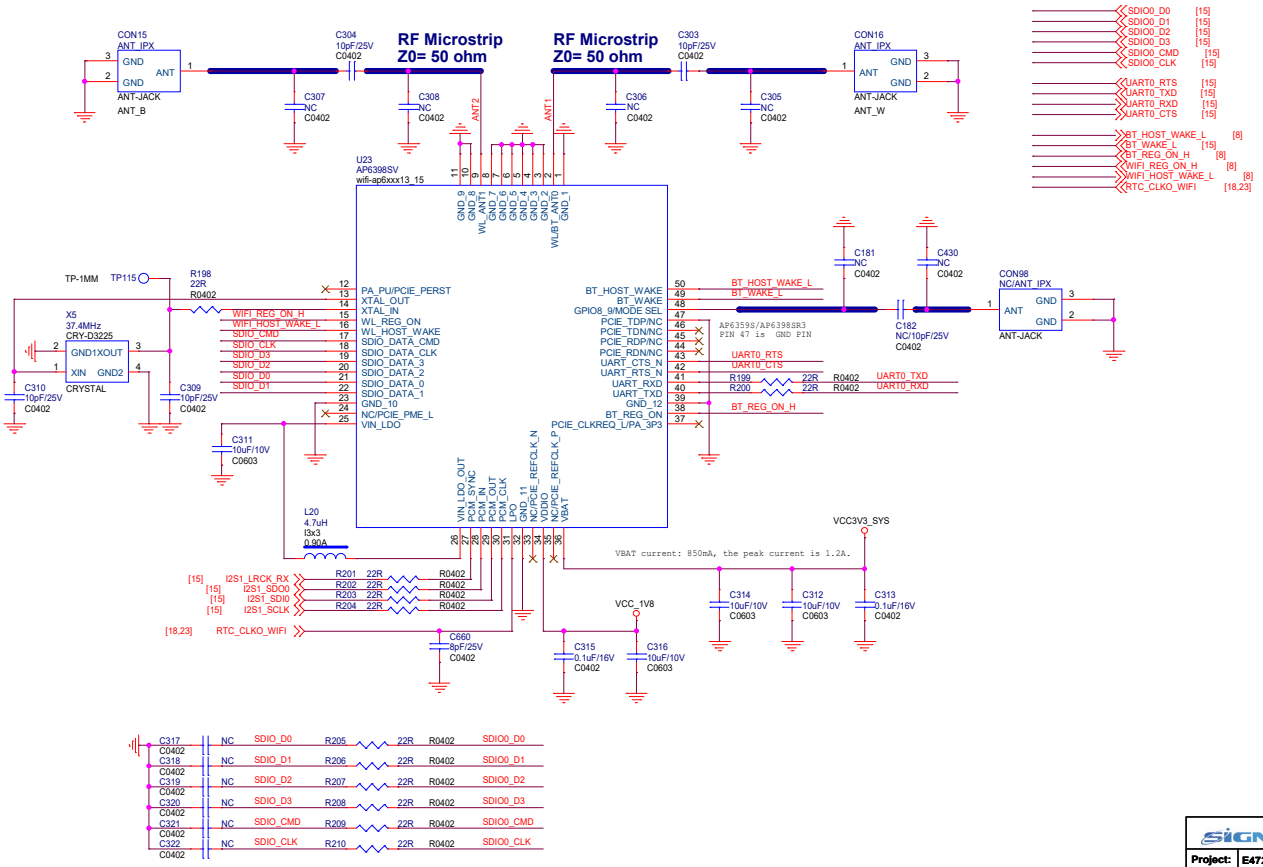




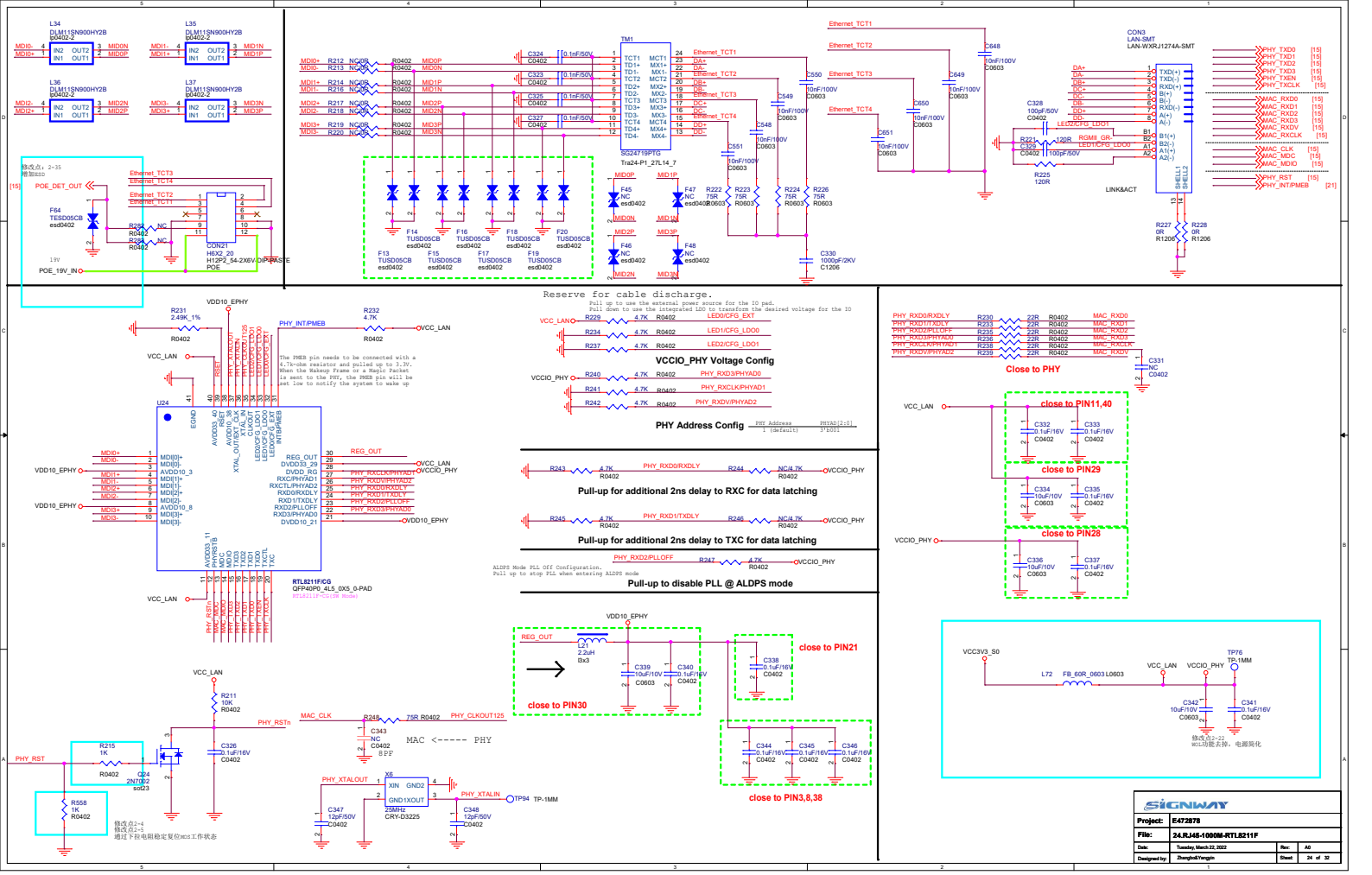
SIGNWAY			
Project:	E472878		
File:	22.Memory-eMMC		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	Zhanglbo&Yangyin	Sheet:	22 of 32

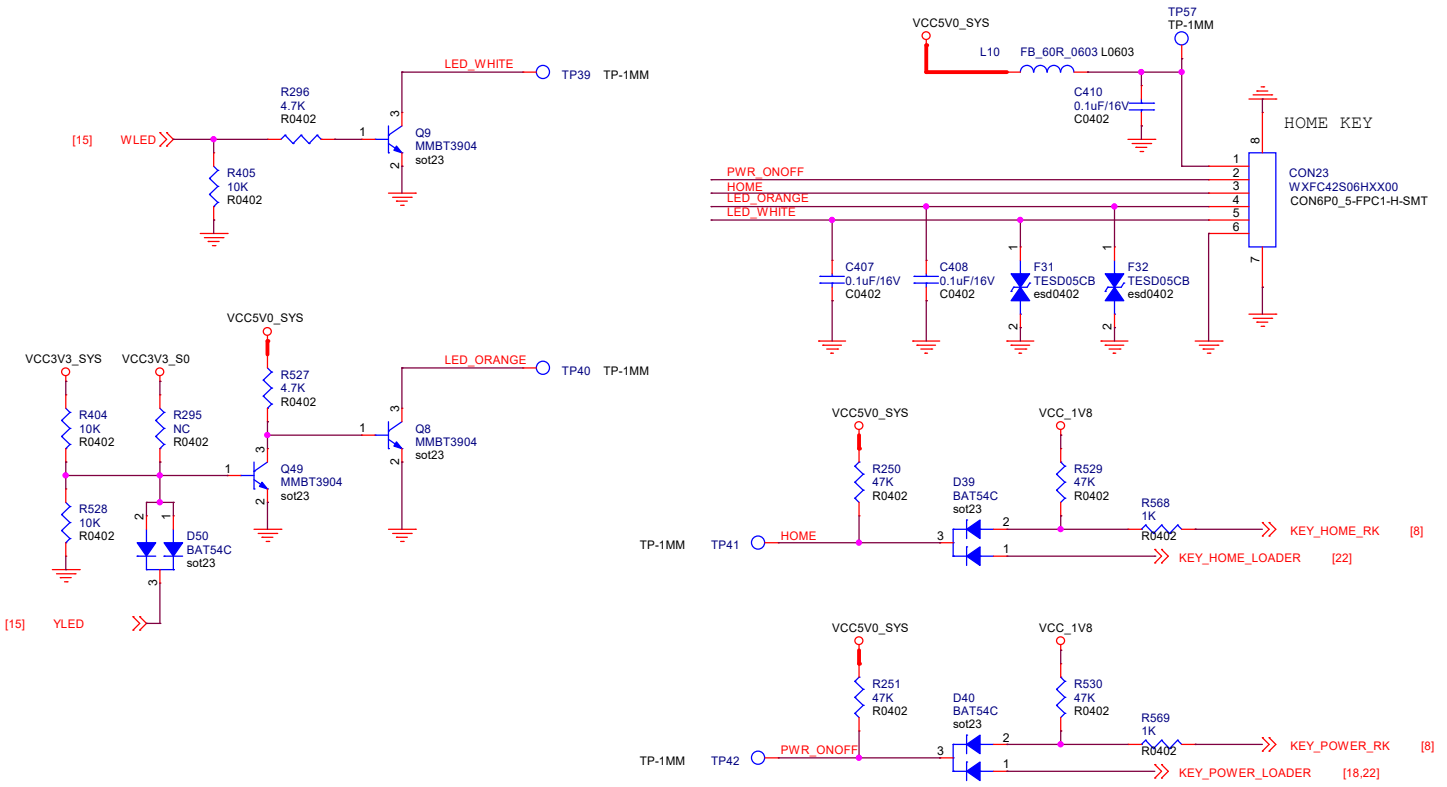
SDIO WIFI/BT MODULE-MIMO

Note:VBAT power supply range is 3.0V~4.8V.

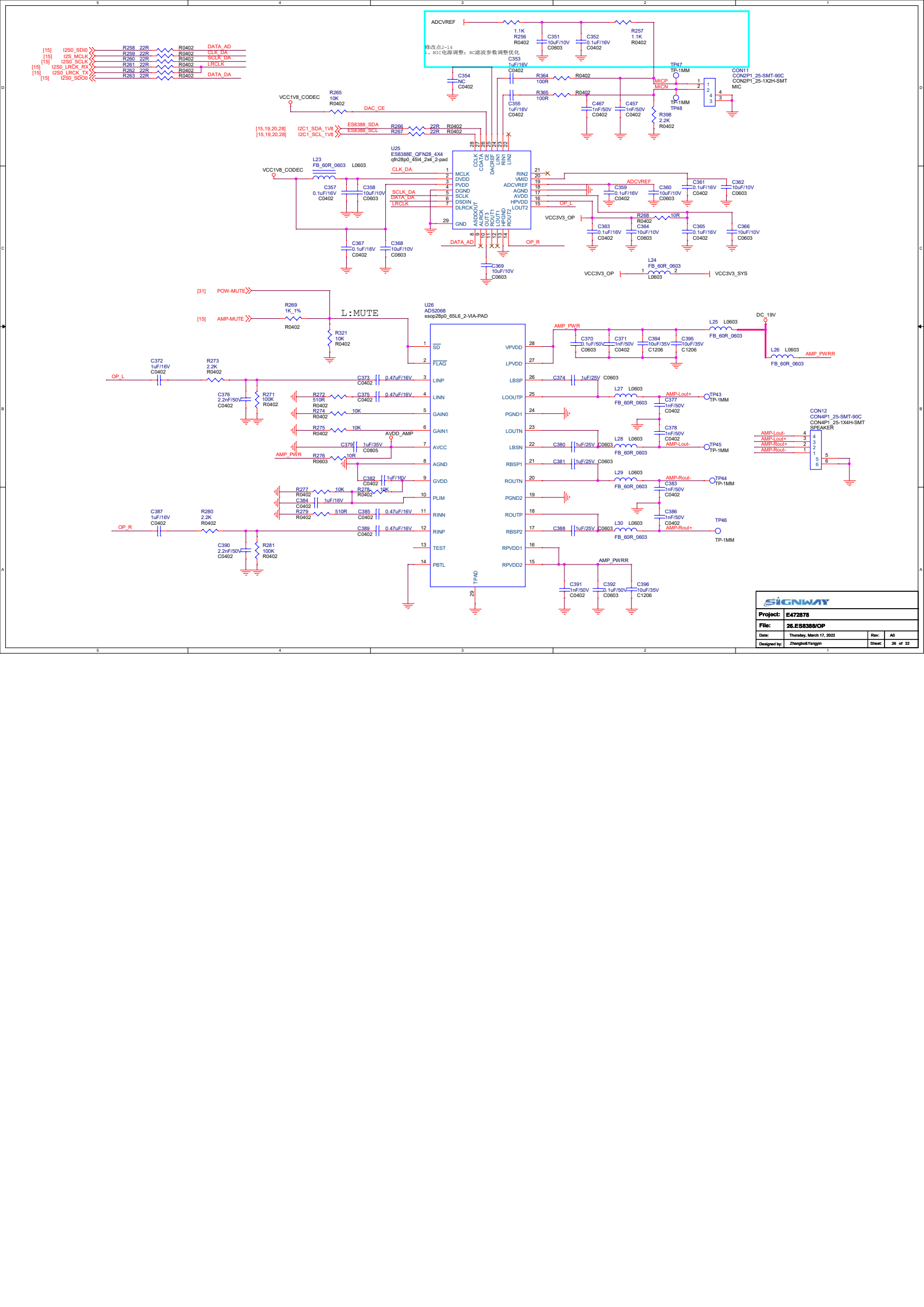


SIGNWAY	
Project:	E472878
File:	23.WIFI/BT-AP6398SV
Date:	Thursday, March 17, 2022
Rev:	A0
Designed by:	Zhanghb&Yangyin
Sheet	23 of 32


L34 DLM11SN900HY2B b0402-2
L35 DLM11SN900HY2B b0402-2
L36 DLM11SN900HY2B b0402-2
L37 DLM11SN900HY2B b0402-2
TM1
Tra24-P1_27L14_7
SG24719PTG
CON3 LAN-SMT LAN-WXRJ1274A-SMT
CON21 H6X2_20 H12P2_54-2X6V_DIP-PASTE
POE
Ethernet_TCT1
Ethernet_TCT2
Ethernet_TCT3
Ethernet_TCT4
LINK&ACT
Reserve for cable discharge.
Pull up to use the external power source for the IO pad.
Pull down to use the integrated LDO to transform the desired voltage for the IO
VCCIO_PHY Voltage Config
PHY Address Config
Pull-up for additional 2ns delay to RXC for data latching
Pull-up for additional 2ns delay to TXC for data latching
Pull-up to disable PLL @ ALDPS mode
ALDPS Mode PLL Off Configuration.
Pull up to stop PLL when entering ALDPS mode
U24
RTL8211F/CG
QFP40P0_4L5_0X5_0-PAD
Close to PHY
close to PIN11,40
close to PIN29
close to PIN28
close to PIN21
close to PIN30
close to PIN3,8,38
MAC <----- PHY
Project: E472878
File: 24.RJ45-1000M-RTL8211F
Date: Tuesday, March 22, 2022
Rev: A0
Designed by: Zhanghuifangjin
Sheet: 24 of 32

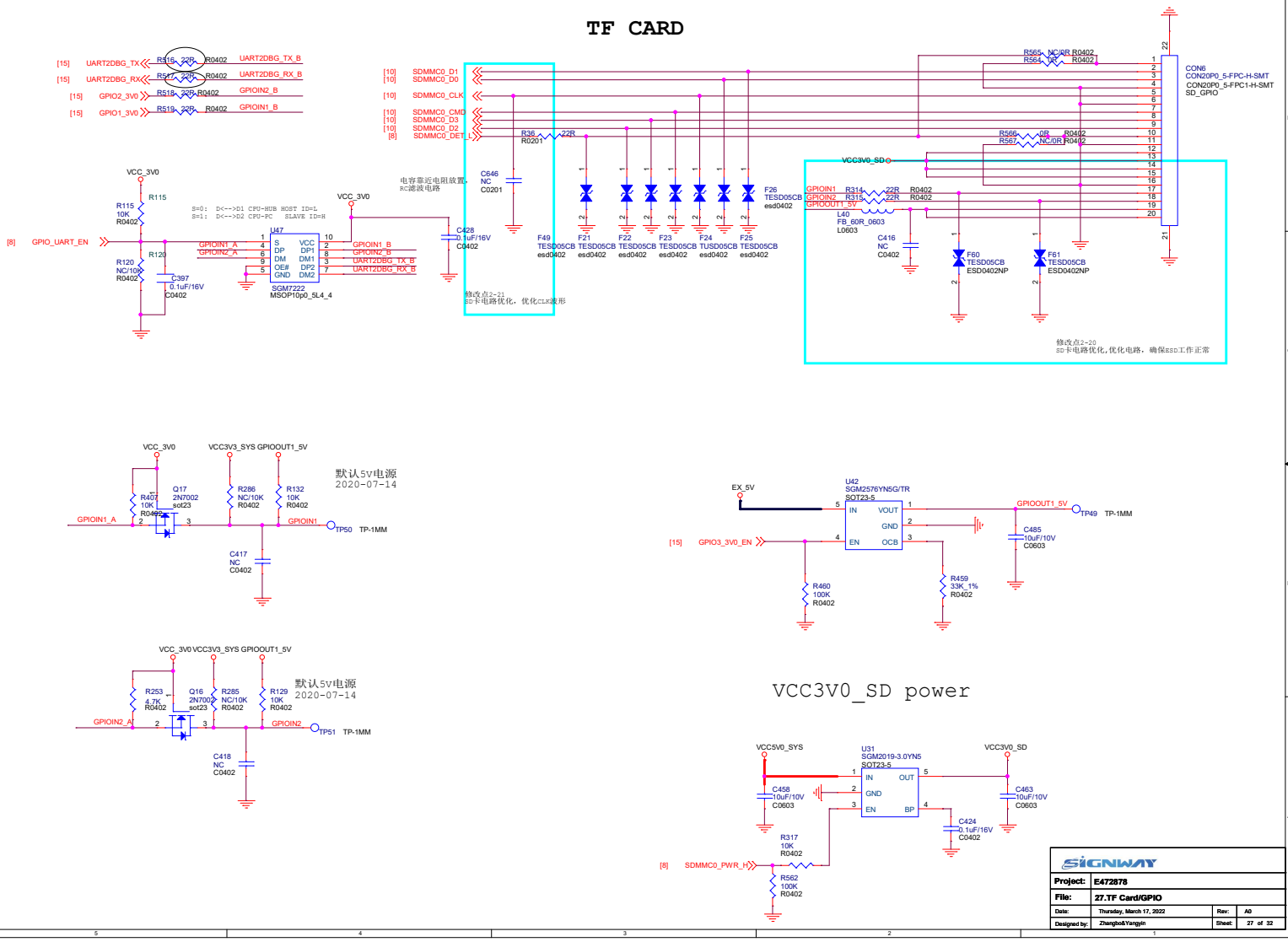


SIGNWAY	
Project:	E472878
File:	25.LED/KEY
Date:	Thursday, March 17, 2022
Rev:	A0
Designed by:	Zhangbo&Yangyin
Sheet:	25 of 32



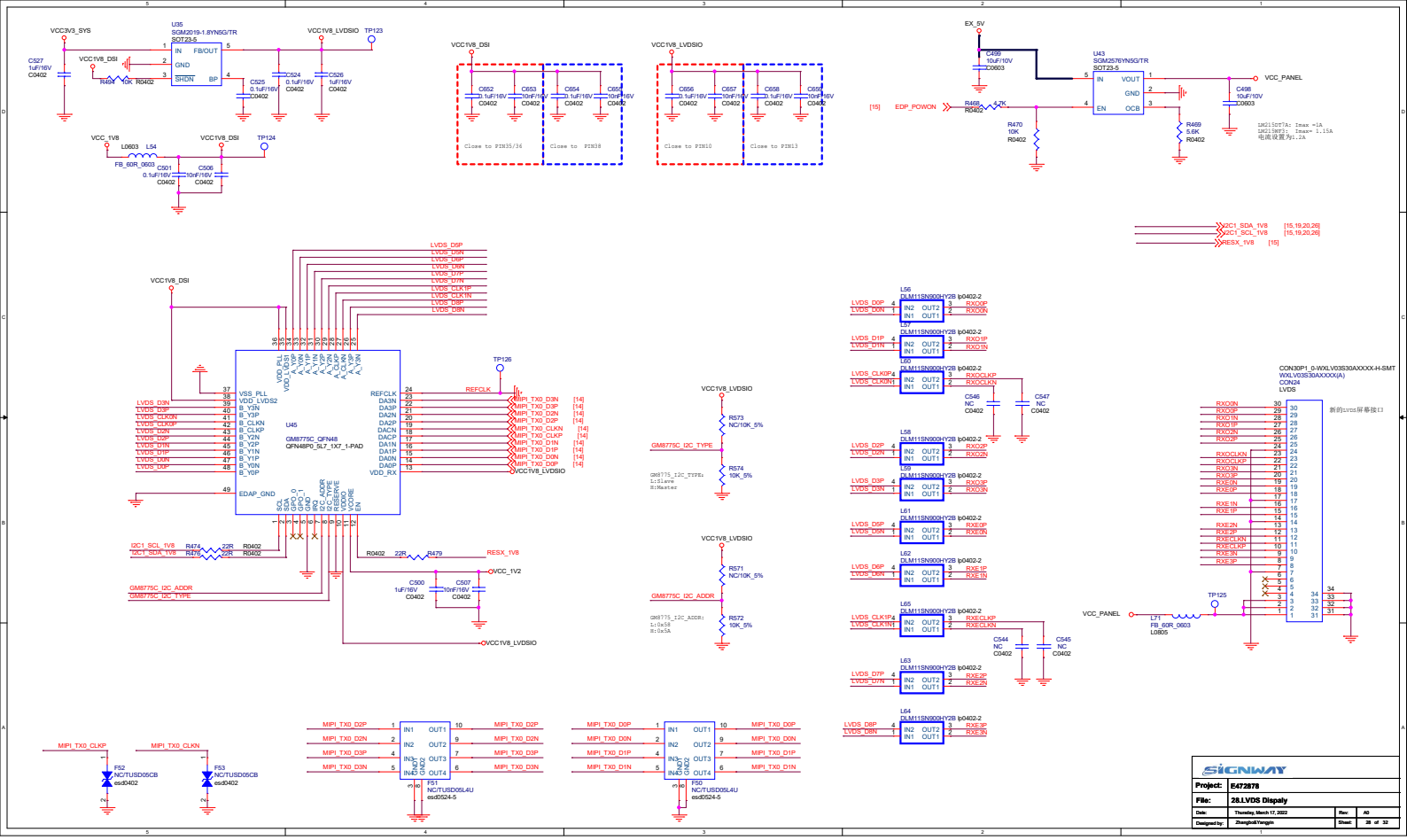
Project:	E472878
File:	26.ES8388/OP
Date:	Thursday, March 17, 2022
Rev:	A0
Designed by:	Zhangbo&Yangyin
Sheet:	26 of 32

TF CARD



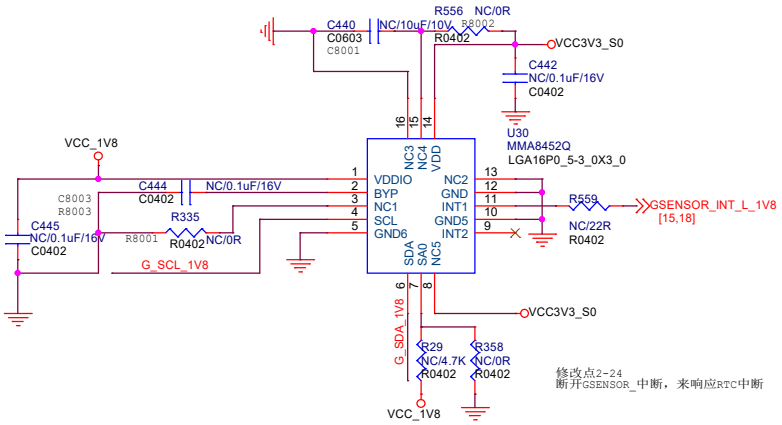
VCC3V0_SD power

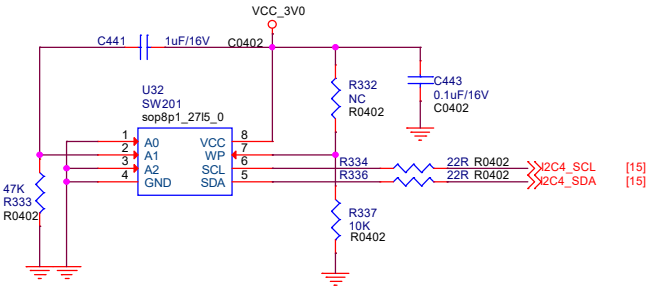
Project:	E472878
File:	27.TF Card/GPIO
Date:	Thursday, March 17, 2022
Rev:	A0
Designed by:	Zhanglbo&Yangyin
Sheet:	27 of 32

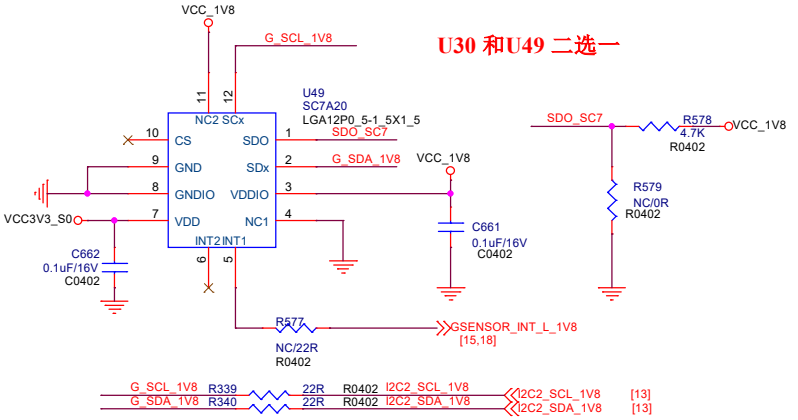

VCC3V3_SYS
U35
SGM2019-1.8YN5G/TR
SOT23-5
VCC1V8_LVDSIO
TP123
VCC1V8_DSI
C527
1uF/16V
C0402
R469 10K R0402
C525
0.1uF/16V
C0402
C524
0.1uF/16V
C0402
C526
1uF/16V
C0402
VCC1V8_DSI
C552
1uF/16V
C0402
C553
10nF/16V
C0402
C554
1uF/16V
C0402
C555
10nF/16V
C0402
Close to PIN35/36
Close to PIN38
VCC1V8_LVDSIO
C556
1uF/16V
C0402
C557
10nF/16V
C0402
C558
1uF/16V
C0402
C559
10nF/16V
C0402
Close to PIN10
Close to PIN13
EX_5V
C499
10uF/10V
C0603
U43
SGM2578YN5G/TR
SOT23-5
VCC_PANEL
C498
10uF/10V
C0603
[15] EDP_POWON
R468
R0402
4.7K
R470
10K
R0402
R469
5.6K
R0402
IN2:SOT7A: Imax =1A
IN2:SOT5: Imax= 1.15A
电流设置为1.2A
VCC1V8_DSI
VCC1V8_LVDSIO
TP124
L0603
L54
FB_60R_0603
C501
0.1uF/16V
C0402
C506
10nF/16V
C0402
I2C1_SDA_1V8 [15,19,20,26]
I2C1_SCL_1V8 [15,19,20,26]
RESX_1V8 [15]
LVDS_D5P
LVDS_D5N
LVDS_D6P
LVDS_D6N
LVDS_D7P
LVDS_D7N
LVDS_CLK1P
LVDS_CLK1N
LVDS_D8P
LVDS_D8N
VCC1V8_DSI
U45
GM8775C_QFN48
QFN48P0_5L7_1X7_1-PAD
VSS_PLL
VDD_LVDS2
B_Y3N
B_Y3P
B_CLKN
B_CLKP
B_Y2N
B_Y2P
B_Y1N
B_Y1P
B_Y0N
B_Y0P
EDAP_GND
REFCLK
DA3N
DA3P
DA2N
DA2P
DACN
DACP
DA1N
DA1P
DA0N
DA0P
VDD_RX
TP126
REFCLK
MIPI_TX0_D3N [14]
MIPI_TX0_D3P [14]
MIPI_TX0_D2N [14]
MIPI_TX0_D2P [14]
MIPI_TX0_CLKN [14]
MIPI_TX0_CLKP [14]
MIPI_TX0_D1N [14]
MIPI_TX0_D1P [14]
MIPI_TX0_D0N [14]
MIPI_TX0_D0P [14]
VCC1V8_LVDSIO
I2C1_SCL_1V8
I2C1_SDA_1V8
R474 22R R0402
R476 22R R0402
R0402 22R R479
RESX_1V8
VCC_1V2
C500
1uF/16V
C0402
C507
10nF/16V
C0402
GM8775C_I2C_ADDR
GM8775C_I2C_TYPE
VCC1V8_LVDSIO
R573
NC/10K_5%
R574
10K_5%
GM8775C_I2C_TYPE
GM8775_I2C_TYPE:
L:Slave
H:Master
VCC1V8_LVDSIO
R571
NC/10K_5%
R572
10K_5%
GM8775C_I2C_ADDR
GM8775_I2C_ADDR:
L:0x58
H:0x5A
L56
DLM11SN900HY2B
L57
DLM11SN900HY2B
L60
DLM11SN900HY2B
L58
DLM11SN900HY2B
L59
DLM11SN900HY2B
L61
DLM11SN900HY2B
L62
DLM11SN900HY2B
L65
DLM11SN900HY2B
L63
DLM11SN900HY2B
L64
DLM11SN900HY2B
LVDS_D0P
LVDS_D0N
LVDS_D1P
LVDS_D1N
LVDS_CLK0P
LVDS_CLK0N
LVDS_D2P
LVDS_D2N
LVDS_D3P
LVDS_D3N
LVDS_D5P
LVDS_D5N
LVDS_D6P
LVDS_D6N
LVDS_CLK1P
LVDS_CLK1N
LVDS_D7P
LVDS_D7N
LVDS_D8P
LVDS_D8N
RXO0P
RXO0N
RXO1P
RXO1N
RXO2P
RXO2N
RXO3P
RXO3N
RXE0P
RXE0N
RXE1P
RXE1N
RXE2P
RXE2N
RXE3P
RXE3N
RXOCLKP
RXOCLKN
RXECLKP
RXECLKN
C546
NC
C0402
C547
NC
C0402
C544
NC
C0402
C545
NC
C0402
CON30P1_0-WXLV03S30AXXXX-H-SMT
W0XLV03S30AXXXX(A)
CON24
LVDS
新的LVDS屏幕接口
TP125
VCC_PANEL
L71
FB_60R_0603
L0805
MIPI_TX0_CLKP
MIPI_TX0_CLKN
F52
NC/TUSD05CB
esd0402
F53
NC/TUSD05CB
esd0402
MIPI_TX0_D2P
MIPI_TX0_D2N
MIPI_TX0_D3P
MIPI_TX0_D3N
F51
NC/TUSD05L4U
esd0524-5
MIPI_TX0_D0P
MIPI_TX0_D0N
MIPI_TX0_D1P
MIPI_TX0_D1N
F50
NC/TUSD05L4U
esd0524-5
SIGNWAY
Project: E472878
File: 28.LVDS Dispaly
Date: Thursday, March 17, 2022
Rev: A0
Designed by: ZhangboWYangjin
Sheet: 28 of 32

	LIS3DH	MMA8452Q	LSM303D
C8001	NC	NC	4.7uF
R8002	0ohm	NC	NC
R8001	NC	0ohm	NC
C8003	NC	0.1uF	0.22uF
R8003	NC	NC	0R
R8004	NC	NC	0R

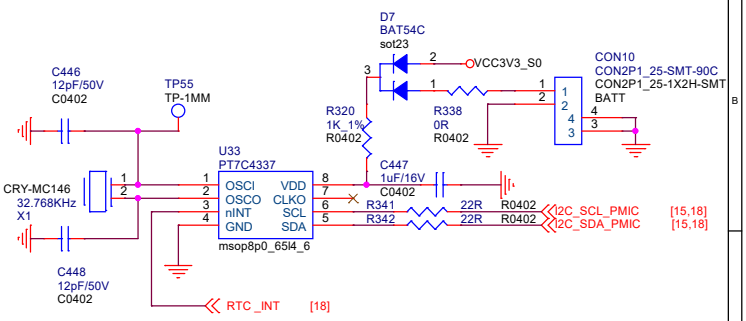
The MMA8452Q's standard slave address is a choice between the two sequential addresses 0011100 and 0011101. The selection is made by the high and low logic level of the SA0 (pin 7) input respectively. The slave addresses are factory programmed and alternate addresses are available at customer request



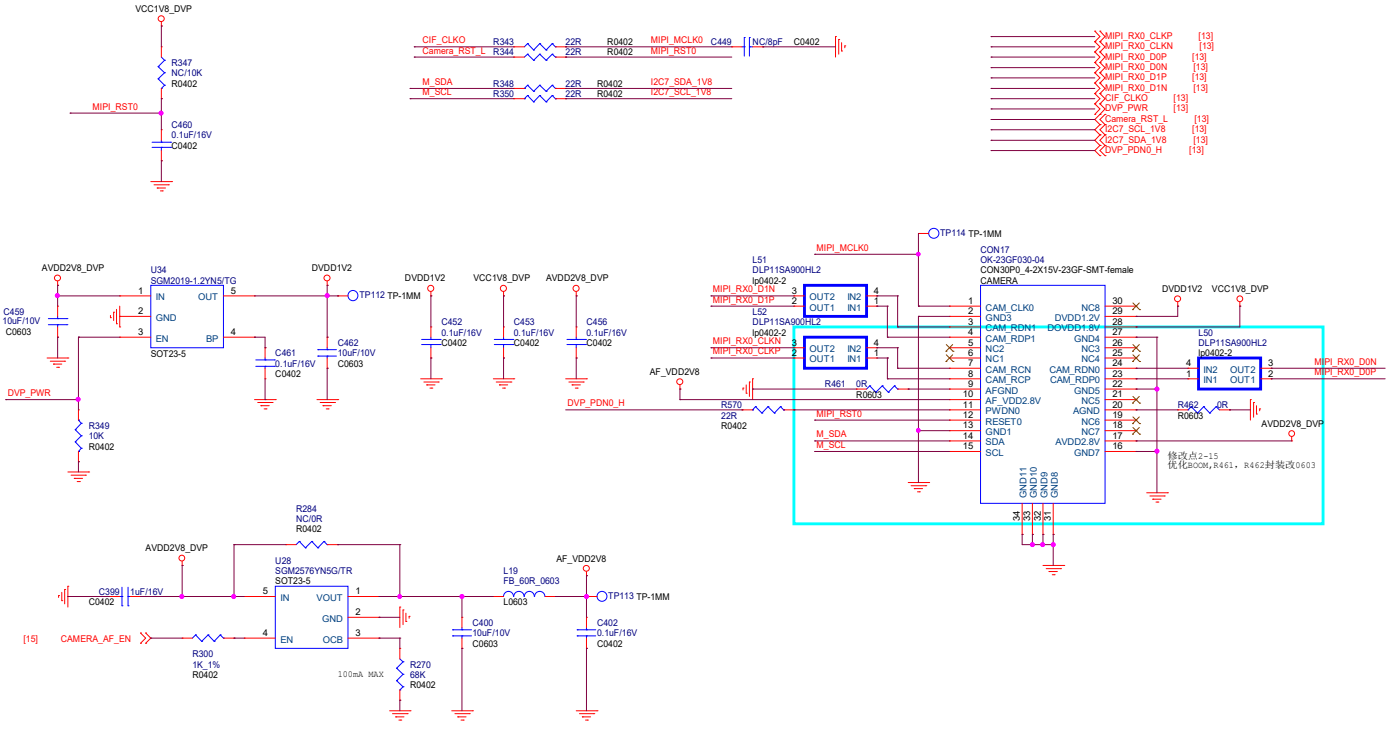




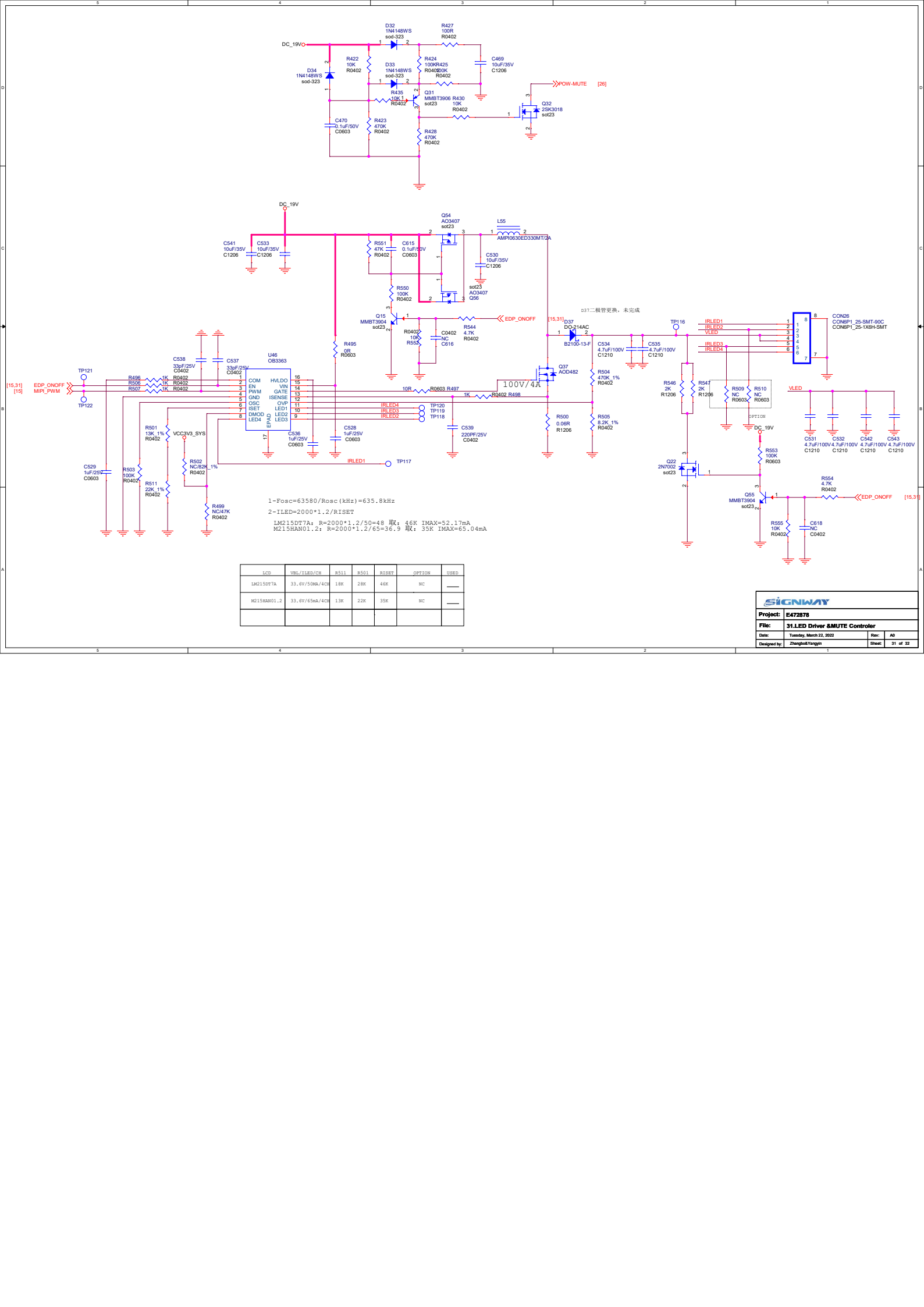
U30 和U49 二选一



SIGNWAY			
Project:	E472878		
File:	29.G-sensor&RTC		
Date:	Tuesday, March 22, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	29 of 32



SIGNWAY			
Project:	E472878		
File:	30.MIPI IN		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	Zhanghb&Yangyin	Sheet:	30 of 32

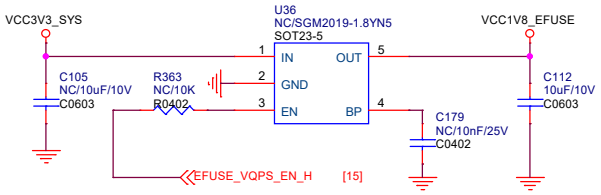


LCD	VBL/ILED/CH	R511	R501	RISET	OPTION	USED
LM215DT7A	33.6V/50MA/4CH	18K	28K	46K	NC	___
M215HAN01.2	33.6V/65mA/4CH	13K	22K	35K	NC	___

SIGNWAY	
Project:	E472878
File:	31.LED Driver &MUTE Controler
Date:	Tuesday, March 22, 2022
Rev:	A0
Designed by:	Zhanglbo&Yangyin
Sheet:	31 of 32

eFUSE

Note: For eFUSE programming, can be removed if do not use eFUSE。



SIGNWAY			
Project:	E472878		
File:	32.eFUSE		
Date:	Thursday, March 17, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	32 of 32