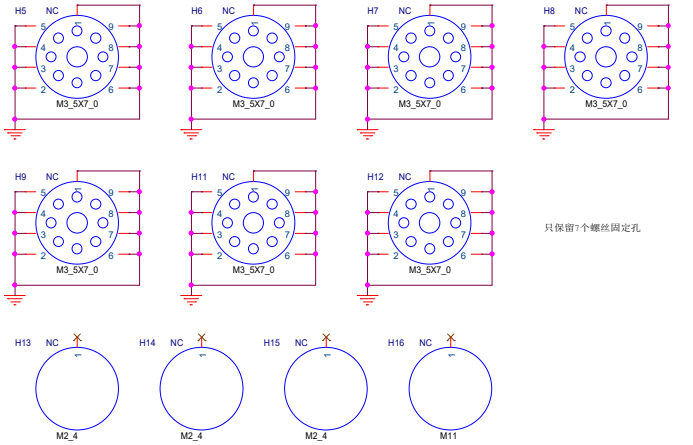
PCB MARK & LABEL

Heat Sink	
Optical Marks	T1 MARK T2 MARK T3 MARK T4 MARK T5 MARK T6 MARK
Label Outline	SN&MAC H1 20mm X 10mm Lot Number H2 10mm X 10mm
Silkcreen	PCB Name & Version ELO3399 (E679524) (USB-C) ELO3399 ENG Version A20xxx A20xxx SMT DIP ROHS
Mounting Hole	

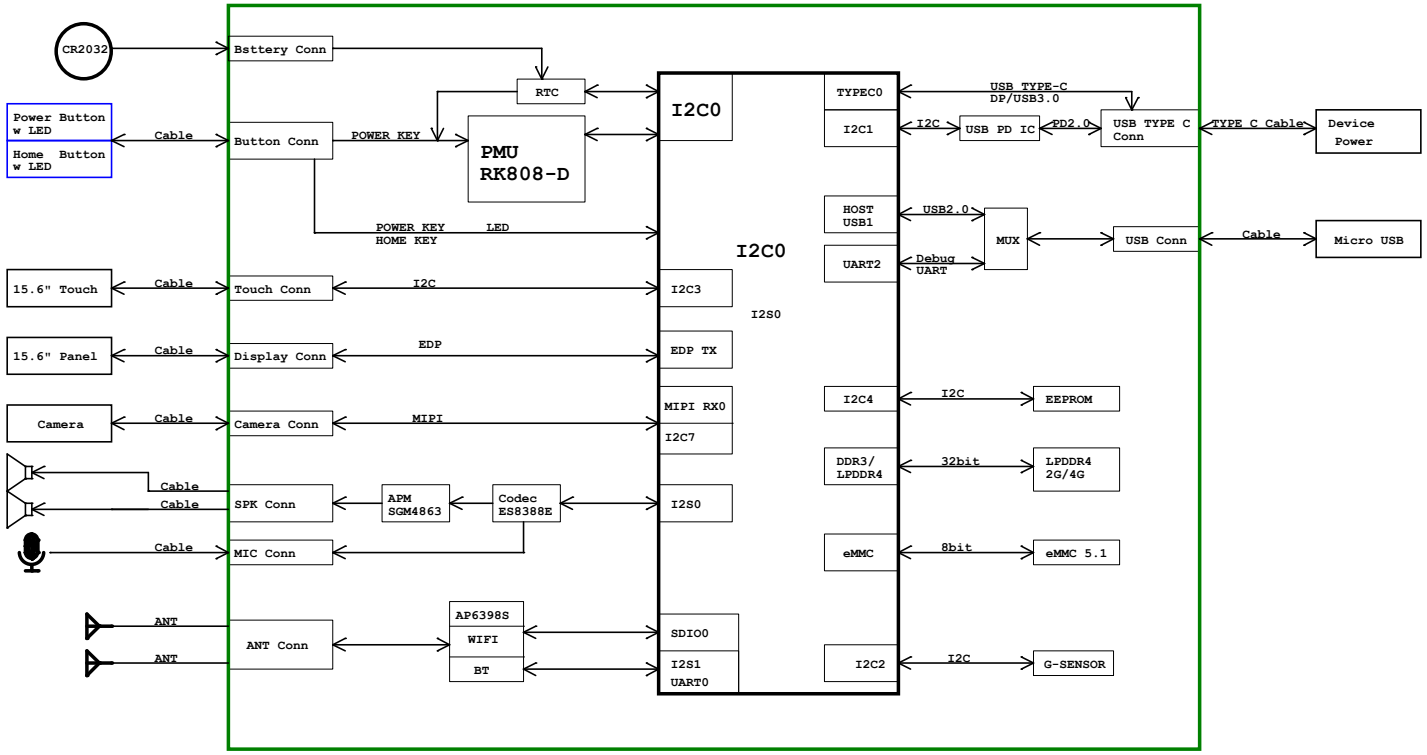
H5-H12: 螺丝固定孔;
H13-H15: 板卡定位柱固定孔，2.4mm直径的NPTH过孔
H16: 板卡定位柱固定孔，1mm直径的NPTH过孔

SIGNWAY			
Project:	E679524		
File:	01.Msc		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHangfubin	Sheet	1 of 32

Change List

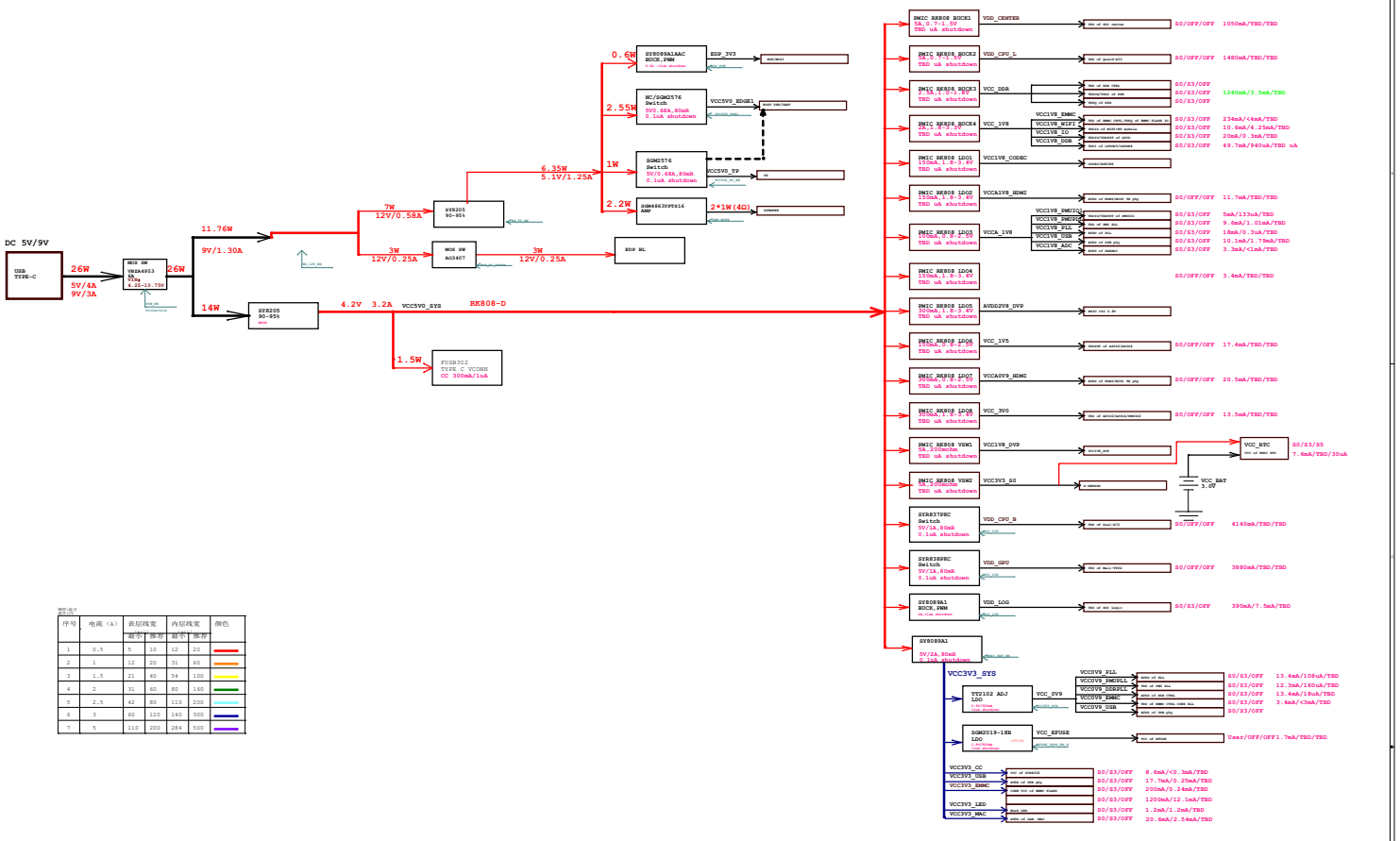
Version	Date	Author	Change Note	Approved
V0.5	August 02, 2020	ZHangliubin	First edition.	ZHangbo
V1.0	August 20, 2020	ZHangliubin	Adjust the power scheme.	ZHangbo
V1.1	August 27, 2020	ZHangliubin	Adjust the Panle power supply U35	ZHangbo
V1.2	September 2, 2020	ZHangliubin	Modify the Block Diagram	ZHangbo

SIGNWAY			
Project:	E679524		
File:	02.Change List		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHangliubin	Sheet:	2 of 32

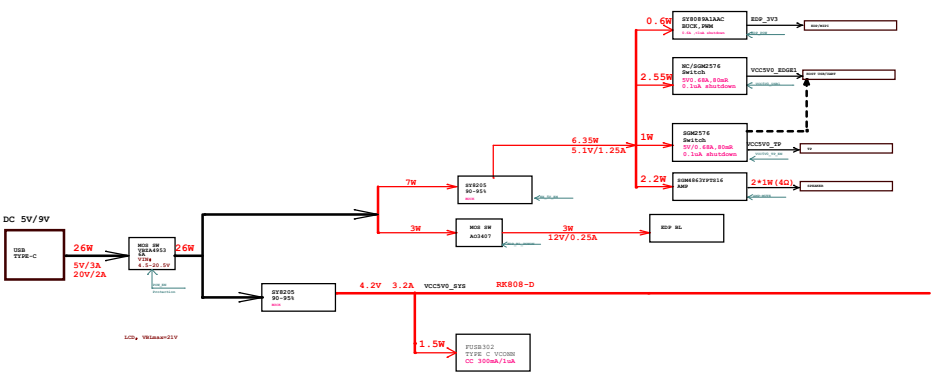


SIGNWAY

Project:	E678524
File:	03.Block Diagram
Date:	Monday, December 09, 2019
Designed by:	zhenghaiwu
Rev:	A0
Sheet:	3 of 32



序号	电流（A）	表层线宽		内层线宽		颜色
		敷铜	蒸发	敷铜	蒸发	
1	0.5	5	10	12	20	
2	1	12	20	31	60	
3	1.5	21	40	54	100	
4	2	31	60	80	140	
5	2.5	42	80	110	200	
6	3	60	120	140	300	
7	5	110	200	284	500	

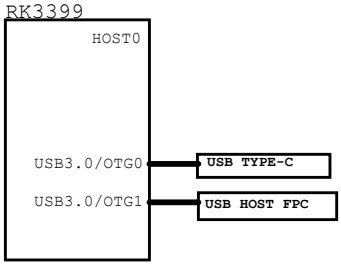


I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_3V0	Rockchip RK808	0x1b	PMIC	100kHz,400KHz
					SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
					PT7C4337	0xd0,0xd1	RTC	100kHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5	I2C1_SDA_1V8 I2C1_SCL_1V8	VCC_1V8	ES8388/1.8V	0x10,0x11	Audio codec	100kHz
					FUSB302MPX/1.8V	0x44,0x46	USB-TypeC Mux	100kHz
								100kHz
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2	I2C2_SDA_1V8 I2C2_SCL_1V8	VCC_1V8	MMA8452Q/1.8V	0x1D,0x1E	G-SENSOR	100kHz,400KHz,
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C3_SDA I2C3_SCL	VCC_3V0	TP/3.3V	TBD	TP TOUCH	100kHz,400KHz,3.4MHz
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C4_SDA I2C4_SCL	VCC_3V0	SW201/3.0V	0xA0 0xE0	EEPROM	10kHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	MAC USE					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2	I2C6_SDA_1V8 I2C6_SCL_1V8	VCC_1V8				20kHz
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2	I2C7_SDA_1V8 I2C7_SCL_1V8	VCC_1V8	MIPI_CSI /1.8V			100kHz

USB MAP

RK3399

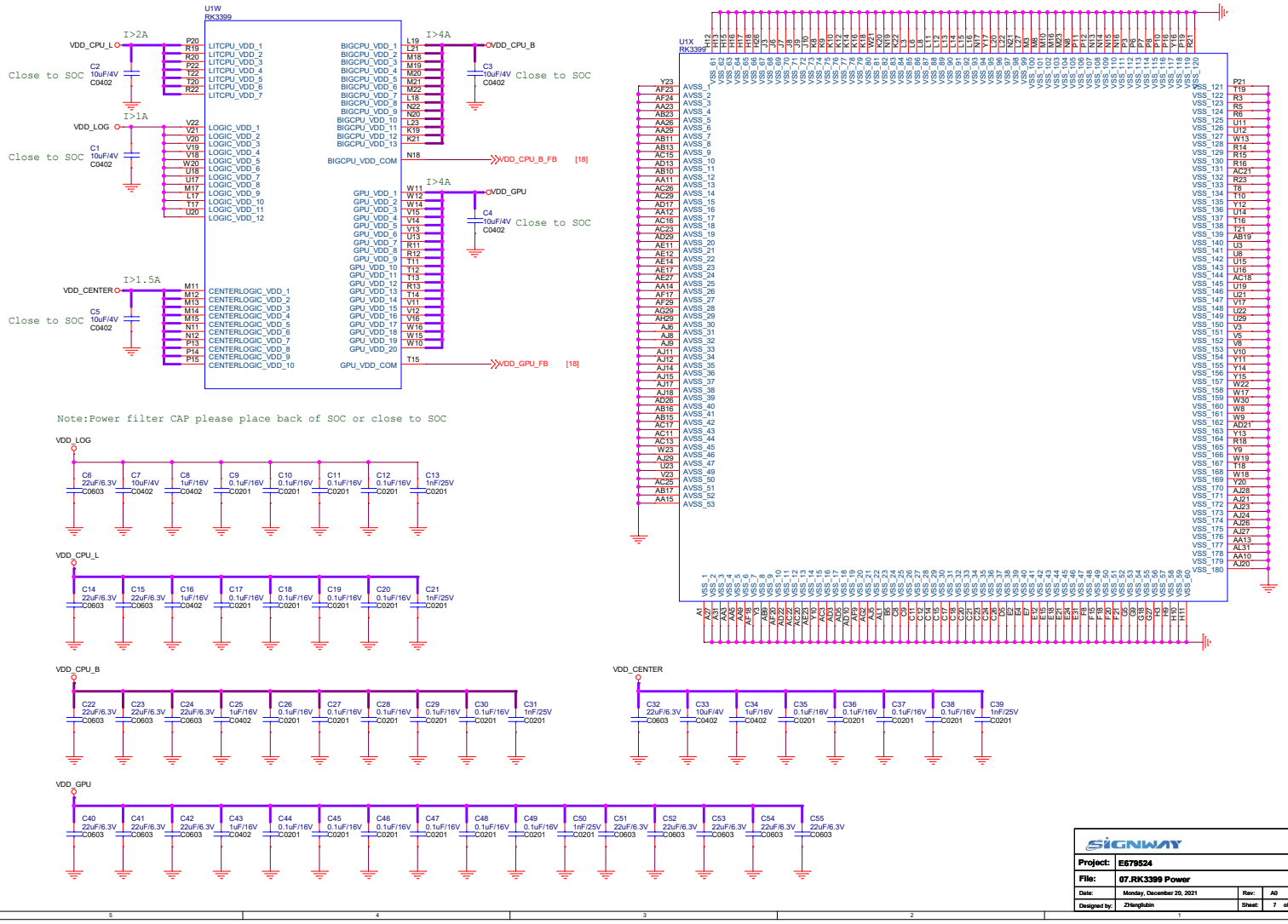


SIGNWAY	
Project:	E679524
File:	05.I2C&USB Map
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	ZHenglishin
Sheet	5 of 32

Power Domain Map

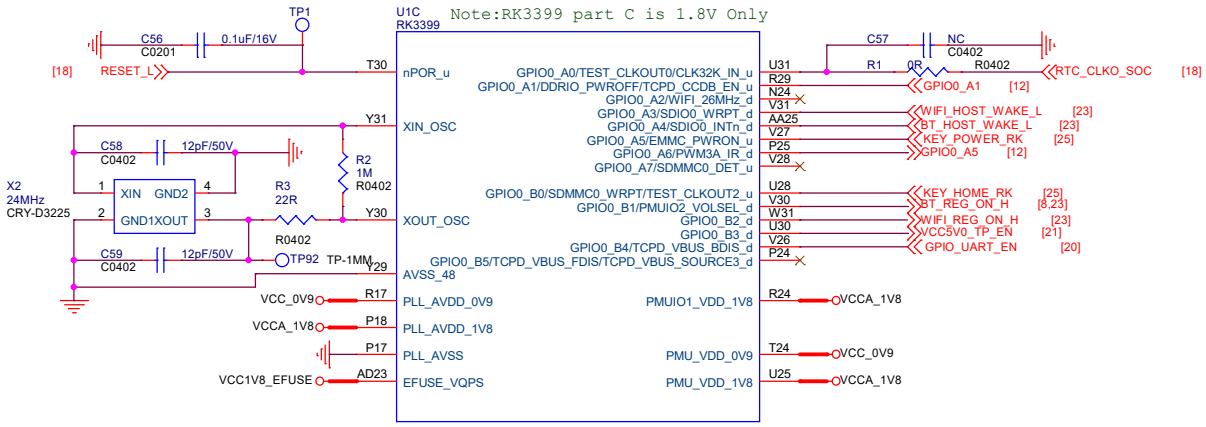
Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuio1_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLDO3
Part E	PMUIO2/PART E	pmu1830_gpio1abcd	3.0V	VCC_1V5	RK808-D Buck4 RK808-D VLDO6
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_LAN	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V	VCC_1V8	RK808-D VLDO3
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLDO6 RK808-D VLDO8
Part J	APIO5/PART J	audio_gpio3d_gpio4a	VCC1V8_CODEC	VCC1V8_CODEC	RK808-D VLDO1
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCC_SDIO	RK808-D VLDO4

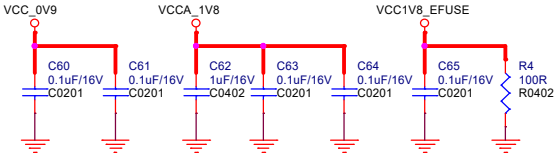
SIGNWAY			
Project:	E679524		
File:	06.Power Domain Map		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHangliubin	Sheet:	6 of 32

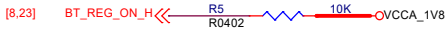


Note:Power filter CAP please place back of SOC or close to SOC

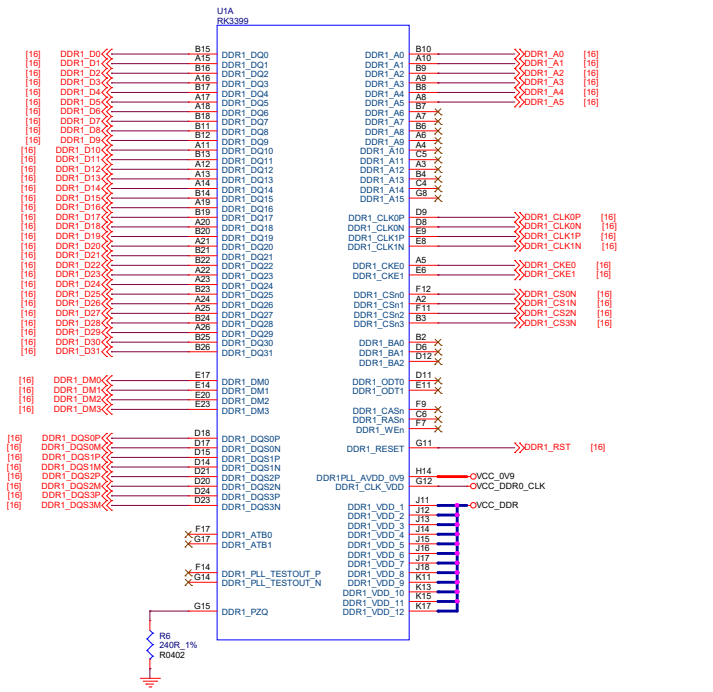
SIGNWAY	
Project:	E679524
File:	07.RK3399 Power
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	ZHenglishin
Sheet:	7 of 32

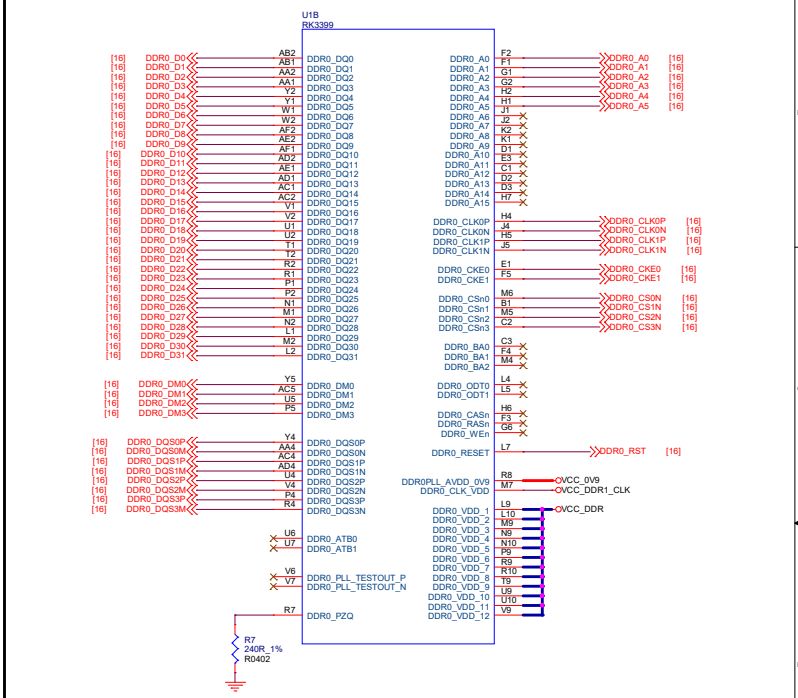




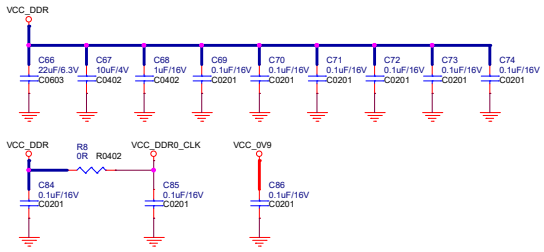


SIGNWAY	
Project:	E679524
File:	08.RK3399 PMU Controler
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	ZHangliubin
Sheet:	8 of 32

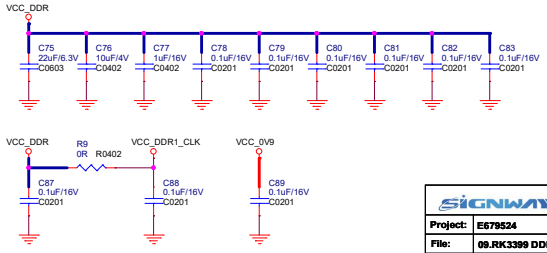




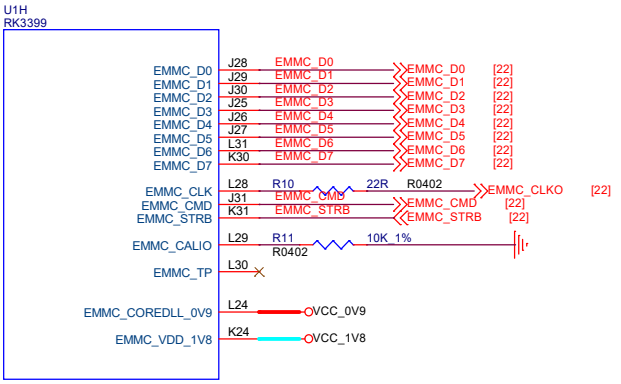
DDR FILTER Note:R10 cannot be deleted



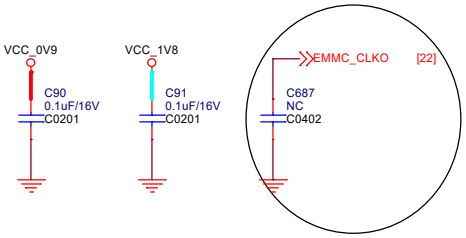
DDR FILTER Note:R11 cannot be deleted

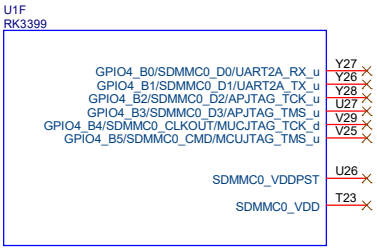


SIGNWAY	
Project:	E679524
File:	09.RK3399 DDR Controler
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	ZHenglishin
Sheet:	9 of 32



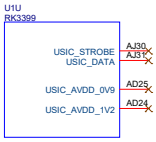
EMMC design rule:
1.Data[0:7], CMD and STRB signals routing parallel as a group, the skew between each other must be less than 100mils;
2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
3.Max trace length < 3.93 inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;
6.R11 close to SOC;



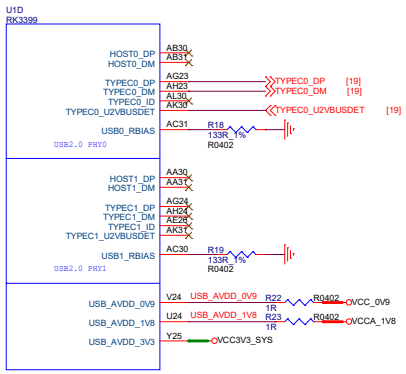


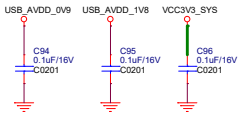
SDMMC design rule:
1.Data[0:7] and CMD signals routing parallel as a group, the skew between each other must be less than 100mils;
2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
3.Max trace length < 3.93 inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;

SIGNWAY			
Project:	E679524		
File:	10.RK3399 Flash&SDMMC Controler		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHangliubin	Sheet:	10 of 32



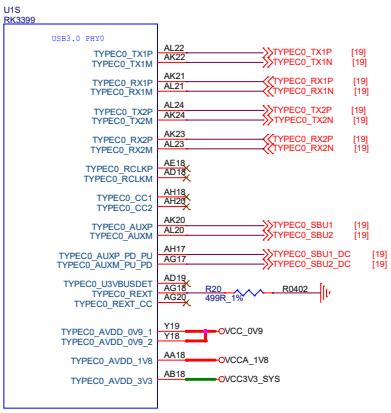
USB2.0

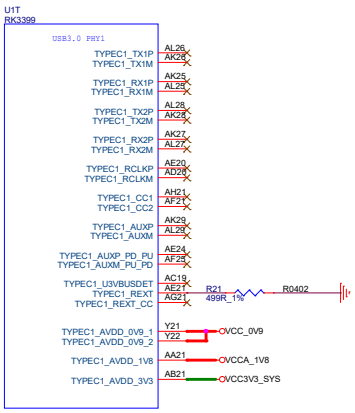


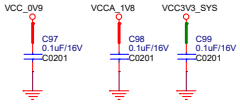


USB2.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals
follows the 3W rule;

USB3.0



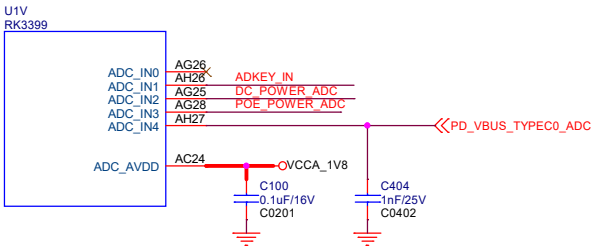




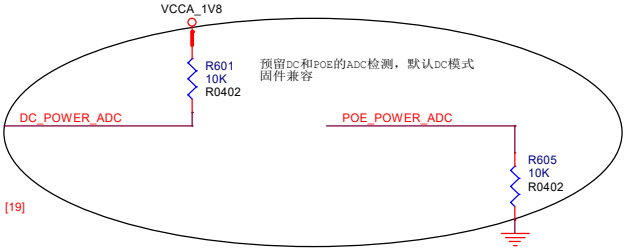
USB3.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between TX and
RX < 1.6 ns;
3.Max trace length < 6 inchs;
4.Max allowed via < 4;
5.Trace impedance 90ohm+/-10%;
6.The distance between other signals
follows the 3W rule;

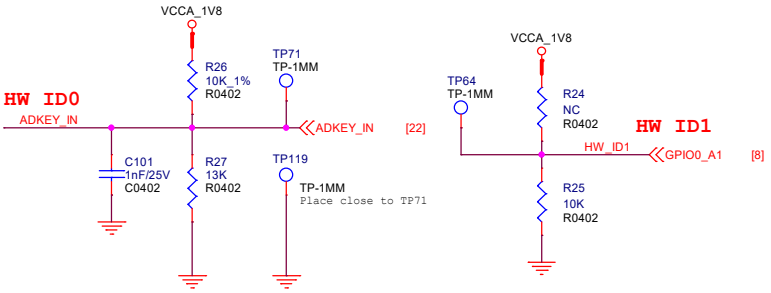
DP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals
follows the 3W rule;

SIGNWAY	
Project:	E679524
File:	11.RK3399 USB/USIC Controler
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	ZHenglishin
Sheet:	11 of 32

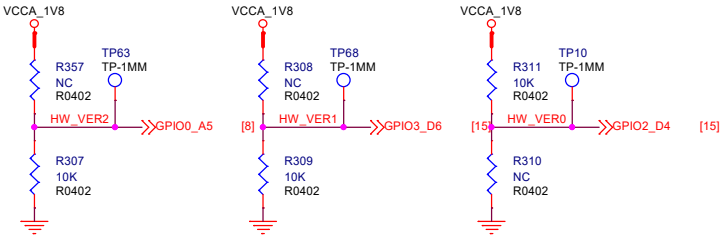


布线较长，预留电容，防止电压波动，
影响ADC检测的稳定性；
靠近CPU引脚放置
20200804





HW Version



RK3399 project hardware ID definiton

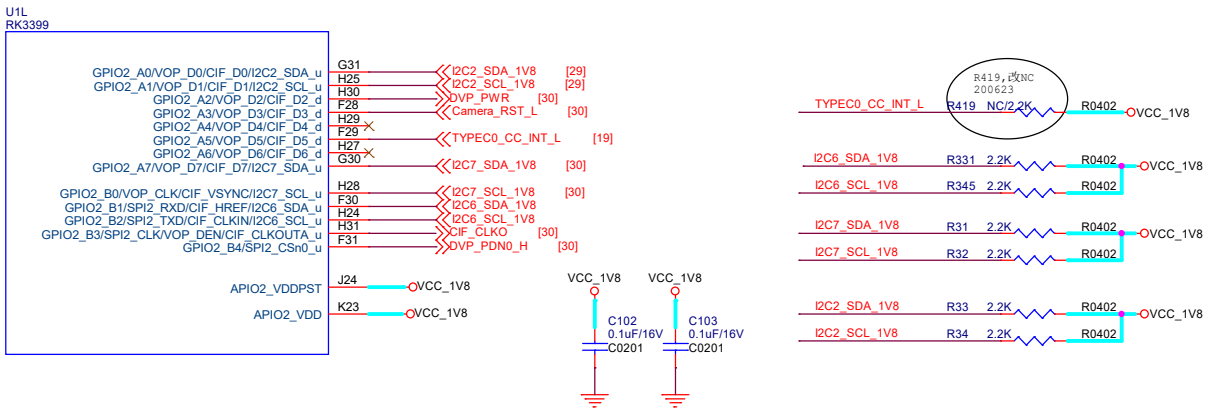
ADC1 Function1: Hold on ZERO when AC plug in cold boot, enter Flash Image Mode.
ADC1 Function2: Secondary defininiton of product hardware ID.
GPIO0_A1: Main definiton of of product hardware ID.

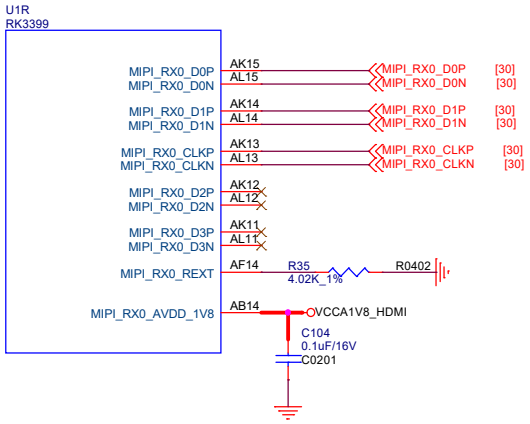
Seq.	GPIO0_A1	R27	ADC	HW ID	Date
01.	Low	NC	1.800V	E472673(15.6)	March 02, 2020
02.	Low	91K	1.622V	E472828(21.5)	
03.	Low	39K	1.433V	E473060(10.1)	
04.	Low	22K	1.238V	E473261(BACKPACK)	
05.	Low	13K	1.017V	E679524(USB-C)	
06.	Low	9.1K	0.858V	TBD	
07.	Low	6.2K	0.689V	TBD	
08.	Low	3.9K	0.505V	TBD	
09.	High	NC	1.800V	TBD	
10.	High	91K	1.622V	TBD	
11.	High	39K	1.433V	TBD	
12.	High	22K	1.238V	TBD	
13.	High	13K	1.017V	TBD	
14.	High	9.1K	0.858V	TBD	
15.	High	6.2K	0.689V	TBD	
16.	High	3.9K	0.505V	TBD	

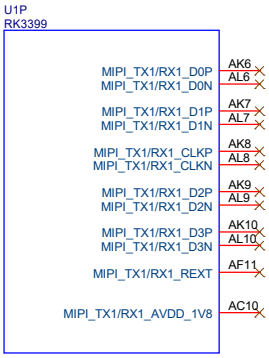
E472673 Hardware Version

Seq.	GPIO0_A5	GPIO3_D6	GPIO2_D4	HW Version	Date
01.	0	0	0	V1(EVT)	March 26, 2020
02.	0	0	1	V2	TBD
03.	0	1	0	V3	TBD
04.	0	1	1	V4	TBD
05.	1	0	0	V5	TBD
06.	1	0	1	V6	TBD
07.	1	1	0	V7	TBD
08.	1	1	1	V8	TBD

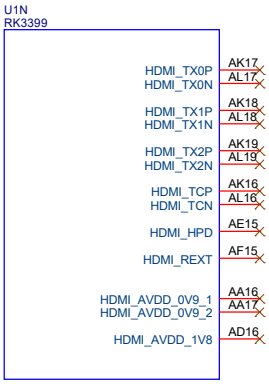
SIGNWAY			
Project:	E679524		
File:	12.RK3399 SARADC/Key		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHangliubin	Sheet:	12 of 32



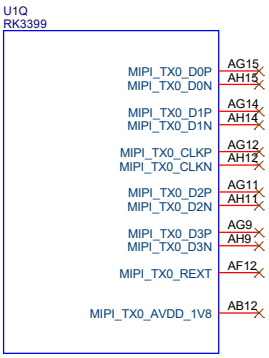


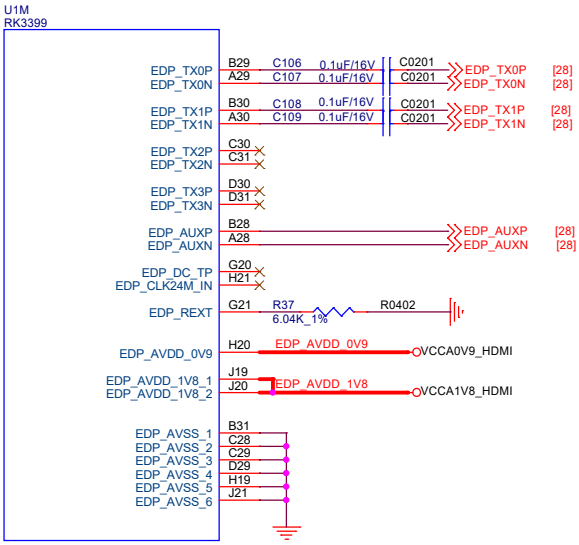


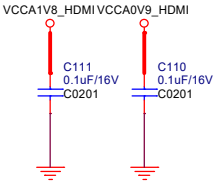
SIGNWAY			
Project:	E679524		
File:	13.RK3399 DVP Interface		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHangliubin	Sheet:	13 of 32



HDMI design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between clk and data < 80 ps;
3.Max trace length < 9.8 inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;







eDP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals
follows the 3W rule;

MIPI design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2 inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

SIGNWAY			
Project:	E679524		
File:	14.RK3399 Display Interface		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHangliubin	Sheet:	14 of 32

U1I
RK3399
Note:RK3399 part I is 3.3V only

GPIO3_A0/MAC_TXD2/SPI4_RXD_d F24
GPIO3_A1/MAC_TXD3/SPI4_TXD_d H23
GPIO3_A2/MAC_RXD2/SPI4_CLK_u E30
GPIO3_A3/MAC_RXD3/SPI4_CSn0_u E25
GPIO3_A4/MAC_TXD0/SPI0_RXD_d G23
GPIO3_A5/MAC_TXD1/SPI0_TXD_d E26
GPIO3_A6/MAC_RXD0/SPI0_CLK_u F27
GPIO3_A7/MAC_RXD1/SPI0_CSn0_u E29
GPIO3_B0/MAC_MDC/SPI0_CSn1_u C27
GPIO3_B1/MAC_RXDV_d F23
GPIO3_B2/MAC_RXER/I2C5_SDA_u G24 — GPIO1_TP [21]
GPIO3_B3/MAC_CLK/I2C5_SCL_u H22
GPIO3_B4/MAC_TXEN/UART1_RX_u G26
GPIO3_B5/MAC_MDIO/UART1_TX_u F25
GPIO3_B6/MAC_RXCLK/UART3_RX_u B27
GPIO3_B7/MAC_CRS/CIF_CLKOUTB/UART3_TX_u A26
GPIO3_C0/MAC_COL/UART3_CTSn/SPDIF_TX_u D27 — GPIO2_TP [21]
GPIO3_C1/MAC_TXCLK/UART3_RTSn_u E28
APIO1_VDDPST J22 — VCC_1V8
APIO1_VDD J23 — VCC3V3_LAN

VCC_1V8 — C187 0.1uF/16V C0201
VCC3V3_S0 — L53 FB_60R_0603 L0603 — VCC3V3_LAN — C114 0.1uF/16V C0201

U1E
RK3399
Note:RK3399 part E is 1.8V/3.0V mode
PART E 3V

GPIO1_A0/ISP0_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD_VBUS_SINK_EN_d R25 — EDP_ONOFF [28]
GPIO1_A1/ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CCo_VCONN_EN_d T31 — TP_RST [21]
GPIO1_A2/ISP0_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCPD_CC1_VCONN_EN_d R26 — TP_INT [21]
GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT_d R27
GPIO1_A4/ISP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG_d R28
GPIO1_A5/AP PWROFF_d R30 — PMIC_SLEEP_H [18]
GPIO1_A6/TSADC_INT_z P26 — OTP_OUT_H [18]
GPIO1_A7/SPI1_RXD/UART4_RX_u P27 — TD1_3V0 [20]
GPIO1_B0/SPI1_TXD/UART4_TX_u R31
GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK_u P28
GPIO1_B2/SPI1_CSn0/PMCU_JTAG_TMS_u P29
GPIO1_B3/I2C4_SDA_u P31 — I2C4_SDA [29]
GPIO1_B4/I2C4_SCL_u P30 — I2C4_SCL [29]
GPIO1_B5_d M24
GPIO1_B6/PWM3B_IR_d M25
GPIO1_B7/SPI3_RXD/I2C0_SDA_u M26 — GPU_SLEEP_H [18] / I2C_SDA_PMIC [16,29]
GPIO1_C0/SPI3_TXD/I2C0_SCL_u N30 — I2C_SCL_PMIC [16,29]
GPIO1_C1/SPI3_CLK_d M27 — CPU_B_SLEEP_H [18]
GPIO1_C2/SPI3_CSn0_u N31 — LED_STATE [18]
GPIO1_C3/PWM2_d M28 — LOG_DVS_PWM [18]
GPIO1_C4/I2C8_SDA_u M29 — EDP_POWON [28]
GPIO1_C5/I2C8_SCL_u M30 — PMIC_INT_L [18]
GPIO1_C6/TCPD_VBUS_SOURCE0_d L25
GPIO1_C7/TCPD_VBUS_SOURCE1_d M31
GPIO1_D0/TCPD_VBUS_SOURCE2_d L26
DFTJTAG_TMS_u AA24
DFTJTAG_TRSTn_d AB24
PMUIO2_VDDPST N23 — VCC_1V5
PMUIO2_VDD P23 — VCC_3V0

1.8V Only	VDDPST=VDDIO=1.8V
3.3V Only	VDDPST=1.8V,VDDIO=3.3V
other	3.0V mode:VDDPST=1.5V,VDDIO=3.0V 1.8V mode:VDDPST=1.8V,VDDIO=1.8V

VCC_1V5 — C116 0.1uF/16V C0201
VCC_3V0 — C117 0.1uF/16V C0201

TP_RST — R313 NC/2.2K — R0402 — VCC_3V0
TP_INT — R316 2.2K — R0402
TP的INT加上拉，reset上拉预留 20200706

I2C_SDA_PMIC — R51 2.2K — R0402 — VCC_3V0
I2C_SCL_PMIC — R52 2.2K — R0402
I2C4_SDA — R53 2.2K — R0402 — VCC_3V0
I2C4_SCL — R54 2.2K — R0402

U1G
RK3399
Note:RK3399 part G is 1.8V only

GPIO2_C0/UART0_RX_u AE9 — UART0_RXD [23]
GPIO2_C1/UART0_TX_u AH8 — UART0_TXD [23]
GPIO2_C2/UART0_CTSn_u AG8 — UART0_CTS [23]
GPIO2_C3/UART0_RTSn_u AL5 — UART0_RTS [23]
GPIO2_C4/SDIO0_D0/SPI5_RXD_u AD8 — SDIO0_D0 [23]
GPIO2_C5/SDIO0_D1/SPI5_TXD_u AK5 — SDIO0_D1 [23]
GPIO2_C6/SDIO0_D2/SPI5_CLK_u AG7 — SDIO0_D2 [23]
GPIO2_C7/SDIO0_D3/SPI5_CSn0_u AE8 — SDIO0_D3 [23]
GPIO2_D0/SDIO0_CMD_u AH6 — SDIO0_CMD [23]
GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1_u AF7 — SDIO0_CLK [23]
GPIO2_D2/SDIO0_DETN/PCIE_CLKREQn_u AL4 — GSENSOR_INT_L_1V8 [29]
GPIO2_D3/SDIO0_PWREN_d AD9 — BT_WAKE_L [23]
GPIO2_D4/SDIO0_BKPWR_d AF8 — GPIO2_D4 [12]
APIO3_VDD_1V8 AB8 — VCC_1V8

SDIO design rule:
1.Data[0:7] and CMD signals routing parallel as a group, the skew between each other must be less than 100mils;
2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
3.Max trace length < 3.93 inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;

VCC_1V8 — C118 0.1uF/16V C0201
VCC_1V8 — R627 2.2K R0402 — GSENSOR_INT_L_1V8 [29]

U1J
RK3399
Note:RK3399 part J is 1.8V/3.0V mode
PART J 1.8V

GPIO3_D0/I2S0_SCLK_d AG3 — I2S0_SCLK [26]
GPIO3_D1/I2S0_LRCK_RX_d AF4 — I2S0_LRCK_RX [26]
GPIO3_D2/I2S0_LRCK_TX_d AJ2 — I2S0_LRCK_TX [26]
GPIO3_D3/I2S0_SDI0_d Y7 — I2S0_SDI0 [26]
GPIO3_D4/I2S0_SDI1SDO3_d AE5
GPIO3_D5/I2S0_SDI2SDO2_d AA6 — GPIO3_D5 [12]
GPIO3_D6/I2S0_SDI3SDO1_d AH2 — PCIE_RL_POWON [28]
GPIO3_D7/I2S0_SDO0_d AH1 — I2S0_SDO0 [26]
GPIO4_A0/I2S_CLK_d AC7 — I2S_MCLK [26]
GPIO4_A1/I2C1_SDA_u AG1 — I2C1_SDA_1V8 [19,26]
GPIO4_A2/I2C1_SCL_u Y6 — I2C1_SCL_1V8 [19,26]
GPIO4_A3/I2S1_SCLK_d AF3 — I2S1_SCLK [23]
GPIO4_A4/I2S1_LRCK_RX_d AA7 — I2S1_LRCK_RX [23]
GPIO4_A5/I2S1_LRCK_TX_d AJ1 — VCC5V0_USB1 [20]
GPIO4_A6/I2S1_SDI0_d AD6 — I2S1_SDI0 [23]
GPIO4_A7/I2S1_SDO0_d AC6 — I2S1_SDO0 [23]
APIO5_VDDPST AA8 — VCC1V8_CODEC
APIO5_VDD Y8 — VCC1V8_CODEC

I2C1_SDA_1V8 — R57 2.2K — R0402 — VCC1V8_CODEC
I2C1_SCL_1V8 — R58 2.2K — R0402

VCC1V8_CODEC — C119 0.1uF/16V C0201
VCC1V8_CODEC — C120 0.1uF/16V C0201

U1K
RK3399
Note:RK3399 part K is 1.8V/3.0V mode

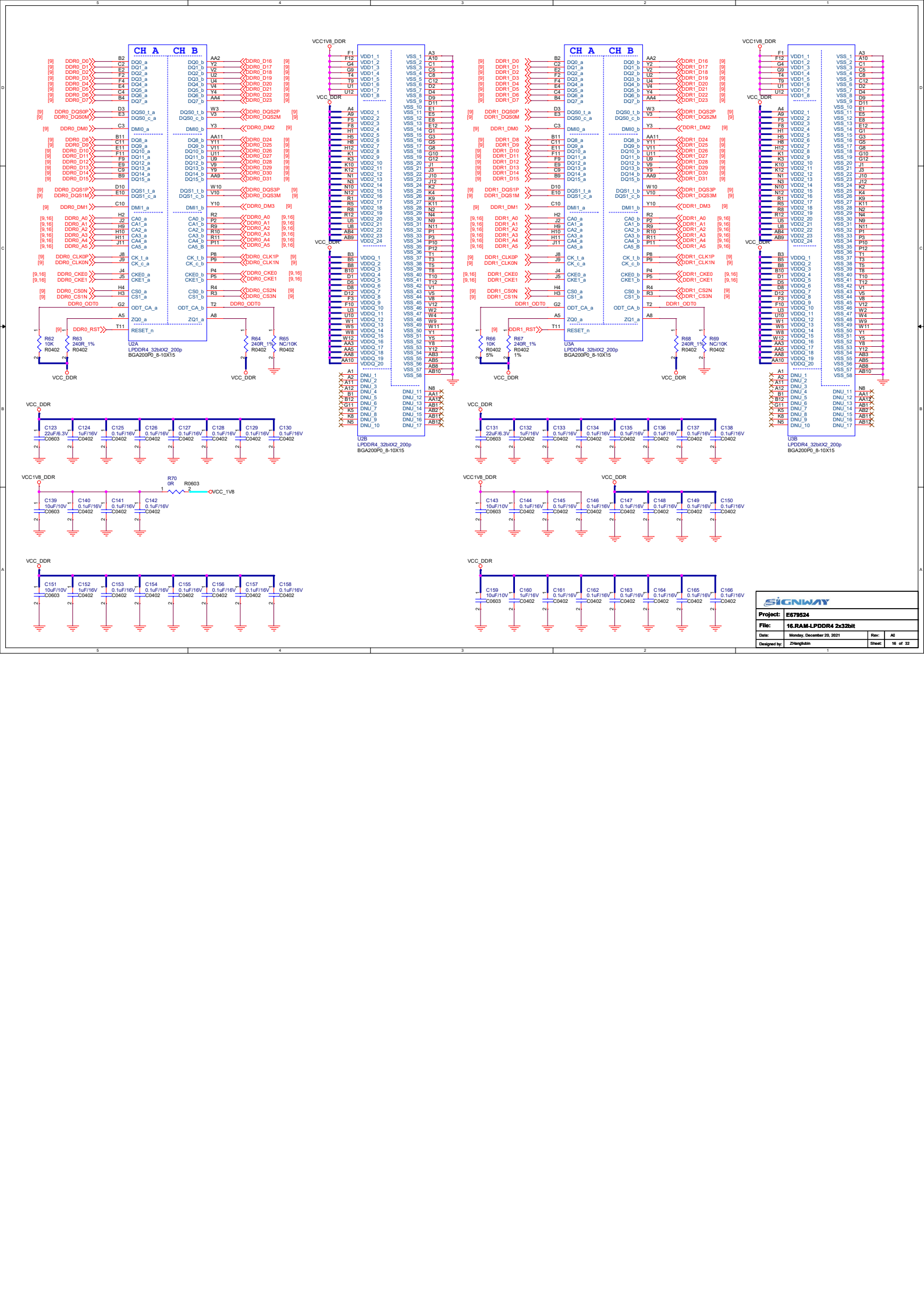
GPIO4_C0/I2C3_SDA/UART2B_RX_u AG6 — I2C3_SDA [21]
GPIO4_C1/I2C3_SCL/UART2B_TX_u AL2 — I2C3_SCL [21]
GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM_d AF5 — MIPI_PWM [28]
GPIO4_C3/UART2C_RX_u AK2 — UART2DBG_RX — UART2DBG_RX [20]
GPIO4_C4/UART2C_TX_u AJ4 — UART2DBG_TX — UART2DBG_TX [20]
GPIO4_C5/SPDIF_TX_d AK1 — AMP_MUTE [26]
GPIO4_C6/PWM1_d AL3 — VLED [25]
GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG_u AD7 — EDP_HPD [28]
GPIO4_D0/PCIE_CLKREQnB_u AE6 — WLED [25]
GPIO4_D1/DP_HOTPLUG_d AK4
GPIO4_D2_d AH5
GPIO4_D3_d AK3
GPIO4_D4_d AH6
GPIO4_D5_d AJ3 — EFUSE_VQPS_EN_H [32]
GPIO4_D6_d AG4 — EX_5V_EN [17] / CAMERA_AF_EN [30]
APIO4_VDDPST AC8 — VCC_1V5
APIO4_VDD AC9 — VCC_3V0

VCC_1V5 — R61 10K R0402 — C121 0.1uF/16V C0201
VCC_3V0 — C122 0.1uF/16V C0201

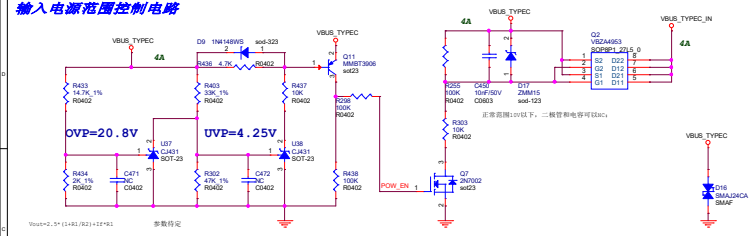
I2C3_SDA — R59 2.2K — R0402 — VCC_3V0
I2C3_SCL — R60 2.2K — R0402
电阻值由2.2K 改为10K. 20210915
UART2DBG_RX — R629 10K — R0402 — VCC_3V0
UART2DBG_TX — R628 2.2K — R0402

SIGNWAY

Project:	E679624
File:	15.RK3399 GPIO
Date:	Monday, December 20, 2021
Rev:	A1
Designed by:	ZHenghubin
Sheet:	15 of 32

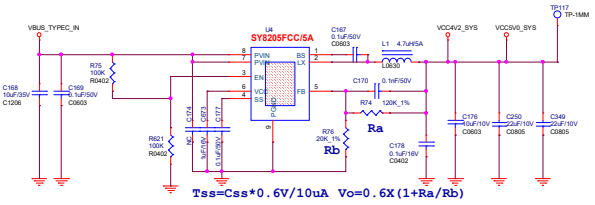

CH A
CH B
U2A
LPDDR4_32bitX2_200p
BGA200P0_8-10X15
U2B
U3A
U3B
VCC1V8_DDR
VCC_DDR
VCCVCC_1V8
R70
0R
R0603
Project: E679524
File: 16.RAM-LPDDR4 2x32bit
Date: Monday, December 20, 2021
Rev: A0
Designed by: ZHenglubin
Sheet: 16 of 32

输入电源范围控制电路



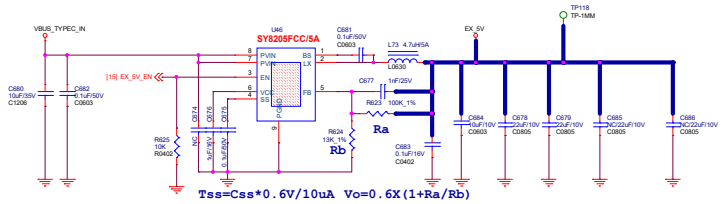
系统电源/BUCK-5V

Revised 2020/11/10

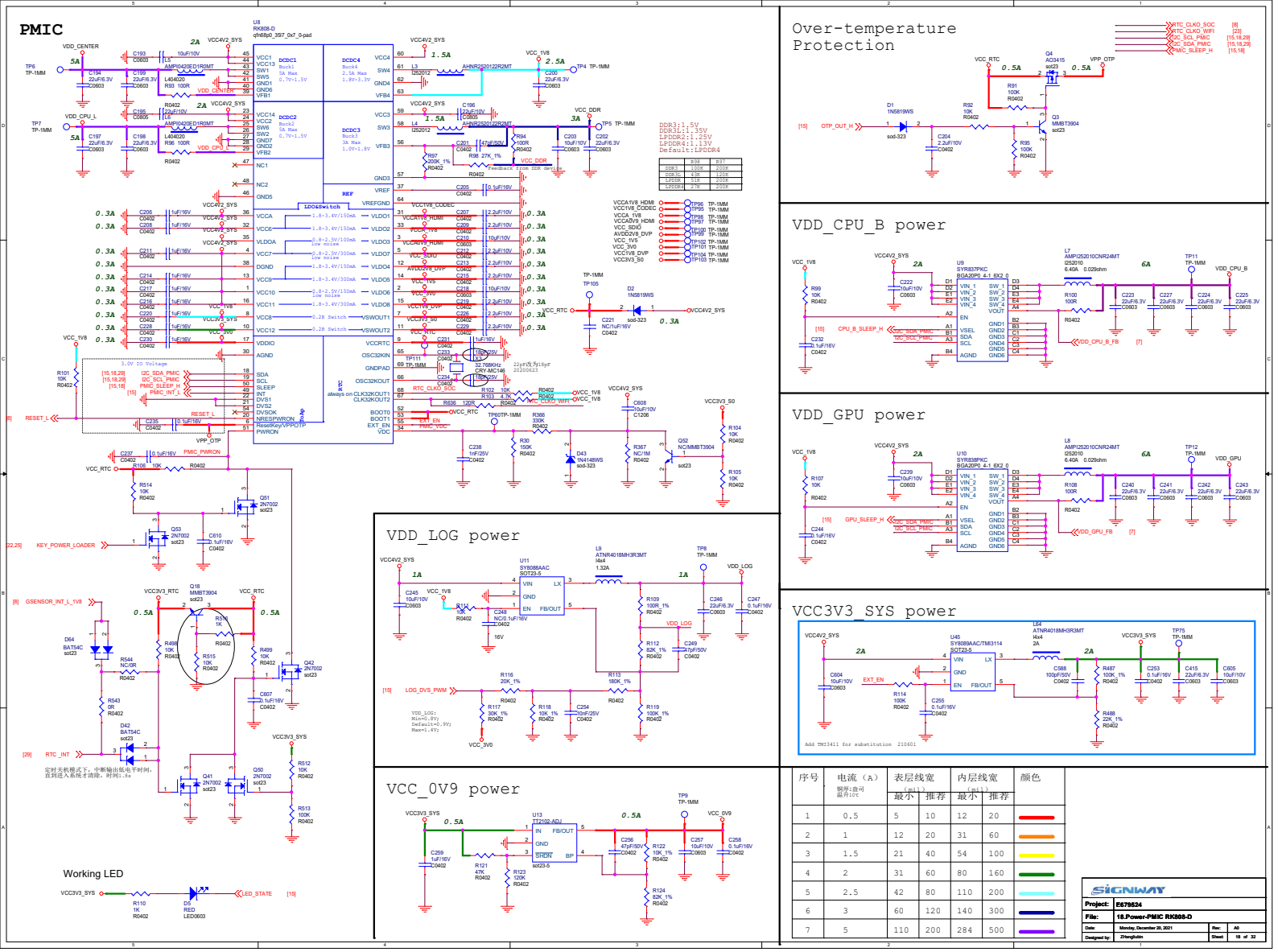


外设电源/BUCK-5.1V

Revised 2020/11/10



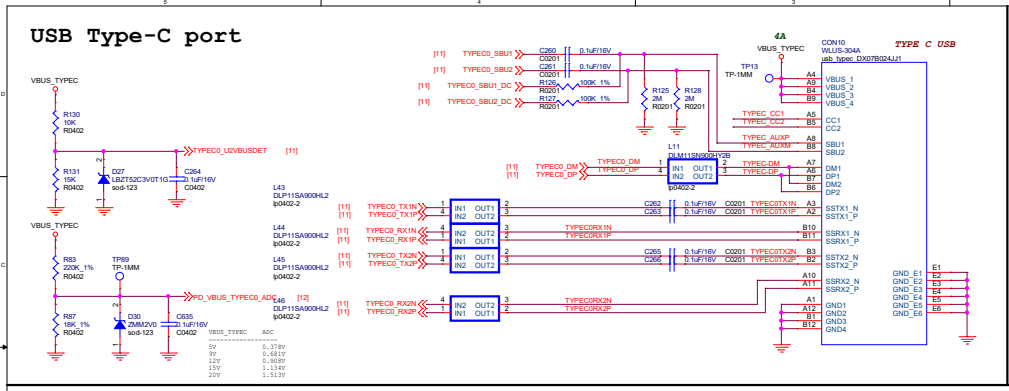
Project:	E679524
File:	17.POWER IN
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	Zhangkaixin
Sheet:	17 of 32

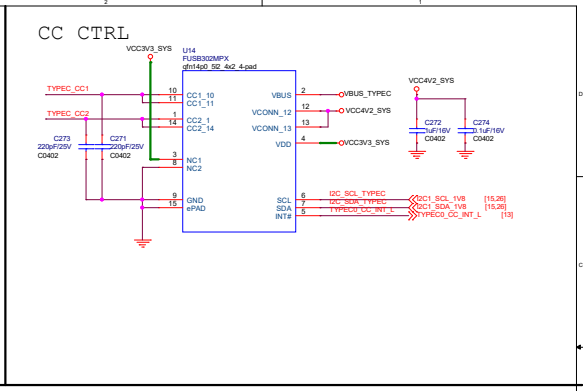


	8/8B	8/8T
DDR3	150R	240K
DDR3L	43K	120K
LPDDR	51K	200K
LPDDR4	27K	240K

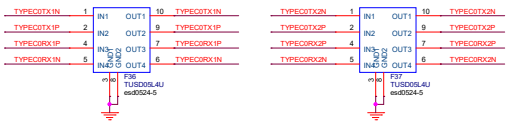
序号	电流（A） 铜厚1盎司 温升10℃	表层线宽（mil） 最小	表层线宽（mil） 推荐	内层线宽（mil） 最小	内层线宽（mil） 推荐	颜色
1	0.5	5	10	12	20	
2	1	12	20	31	60	
3	1.5	21	40	54	100	
4	2	31	60	80	160	
5	2.5	42	80	110	200	
6	3	60	120	140	300	
7	5	110	200	284	500	

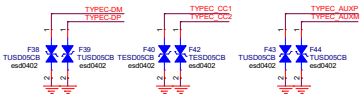
Project:	E679524
File:	18.Power-PMIC RK808-D
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	ZHanghdm
Sheet	18 of 32





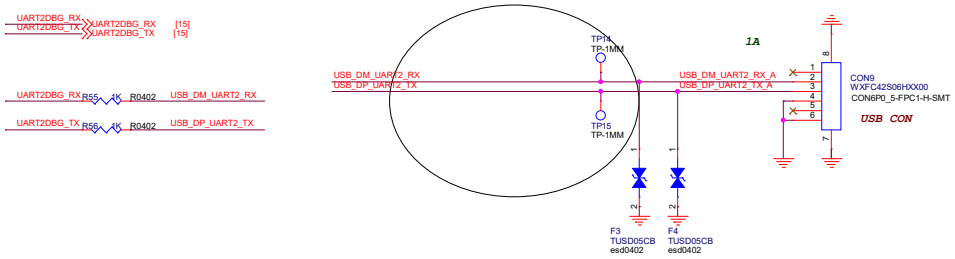
ESD





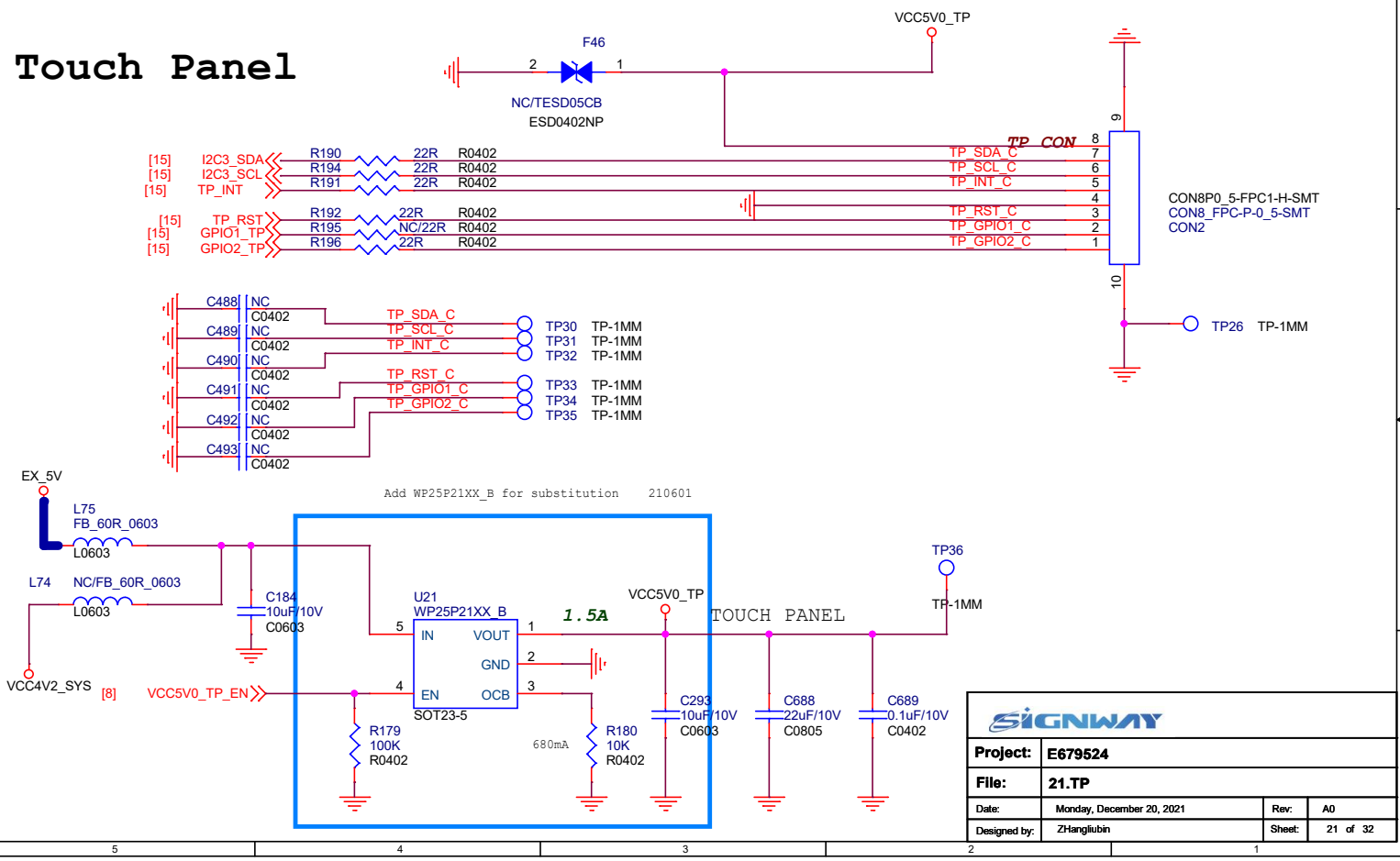
SIGNWAY	
Project:	E879524
File:	19.TYPE-C
Date:	Monday, December 20, 2021 — Rev: A0
Designed by:	Zhenghaibin — Sheet: 19 of 32

OTG USB & DEBUG UART



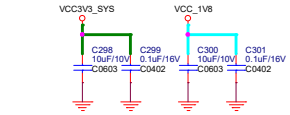
SIGNWAY			
Project:	E679524		
File:	20.USB&DEBUG UART		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHenglubin	Sheet:	20 of 32

Touch Panel



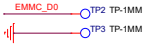
SIGNWAY			
Project:	E679524		
File:	21.TP		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHangliubin	Sheet:	21 of 32

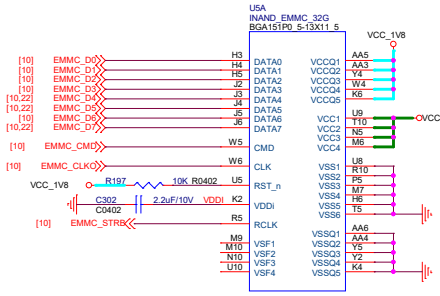
eMMC FLASH

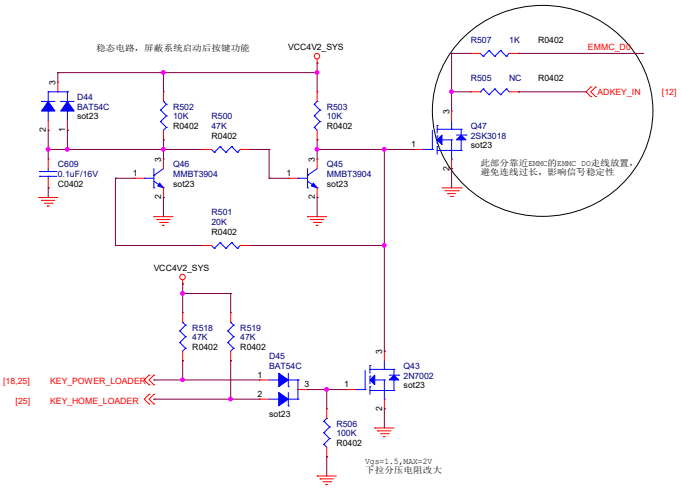


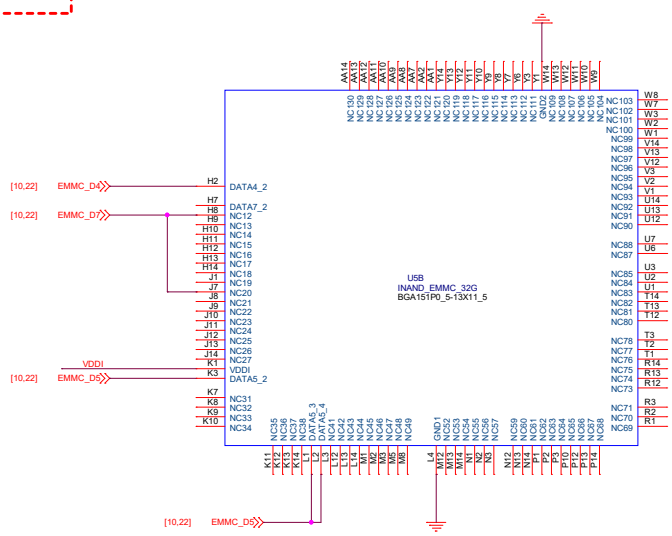
Note:All the Power filter capacitors should be placed close to the power pins of eMMC

Note:
Reserve TestPoint for firmware update.
If EMMC_CLKO=0V at power-on reset,
then system will enter into Maskrom mode.





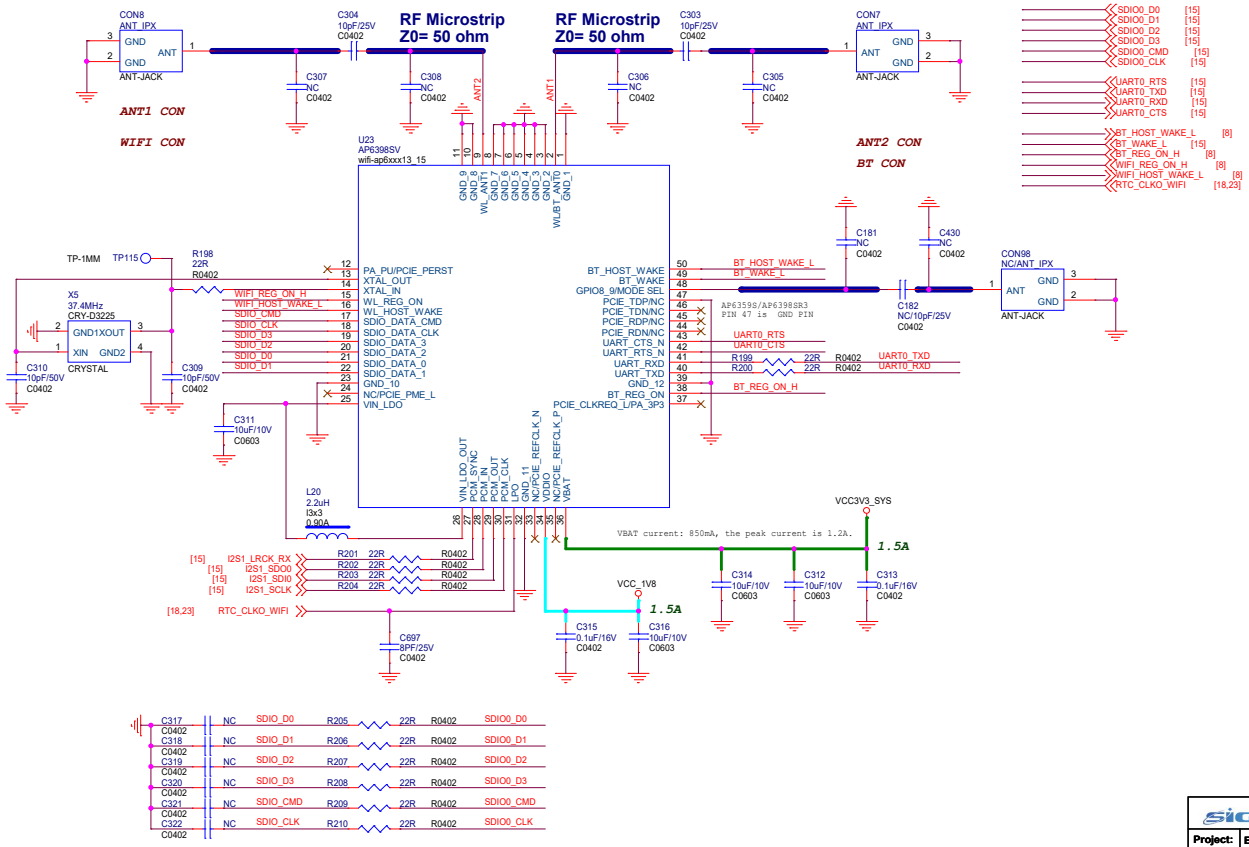




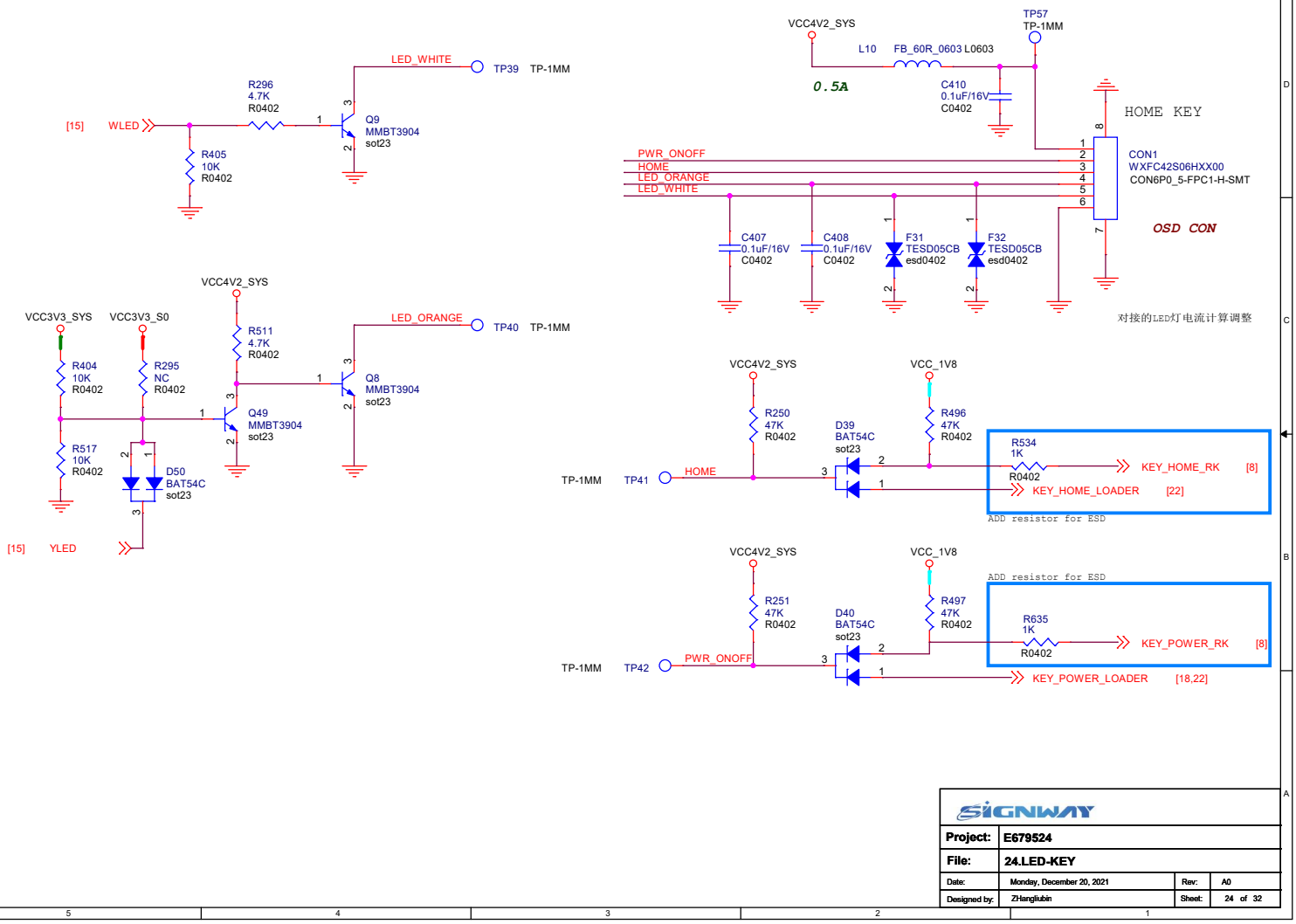
Project:	E679524
File:	22.Memory-eMMC
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	ZHenglishin
Sheet:	22 of 32

SDIO WIFI/BT MODULE-MIMO

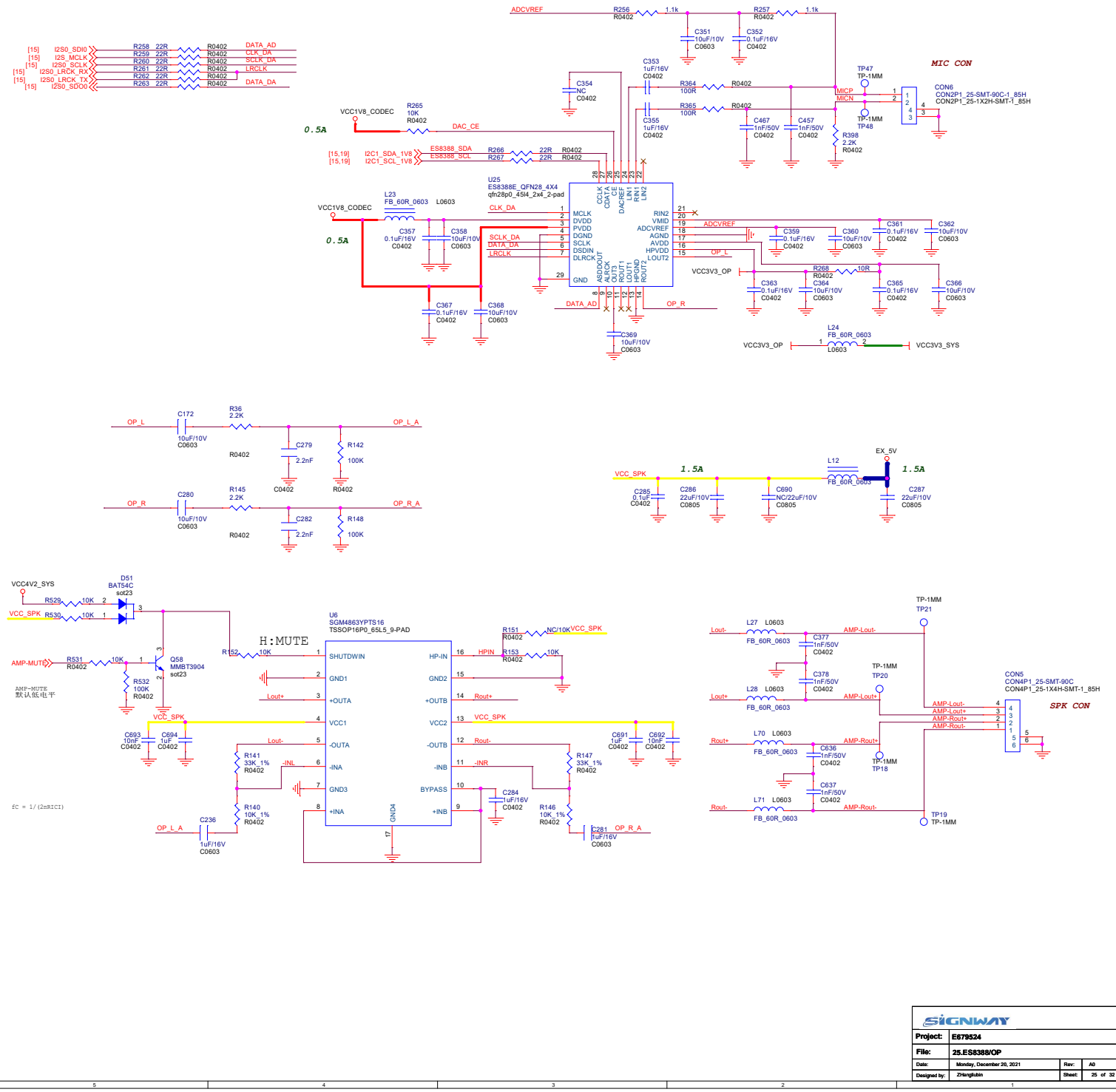
Note:VBAT power supply range is 3.0V~4.8V.



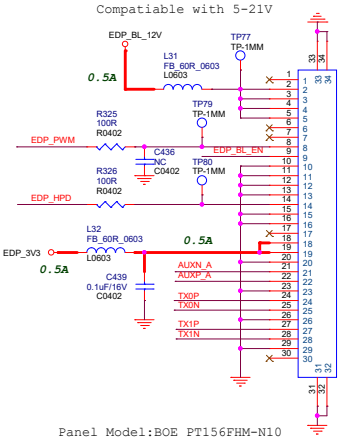
Project:	E679524
File:	23.WIFI/BT-AP6398SV
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	ZHanglubin
Sheet:	23 of 32



SIGNWAY			
Project:	E679524		
File:	24.LED-KEY		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHangliubin	Sheet:	24 of 32

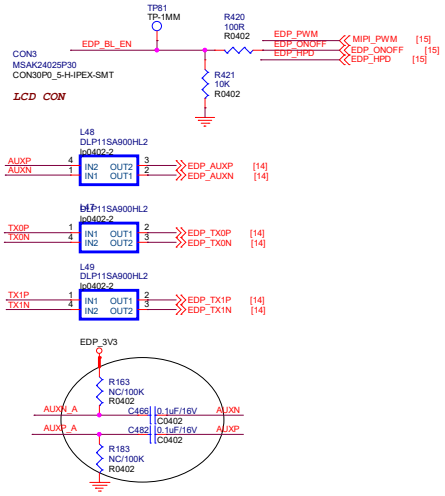


Project:	E679524
File:	25.ES8388/OP
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	ZHangliubin
Sheet:	25 of 32

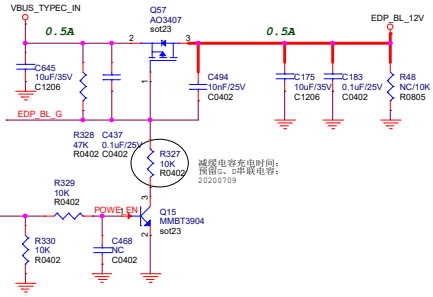


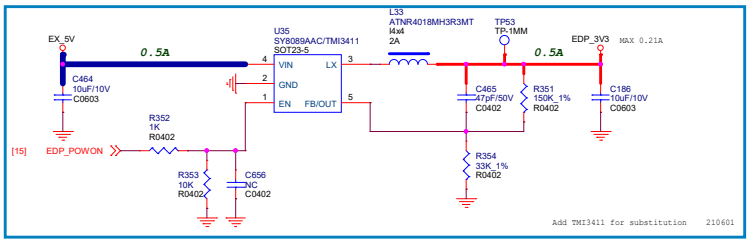
Panel Model:BOE PT156FHM-N10

eDP Panel

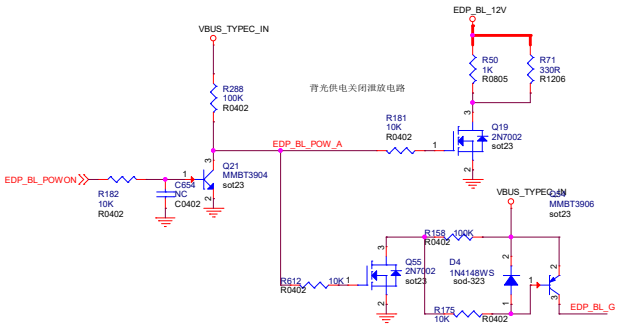


注意：
1、eDP1.2a及以上协议的eDP显示屏，Aux的偏置电阻不贴。
2、若是较低协议的显示屏，需要贴片。
20200706





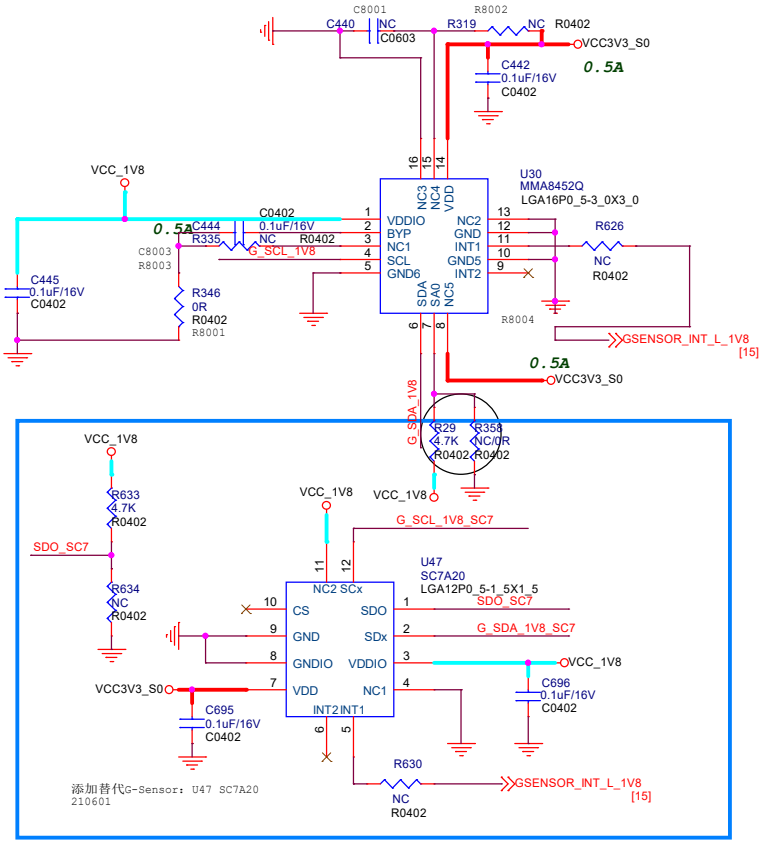
SY8089AAC的最小压降？？

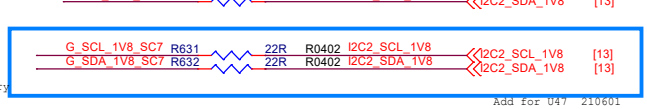


Project:	E679524
File:	26.Edp Dispaly
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	ZHanghbin
Sheet:	26 of 32

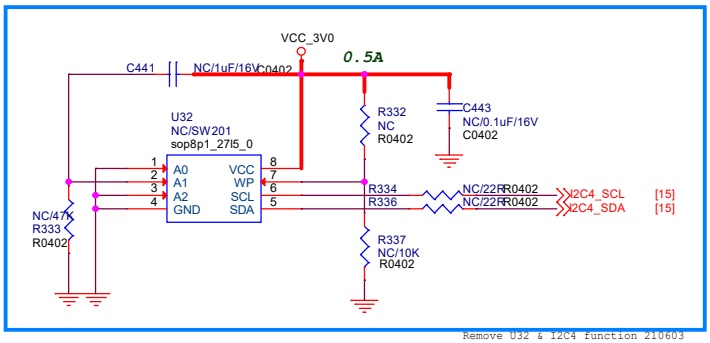
	LIS3DH	MMA8452Q	LSM303D
C8001	NC	NC	4.7uF
R8002	0ohm	NC	NC
R8001	NC	0ohm	NC
C8003	NC	0.1uF	0.22uF
R8003	NC	NC	0R
R8004	NC	NC	0R

The MMA8452Q's standard slave address is a choice between the two sequential addresses 0011100 and 0011101. The selection is made by the high and low logic level of the SA0 (pin 7) input respectively. The slave addresses are factory programmed and alternate addresses are available at customer request

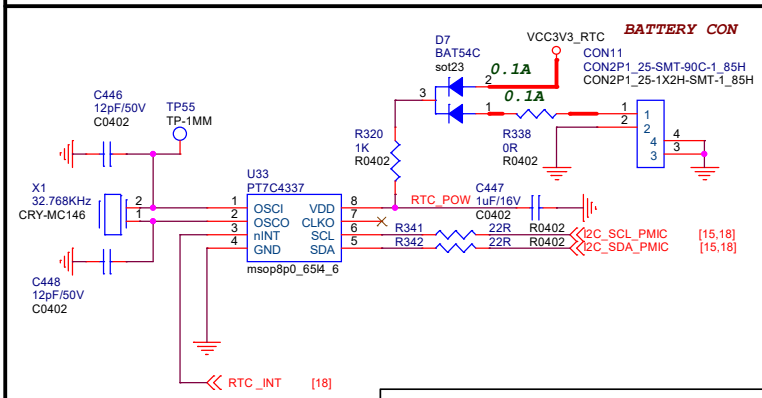




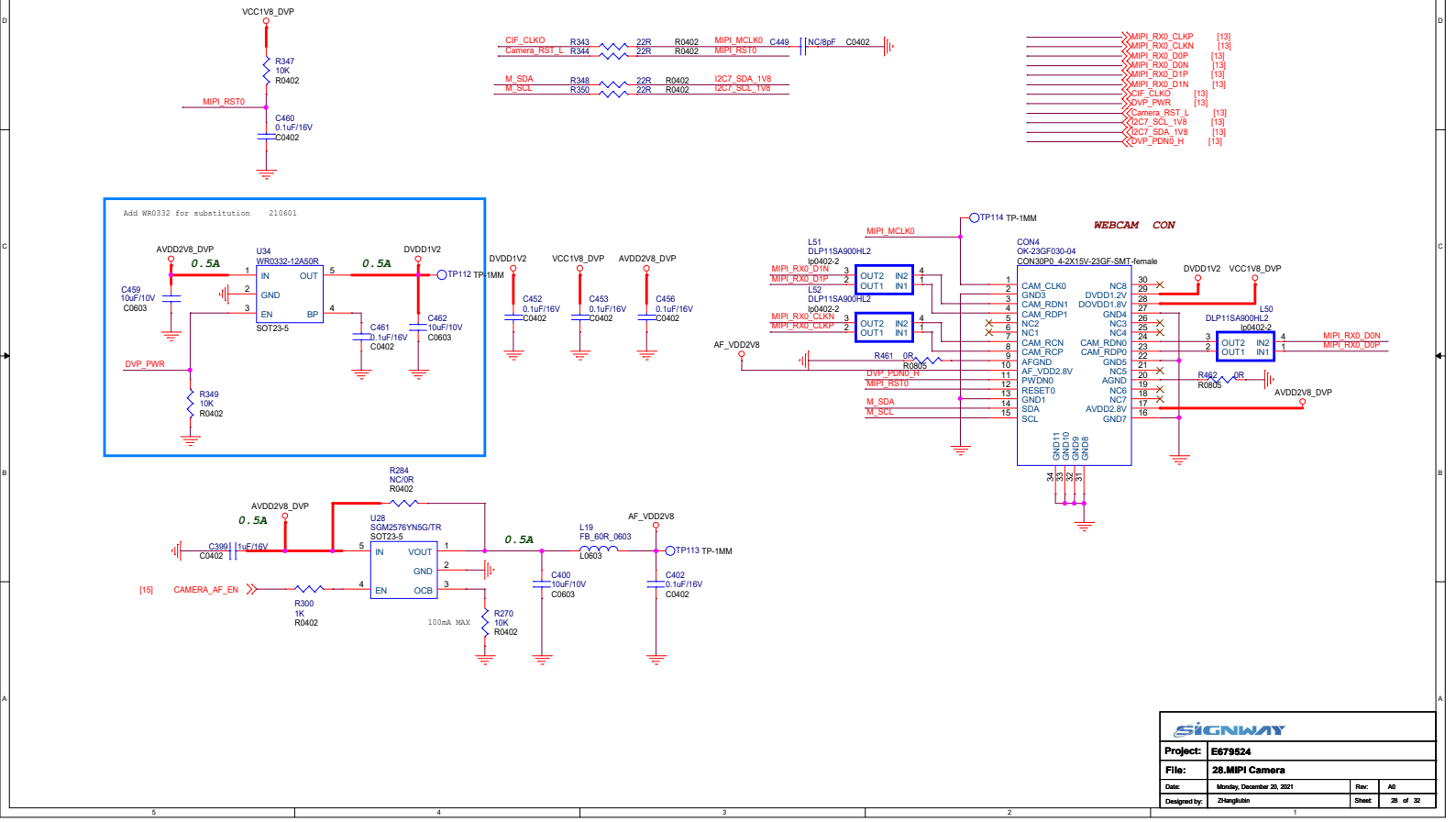
Add for U47 210601



Remove U32 & I2C4 function 210603



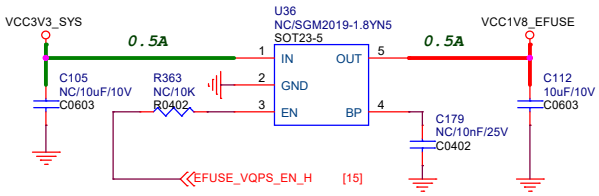
SIGNWAY			
Project:	E679524		
File:	27.G-sensor&RTC		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHangliubin	Sheet:	27 of 32



Project:	E679524
File:	28.MIPI Camera
Date:	Monday, December 20, 2021
Rev:	A0
Designed by:	ZHangfubin
Sheet:	28 of 32

eFUSE

Note: For eFUSE programming, can be removed if do not use eFUSE。



SIGNWAY			
Project:	E679524		
File:	29.eFUSE		
Date:	Monday, December 20, 2021	Rev:	A0
Designed by:	ZHangliubin	Sheet:	29 of 32