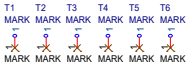
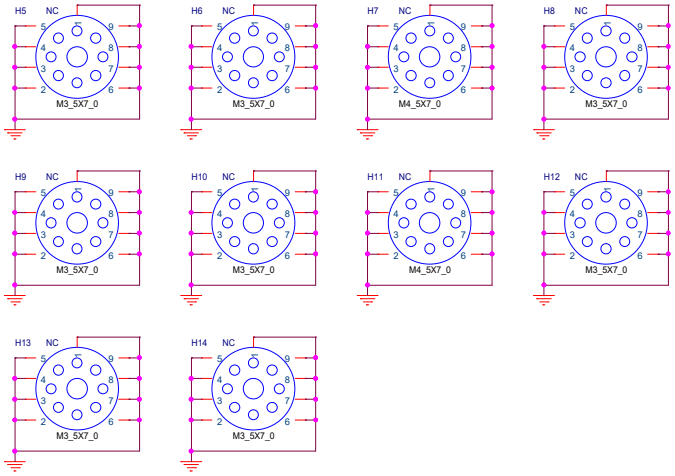
PCB MARK & LABEL

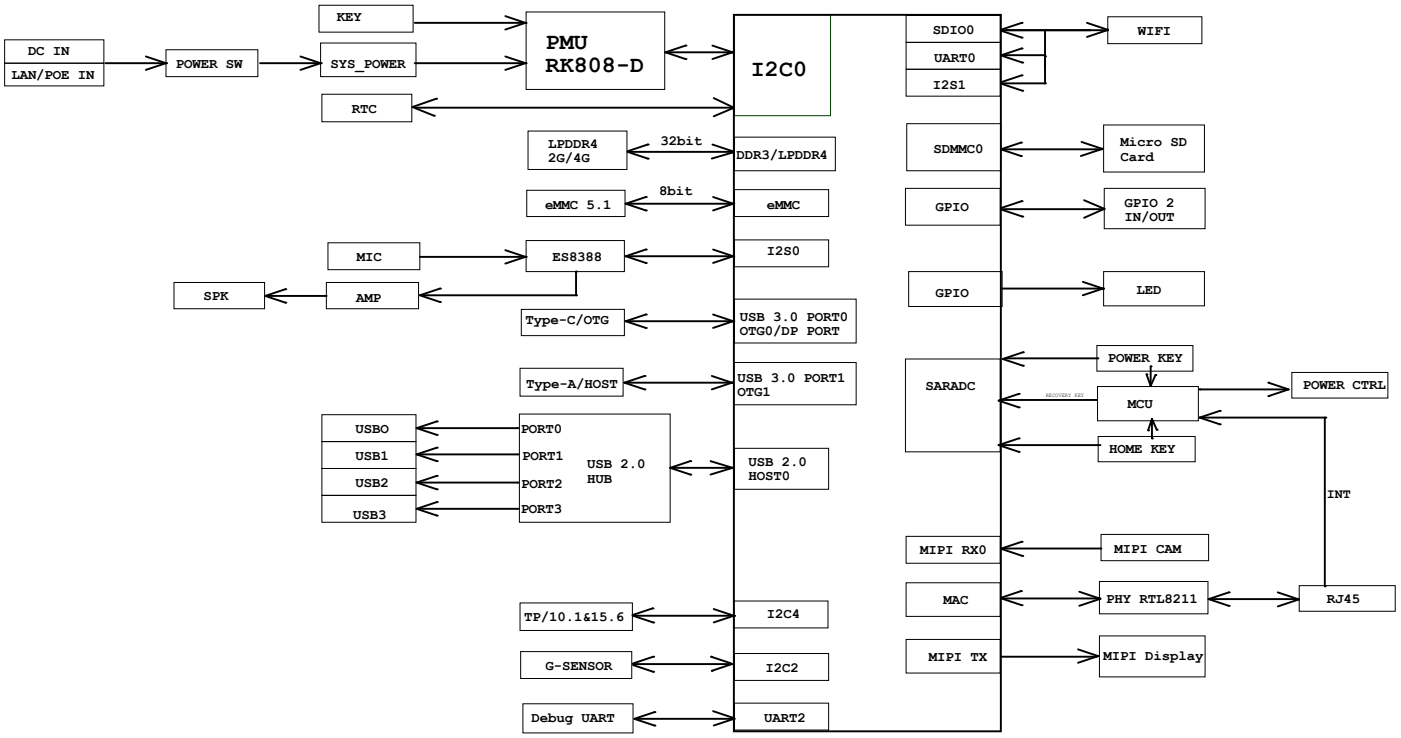
Heat Sink	
Optical Marks	
Label Outline	
Silkcreen	
Mounting Hole	

SIGNWAY			
Project:	E473060		
File:	01.Msc		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	ZhangboB,Yangyin	Sheet	1 of 32

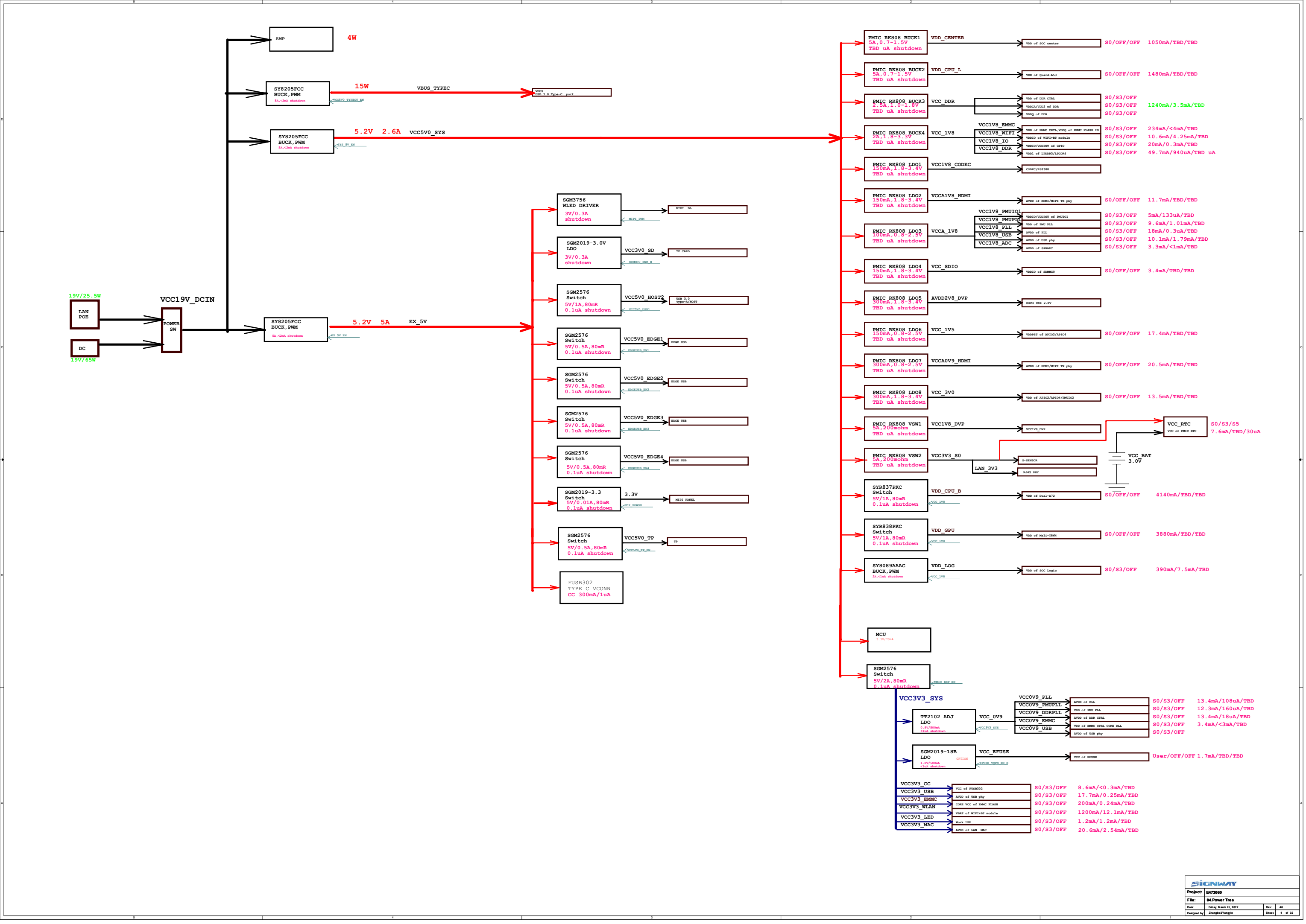
Change List

Version	Date	Author	Change Note	Approved
V0.1	April 24, 2020	Zhangbo&Yangyin	First edition.	Zhouchangliang

Project:	E473060
File:	02.Change List
Date:	Friday, March 25, 2022
Rev:	A0
Designed by:	Zhangbo&Yangyin
Sheet:	2 of 32



Project:	E473060
File:	03.Block Diagram
Date:	Friday, March 29, 2024
Rev:	A0
Designed by	ZhangkaiShangyin
Sheet	3 of 32

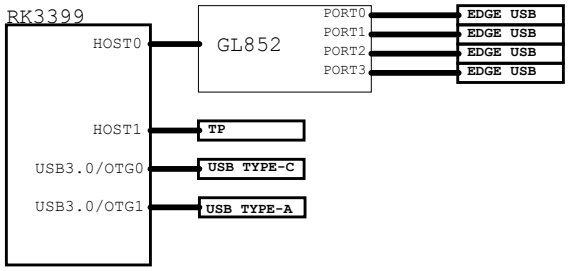


19V/25.5W
LAN POE
DC
19V/65W
VCC19V_DCIN
POWER SW
AMP
4W
SY8205FCC BUCK,PWM
15W
VBUS_TYPEC
SY8205FCC BUCK,PWM
5.2V 2.6A
VCC5V0_SYS
SY8205FCC BUCK,PWM
5.2V 5A
EX_5V
SGM3756 WLED DRIVER
3V/0.3A shutdown
SGM2019-3.0V LDO
3V/0.3A shutdown
VCC3V0_SD
SGM2576 Switch
5V/1A,80mR 0.1uA shutdown
VCC5V0_HOST2
SGM2576 Switch
5V/0.5A,80mR 0.1uA shutdown
VCC5V0_EDGE1
VCC5V0_EDGE2
VCC5V0_EDGE3
VCC5V0_EDGE4
SGM2019-3.3 Switch
5V/0.01A,80mR 0.1uA shutdown
3.3V
VCC5V0_TP
FUSB302 TYPE C VCONN CC 300mA/1uA
PMIC RK808 BUCK1 5A,0.7-1.5V TBD uA shutdown
VDD_CENTER
S0/OFF/OFF 1050mA/TBD/TBD
PMIC RK808 BUCK2 5A,0.7-1.5V TBD uA shutdown
VDD_CPU_L
S0/OFF/OFF 1480mA/TBD/TBD
PMIC RK808 BUCK3 2.5A,1.0-1.8V TBD uA shutdown
VCC_DDR
S0/S3/OFF 1240mA/3.5mA/TBD
PMIC RK808 BUCK4 2A,1.8-3.3V TBD uA shutdown
VCC_1V8
VCC1V8_EMMC
VCC1V8_WIFI
VCC1V8_IO
VCC1V8_DDR
S0/S3/OFF 234mA/<4mA/TBD
S0/S3/OFF 10.6mA/4.25mA/TBD
S0/S3/OFF 20mA/0.3mA/TBD
S0/S3/OFF 49.7mA/940uA/TBD uA
PMIC RK808 LDO1
VCC1V8_CODEC
PMIC RK808 LDO2 150mA,1.8-3.4V TBD uA shutdown
VCCA1V8_HDMI
S0/OFF/OFF 11.7mA/TBD/TBD
PMIC RK808 LDO3 100mA,0.8-2.5V TBD uA shutdown
VCCA_1V8
VCC1V8_PMUIO2
VCC1V8_PMUPLL
VCC1V8_PLL
VCC1V8_USB
VCC1V8_ADC
S0/S3/OFF 5mA/133uA/TBD
S0/S3/OFF 9.6mA/1.01mA/TBD
S0/S3/OFF 18mA/0.3uA/TBD
S0/S3/OFF 10.1mA/1.79mA/TBD
S0/S3/OFF 3.3mA/<1mA/TBD
PMIC RK808 LDO4 150mA,1.8-3.4V TBD uA shutdown
VCC_SDIO
S0/OFF/OFF 3.4mA/TBD/TBD
PMIC RK808 LDO5 300mA,1.8-3.4V TBD uA shutdown
AVDD2V8_DVP
PMIC RK808 LDO6 150mA,0.8-2.5V TBD uA shutdown
VCC_1V5
S0/OFF/OFF 17.4mA/TBD/TBD
PMIC RK808 LDO7 300mA,0.8-2.5V TBD uA shutdown
VCCA0V9_HDMI
S0/OFF/OFF 20.5mA/TBD/TBD
PMIC RK808 LDO8 300mA,1.8-3.4V TBD uA shutdown
VCC_3V0
S0/OFF/OFF 13.5mA/TBD/TBD
PMIC RK808 VSW1 5A,200mohm TBD uA shutdown
VCC1V8_DVP
VCC_RTC
S0/S3/S5 7.6mA/TBD/30uA
PMIC RK808 VSW2 5A,200mohm TBD uA shutdown
VCC3V3_S0
LAN_3V3
VCC_BAT 3.0V
SYR837PKC Switch 5V/1A,80mR 0.1uA shutdown
VDD_CPU_B
S0/OFF/OFF 4140mA/TBD/TBD
SYR838PKC Switch 5V/1A,80mR 0.1uA shutdown
VDD_GPU
S0/OFF/OFF 3860mA/TBD/TBD
SY8089AAAC BUCK,PWM
VDD_LOG
S0/S3/OFF 390mA/7.5mA/TBD
MCU
SGM2576 Switch 5V/2A,80mR 0.1uA shutdown
VCC3V3_SYS
TT2102 ADJ LDO
VCC_0V9
VCC0V9_PLL
VCC0V9_PMUPLL
VCC0V9_DDRPLL
VCC0V9_EMMC
VCC0V9_USB
S0/S3/OFF 13.4mA/108uA/TBD
S0/S3/OFF 12.3mA/140uA/TBD
S0/S3/OFF 13.4mA/10uA/TBD
S0/S3/OFF 3.4mA/<3mA/TBD
S0/S3/OFF
SGM2019-18B LDO
VCC_EFUSE
User/OFF/OFF 1.7mA/TBD/TBD
VCC3V3_CC
VCC3V3_USB
VCC3V3_EMMC
VCC3V3_WLAN
VCC3V3_LED
VCC3V3_MAC
S0/S3/OFF 8.6mA/<0.3mA/TBD
S0/S3/OFF 17.7mA/0.25mA/TBD
S0/S3/OFF 200mA/0.24mA/TBD
S0/S3/OFF 1200mA/12.1mA/TBD
S0/S3/OFF 1.2mA/1.2mA/TBD
S0/S3/OFF 20.6mA/2.54mA/TBD
SIGNWAY

I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_3V0	Rockchip RK808	0x1b	PMIC	100kHz,400KHz
					SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
					PT7C4337	0xd0,0xd1	RTC	100kHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5	I2C1_SDA_1V8 I2C1_SCL_1V8	VCC_1V8	ES8388/1.8V	0x10,0x11	Audio codec	100kHz
					FUSB302MPX/1.8V	0x44,0x46	USB-TypeC Mux	100kHz
					GL852	0X2C	USB HUB	100kHz
					———	———	———	———
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2	I2C2_SDA_1V8 I2C2_SCL_1V8	VCC_1V8	MMA8452Q/1.8V	0x1D,0x1E	G-SENSOR	100kHz,400KHz,
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C3_SDA I2C3_SCL	VCC_3V0	TP/3.3V	TBD	TP TOUCH	100kHz,400KHz,3.4MHz
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C4_SDA I2C4_SCL	VCC_3V0	SW201/3.0V	0xA0 0xE0	EEPROM	10kHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	MAC USE					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2	NOT USE					
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2	I2C7_SDA_1V8 I2C7_SCL_1V8	VCC_1V8	MIPI_CSI /1.8V			100kHz

USB MAP

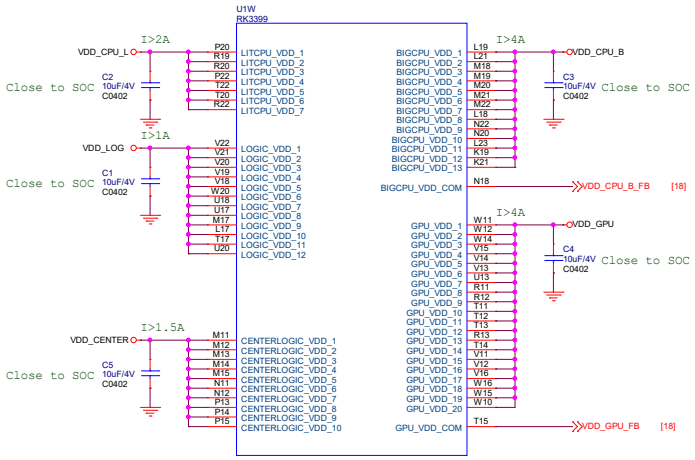


SIGNWAY			
Project:	E473060		
File:	05.I2C&USB Map		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhanghb&Yangyin	Sheet:	5 of 32

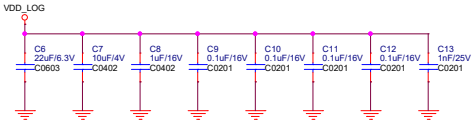
Power Domain Map

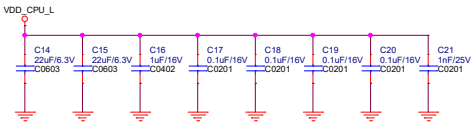
Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuio1_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLDO3
Part E	PMUIO2/PART E	pmu1830_gpio1abcd	3.0V	VCC_1V5	RK808-D Buck4 RK808-D VLDO6
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_LAN	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V	VCC_1V8	RK808-D VLDO3
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLDO6 RK808-D VLDO8
Part J	APIO5/PART J	audio_gpio3d_gpio4a	VCC1V8_CODEC	VCC1V8_CODEC	RK808-D VLDO1
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCC_SDIO	RK808-D VLDO4

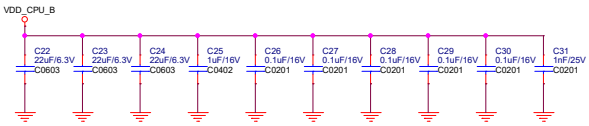
SIGNWAY			
Project:	E473060		
File:	06.Power Domain Map		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	6 of 32

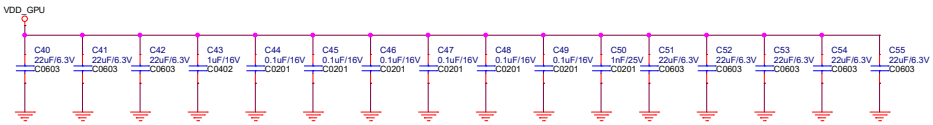


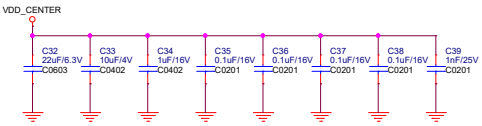
Note:Power filter CAP please place back of SOC or close to SOC

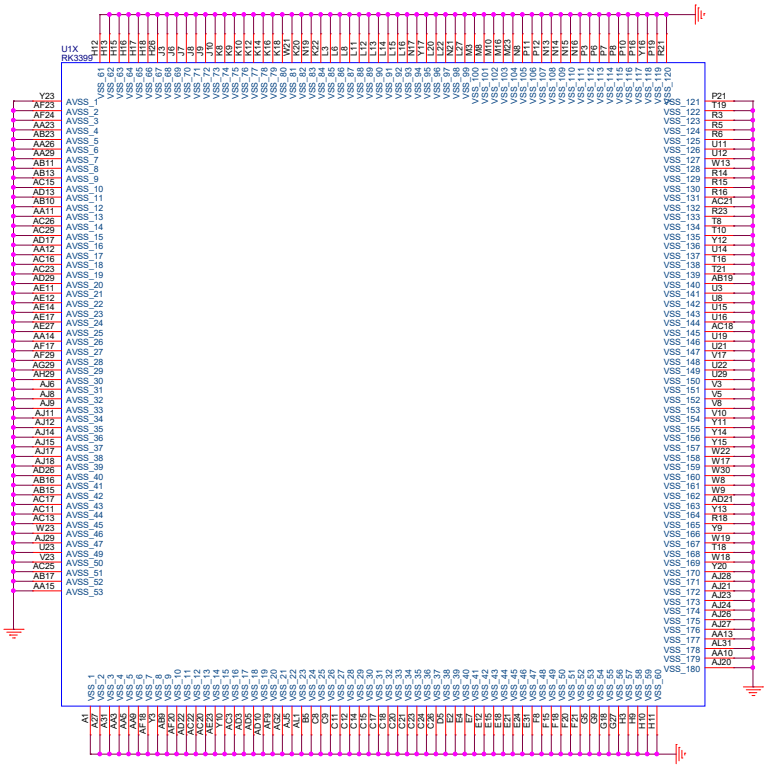




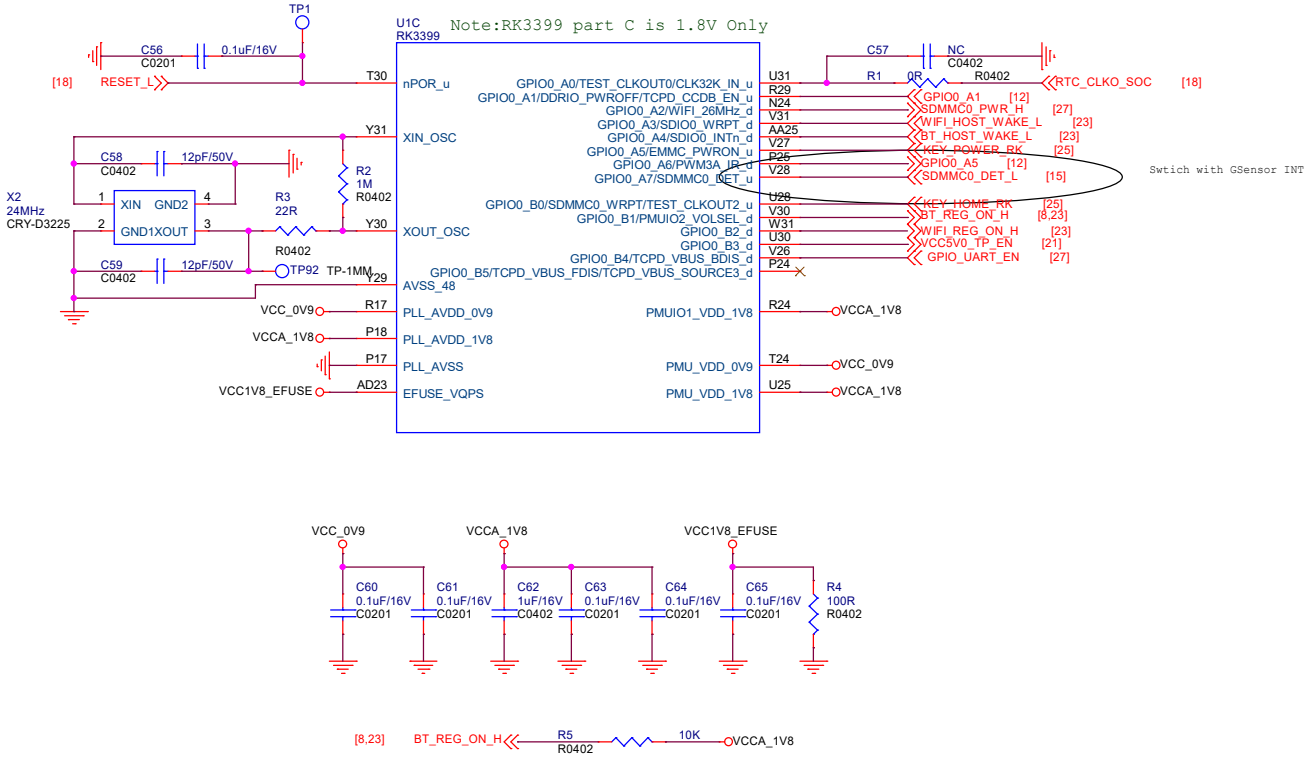




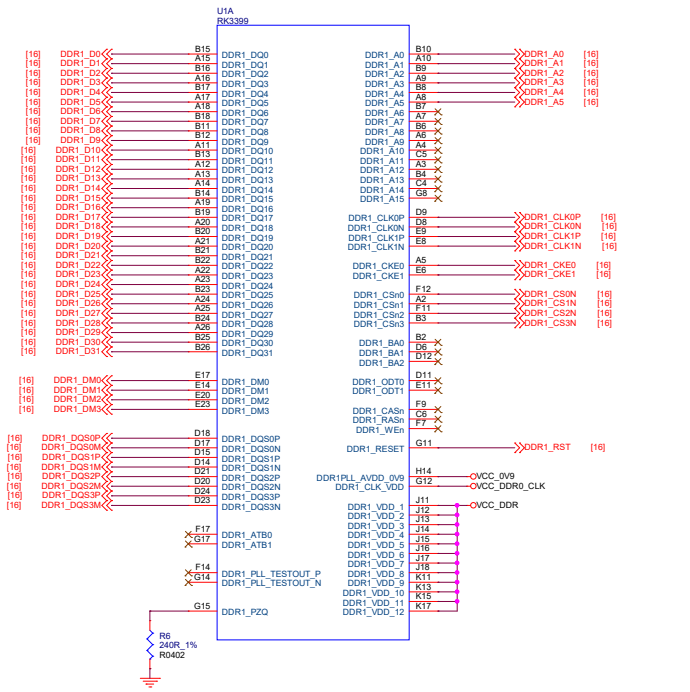


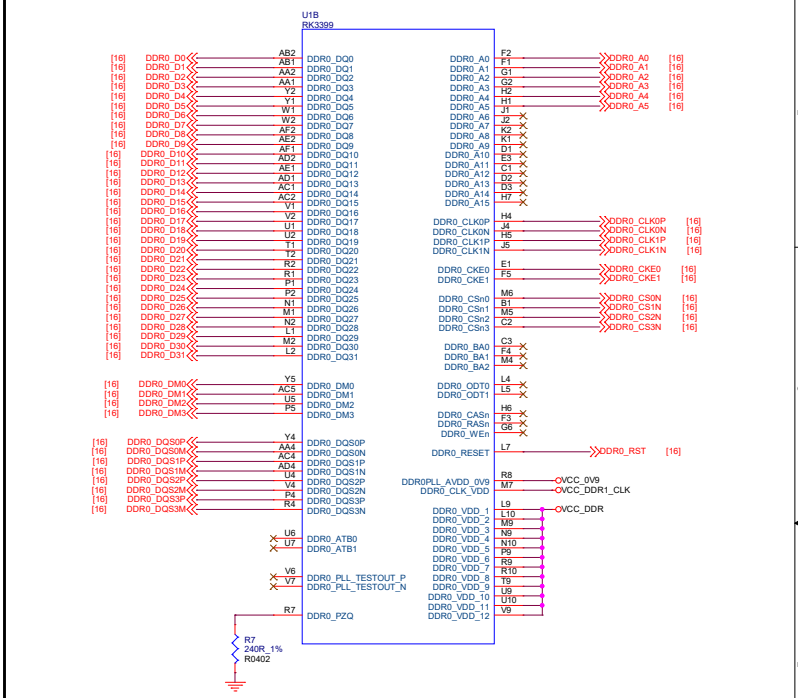


SIGNWAY	
Project:	E473060
File:	07.RK3399 Power
Date:	Friday, March 25, 2022
Rev:	A0
Designed by:	Zhanghb&Yangyin
Sheet:	7 of 32

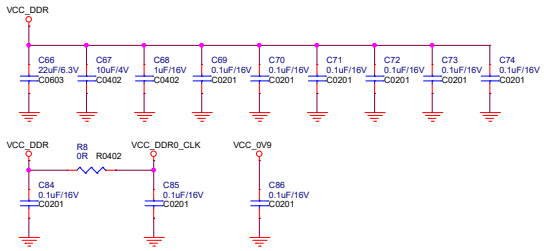


SIGNWAY			
Project:	E473060		
File:	08.RK3399 PMU Controler		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	8 of 32





DDR FILTER Note:R10 cannot be deleted



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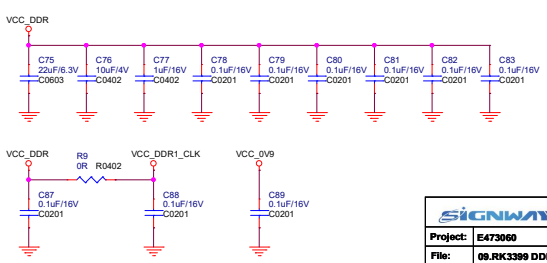

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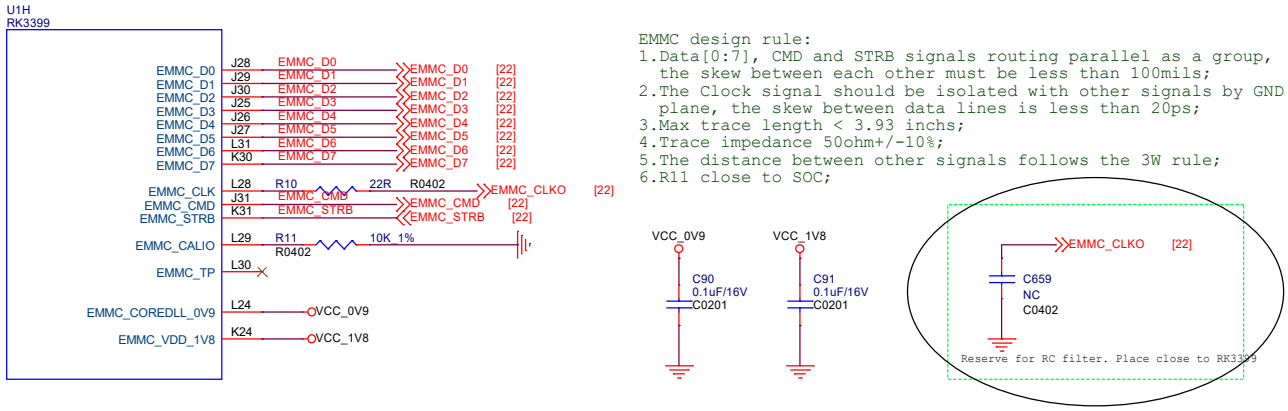
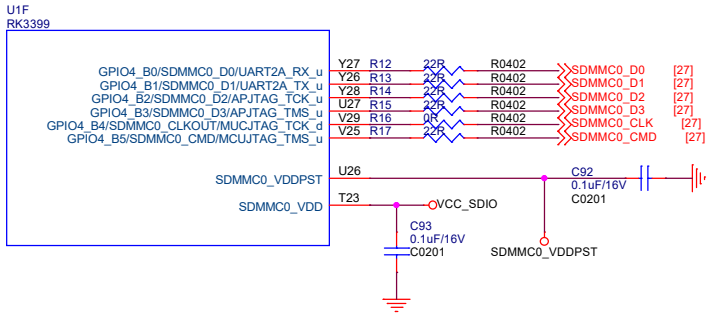
Project:	E473060
File:	09.RK3399 DDR Controler
Date:	Friday, March 25, 2022
Rev:	A0
Designed by:	Zhanghao&Yangyin
Sheet:	9 of 32

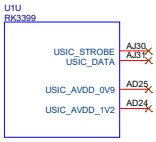


EMMC design rule:
1.Data[0:7], CMD and STRB signals routing parallel as a group, the skew between each other must be less than 100mils;
2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
3.Max trace length < 3.93 inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;
6.R11 close to SOC;

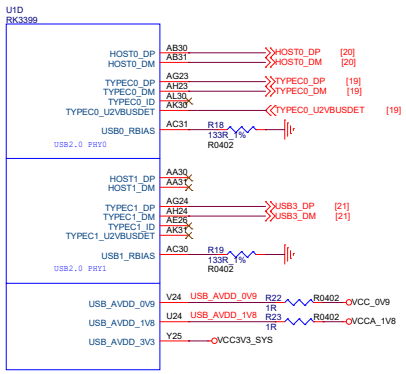


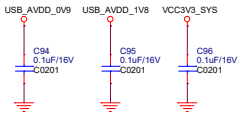
SDMMC design rule:
1.Data[0:7] and CMD signals routing parallel as a group, the skew between each other must be less than 100mils;
2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
3.Max trace length < 3.93 inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;

SIGNWAY			
Project:	E473060		
File:	10.RK3399 Flash&SDMMC Controler		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	10 of 32



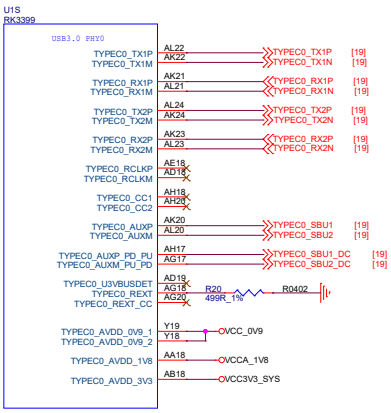
USB2.0

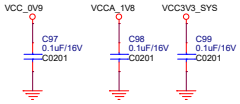


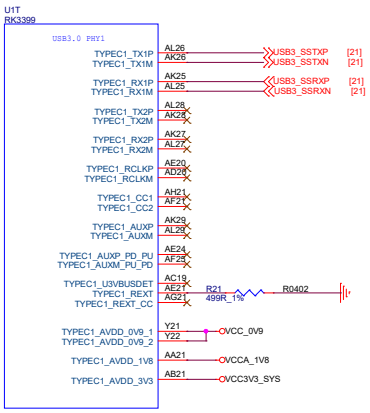


USB2.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals
follows the 3W rule;

USB3.0



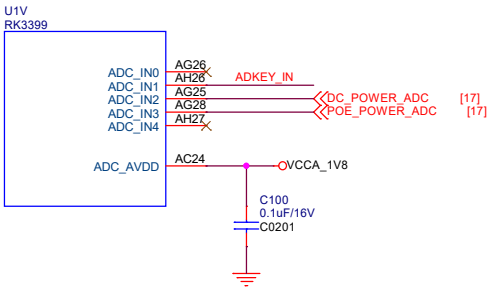


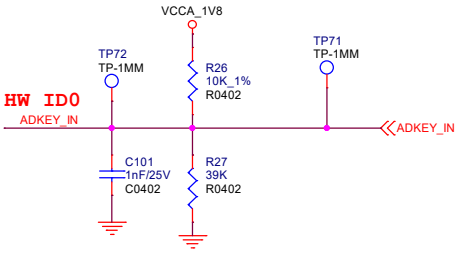


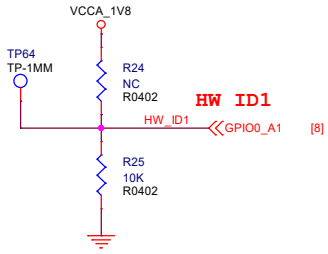
USB3.0 design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between TX and
RX < 1.6 ns;
3.Max trace length < 6 inchs;
4.Max allowed via < 4;
5.Trace impedance 90ohm+/-10%;
6.The distance between other signals
follows the 3W rule;

DP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals
follows the 3W rule;

SIGNWAY	
Project:	E473060
File:	11.RK3399 USB/USIC Controler
Date:	Friday, March 25, 2022
Rev:	A0
Designed by:	Zhangbo&Yangyin
Sheet:	11 of 32



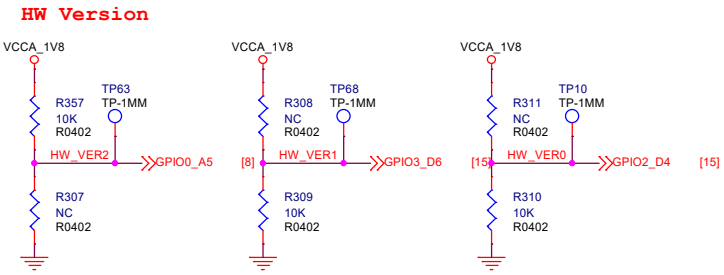




RK3399 project hardware ID definiton

ADC1 Function1: Hold on ZERO when AC plug in cold boot, enter Flash Image Mode.
ADC1 Function2: Secondary defininiton of product hardware ID.
GPIO0_A1: Main defininiton of of product hardware ID.

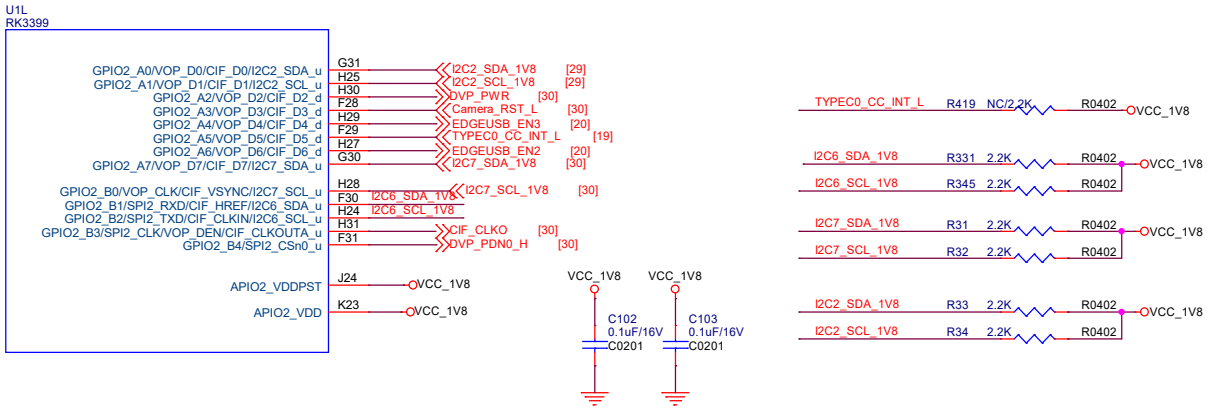
Seq.	GPIO0_A1	R27	ADC	HW ID	Date
01.	Low	NC	1.800V	E472673(15.6)	March 02, 2020
02.	Low	91K	1.622V	E472828(21.5)	
03.	Low	39K	1.433V	E473060(10.1)	
04.	Low	22K	1.238V	E473261(BACKPACK)	
05.	Low	13K	1.017V	E679524(USB-C)	
06.	Low	9.1K	0.858V	TBD	
07.	Low	6.2K	0.689V	TBD	
08.	Low	3.9K	0.505V	TBD	
09.	High	NC	1.800V	TBD	
10.	High	91K	1.622V	TBD	
11.	High	39K	1.433V	TBD	
12.	High	22K	1.238V	TBD	
13.	High	13K	1.017V	TBD	
14.	High	9.1K	0.858V	TBD	
15.	High	6.2K	0.689V	TBD	
16.	High	3.9K	0.505V	TBD	

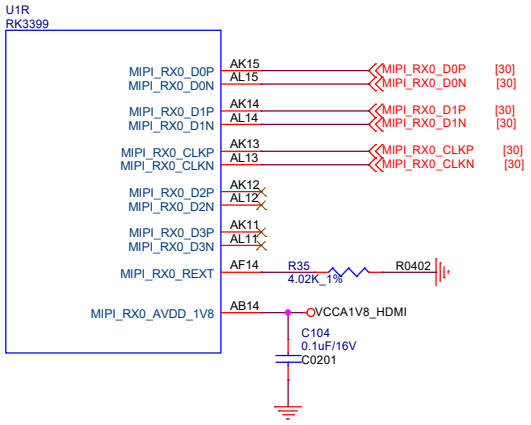


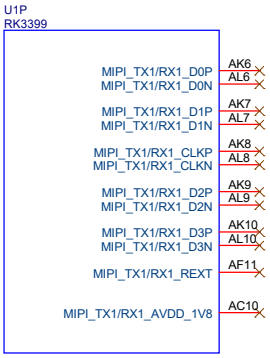
E473060 Hardware Version

Seq.	GPIO0_A5	GPIO3_D6	GPIO2_D4	HW Version	Date
01.	0	0	0	V1(EVT)	March 26, 2020
02.	0	0	1	V2	TBD
03.	0	1	0	V3	TBD
04.	0	1	1	V4	TBD
05.	1	0	0	V5	sep22.2021
06.	1	0	1	V6	TBD
07.	1	1	0	V7	TBD
08.	1	1	1	V8	TBD

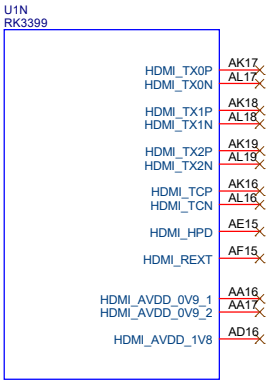
SIGNWAY			
Project:	E473060		
File:	12.RK3399 SARADC/Key		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	12 of 32



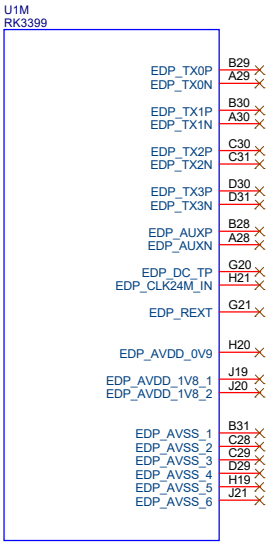




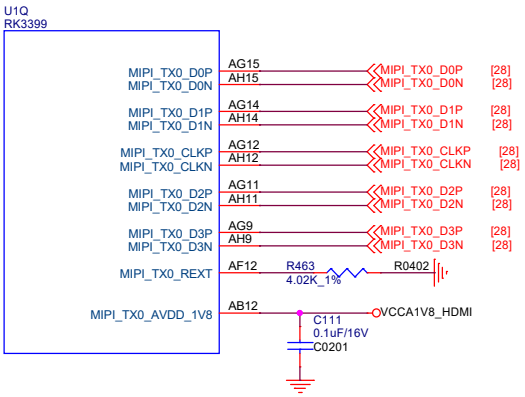
SIGNWAY	
Project:	E473060
File:	13.RK3399 DVP Interface
Date: Friday, March 25, 2022	Rev: A0
Designed by: Zhangbo&Yangyin	Sheet: 13 of 32



HDMI design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between clk and data < 80 ps;
3.Max trace length < 9.8 inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;



eDP design rule:
1.Max intra-pair skew < 4 ps;
2.Max trace length < 6 inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals
follows the 3W rule;



MIPI design rule:
1.Max intra-pair skew < 4 ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2 inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

SIGNWAY			
Project:	E473060		
File:	14.RK3399 Display Interface		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	14 of 32

U1I
RK3399
Note:RK3399 part I is 3.3V only

GPIO3_A0/MAC_TXD2/SPI4_RXD_d F24 MAC_TXD2 R39 22R R0402 PHY_TXD2 [24]
GPIO3_A1/MAC_TXD3/SPI4_TXD_d H23 MAC_TXD3 R40 22R R0402 PHY_TXD3 [24]
GPIO3_A2/MAC_RXD2/SPI4_CLK_u E30 MAC_RXD2 [24]
GPIO3_A3/MAC_RXD3/SPI4_CSn0_u E25 MAC_RXD3 [24]
GPIO3_A4/MAC_TXD0/SPI0_RXD_d D26 MAC_TXD0 R41 22R R0402 PHY_TXD0 [24]
GPIO3_A5/MAC_TXD1/SPI0_TXD_d G23 MAC_TXD1 R42 22R R0402 PHY_TXD1 [24]
GPIO3_A6/MAC_RXD0/SPI0_CLK_u E26 MAC_RXD0 [24]
GPIO3_A7/MAC_RXD1/SPI0_CSn0_u P27 MAC_RXD1 [24]

GPIO3_B0/MAC_MDC/SPI0_CSn1_u E29 MAC_MDC [24]
GPIO3_B1/MAC_RXDV_d C27 MAC_RXDV [24]
GPIO3_B2/MAC_RXER/I2C5_SDA_u F23 GPIO1_TP [21]
GPIO3_B3/MAC_CLK/I2C5_SCL_u G24 MAC_CLK_RX R43 0R R0402 MAC_CLK [24]
GPIO3_B4/MAC_TXEN/UART1_RX_u H22 MAC_TXEN R44 22R R0402 PHY_TXEN [24]
GPIO3_B5/MAC_MDIO/UART1_TX_u G26 MAC_MDIO [24]
GPIO3_B6/MAC_RXCLK/UART3_RX_u F25 MAC_RXCLK [24]
GPIO3_B7/MAC_CRS/CIF_CLKOUTB/UART3_TX_u B27 PHY_RST [24]

GPIO3_C0/MAC_COL/UART3_CTSn/SPDIF_TX_u D27
GPIO3_C1/MAC_TXCLK/UART3_RTSn_u E28 MAC_TXCLK R45 22R R0402 GPIO2_TP [21] PHY_TXCLK [24]

C113 120R C0402
C663 NC C0402

APIO1_VDDPST J22 VCC1V8
APIO1_VDD J23 VCC3V3_LAN

VCC3V3_S0 L53 FB_60R_0603 L0603 VCC3V3_LAN
C114 0.1uF/16V C0201
C115 0.1uF/16V C0201

PHY_TXD0 R46 4.7K R0402 VCC3V3_LAN
PHY_TXD1 R47 4.7K R0402
PHY_TXD2 R48 4.7K R0402
PHY_TXD3 R49 4.7K R0402
MAC_MDIO R50 1.5K R0402

保留磁珠，通过修改PMU芯片供电方案解决漏电问题
L53修改为PMOS开关，防止漏电

U1E
RK3399
Note:RK3399 part E is 1.8V/3.0V mode
PART E 3V

GPIO1_A0/ISP0_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD_VBUS_SINK_EN_d R25
GPIO1_A1/ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CC0_VCONN_EN_d T27
GPIO1_A2/ISP0_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCPD_CC1_VCONN_EN_d R26
GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT_d R27
GPIO1_A4/ISP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG_d R28
GPIO1_A5/AP PWROFF_d R30
GPIO1_A6/TSADC_INT_z P26
GPIO1_A7/SPI1_RXD/UART4_RX_u P27

GPIO1_B0/SPI1_TXD/UART4_TX_u R31
GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK_u P28
GPIO1_B2/SPI1_CSn0/PMCU_JTAG_TMS_u P29
GPIO1_B3/I2C4_SDA_u P31
GPIO1_B4/I2C4_SCL_u P30
GPIO1_B5_d M24
GPIO1_B6/PWM3B_IR_d M25
GPIO1_B7/SPI3_RXD/I2C0_SDA_u M26

GPIO1_C0/SPI3_TXD/I2C0_SCL_u N30
GPIO1_C1/SPI3_CLK_d M27
GPIO1_C2/SPI3_CSn0_u N31
GPIO1_C3/PWM2_d M28
GPIO1_C4/I2C8_SDA_u M29
GPIO1_C5/I2C8_SCL_u M30
GPIO1_C6/TCPD_VBUS_SOURCE0_d L25
GPIO1_C7/TCPD_VBUS_SOURCE1_d M31

GPIO1_D0/TCPD_VBUS_SOURCE2_d L26

DFTJTAG_TMS_u AA24
DFTJTAG_TRSTn_d AB24

PMUIO2_VDDPST N23 VCC1V5
PMUIO2_VDD P23 VCC3V0

TP_RST [21]
TP_INT [21]
HUB_RST1 [20]
PD_TYPEC0_EN [19]
PMIC_SLEEP_H [18]
OTP_OUT_H [18]
ID1_3V0 [20]

ID2_3V0 [20]
ID3_3V0 [20]
ID4_3V0 [20]
I2C4_SDA [29]
I2C4_SCL [29]
EX_5V_EN [17]
GPI2_SLEEP_H [18]
I2C_SDA_PMIC [18,29]

I2C_SCL_PMIC [18,29]
CPU_B_SLEEP_H [18]
LED_STATE [18]
LOG_DVS_PWM [18]
EDP_POWDN [28]
PMIC_INT_L [18]
GPIO1_3V0 [27]
GPIO2_3V0 [27]

PD_VBUS_TYPEC0_EN [19]

1.8V Only	VDDPST=VDDIO=1.8V
3.3V Only	VDDPST=1.8V,VDDIO=3.3V
other	3.0V mode:VDDPST=1.5V,VDDIO=3.0V 1.8V mode:VDDPST=1.8V,VDDIO=1.8V

VCC_1V5 C116 0.1uF/16V C0201
VCC_3V0 C117 0.1uF/16V C0201

I2C_SDA_PMIC R51 2.2K R0402 VCC_3V0
I2C_SCL_PMIC R52 2.2K R0402
I2C4_SDA R53 2.2K R0402 VCC_3V0
I2C4_SCL R54 2.2K R0402

U1G
RK3399
Note:RK3399 part G is 1.8V only

GPIO2_C0/UART0_RX_u AE9 UART0_RXD [23]
GPIO2_C1/UART0_TX_u AH8 UART0_TXD [23]
GPIO2_C2/UART0_CTSn_u AG8 UART0_CTS [23]
GPIO2_C3/UART0_RTSn_u AL5 UART0_RTS [23]
GPIO2_C4/SDIO0_D0/SPI5_RXD_u AD8 SDIO0_D0 [23]
GPIO2_C5/SDIO0_D1/SPI5_TXD_u AK5 SDIO0_D1 [23]
GPIO2_C6/SDIO0_D2/SPI5_CLK_u AG7 SDIO0_D2 [23]
GPIO2_C7/SDIO0_D3/SPI5_CSn0_u AE8 SDIO0_D3 [23]

GPIO2_D0/SDIO0_CMD_u AH6 SDIO0_CMD [23]
GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1_u AF7 SDIO0_CLK [23]
GPIO2_D2/SDIO0_DETN/PCIE_CLKREQn_u AL4 GSENSOR_INT_L_1V8 [29]
GPIO2_D3/SDIO0_PWREN_d AD9 SPI_WAKE_L [23]
GPIO2_D4/SDIO0_BKPWR_d AF8 GPIO2_D4 [12]

APIO3_VDD_1V8 AB8 VCC_1V8

SDIO design rule:
1.Data[0:7] and CMD signals routing parallel as a group, the skew between each other must be less than 100mils;
2.The Clock signal should be isolated with other signals by GND plane, the skew between data lines is less than 20ps;
3.Max trace length < 3.93 inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;

VCC_1V8 C118 0.1uF/16V C0201
VCC_1V8 R542 2.2K R0402 GSENSOR_INT_L_1V8 [29]
Reserve for Pull-up

U1J
RK3399
Note:RK3399 part J is 1.8V/3.0V mode
PART J 1.8V

GPIO3_D0/I2S0_SCLK_d AG3 I2S0_SCLK [26]
GPIO3_D1/I2S0_LRCK_RX_d AF4 I2S0_LRCK_RX [26]
GPIO3_D2/I2S0_LRCK_TX_d AJ2 I2S0_LRCK_TX [26]
GPIO3_D3/I2S0_SDI0_d Y7 I2S0_SDI0 [26]
GPIO3_D4/I2S0_SDI1SDO3_d AE5 LAN_POWER_EN [24]
GPIO3_D5/I2S0_SDI2SDO2_d AA6 RESX_1V8 [28]
GPIO3_D6/I2S0_SDI3SDO1_d AH2 GPIO3_D6 [12]
GPIO3_D7/I2S0_SDO0_d AH1 I2S0_SDO0 [26]

GPIO4_A0/I2S_CLK_d AC7 I2S_MCLK [26]
GPIO4_A1/I2C1_SDA_u AG1 I2C1_SDA_1V8 [19,20,26]
GPIO4_A2/I2C1_SCL_u Y6 I2C1_SCL_1V8 [19,20,26]
GPIO4_A3/I2S1_SCLK_d AF3 I2S1_SCLK [23]
GPIO4_A4/I2S1_LRCK_RX_d AA7 I2S1_LRCK_RX [23]
GPIO4_A5/I2S1_LRCK_TX_d AJ1 VCC5V0_USB1 [21]
GPIO4_A6/I2S1_SDI0_d AD6 I2S1_SDI0 [23]
GPIO4_A7/I2S1_SDO0_d AC6 I2S1_SDO0 [23]

APIO5_VDDPST AA8 VCC1V8_CODEC
APIO5_VDD Y8 VCC1V8_CODEC

I2C1_SDA_1V8 R57 2.2K R0402 VCC1V8_CODEC
I2C1_SCL_1V8 R58 2.2K R0402

VCC1V8_CODEC C119 0.1uF/16V C0201
VCC1V8_CODEC C120 0.1uF/16V C0201

U1K
RK3399
Note:RK3399 part K is 1.8V/3.0V mode

GPIO4_C0/I2C3_SDA/UART2B_RX_u AG6 I2C3_SDA [21]
GPIO4_C1/I2C3_SCL/UART2B_TX_u AL2 I2C3_SCL [21]
GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM_d AF5 MIPI_PWM [28]
GPIO4_C3/UART2C_RX_u AK2 UART2DBG_RX UART2DBG_RX [27]
GPIO4_C4/UART2C_TX_u AJ4 UART2DBG_TX UART2DBG_TX [27]
GPIO4_C5/SPDIF_TX_d AK1 AMP_MUTE [26]
GPIO4_C6/PWM1_d AL3 YLED [25]
GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG_u AD7

GPIO4_D0/PCIE_CLKREQnB_u AE6 WLED [25]
GPIO4_D1/DP_HOTPLUG_d AK4 GPIO3_3V0_EN [27]
GPIO4_D2_d AH3 POE_DET_OUT [24]
GPIO4_D3_d AK3 EFUSE_VOPS_EN_H [32]
GPIO4_D4_d AH5 EDGEUSB_EN4 [20]
GPIO4_D5_d AJ3 EDGEUSB_EN1 [20]
GPIO4_D6_d AG4 CAMERA_AF_EN [30]

APIO4_VDDPST AC8 VCC_1V5
APIO4_VDD AC9 VCC_3V0

UART2DBG_RX R55 22R R0402
UART2DBG_TX R56 22R R0402

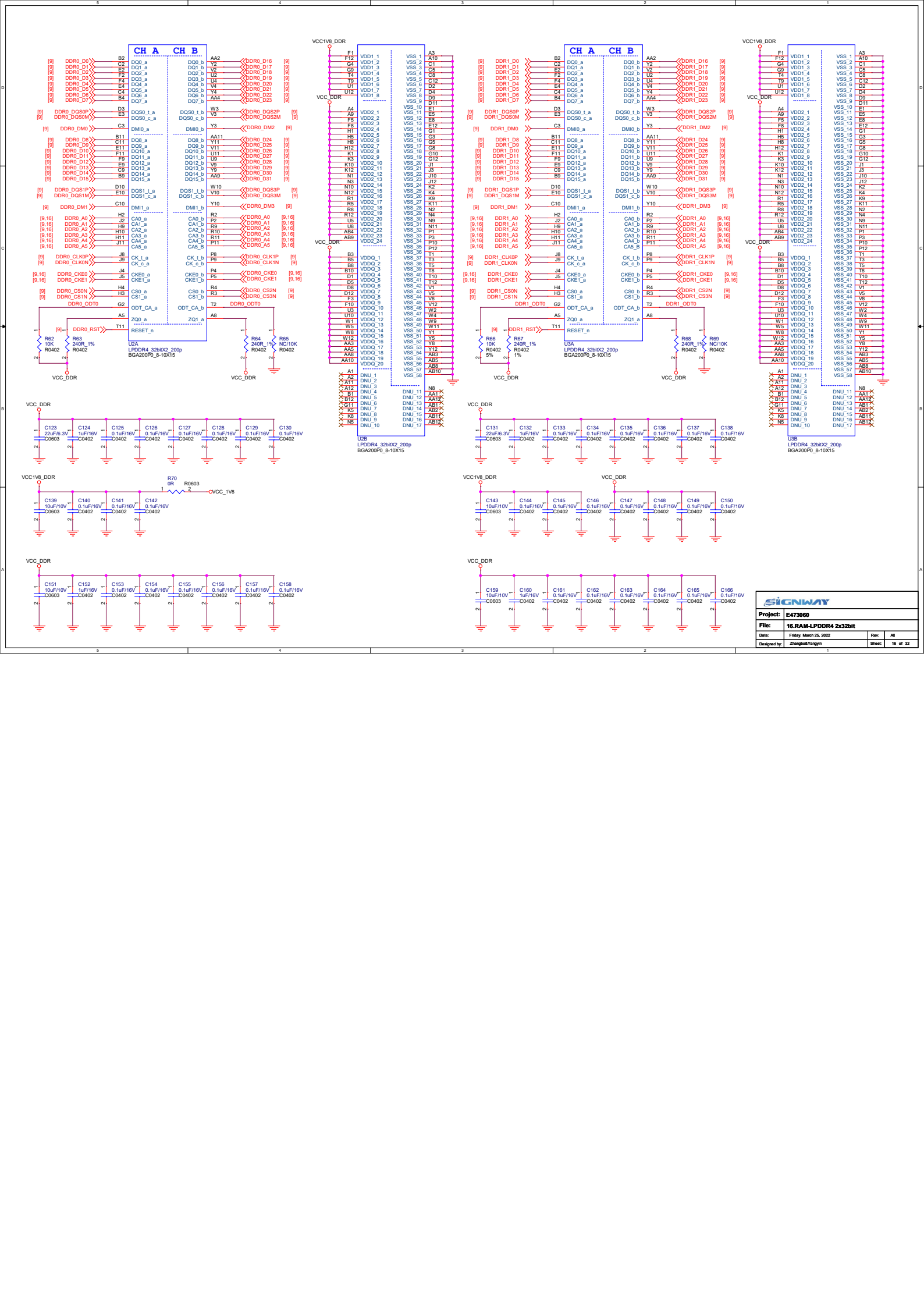
CON99
NC/CON3P2.0
CON3P2_0-1X3H-DIP
1 2 3

F1 TESD05CB esd0402
F2 TESD05CB esd0402

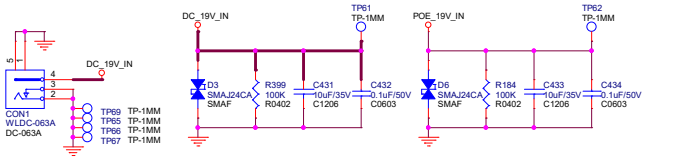
I2C3_SDA R59 2.2K R0402 VCC_3V0
I2C3_SCL R60 2.2K R0402

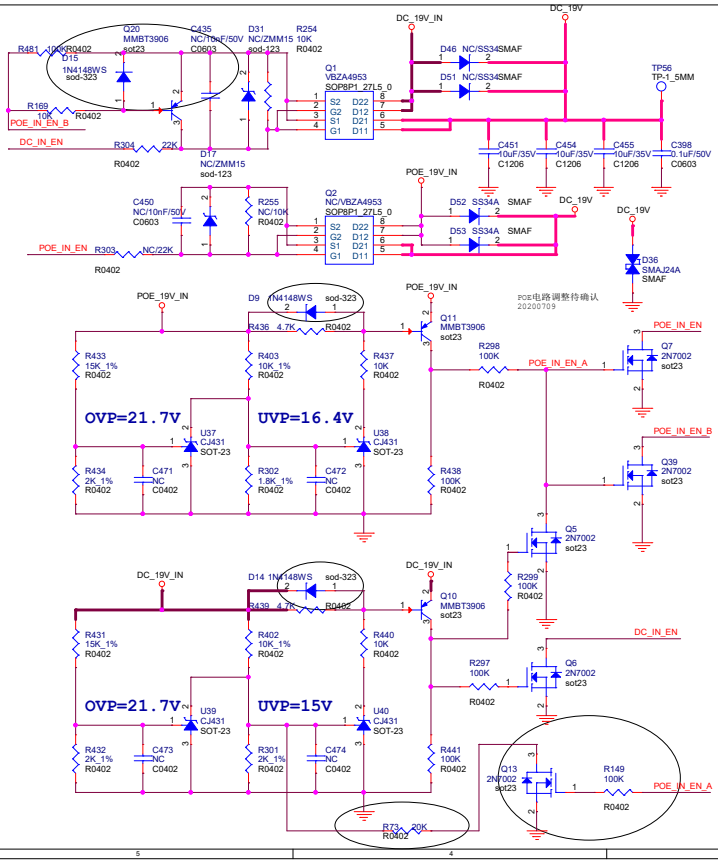
VCC_1V5 R61 10K R0402 C121 0.1uF/16V C0201
VCC_3V0 C122 0.1uF/16V C0201

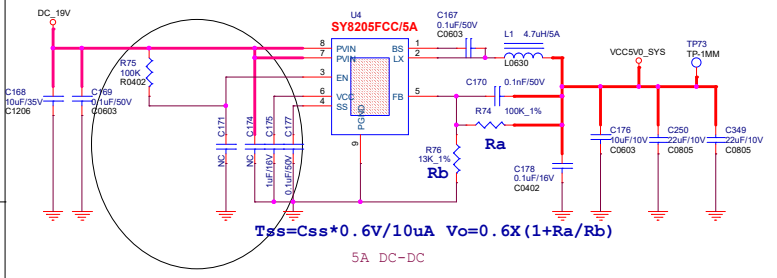
SIGNWAY
Project: E473060
File: 15.RK3399 GPIO
Date: Friday, March 25, 2022 Rev: A0
Designed by: ZhangkaiYangjin Sheet: 15 of 32

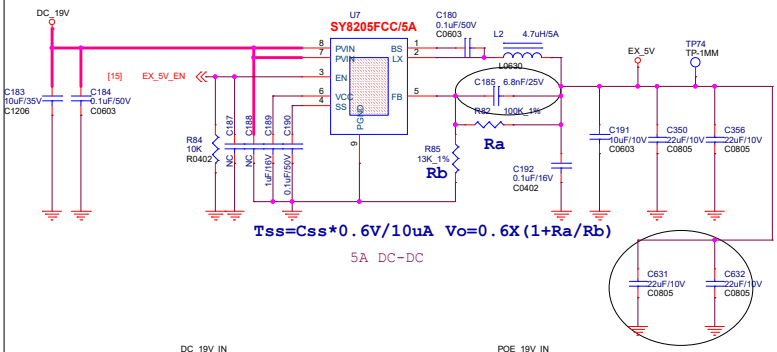

CH A
CH B
U2A
LPDDR4_32bitX2_200p
BGA200P0_8-10X15
U2B
LPDDR4_32bitX2_200p
BGA200P0_8-10X15
U3A
LPDDR4_32bitX2_200p
BGA200P0_8-10X15
U3B
LPDDR4_32bitX2_200p
BGA200P0_8-10X15
VCC1V8_DDR
VCC_DDR
VCC_1V8
DDR0_RST
DDR1_RST
DDR0_ODT0
DDR1_ODT0
R62 10K R0402
R63 240R_1% R0402
R64 240R_1% R0402
R65 NC/10K R0402
R66 10K R0402 5%
R67 240R_1% R0402 1%
R68 240R_1% R0402
R69 NC/10K R0402
R70 0R R0603
SIGNWAY
Project: E473060
File: 16.RAM-LPDDR4 2x32bit
Date: Friday, March 25, 2022
Rev: A0
Designed by: Zhanghb&Yangyin
Sheet: 16 of 32

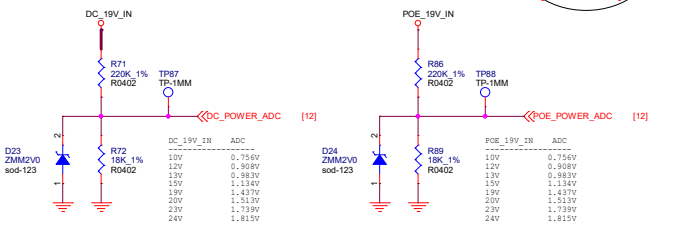
DC IN&SYSTEM Power



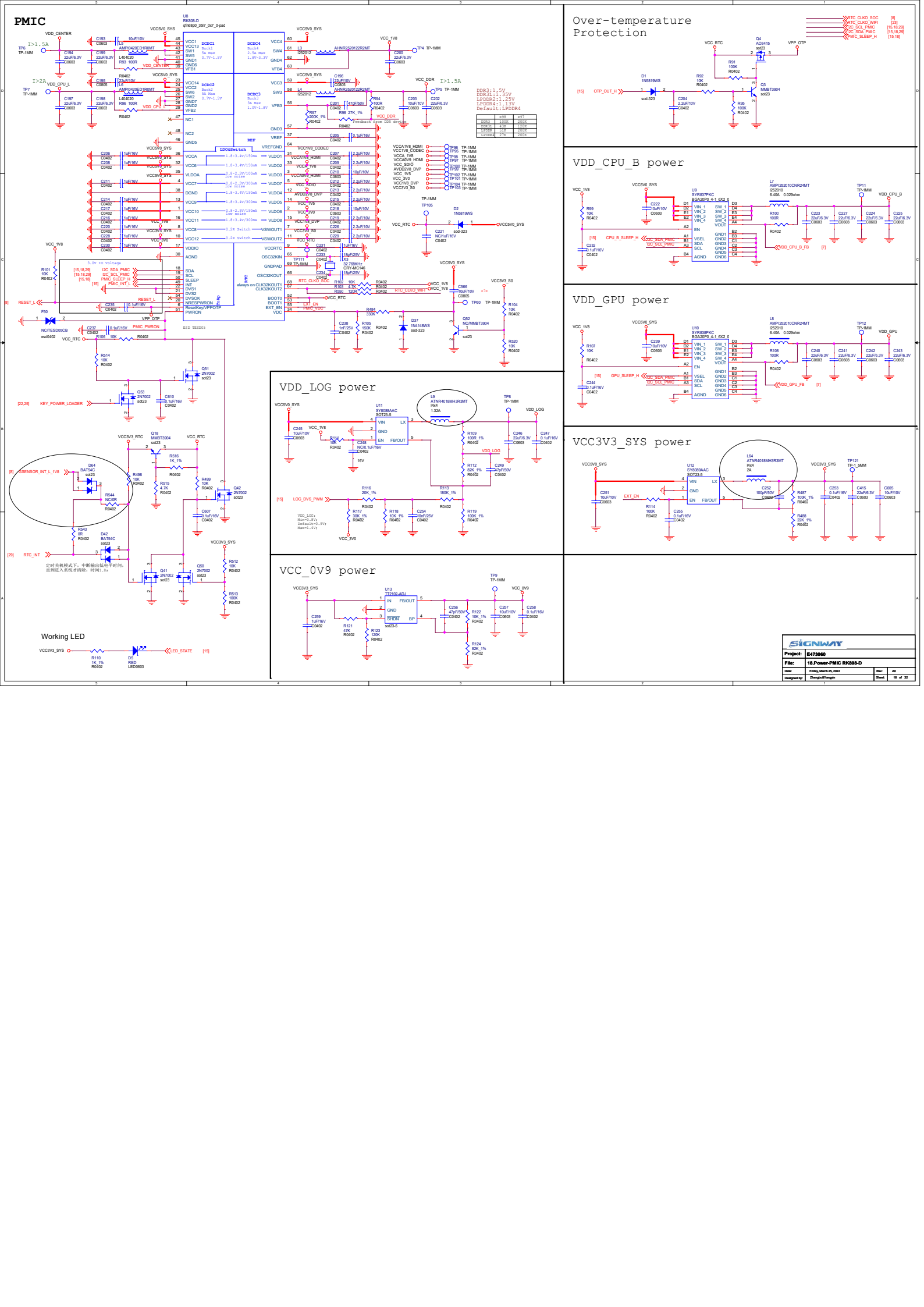




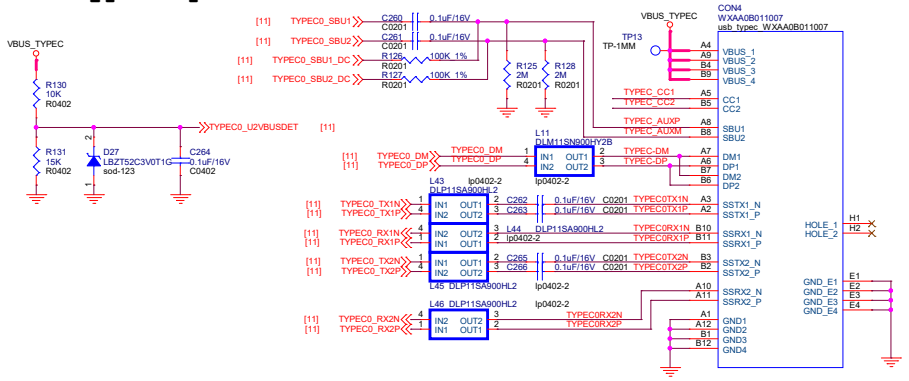




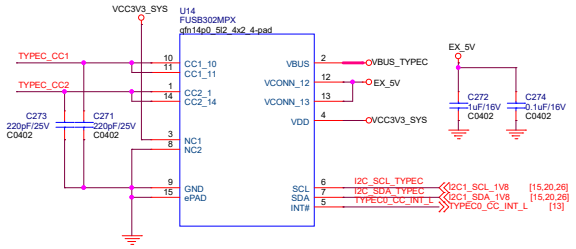
SIGNWAY	
Project:	E473060
File:	17.Power-DC IN&POWER SW
Date:	Friday, March 25, 2022
Rev:	A0
Designed by:	Zhanglbo&Yangyin
Sheet:	17 of 32


PMIC
U8
RK808-D
qfn68p0_3S7_0x7_0-pad
VCC5V0_SYS
VCC_1V8
VCC_CENTER
VCC_CPU_L
VCC_DDR
VCC_RTC
VCC3V3_SYS
VCC3V3_S0
VDD_CPU_B
VDD_GPU
VDD_LOG
VCC_0V9
DCDC1
DCDC2
DCDC3
DCDC4
LDO&Switch
REF
RTC_CLKO_SOC
RTC_CLKO_WIFI
I2C_SCL_PMIC
I2C_SDA_PMIC
PMIC_SLEEP_H
Over-temperature Protection
VPP_OTP
OTP_OUT_H
VDD_CPU_B power
VDD_GPU power
VCC3V3_SYS power
VDD_LOG power
VCC_0V9 power
Working LED
LED_STATE
KEY_POWER_LOADER
RESET_L
PMIC_PWRON
RTC_INT
GSENSOR_INT_L_1V8
定时关机模式下，中断输出低电平时间，直到进入系统才消除，时间1.ss
SIGNWAY
Project: E473060
File: 18.Power-PMIC RK808-D
Date: Friday, March 25, 2022
Rev: A0
Designed by: ZhangboXiYangyin
Sheet 18 of 32

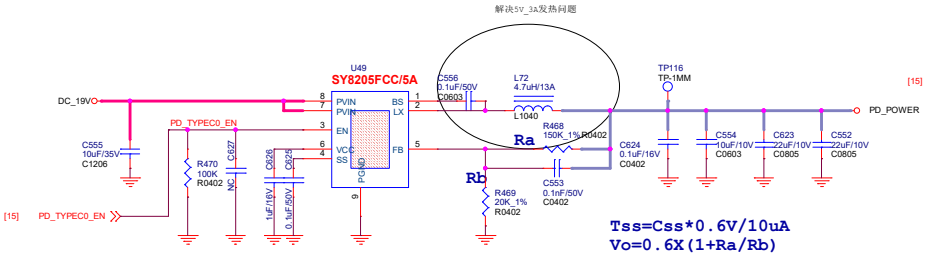
USB Type-C port



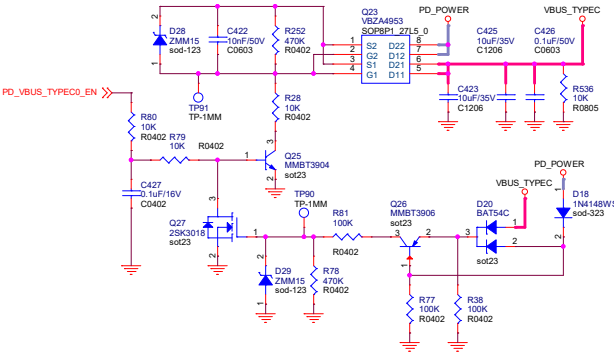
CC CTRL



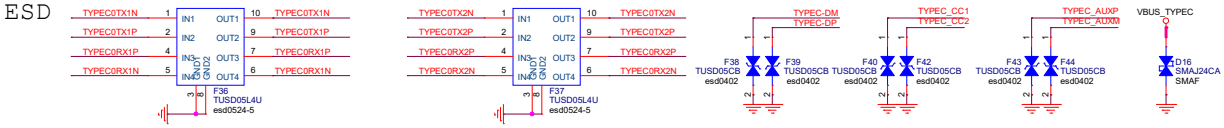
PD POWER



Type-C VBUS Switch



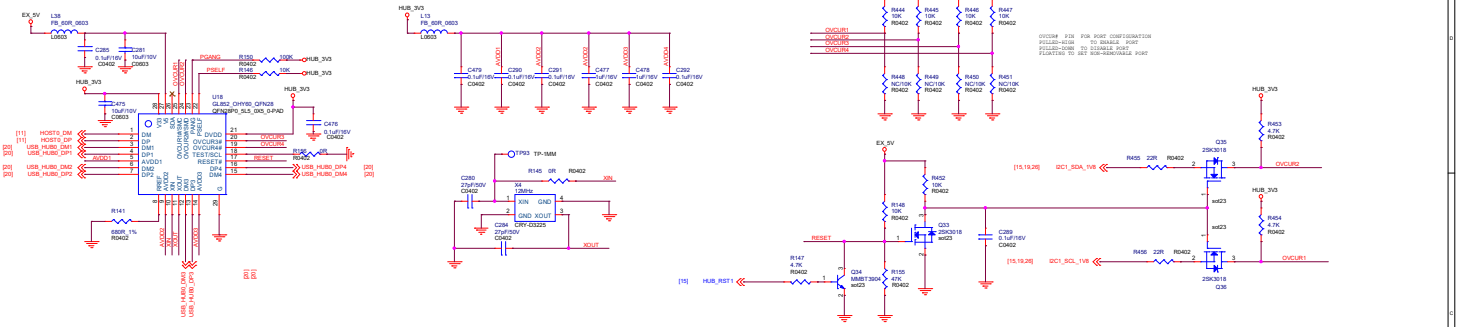
ESD



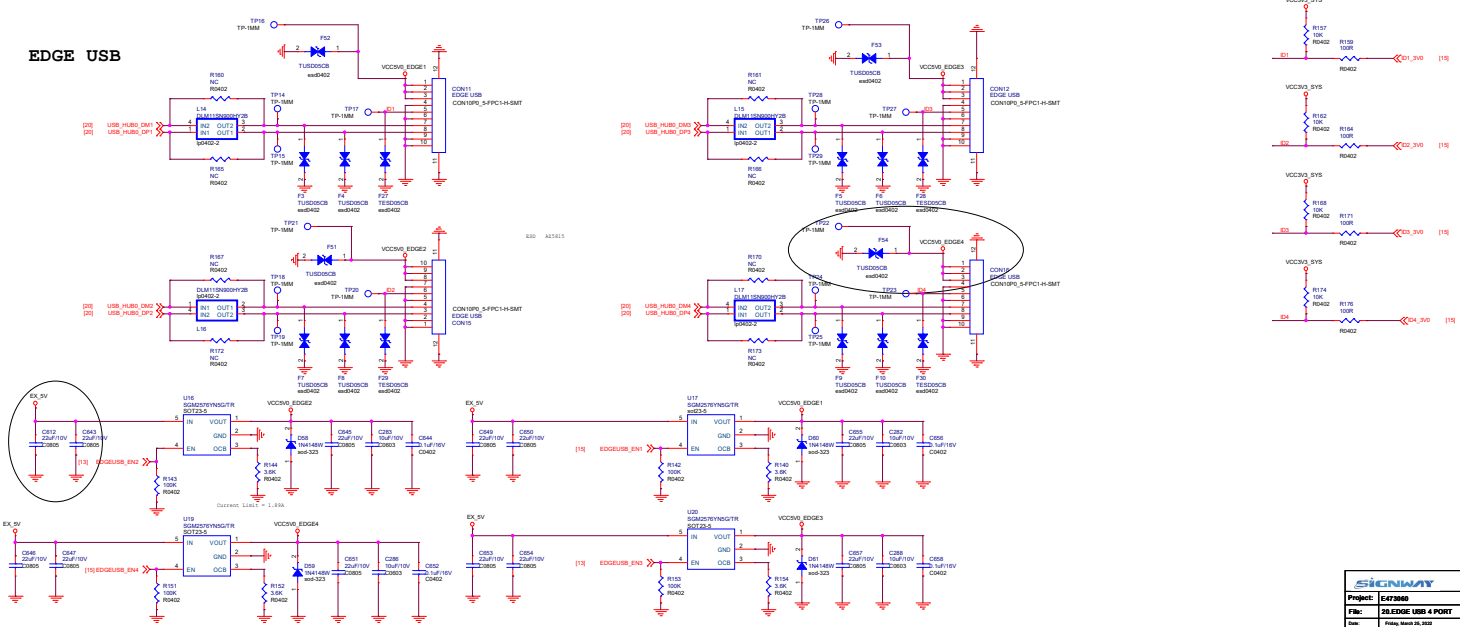
SIGNWAY	
Project:	E473060
File:	19.TYPE-C
Date:	Friday, March 25, 2022
Rev:	A0
Designed by:	Zhanghb5Yangyin
Sheet:	19 of 32

USB2.0 HUB

SMBUS ADDRESS : 0X2C



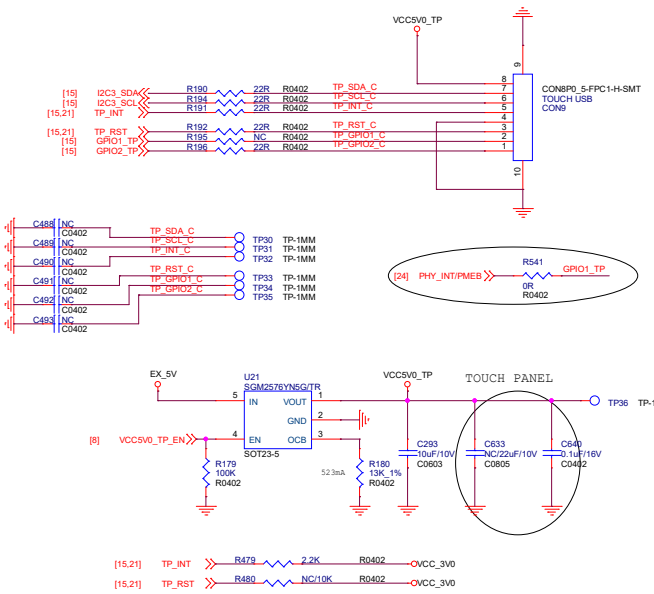
EDGE USB



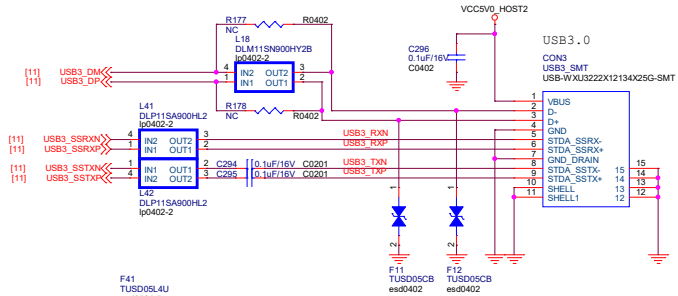
Project:	E473960
File:	35.EDGE USB 4 PORT
Date:	Friday, March 26, 2020
Rev:	A0
Designed by	ZhangkaiShangyin
Sheet	35 of 52

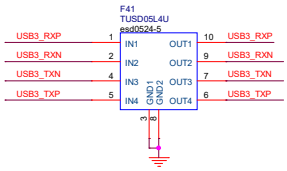
Touch Panel

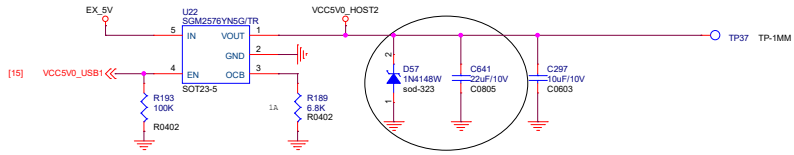
10.1' TOUCH



USB3.0 port

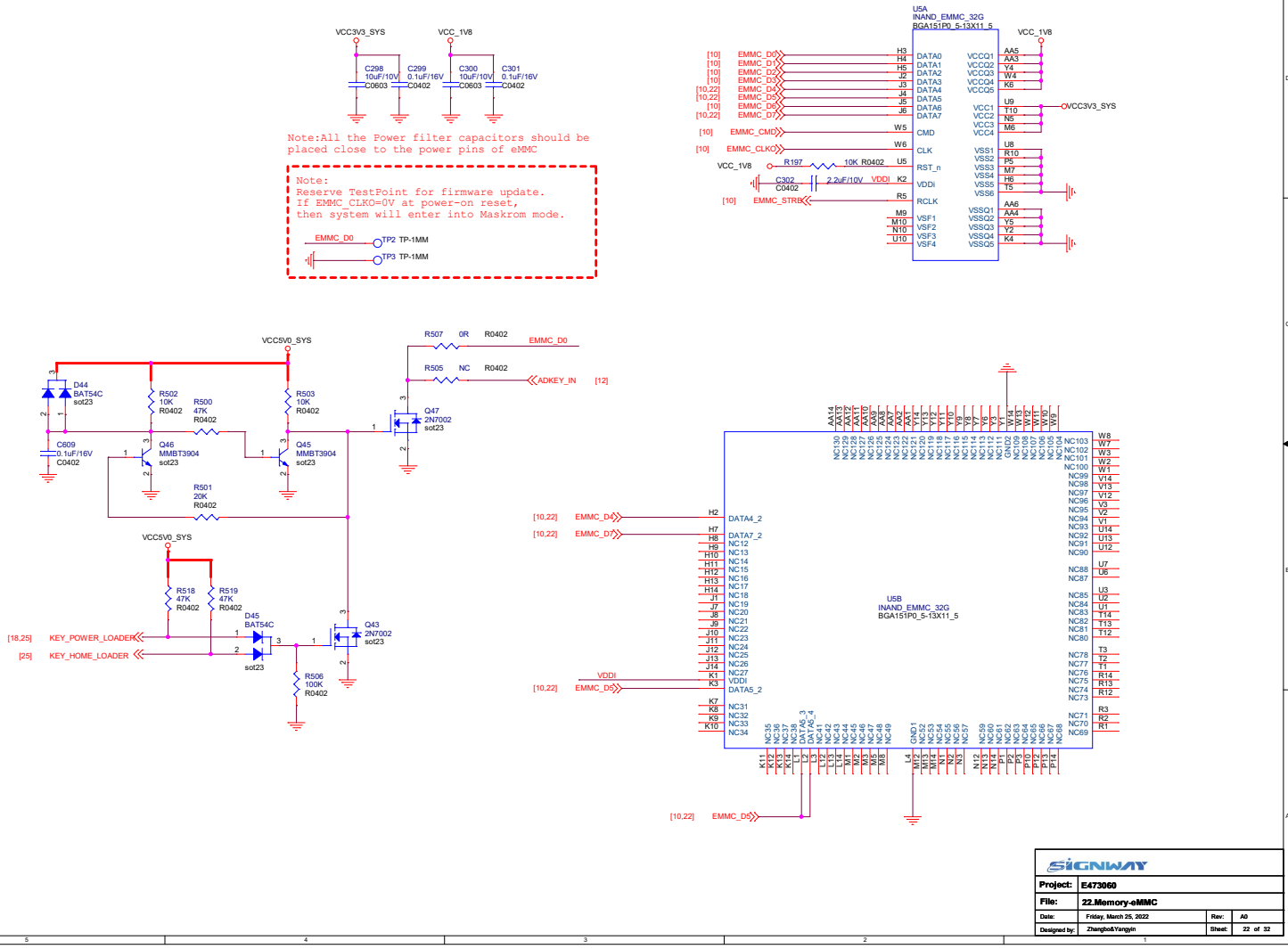






SIGNWAY			
Project:	E473060		
File:	21.USB 3.0HOST &TP		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhanghb&Yangyin	Sheet:	21 of 32

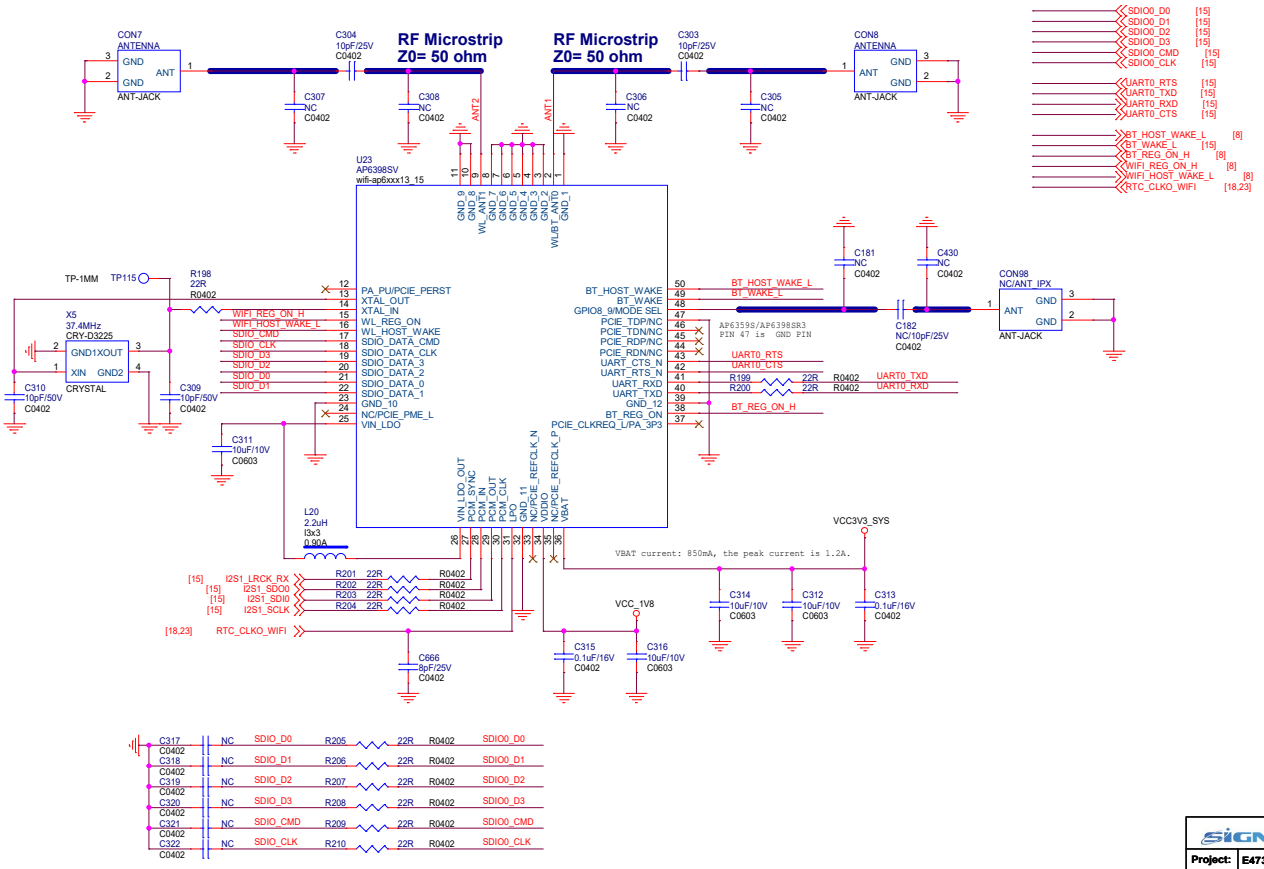
eMMC FLASH



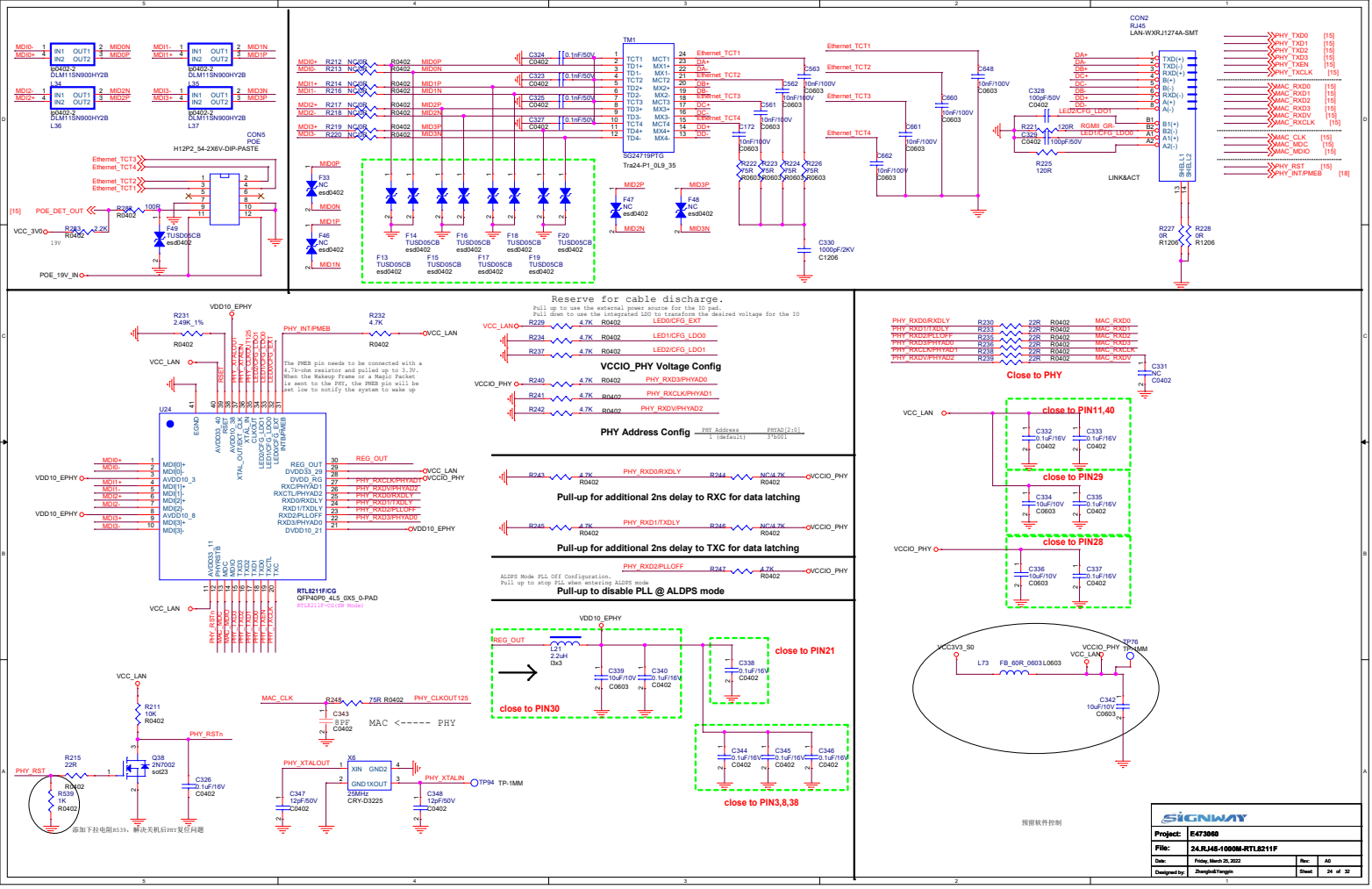
SIGNWAY			
Project:	E473060		
File:	22.Memory-eMMC		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhanghb&Yangyin	Sheet:	22 of 32

SDIO WIFI/BT MODULE-MIMO

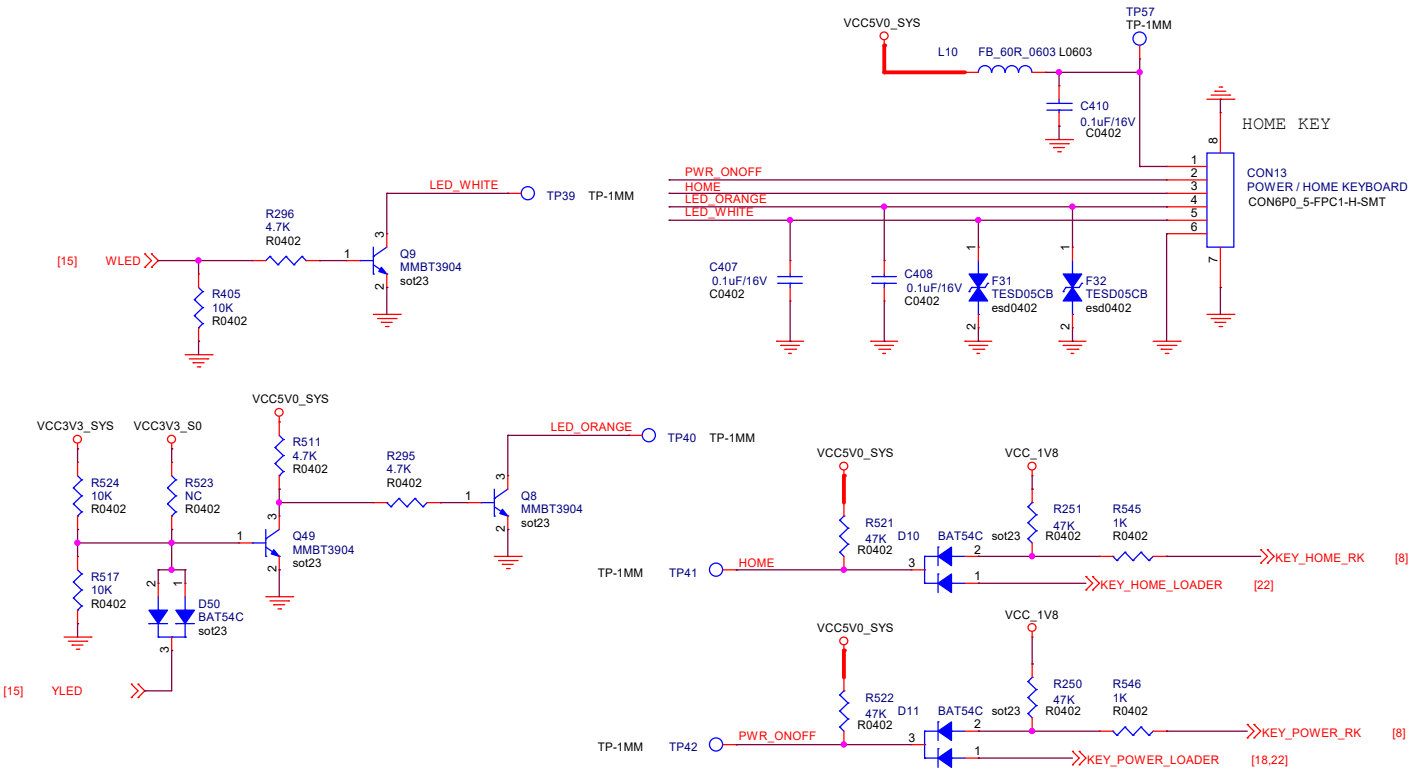
Note:VBAT power supply range is 3.0V~4.8V.



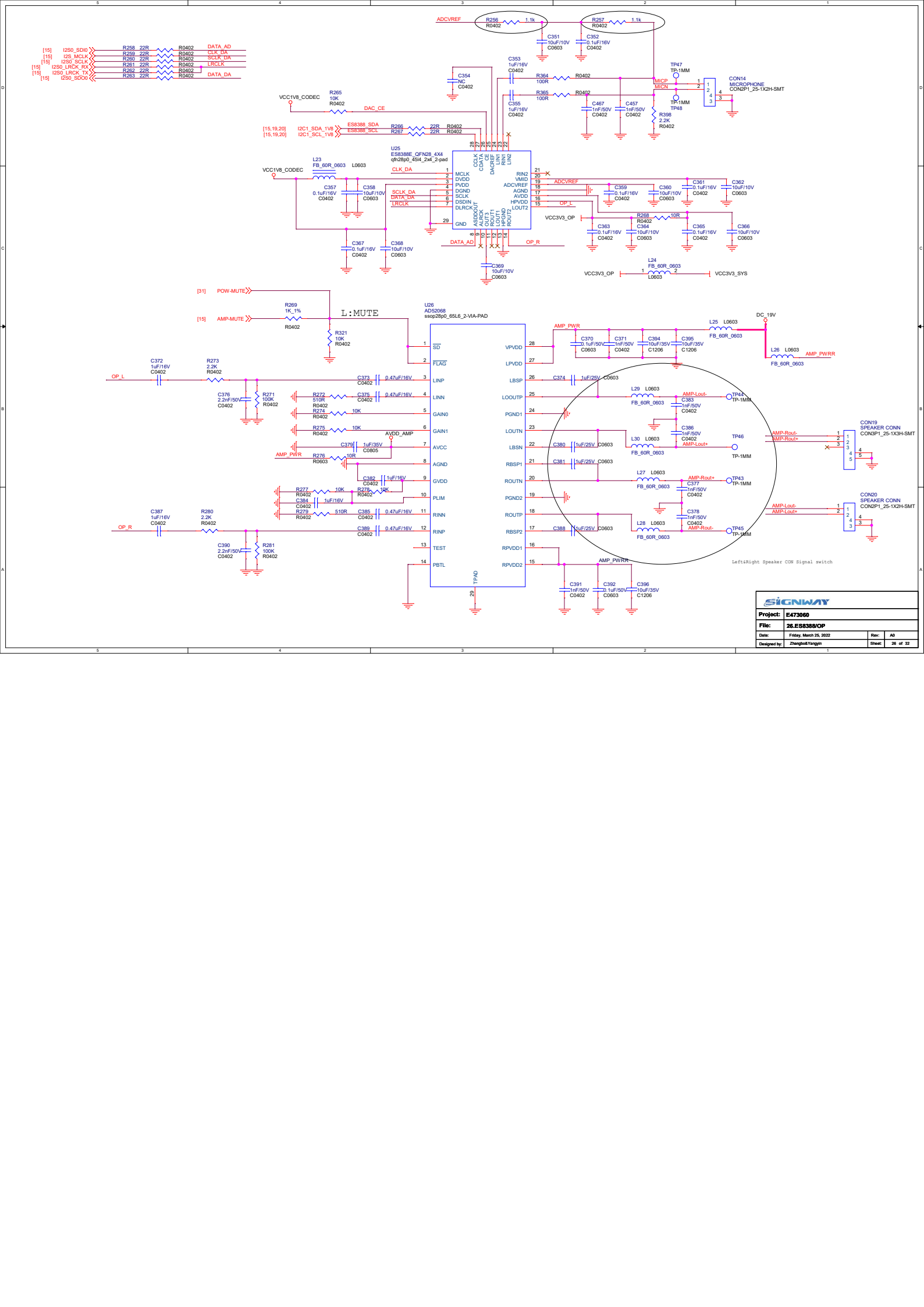
Project:	E473060
File:	23.WIFI/BT-AP6398SV
Date:	Friday, March 25, 2022
Rev:	A0
Designed by:	Zhanghb&Yangyin
Sheet	23 of 32



Project:	E473068
File:	24.RJ45-1000M-RTL8211F
Date:	Friday, March 25, 2022
Rev:	A0
Designed by:	Zhanghuifeng
Sheet:	24 of 32



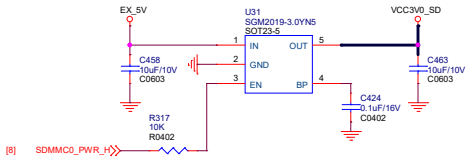
Project:	E473060
File:	25.LED/KEY
Date:	Friday, March 25, 2022
Rev:	A0
Designed by:	Zhangbo&Yangyin
Sheet:	25 of 32

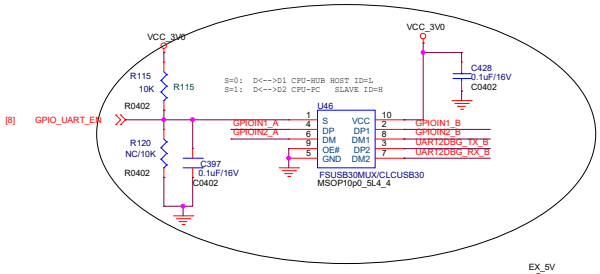


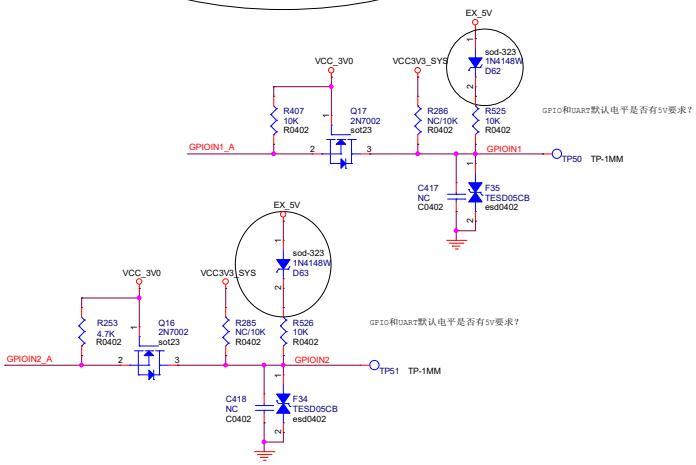
SIGNWAY	
Project:	E473060
File:	26.ES8388/OP
Date:	Friday, March 25, 2022
Rev:	A0
Designed by:	Zhanghb&Yangyin
Sheet:	26 of 32

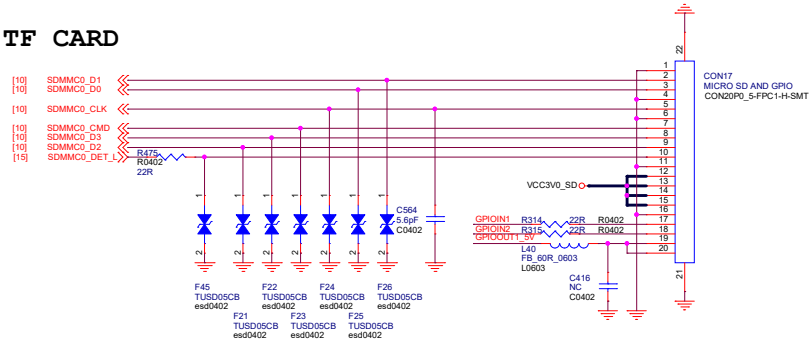
TF CARD

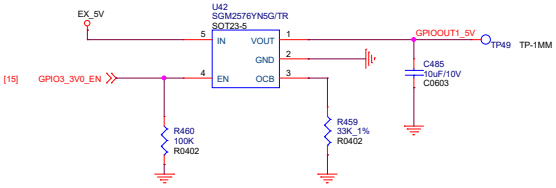
VCC3V0_SD power



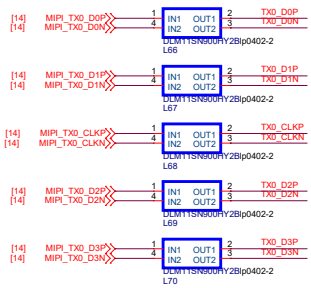


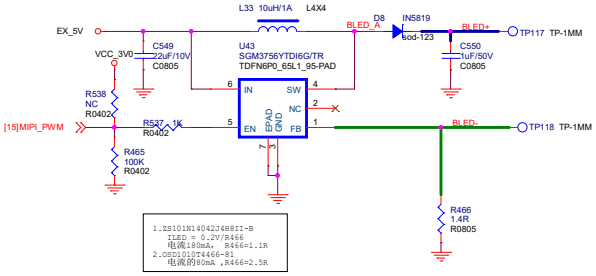


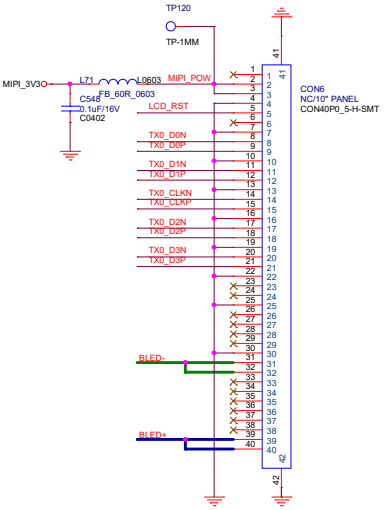


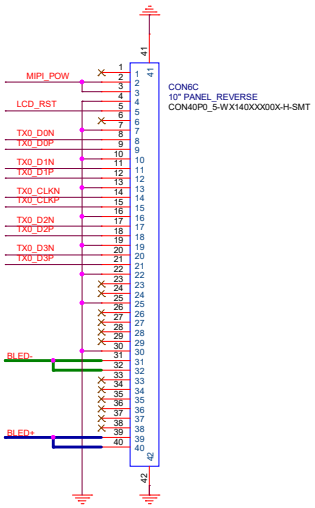


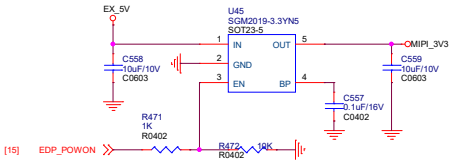
SIGNWAY	
Project:	E473060
File:	27.TF Card/GPIO
Date:	Friday, March 25, 2022
Rev:	A0
Designed by:	Zhanghb&Yangyin
Sheet:	27 of 32

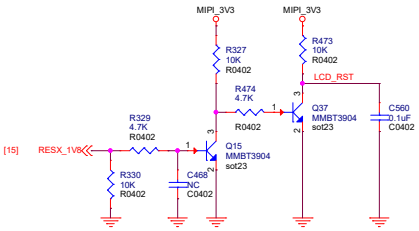








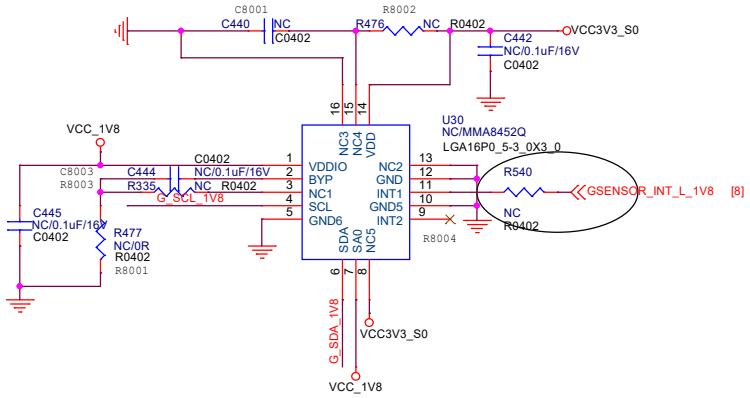


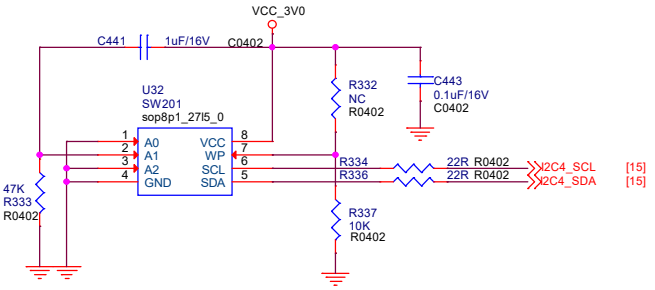


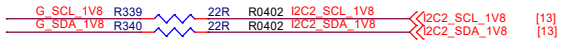
SIGNWAY	
Project:	E473060
File:	28.MIPI Dispaly
Date: Friday, March 25, 2022	Rev: A0
Designed by: Zhanghb&Yangyin	Sheet: 28 of 32

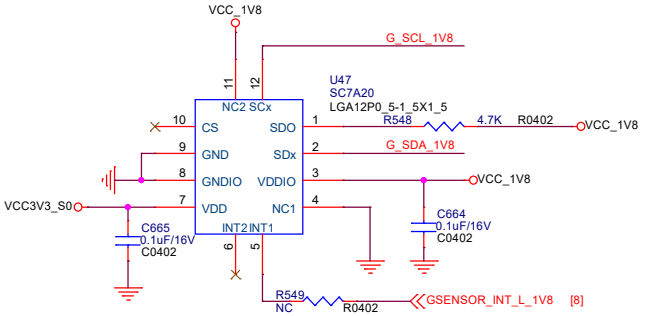
	LIS3DH	MMA8452Q	LSM303D
C8001	NC	NC	4.7uF
R8002	0ohm	NC	NC
R8001	NC	0ohm	NC
C8003	NC	0.1uF	0.22uF
R8003	NC	NC	0R
R8004	NC	NC	0R

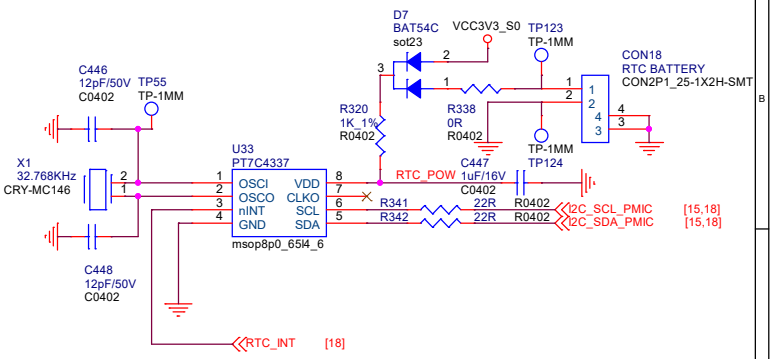
The MMA8452Q's standard slave address is a choice between the two sequential addresses 0011100 and 0011101. The selection is made by the high and low logic level of the SA0 (pin 7) input respectively. The slave addresses are factory programmed and alternate addresses are available at customer request



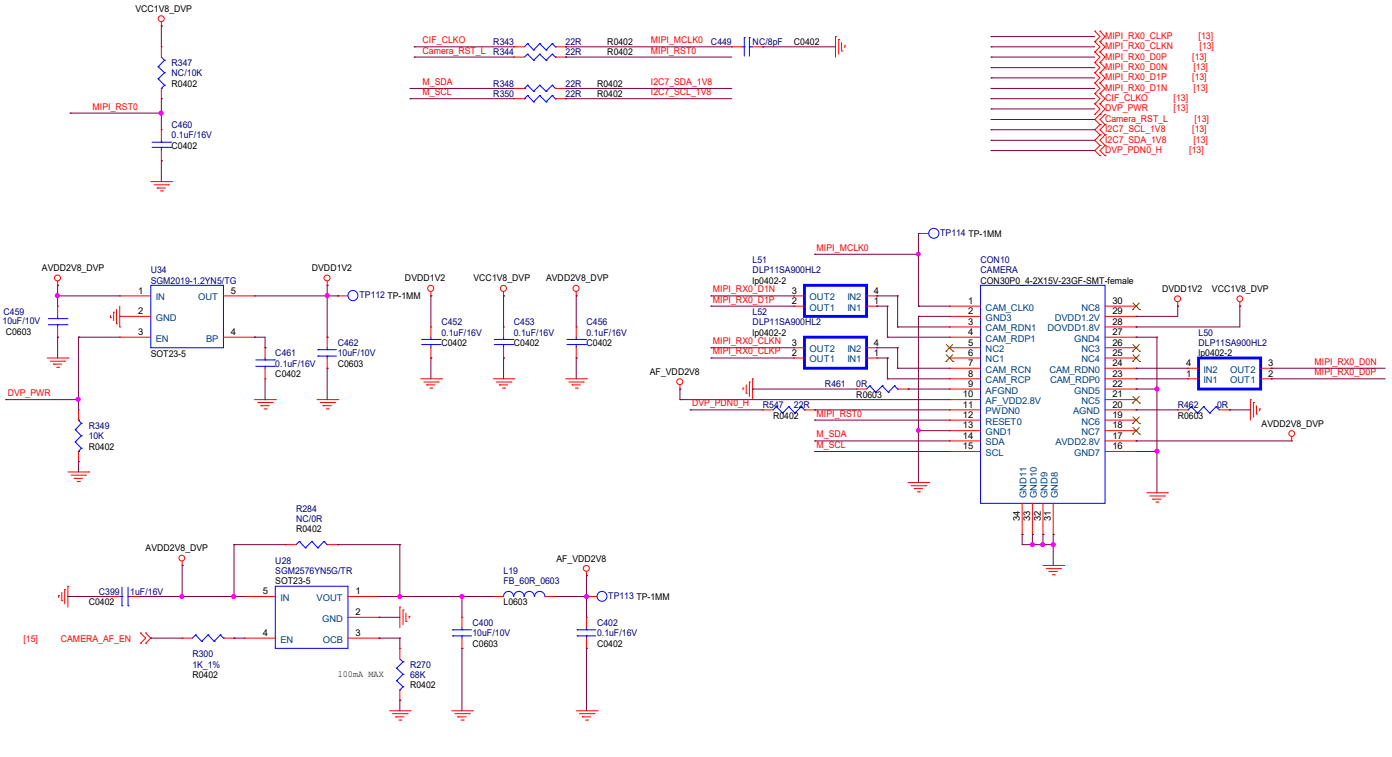




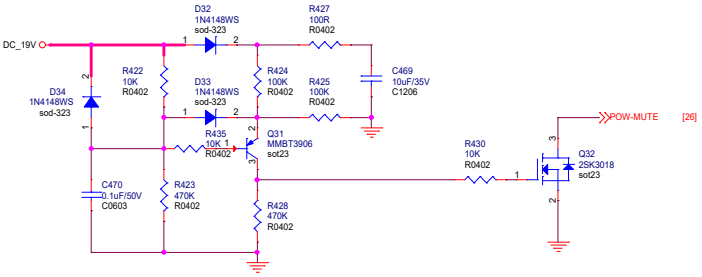




SIGNWAY			
Project:	E473060		
File:	29.G-sensor&RTC		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	29 of 32



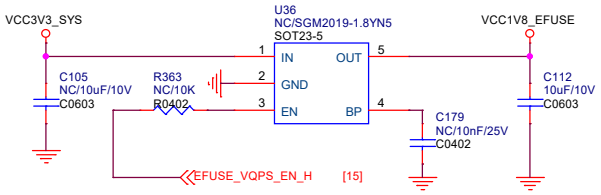
SIGNWAY			
Project:	E473060		
File:	30.MIPI IN		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	30 of 32



SIGNWAY			
Project:	E473060		
File:	31.POWER&KEY Controler		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhanghb&Yangyin	Sheet	31 of 32

eFUSE

Note: For eFUSE programming, can be removed if do not use eFUSE。



SIGNWAY			
Project:	E473060		
File:	32.eFUSE		
Date:	Friday, March 25, 2022	Rev:	A0
Designed by:	Zhangbo&Yangyin	Sheet:	32 of 32