## Circuit Description

1. Power Supply

Power supply of the radio is derived from the battery, which supplies battery B+ after passing through fuse 3A and then feeds through power switch. The power supplies voltage for three AVRs. IC505 supplies 5V (5M) voltage for the control circuit. IC9 supplies 5V (5C) voltage for the shared circuit. And IC6 supplies voltage for the transmit/receive circuit. In transmit mode, 5TC becomes low voltage and Q3 is turned on to supply 5V(5T) voltage for the transmit circuit. In receive mode, 5RC becomes low voltage and Q2 is turned on to supply 5V (5R) voltage for the receive circuit.

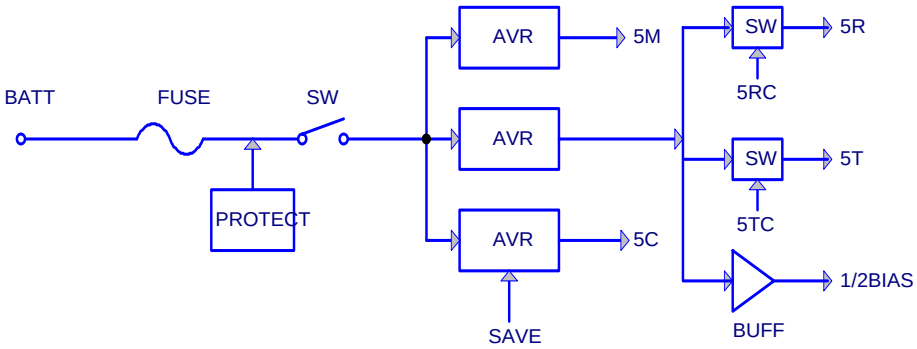


Fig. 1 Power Supply Block Diagram

**2. PLL Frequency Synthesizer**

PLL circuit generates the first local oscillator signal for reception and RF signal for transmission.

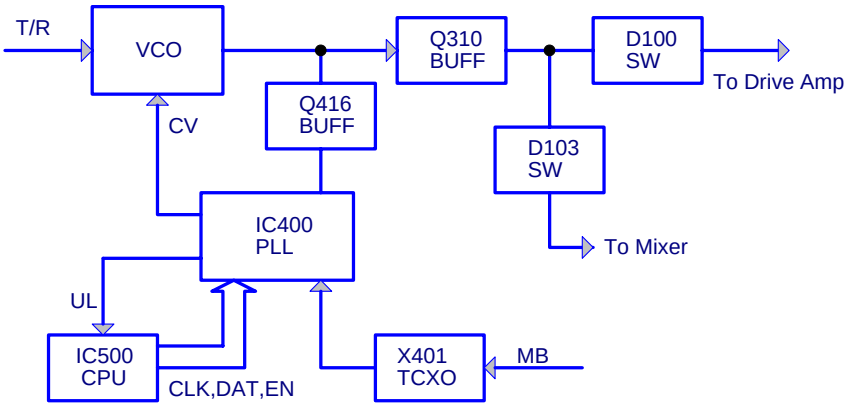


Fig2. PLL circuit

**1) PLL**

IC400 is fractional divider. Step frequency of PLL circuit is 2.5KHz or 6.25KHz. A 16.8MHz reference oscillator signal is divided at IC400 by a fixed counter to generate a 20KHz or 50KHz reference frequency. Output signal from VCO is buffer amplified by Q416 and divided at IC400 by a frequency divider. Divided signal is compared in the phase comparator with 20KHz or 50KHz reference signal of IC400.

Output signal from phase comparator is filtered through a low pass filter and passed to the VCO to control oscillator frequency.

**2) VCO**

The operating frequency is generated by Q352 in transmit mode and by Q350 in receive mode. Operating frequency generates a control voltage by phase comparator to control varactor diodes so that the oscillator frequency is the same as the MCU preset frequency (D350, D352, D354 and D355 in transmit mode and D351, D353, D356 and D357 in receive mode). T/R pin is set high level in receive mode and low in transmit mode. The output from Q352 and Q350 is amplified by Q354 and sent to buffer amplifier.

**3) Unlock Detector**

An unlock condition appears if low level appears at LOCK pin of IC400. Transmission is forbidden if this condition is detected by microprocessor.

## 3. Receiver

The receiver utilizes double conversion superheterodyne.

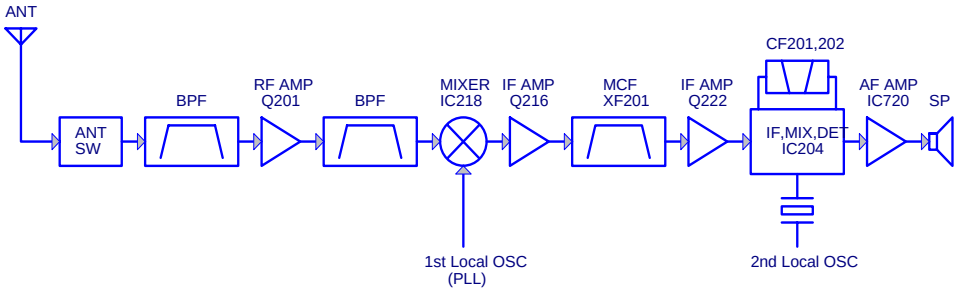


Fig.3 Receiver Section Configuration

**1) Front-end Amplifier**

The signal from antenna is amplified at RF amplifier (Q201) after passing through a transmit/receive switch circuit and a band pass filter. The amplified signal is filtered through a band pass filter to remove unwanted signals before it passes the first mixer.

**2) First Mixer**

The signal from RF amplifier is mixed with the first local oscillator signal from PLL frequency synthesizer circuit at the first mixer (IC218) to create a 44.85MHz first IF signal. The first IF signal is then fed through a crystal filter (XF201) to further remove spurious signals from adjacent channel.

**3) IF Amplifier**

The first IF signal is amplified by Q216 before passing through crystal filter and by Q222 after crystal filter and then enters IF processing chip IC204. The signal is mixed with the second local oscillator signal again in IC204 to create a 455KHz second IF signal. The second IF signal then passes through a 455KHz ceramic filter (wideband: CF201/narrowband: CF202) to eliminate unwanted signals before it is amplified and detected in IC204.

**4) Narrowband/Wideband Switch Circuit**

Turn on ceramic filter CF201 (wideband)/CF202 (narrowband) to set each channel as

wideband or narrowband. W/N pin of IC500 outputs wideband (high level) and narrowband (low level) signal.

**5) AF Amplifier**

The result AF signal from IC204 is amplified by IC606, and then passes through AF processing chip IC601 and compander IC603. The processed AF signal is then amplified by an AF power amplifier (IC720) to drive the speaker.

**4. Transmitter**

**1) AF and Signaling**

Modulating signal from the microphone passes through Q700 switch and compander IC603 before it enters AF processing chip IC601. Under the control of MCU, IC601 produces DTMF/CTCSS/CDCSS/2-Tone/5-Tone signaling, which then pass through MOD and enter VCO together with the modulating signal for direct FM modulation. (See fig.5)

**2) RF Amplifier**

The transmit signal from VCO buffer amplifier (Q310) is amplified by Q101 and Q102. The amplified signal is then amplified by the power amplifier Q105 and Q107 (include a two-stage FET amplifier) to create 4.0W RF power. (See fig.4)

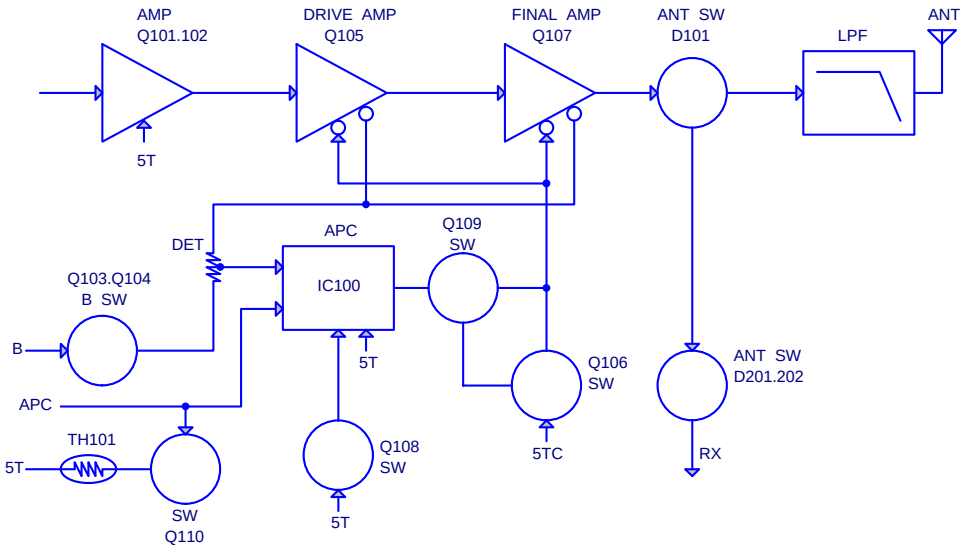


Fig.4 APC System

**3) Antenna Switch and LPF**

Output signal from RF amplifier passes through a low-pass filter network and a transmit/receive switch circuit comprised of D101, D201 and D202 before it reaches the antenna terminal. D201 and D202 is turned on (conductive) in transmit mode and off (isolated) in receive mode.

**4) APC**

The automatic power control (APC) circuit stabilizes the transmit output power by detecting the drain current of final stage amplifier FET. IC100 (2/2) compares the preset reference voltage with the voltage obtained from final current. APC voltage is proportional to the difference between auto detect voltage and reference voltage

output from IC100 (1/2). The output voltage controls FET power amplifier and keeps the transmitter output power constant. The output voltage can be varied by the microprocessor, which hence controls the transmitter output power.

## 5. Signalling Section

The block diagram of signaling section is shown as figure 5.

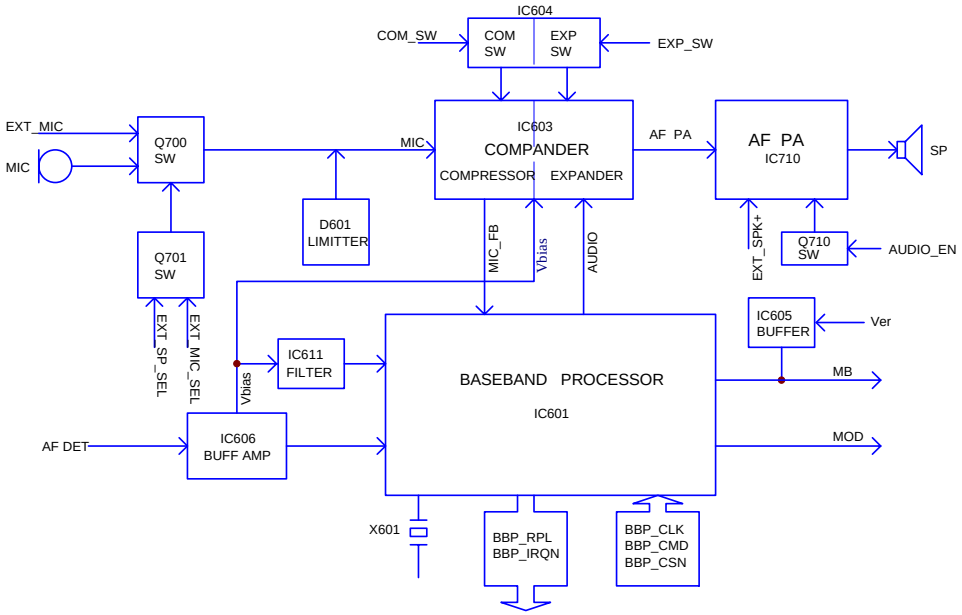


Fig.5 AF and Signalling Circuit

In the transmit section, signallings (CTCSS, CDCSS, DTMF, 2-Tone and 5-Tone) are produced by IC601 under the control of MCU and enter VCO together with AF signal from MIC for modulation.

In the receive section, after buffer amplified together with IF demodulation signals, the signallings enter IC601 for decode. The decoded data is then sent to MCU for recognition.

## 6. Control System

The IC500 CPU operates at 9.8304MHz.

The block diagram of MCU control system is shown as following:

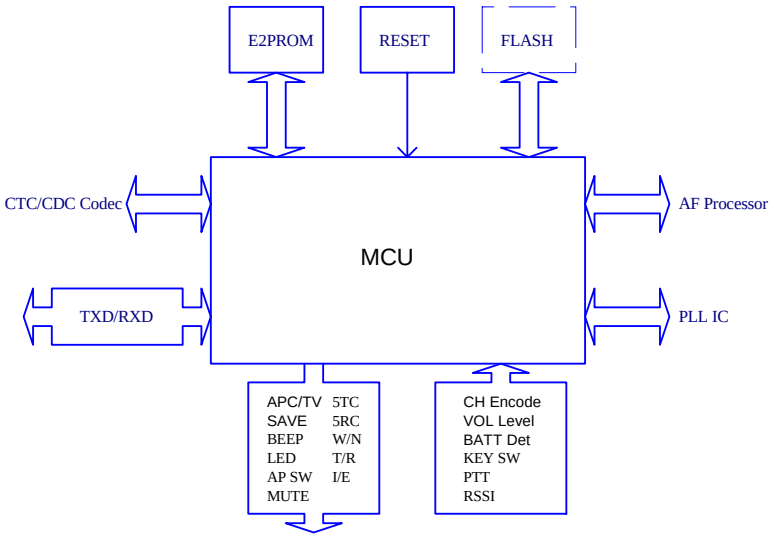


Fig.6 MCU Block Diagram

Circuit in this section is mainly comprised of MCU, EEPROM, FLASH and reset IC etc. MCU control circuit accomplishes the following functions: accomplish the reset initialization according to the programmed feature of the radio when power on; detect key signal and monitor battery voltage; send necessary frequency data to PLL according to encode of the channel; switch and control transmit/receive according to the signal input from PTT; turn on/off the mute circuit according to the input signaling decode signal and squelch level signal; output control signal to control the light/off of LED; output BEEP signal to drive the speaker.