Circuit Description

Realization Methods for Basic Functional Modules

PLL Frequency Synthesizer

The PLL circuit generates local oscillator signals for reception and RF carrier signals for transmission.

The PLL circuit consists of the VCO oscillator circuit and baseband processor chip and realizes frequency tracking and channel conversion under the control of MCU signals.

1. PLL

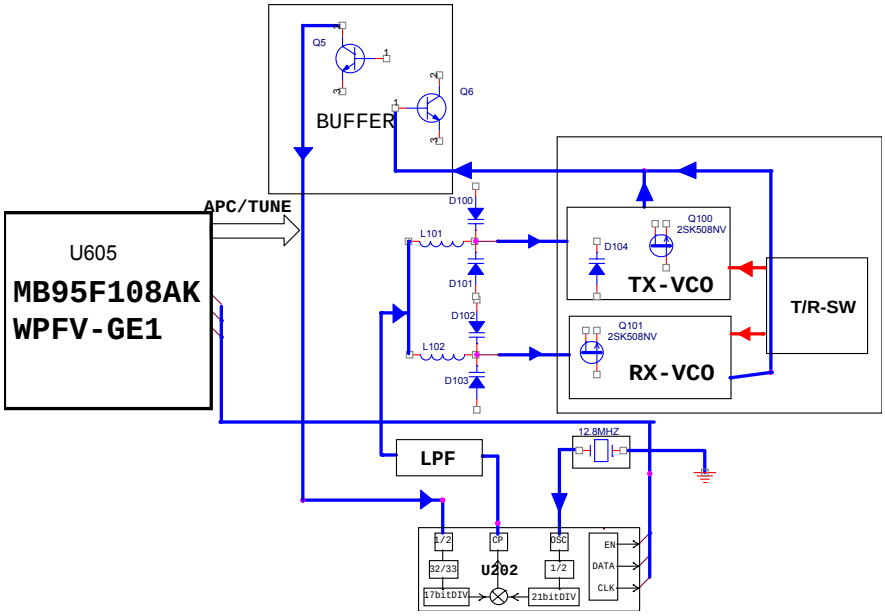

Figure 2

The step frequency of the PLL circuit is 5.0KHz, 6.25KHz, 10.0KHz or 12.5KHz. Therefore, the reference oscillator signal (38.4MHz) is divided into 5.0KHz, 6.25KHz, 10.0KHz or 12.5KHz reference signals by a fixed counter in PLL of U202. Signals output by VCO pass through buffer Q102 followed by amplifier Q103 and enters PLL of U200 for frequency division by a variable divider. The signals from the frequency division are compared with reference signals in the phase comparator PD of PLL. Signals output by the phase comparator is added to the varactors D100, D101, D102 and D103 of VCO to control the output frequency after passing through a low pass filter.

2. VCO

The VCO section is realized by the oscillator circuit of three-point capacitor.

In transmitting mode, the operation frequency of VCO is generated by Q100; in receiving mode, the operation frequency of VCO is generated by Q101.

U202 generates a control voltage via the phase comparator to control varactors (D100 and D101 in transmitting mode; D102 and D103 in receiving mode) to bring the oscillator frequency of VCO in line with the preset frequency of MCU within a broader frequency range.

The switching tube Q652 switches between transmitting and receiving under the control of T/R. In transmitting mode, T/R is set as low level and Q100 operates when Q653 becomes conductive. In receiving mode, T/R is set as high level and Q101 operates when Q653 cuts off. Output from Q100 and Q101 is sent to the buffer amplifier for process after passing through amplifier Q102.

If PLL is unlocked, LD pin of U202 outputs low level. When this situation is detected by a microprocessor, transmitting and receiving operations are suspended and an alert tone sounds.

RF Power Amplifying Circuit (Tx Section)

Block Diagram for RF Power Amplifying Circuit

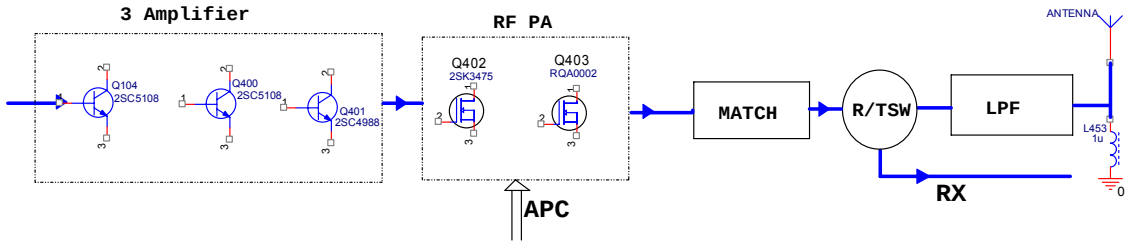

Figure 3

To obtain the required RF power, RF signals from VCO is amplified by driving amplifiers Q400 and Q401 after passing through buffer Q104. The amplified RF signals enters driver Q402, which performs power pre-amplification on the input signals to derive a certain power to drive the final power amplifier. The final power amplifier Q403 performs power amplification again on the input RF signals to derive the required power. Then the amplified RF signals pass through Tx-Rx switching diode D401 followed by the LC low pass filter circuit (LPF). The signals are transmitted through the antenna after ultraharmonics are filtered by the LPF.

Rx Amplification (LNA) and RF Bandpass Network (BPF)

To obtain better frequency selectivity, the Rx bandpass utilizes multiple electrically tunable circuits. The block diagram is shown below:

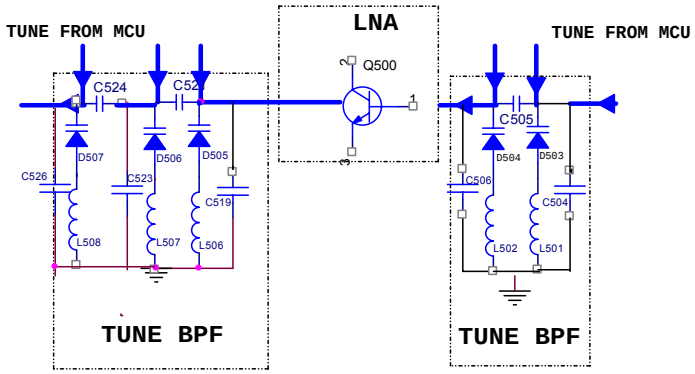

Figure 4

The Rx signals input from the antenna is filtered to remove out-of-band signals at the electrically tunable bandpass network (D503, D504, L501, L502, C503, C505 and 507) and then amplified by low-noise amplifier (LNA) Q500 to obtain a certain level required by reception. The signals pass through the three-level bandpass network (mainly consisting of D505, D506, D507 and periphery components) to effectively restrain the out-of-band interference and to derive pure Rx RF signals, which will be fed to the mixing stage.

The electrically tunable control signals are provide by MCU. The required level can be obtained through table looking up or formula computing to accurately control varactors to operate within proper voltage range. It constitutes a bandpass filter with the periphery inductive capacitors to track the Rx frequency under the change of MCU control voltage and to obtain the preset Rx sensitivity requirements and out-of-band interference requirements.

Mixing Circuit (MIXER) and IF Bandpass Network (BPF)

Block Diagram for the Mixing Circuit

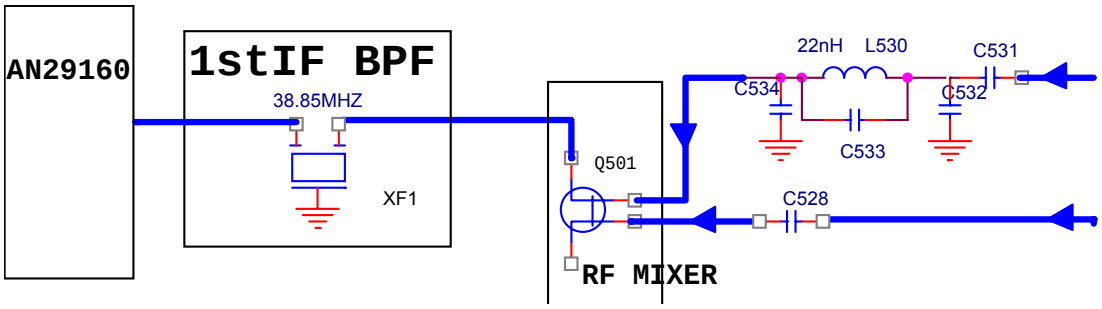

Figure 5

The mixer mainly processes the local oscillator signals and Rx RF signals output by VCO. The first IF from the mixer is used by the demodulator chip to discriminate frequency. Here the active mixer

is utilized.

The mixer tube (Q501) utilizes dual gate FET MOS (3SK318) and has better noise characteristics and square law characteristics. The isolation between the local oscillator signals and the Rx signals is high. To ensure proper sensitivity and certain gain for the mixer tube, tune delicately via the offset.

The signals output from the mixer pass through inductor L509 to remove residual spurious and then enter the first IF filter. The filter utilizes the first-class crystal filter to ensure sufficient bandwidth and excellent selectivity. The signals finally enter baseband processing chip AN29160 for demodulation.

APC/TUNE Automatic Power Control Circuit

Block Diagram for the Circuit:

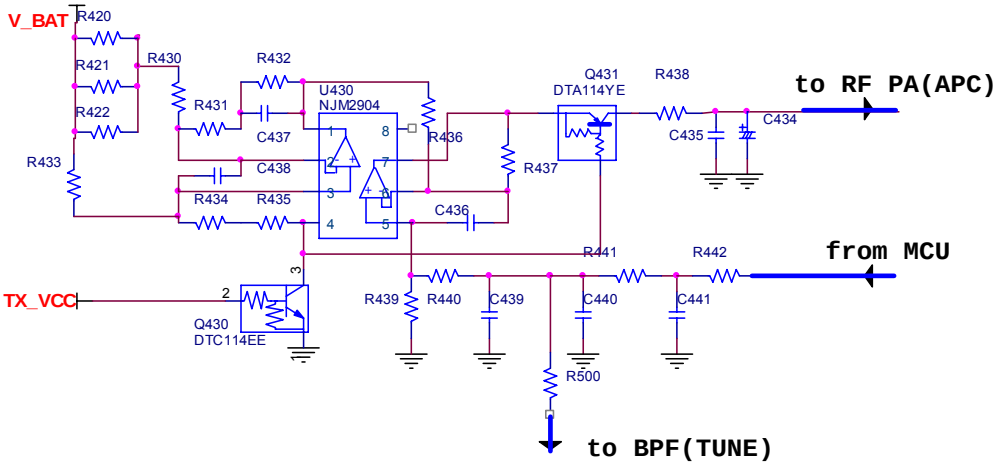

Figure 6

Subject to the selected channel, MCU outputs the corresponding PWM waveform, which is reshaped by the RC filter network (R441, R442, C440 and C441) to derive the APC/TUNE control signal level. One part of them is used as the control voltage of the electrically tunable circuit after passing through R500. In transmitting mode, the levels are voltage-divided by R439 and R440 to obtain the APC reference voltage.

The transmitting current passes through R420, R421 and R422 to derive the error detect voltage. The voltage is amplified by operational amplifier IC U430 and then compared with APC reference voltage to output APC control voltage and to form closed-loop negative feedback power control when the transmitting current changes.

Audio and Signalling Processing Circuit

Baseband processing IC AN29160 has high integration level and powerful functions. Many of the processing functions (as VCO level detect&output, SQ signal level detect&output, Tx-Rx audio processing switch, audio amplifier, etc) and can be realized inside. The Tx-Rx sharing can also be realized.

Block Diagram for Tx Audio&Signalling Process

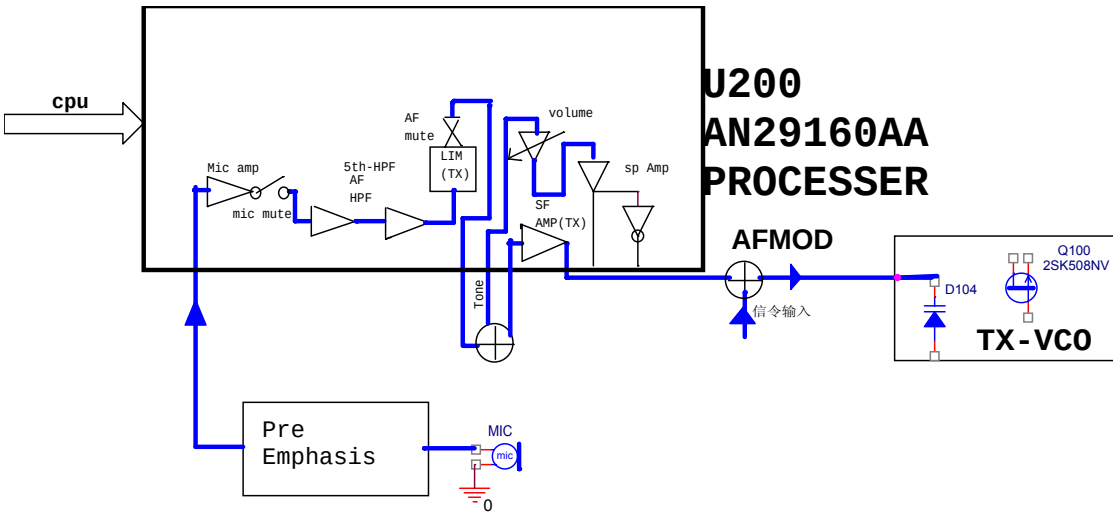

Figure 7

Tx Audio Process: Audio signals input from the MIC is converted to electrical signals through the audioelectric conversion of MIC and the amplitude limit of them are amplified by U200 after the signals are pre-emphasized. The processed signals go to the low-pass filter circuit to remove frequencies above 3KHz and then go to VCO for direct frequency modulation after passing through potentiometer VR200.

Tx Sinalling Process: MCU outputs, via the QTO port, signalling encoder waveform, which is divided into two parts for modulation after passing through the RC network. One part is used to modulate PLL reference-frequency oscillator directly, while the other part is used to modulate VCO. VR260 balances the modulation and adjust the signal amplitude ratio of one part to the other, which optimizes the singalling waveform modulated on the carrier.

Block Diagram for Rx Audio&Signalling Process

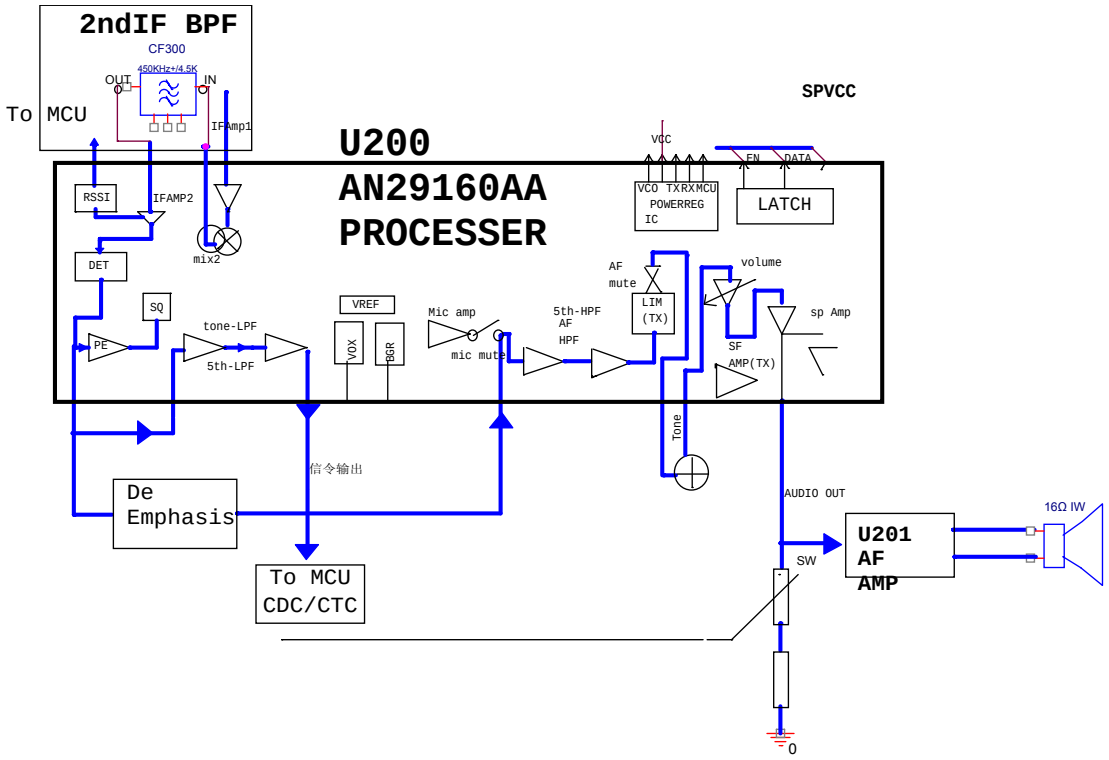

Figure 8

U200 outputs initial audio signals (including noise, signaling, audio, etc) after performing frequency-discrimination and demodulation on the received signals. Therefore, the audio process is divided into three parts:

Rx Audio Process: One part of the audio signal output by U200 is fed to the RC low-pass filter and de-emphasis circuit and then amplified by U200. The audio signal is recovered after frequencies below 300Hz are removed. The recovered audio signal is adjusted by the potentiometer and then goes to audio power amplifier IC (U201), which amplifies power for the input audio signals to drive the speaker directly. To obtain higher power, the BTL bridge dual output is utilized.

Rx Signalling Process: One part of the audio signal output by U200 is fed to the 300Hz low-pass filter circuit (U640). After audio signals above 300Hz are removed, CTCSS/CDCSS goes to the QTIN pin of CPU. CPU decodes the input signallings.

Noise Signalling Process: One part of the audio signal output by U200 goes to U200 again. After the signal is filtered, amplified and rectified inside U200, a DC voltage signal (SQ) corresponding to the noise component is derived. The DC signal is fed to the BUSY pin of MCU via the ND pin of U200. Then MCU processes the input signals.

MCU Control Section

The block diagram for the MCU control section is shown below. MCU works under the 7.3728MHz clock frequency.

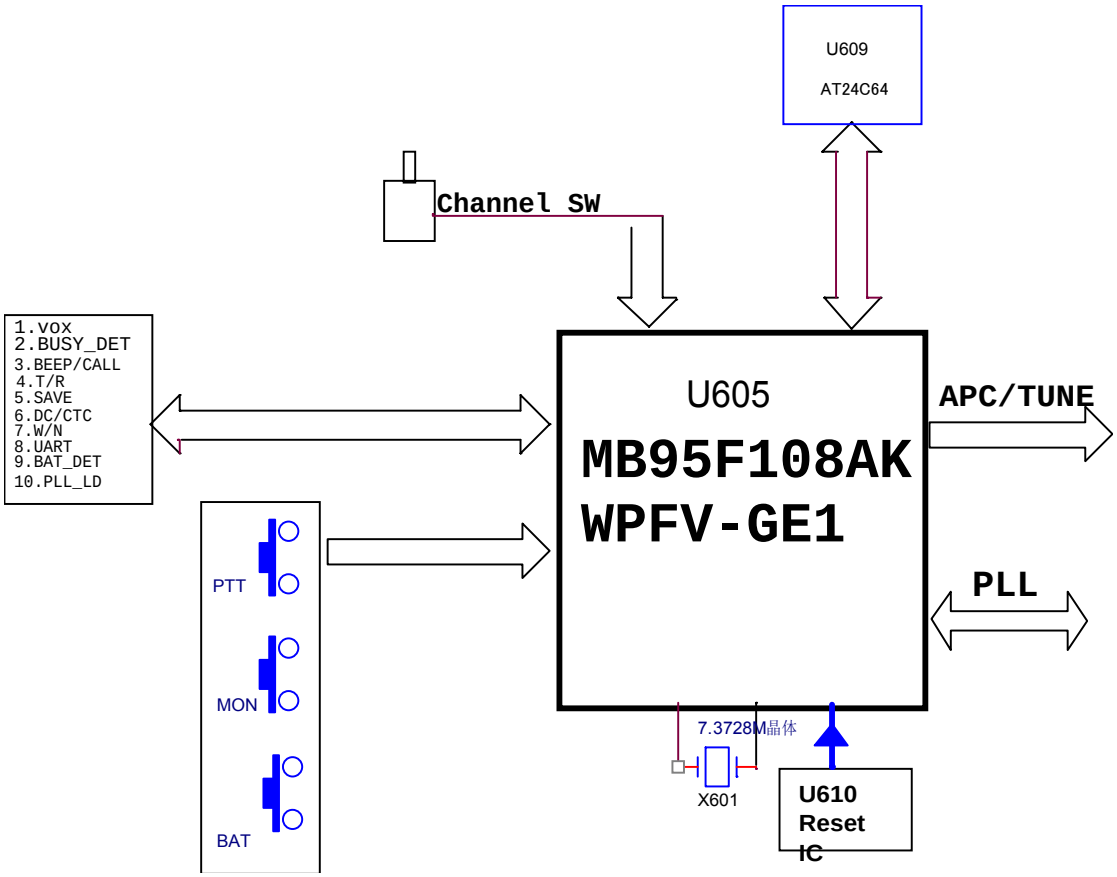

Figure 9

The MCU control section is composed of MCU, EEPROM, RESET IC, keys, Channel Selector knob, etc. Main functions realized by this circuit section are:

1. Control Signal:

   Control of battery save mode

   Control of high/low power switch

   Control of band/narrow band switch

   Control of Tx-Rx switch

   Control of APC/TUNE output voltage

   Control of Tx power supply and power supply of audio power amplifier

   Control of squelch ON detect

2. Signal Detect

Detect of external PTT, MONI and VOX

Detect of PLL unlock (UL)

Detect of VOX ON level

Detect of battery power alarm

Detect of enabling and checking external remote speaker microphone

3. Data Transfer and Process

EEPROM data initiation

Programming data transfer

Encoding process of channel selector knob

Signalling encoding and decoding

Data transfer of baseband processing chip (PLL)

Power Supply Process

Block Diagram for the Circuit

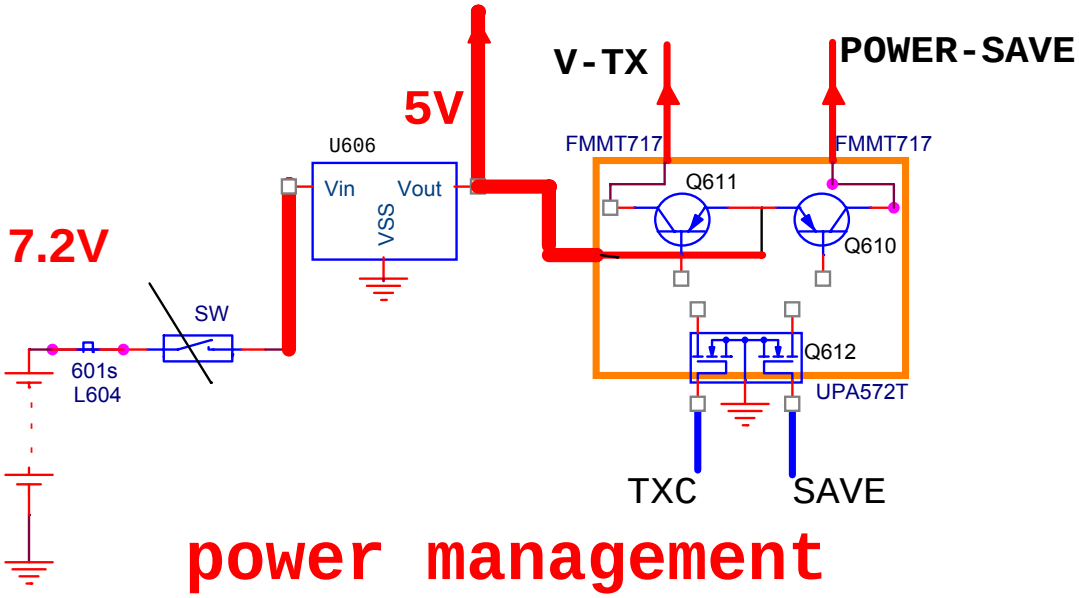

Figure 10

After the radio is powered on, the battery voltage is provided to the RF power amplifier and audio power amplifier to meet the requirements of sufficient power amplification after filtered by L604 and C682. Another path is input with the regulator IC (U606) of 5V and outputs voltage of VCC_5V for use by MCU and the baseband processing chip after regulated. Because the radio works under the half duplex mode, it is required to control the Tx and Rx power supply alternately. To meet the requirement of the battery save mode, MCU should output a pulse signal with fixed duty factor

(control signal of SAVE). When the SAVE signal of MCU is of high level, Q610 becomes conductive and provides a 5V voltage (V_SAVE) for the operating circuit. PLL and the receiving circuit operate. When the SAVE signal is a pulse signal, the radio enter the battery save mode. When transmitting, TXC, control signal of CPU, is of high level. Q611 becomes conductive and provide a 5V voltage for the transmitting circuit and the transmitting circuit operates.

Power supplies of the Tx section and Rx section both have symmetrical regulation measures. When the load change changes the output voltage/current, the regulator closed-loop feedback circuit operates, regulating the output voltage at 5V.

VOX Realization

The block diagram is shown below:

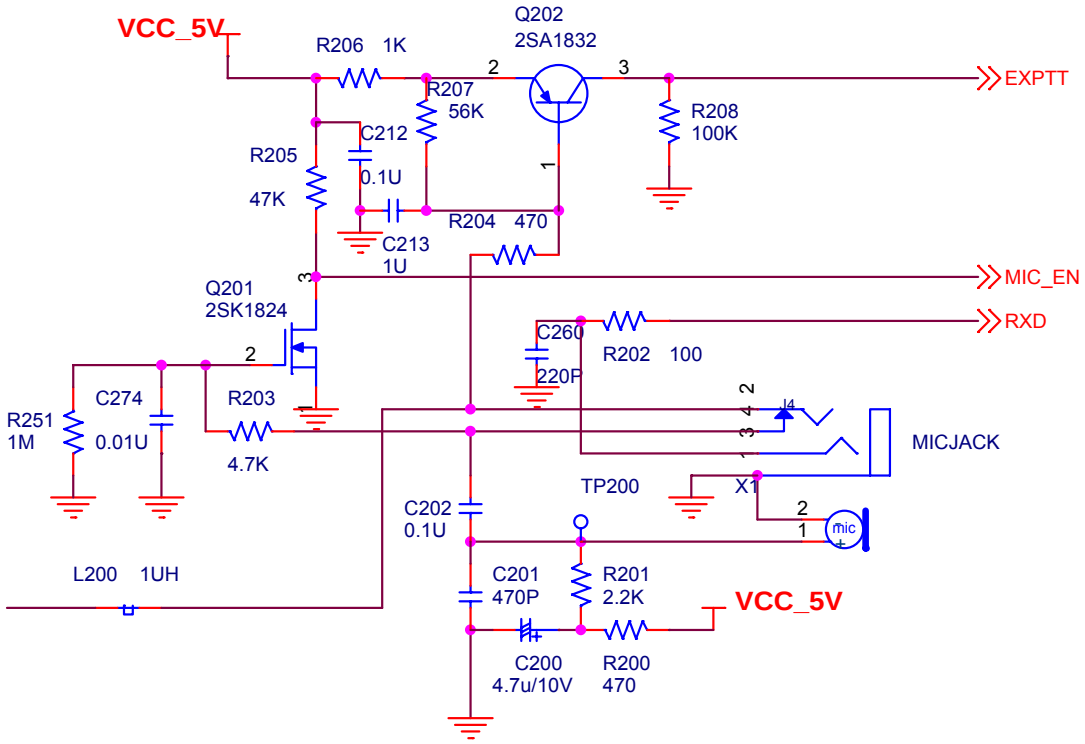

Figure 11

After the function key VOX is held down, the radio enters the VOX status. The VOX function can only be enabled when MCU detect that MIC enabling signal (MIC_EN) and external VOX enabling signal (EXT-PTT) switch from low level to high level almost at the same time (within hundreds of milliseconds). Otherwise, it is detected as the earpiece without VOX and the VOX function is off.

When the remote speaker microphone with VOX is inserted into the earpiece jack, Q201 cuts off. MIC_EN switches from low level to high level and Q202 completes the circuit with R204 and the external remote speaker microphone simultaneously. Q202 becomes conductive. EXT-PTT switches from low level to high level, which is detected by MCU as insert of a remote speaker microphone with VOX. The VOX function is enabled. When the VOX detect level (5 levels available) meets the preset requirements, the radio transmits and the audio signal goes to the baseband processing IC AN29160 through the processing path.

If a remote speaker microphone without VOX (remote speaker microphone with PTT) is inserted, Q201 cuts off. MIC_EN switches from low level to high level but Q202 can not complete the circuit and keep the cut-off status. EXT-PTT is of low level. MCU detects as the remote speaker microphone without VOX and the radio returns to the common mode. Press the PTT key on the remote speaker microphone to transmit.

Semiconductor Data

Pin No.	Pin Name	TC-610	TC-620	I/O	Description
1	AVcc	Vcc	Vcc		Power supply pin for A/D, connecting power supply
2	AVR	Vcc	Vcc		A/D reference input pin, connecting power supply
3	PE3/INT13	PTT	PTT	I	PTT key (connected with pull-up resistor) (valid at low level)
4	PE2/INT12	A_KEY	A_KEY	I	SK1, programmable function key (connected with pull-up resistor) (valid at low level)
5	PE1/INT11	EXT-PTT	EXT-PTT	I	PTT key on the earpiece (connected with pull-down resistor) (valid at high level)
6	PE0/INT10	B_KEY	B_KEY	I	SK2, programmable function key (connected with pull-up resistor) (valid at low level)
7	P83	ENC3	ENC3	I	Encoder input of channel selector knob(connected with pull-up resistor)
8	P82	ENC2	ENC2	I	
9	P81	ENC1	ENC1	I	
10	P80	ENC0	ENC0	I	
11	P71/TI0	T/R	T/R	O	Tx-Rx switch control H(R)/L(T)
12	P70/TO0	Reserve	Reserve	O	Reserved
13	MOD	For down -loading	For down -loading	I	An operating mode designation pin. When downloading, this pin is connected with Vcc and a resistor of 47K is also connected between the

					pin and the grounded Vss. When not downloading, only a resistor of 47K is connected between the pin and the grounded Vss.
14	X0	OSC0	OSC0		Connecting pin of 7.3728MHzMHz master crystal oscillator
15	X1	OSC1	OSC1		
16	Vss	GND	GND		Power supply (GND) pin (When recording, it is connected with the GND recording port signals.)
17	Vcc	VCC	VCC		MCU 5V power supply (When recording, it is connected with the VCC recording port signals)
18	PG0	C	C		This port can not be used as IO and a capacitor is connected between the port and the grounded Vss.
19	PG2/X1A	OSC32K	OSC32K		Subsystem clock pin (Reserved）
20	PG1/X0A	OSC32K	OSC32K		
21	/RST	RESET	RESET	I	Reset (When recording, it is connected with the RSTX recording port signals.)
22	P00/INT00	Reserve	Reserve	O	Reserved
23	P01/INT01	Reserve	Reserve	O	
24	P02/INT02	Reserve	Reserve	O	
25	P03/INT03	Reserve	Reserve	O	
26	P04/INT04	PLLEN2	PLLEN2	I/O	PLL ENABLE
27	P05/INT05	PLLDATA2	PLLDATA2	I/O	PLL DATA
28	P06/INT06	PLLCLK2	PLLCLK2	I/O	PLL CLOCK
29	P07/INT07	UL2	UL2	I/O	TB31202 PLL circuit unlock detect (H: Lock L Unlock) (connected with pull-up resistor)
30	P10/UI0	RXD	RXD	I	UART RX (When recording, it is connected with the UI recording port signals)
31	P11/UO0	TXD	TXD	O	UART TX (When recording, it is connected with the UO recording port signals)
32	P12/UCK0	Reserve	Reserve	O	Reserved
33	P13/TRG0/ADTG	Reserve	Reserve	I	Reserved
34	P14/PPG0	MIC_EN	MIC_EN	I	Check whether the MIC is connected(connected with pull-down resistor) (valid at high level)
35	P20/PPG00	CTC_DCS	CTC_DCS	PWM	CTCSS/CDCSS output
36	P21/PPG01	Reserve	Reserve	O	Reserved
37	P22/TO00	TONE	TONE	O	BEEP tone output/CALL tone output
38	P23/TO01	W/N	W/N	O	Wide/Narrow band control W(L)/N(H)
39	P24/EC0	Reserve	Reserve	O	Reserved

40	P50/SCL0	SCL	SCL	SCL	EEPROM CLOCK
41	P51/SDA0	SDA	SDA	SDA	EEPROM DATA
42	P52/PPG1	AP/TU	AP/TU	PWM	Auto power control/adjust
43	P53/TRG1	TX_CTRL	TX_CTRL	O	Tx power supply control “H”: valid Transmission is on.
44	P60/PPG10	PLLCLK	PLLCLK	O	PLL CLK
45	P61/PPG11	PLLDATA	PLLDATA	O	PLL DATA
46	P62/TO10	PLLEN	PLLEN	O	PLL ENABLE
47	P63/TO11	Reserve	Reserve	O	Reserved
48	P64/EC1	Reserve	Reserve	O	Reserved
49	P65/SCK	Reserve	Reserve	O	Reserved
50	P66/SOT	Reserve	Reserve	O	Reserved
51	P67/SIN	Self	Self	I	For test (used to enter the factory clone mode, connected with pull-up resistor)
52	P43/AN11	SPCNT	SPCNT	O	Power supply control of main audio "H": audio ON
53	P42/AN10	PCONT	PCONT	O	Power supply control pin of AN29160AA
54	P41/AN09	RLED	RLED	O	Red LED
55	P40/AN08	GLED	GLED	O	Green LED
56	P37/AN07	Reserve	Reserve	O	Reserved
57	P36/AN06	Reserve	Reserve	O	Reserved
58	P35/AN05	TI	TI	I/AD	CTCSS/CDCSS input
59	P34/AN04	BUSY	BUSY	I/AD	Channel busy check (requiring 10-digit AD)
60	P33/AN03	BAT_DET	BAT_DET	I/AD	Battery voltage detect (requiring 10-digit AD)
61	P32/AN02	Reserve	Reserve	O	Reserved
62	P31/AN01	Reserve	VOX	I/AD	VOX detect (requiring 10-digit AD)
63	P30/AN00	Reserve	Reserve	O	Reserved
64	AVss	GND	GND		Power supply (GND) pin for A/D, ground