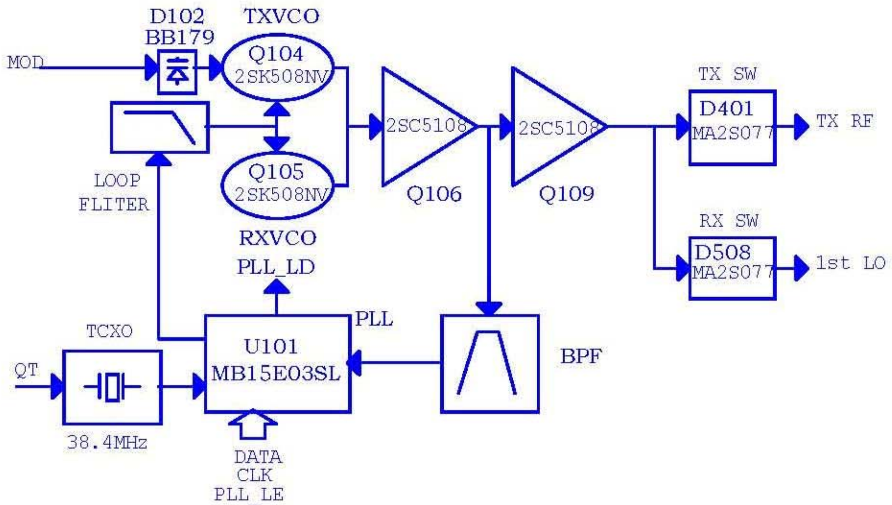
a. Block diagram of PLL circuit:



PLL circuit mainly generates RF carrier signal (for Tx) and 1st local oscillator (for Rx).

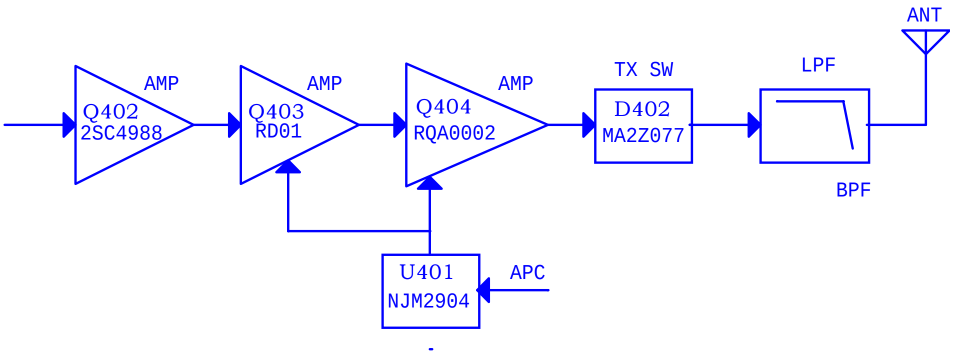
PLL: Incremental frequencies of PLL circuit are 5.0 KHz, 6.25 KHz, 10.0 KHz and 12.5 KHz. At U101, 38.4MHz reference oscillator signal, after going through a fixed calculator, is divided into 4 reference frequencies (5.0 KHz, 6.25 KHz, 10.0 KHz and 12.5 KHz) at PLL. The signal output from VCO (Tx VCO or Rx VCO), after buffer amplified at Q106, is frequency divided at PLL. After that, the signal is compared to the reference frequency by phase detector of PLL. The signal is sent to a low-pass filter and uploaded to a varactor so that output frequency can be controlled.

VCO: there are total 2 VCO modules. One for Rx while the other for Tx. In Tx mode, PLL, using a phase detector and a low pass filter, generates a control voltage for varactor control, which is to generate a RF carrier signal that in accordance with MCU preset frequency at Tx VCO. The modulation signal, after going through D102, is modulated to RF carrier and sent to RF power amplifier circuit after buffer amplification.

In Rx mode: Rx PLL, using a phase detector and a low pass filter, generates a control voltage for varactor control, which is to generate a 1st local oscillator signal that in accordance with MCU preset frequency at Rx VCO. Then, the processed signal is mixed with the RF signal being received at mixer Q502. Finally, a 1st IF signal is generated.

Unlock Detector: if low level is appeared at LD pin of U101, unlock status is determined. When the condition is detected by CPU, no Tx and Rx operation is enabled as well as an unlock alarm is sounded.

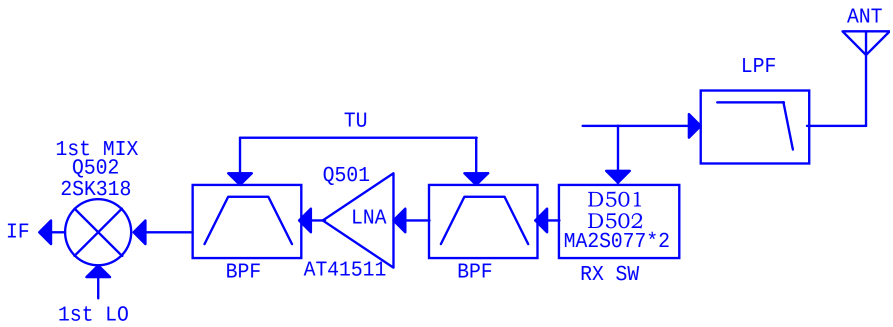
b. Block diagram of RF power amplifier:



The carrier signal having been modulated at Q109 is power amplified at Q402. Then, the signal enters Q403 so that enough power is achieved to drive final power amplifier. At Q404, the input RF signal is power amplified again to acquire the demanded power. By then, the RF signal goes through diode D402 and enters a low pass filter (LPF) circuit. In LPF, the higher harmonic is filtered. At last, the signal is transmitted from the antenna.

Control circuit is consisted of U401, Q405 and Q406. U401, by controlling the biasing voltage of grid at Q403 and Q404, controls Tx current, which accordingly completes power control.

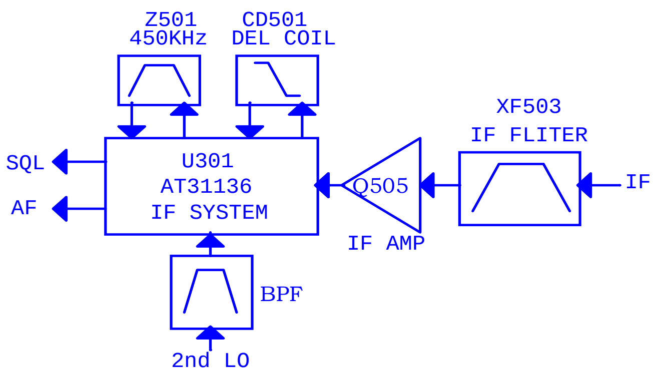
c. Block diagram for Rx low noise amplifier and 1st mixer:



RF signal, whatever useful or not, is received by the antenna. After it goes through the band-pass filter (composed of D503, D504 and D505), the interference signal is filtered, which leaves useful RF signal to enter HF low noise amplifier Q501. At Q501, the signal is amplified; the amplified signal re-enters band-pass filter (compose of D506 and D507) for interference signal filter. Useful RF signal and 1st local oscillator signal output from VCO are mixed at Q502.

MCU, using APC/TU pin, outputs a voltage for the control of center frequency at electric tuning band-pass filter.

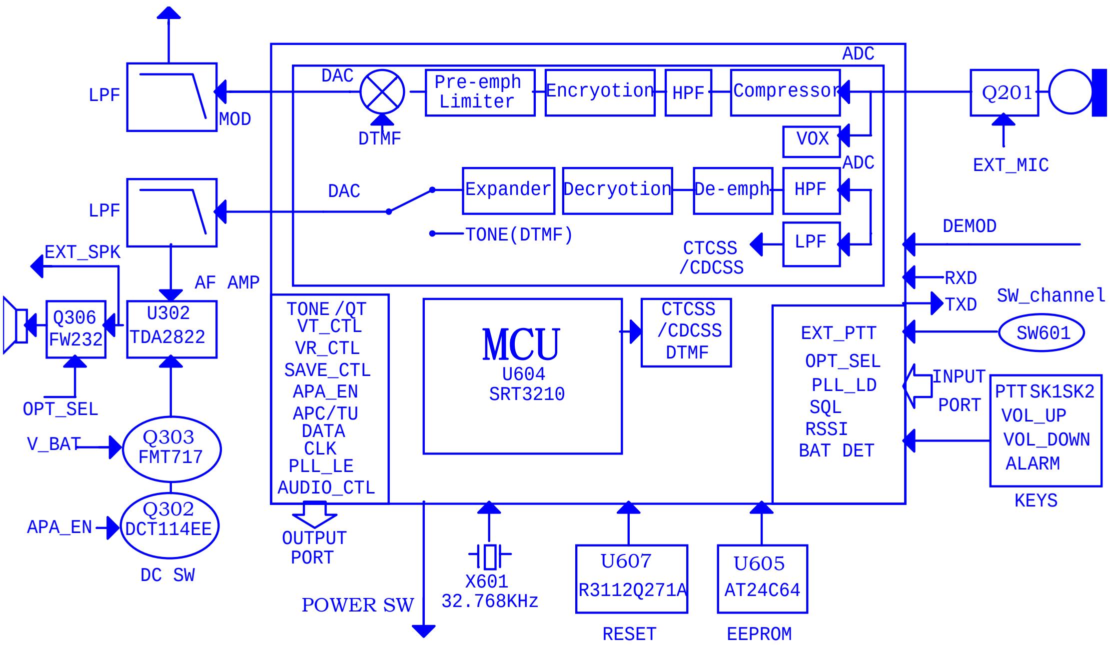
1.2.2 IF Processing and Audio Demodulation



A 1st IF signal (38.85MHz) is generated after the mixing signal at Q502 is filtered in the crystal filter XF503. The IF signals are amplified at Q505 and processed at IF demodulator U301. At U301, a 2nd IF signal is generated after the 1st IF signal and 2nd local oscillator signal go through 2nd mixer; the 2nd IF signal is demodulated at U301 and an audio signal is output. The audio signal is then sent to MCU for A-D conversion and filter. After that, the signal is divided into 2 ways for further process. Thereof, one way of signal starts CTCSS and CDCSS demodulation; the other one starts filter, de-emphasis, demodulation, digital audio signal volume control and D-A conversion. After the processes above, an audio signal is generated. The signal enters audio power amplifier U302 for power amplification. In the final, speaker is accordingly driven.

1.2.3 MCU Control, Signal Processing and Audio Amplification

The circuit diagram of the section is shown below:



a. MCU Control Circuit

MCU control circuit is consisted of MCU, EEPROM and various keys. Main features are: to initialize the radio data and store the data in EEPROM; to detect and process signal and battery voltage conditions generated by external keys, LD and VOX-DET; to transmit the data required by PLL according to various channel encoding conditions; to process switch and control between Rx and Tx according to the input PTT signal; to control enable or disable of squelch circuit according to the input signalling decoding signal and squelch level signal; to control high/low power switch, audio power amplifier, VCO power supply, Rx power supply and Tx power supply by controlling the output signal; in programming, to transmit and receive data by the communication between RXD (or TXD) and PC according to RS232 protocol.

b. Signal Processing

b.1 Tx Baseband Process

As the audio signal input from MIC enters U604, a digital signal process is started after an A-D (analog to digital) conversion is finished. Then, the signal is divided into 2 ways after a digital low-pass filter: one way is taken as the signal for VOX detection; the other one is processed at AGC, compandor, high pass filter, encryption and pre-emphasis operations and superposed with the CTCSS/CDCSS signal generated by MCU. After a D-C conversion, a baseband signal is output. In the final, the signal is sent to VCO for modulation after it is filtered at a passive LPF.

b.2 Rx Baseband Process

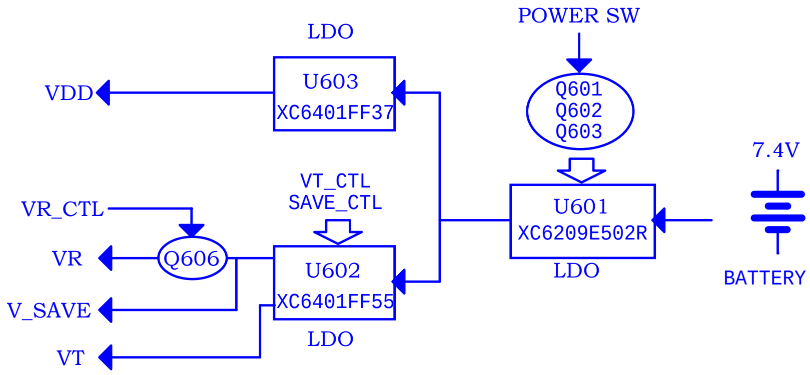
After the DEMOD signal demodulated at IF enters U604, a digital signal is generated as A-D conversion is completed. Then, the signal enters digital LPF for further filter. The signal is divided into 2 ways. In one way, CTCSS/CDCSS signalling decoding is done; in the other way, the signal, after the high pass filter, begins the processes including de-emphasis, decryption and signal extension (volume control of audio digital signal). In the end, an audio signal is output after the D-A conversion.

b.3 Audio Power Amplifier

The digital audio signal demodulated at U604, after volume control process (MCU internal digital gain control), is converted to analog signal by D-A conversion. The signal entering audio power amplifier U302 is power amplified, after which the speaker is driven to sound.

1.2.4 Power Supply Process

Block diagram of power supply:



Power Supply: After a 7.4V battery voltage goes through LDO IC U601, a steady 5V DC voltage is generated. Then, the voltage is divided into 2 ways. In one way, a 4.5V DC voltage that supplying power to Tx, Rx and VCO circuit is generated after it is converted at LDO U602. In the other way, a 3.3V voltage that supplying power to MCU, EEPROM and PLL is generated after it is converted at LDO U603.