MBH2BT01 SPEC SHEET

Revision 0.2E

Feb 14, 2003

FUJITSU MEDIA DEVICES LIMITED

All specifications are preliminary which may be changed without any prior notice

1. APPLICATION

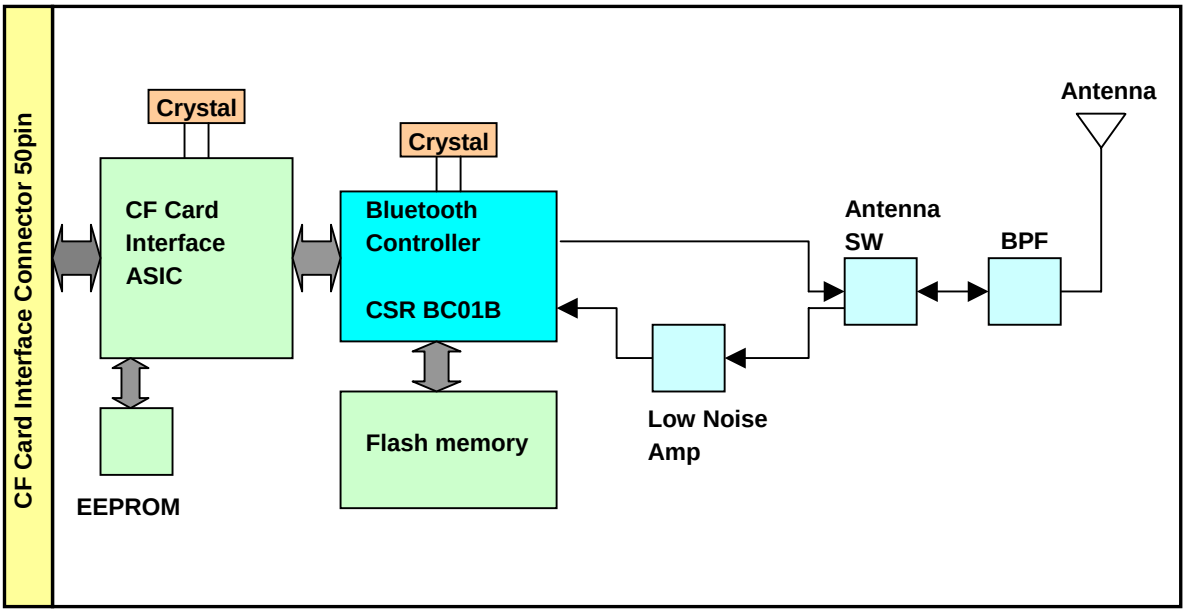
This document is applied for MBH2BT01 CF Card implemented Bluetooth™ specification.

2. FEATURES

MBH2BT01 is the Bluetooth™ CF Card included RF, Baseband, Link Manager and HCI.
MBH2BT01 enables wireless communication at 2.4GHz (ISM band).

- ComapctFlash Card TYPE I Extended
- Power Class 2
- Built-in antenna
- Support both 3.3V and 5V operation
- Bluetooth qualified

3. BLOCK DIAGRAM



4. ELECTRICAL CHARACTERISTICS

4-1. FUNCTIONS

4-1-1. CF Interface Part

CompactFlash Specification Revision 1.4 compliant

Including Card Information Structure (CIS)

Supply voltage 5V or 3.3V

16550A UART compatible register
(Supported 921.6kbps using the special driver software)

4-1-2. Bluetooth Part

Bluetooth Specification Version 1.1 compliant

Carrier Frequency	2400 to 2483.5 MHz (ISM radio band)
Modulation	0.5 BT Gaussian-filtered 2FSK at 1Msymbol/s Modulation index: 0.25 to 0.35
Symbol Rate	1Mbps
Transmission Speed	Asymmetrical : Forward 723.2kbps (Max), Reverse 57.6kbps Symmetrical : 433.9kbps (Max)
Channel	79
Transmit Power	Power Class 2
Built-in antenna	Ceramic chip antenna

4-2. ELECTRICAL CHARACTERISTICS

4-2-1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Value	Unit
Supply Voltage	Vcc		6.5	V
Input Voltage	Vin	50Pin	GND-0.5 ~ Vcc+0.5	V
Power Consumption	Pd		700	mW
Operating Temperature	Topr		0 ~ +60	ºC
Storage Temperature	Tstg		-20 ~ +75	ºC

4-2-2. Recommendable Operating Condition

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	Vcc		4.5	5.0	5.5	V
			3.135	3.3	3.465	V
Operating Temperature	Topr		+10		+40	ºC

4-2-3. Power Consumption

Vcc=3.3V, Ta=25±2ºC

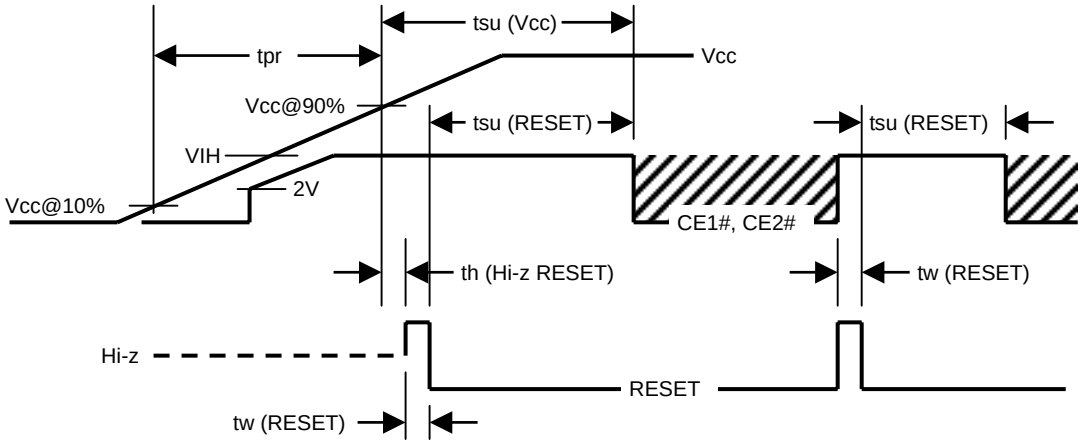
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Consumption	Icc1	Receiver		92	110	mA
	Icc2	Transmitter (DH1: maximum output power)		92	110	mA
	Icc5	Transmitter (DH5: maximum output power)		98	130	mA
	Icc6	Standby mode		8	20	mA

4-2-4. Input/Output Terminal Characteristics

Ta=25±2ºC

Items	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
		Vcc = 3.3V			Vcc = 5.0V			
Input Voltage CMOS	VIH	2.4			4.0			V
	VIL			0.6			0.8	V
Input Voltage TTL	VIH	2.0			2.0			V
	VIL			0.6			0.8	V
Output Voltage	VOH	Vcc-0.8			Vcc-0.8		GND+0.4	V
	VOL			GND+0.4				V

4-2-5. CF Interface Power-UP/Reset Timing



Items	Symbol	Condition	Min	Max	Unit
Card Enable Setup Time	tsu (Vcc)		40		ms
RESET Setup Time	tsu (RESET)		20		ms
Vcc Rising Time	tpr	10% → 90% of Vcc	0.1	300	ms
RESET Width	tw (RESET)		10		ms
	th (Hi-z RESET)		1		ms

4-2-6. CF Interface Input-Output Timing

Complies with CompactFlash Specification Revision 1.4.

4-2-7. Transmitter Characteristics

Vcc=3.3V, Ta=25±2ºC

Parameter	Condition	Min	Typ	Max	Unit
Output Power	Max setting	-4	0	4	dBm
Power Density				4	dBm
Power Control Range			30		dB
Power Control Step Size			4		dB
Output Spectrum (Frequency Range)		2.4		2.4835	GHz
Output Spectrum (20dB Bandwidth)	Difference of frequencies between 20dB below of the peak power			1	MHz
Initial Carrier Frequency Tolerance	Integration of the frequency deviation of the DH1 packets' 4 preamble	-75		+75	kHz
Carrier Frequency Drift	1 Slot 3 Slot 5 Slot	-25 -40 -40		+25 +40 +40	kHz kHz kHz
Modulation Characteristics	8 bit sequence 01010101	±115			kHz
	8 bit sequence 00001111 (Avg)	±140		±175	kHz
Adjacent Channel Power	|M-N|=2 |M-N|>=3			-20 -40	dBm dBm

*Measuring method complies with Bluetooth™ Test Specification-RF.

*Measured by using coaxial cable.

4-2-8. Out of Band Spurious Emissions

Complies with ETS 300 328 and FCC Part 15.247.

4-2-9. Receiver Characteristics

Vcc=3.3V, Ta=25±2ºC

Parameter	Condition	Min	Typ	Max	Unit
Receiver Sensitivity	BER <= 0.1% DH1 mode			-75	dBm
Sensitivity (BER) - Single-Slot Packets	Input level = -70dBm DH1 mode			0.1	%
Sensitivity (BER) - Multi-Slot Packets	Input level = -70dBm DH5 mode			0.1	%
C/I Performance	Prescript interface and wanted single settings			0.1	%
Blocking Performance	30MHz to 12.75GHz Interferer signal			0.1	%
Intermodulation Performance	3^{rd}, 4^{th}, 5^{th} order intermodulation			0.1	%
Maximum Input Level	Input level = -20dBm			0.1	%

*Measuring method is compliant with Bluetooth™ Test Specification-RF.

*Measured by using coaxial cable.

4-3. CARD CONFIGURATION

4-3-1. Memory Map

Memory interface shall be selected after being initially powered-up.
Address space of the memory interface is as follows:

<1> Common Memory	Memory area for user data.
<2> Attribute Memory	Memory area for CIS and Card Configuration Register.
	This memory has Read and Write functions.
	You can change to Bluetooth function triggering at FCRs (when writing).

4-3-2. Memory Space

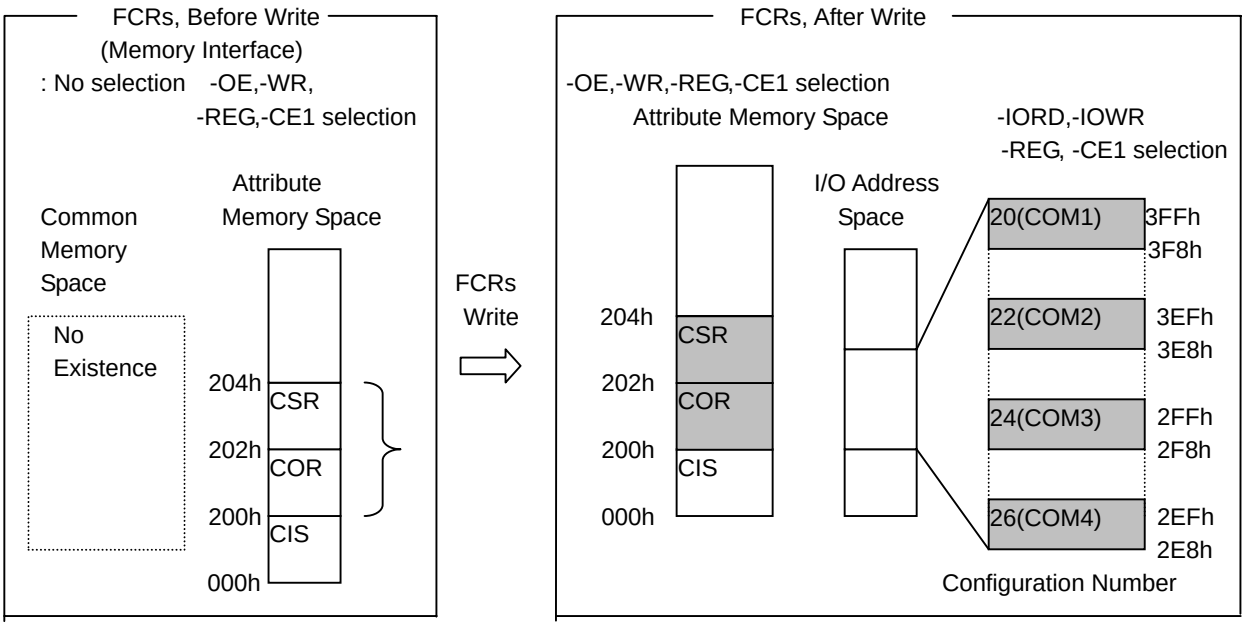
4-3-2-1. Attribute Memory Space

Attribute memory is accessed only even number's sections.
Attribute memory is a memory space selected by -REG, -CE, -WE and -OE signals.
It contains two areas as follows:

<1> Card Information Structure (CIS)	Data noted the features of the device.
<2> Card Configuration Register	Register area for the setup of the operating environment of the device by the system.

4-3-3. I/O Address

I/O address space is the area with I/O interface selected by -REG, -CE1, -IORD, -IOWR signals.



4-3-4. Change Memory Interface to I/O Interface

This device can change the Memory Interface to the I/O Interface by changing FCRs. Before setup the FCRs, we must confirm the CIS to determine the I/O address space, interrupt request and others. In addition, we also confirm other requests from the device. We need to select the proper setup of this device not to loss the hardware and software compatibility.
In fact, by writing the configuration entry number to the Function Configuration Index in the Configuration Option Register (COR) of FCRs, the I/O Interface is automatically initialized.
In addition, you can't re-write to FCRs after changing the I/O Interface. However in case you have to re-write, please reset it.

4-3-5. Initialization of I/O Interface

This device can change to an I/O Interface triggering at Function Configuration Index (when writing) of CCR in the Attribute Space.
If you write an I/O Interface once, the system OS can't change a Memory Interface but RESET it.
The system can't access the device until the initialization of I/O Interface would be completed.

4-3-6. Attribute Memory Access

-CE1	-REG	-WE	-OE	A0	VPP1,2	A1-6	Operating mode	I/O pins D0 – D7
H	X	X	X	X	VCC	X		High-Z
H	L	H	L	X	VCC	X		High-Z
L	L	H	L	L	VCC	X	Read	Even byte
L	L	H	L	H	VCC	X	Read	Invalid
H	L	L	H	X	VCC	X		Don't care
L	L	L	H	L	VCC	X	Write	Even byte
L	L	L	H	H	VCC	X	Write	Don't care

4-3-7. Internal Register

4-3-7-1. Function Configuration Register (FCR)

This device can be configured by FCRs. The FCRs is in an Attribute Memory Space and the address is determined by Configuration Register Address of CIS.
This device contains of 2 registers. These registers is able to Read and Write functions.

-WE	-OE	-CE	-REG	A4-A9	A3,2	A1	A0	Selected register	Addres
H L	L H	L L	L L	H H	L L	L L	L L	COR READ COR WRITE	0200h
H L	L H	L L	L L	H H	L L	H H	L L	CSR READ CSR WRITE	0202h

*Function Configuration Register shall be reset by system hardware reset.

(1) Card Configuration Option Register (COR)

COR is used to the configuration and the software reset. This register has Read and Write functions with 3 fields. The default setting is 00h. When software reset, this register can't be default condition. Hardware reset keeps 00h until host would change the setup.
By writing Configuration Entry Number of Configuration entry Topple to Function Configuration Index, the device is able to use I/O Address Space supported it.
Please refer to the UART register about the support of the Configuration Entry Number and I/O address Space.

D7	D6	D5	D4	D3	D2	D1	D0
SReset	Not used(LevIREQ)	Function Configuration Index					

D7: SRESET (Soft Reset)		This device would be reset if this bit sets 1. When this bit is 1, all the Function Configuration Register would be clear but this bit. It's same function as hardware reset except this bit sets 1. When 0, the device is the condition of reset cancellation at power Supply.			
D6 : Not used		This bit sets 1.			
Function Configuration Index	D5 Card Enable	When this bit is 1, this device change from Memory Interface to I/O Interface. When 0, it doesn't work as a I/O functions.			
	D4, 3	0 is expected			
	D2, 1	D2	D1	I/O base address	Depends on I/O base address
		0 0 1 1	0 1 0 1	3F8h 2F8h 3E8h 2E8h	COM1 COM2 COM3 COM4
	D0	0 is expected			

(2) Card Configuration Status Register (CSR)

D7	D6	D5	D4	D3	D2	D1	D0
Changed	SigChg	Iosi8	RFU	Audio	PwrDwn	Intr	IntAck

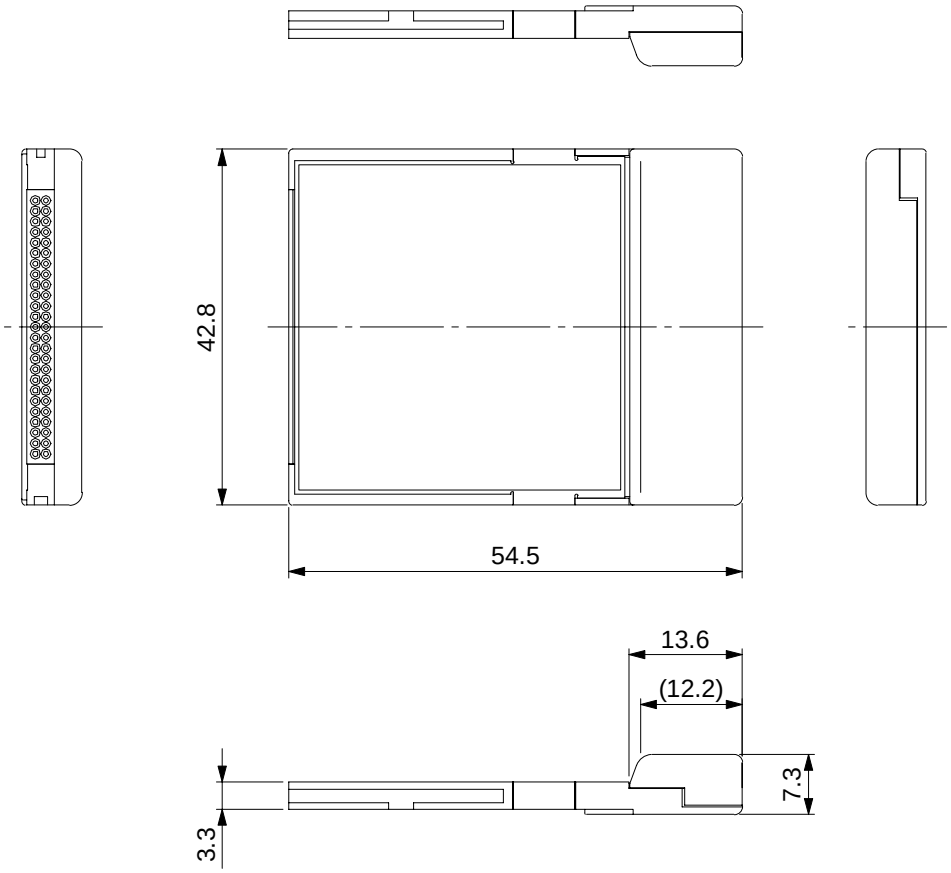
D7 – D0	Not used (All 0)

4-3-8. UART Register (I/O Interface)

This device is supported UART with each 16 bytes FIFO memory at the transmitter and receiver part. This UART register is compatible with 16550A.

5. MECHANICAL CHARACTERISTICS

5-1. APPEARANCE AND DIMENSIONS



Unit: mm

5-2. CF INTERFACE ASSIGNMENTS AND PIN DESCRIPTION

· CF (50 Pin) Interface Assignments

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	GND	14	A6	26	-CD1	39	NC
2	D3	15	A5	27	NC	40	-VS2
3	D4	16	A4	28	NC	41	RESET
4	D5	17	A3	29	NC	42	-WAIT
5	D6	18	A2	30	NC	43	-INPACK
6	D7	19	A1	31	NC	44	-REG
7	-CE1	20	A0	32	NC	45	-SPKR
8	NC	21	D0	33	-VS1	46	-STSCHG
9	-OE	22	D1	34	-IORD	47	NC
10	A9	23	D2	35	-IOWR	48	NC
11	A8	24	-IOIS16	36	-WE	49	NC
12	A7	25	-CD2	37	-IREQ	50	GND
13	VCC			38	VCC		

· Pin Description

Pin No.	Symbol	I/O	Description
2~6, 21~23	D0 ~ D7	I/O	Data bus
10~12 14~20	A0 ~ A9	I	Address bus
7	-CE1	I	Card Enable
9	-OE	I	Output Enable
36	-WE	I	Write Enable
26	-CD1	I	Card Detect 1
25	-CD2	I	Card Detect 2
44	-REG	I	Register select & I/O Enable
41	RESET	I	Card Reset
42	-WAIT	O	Extend bus cycle
34	-IORD	I	I/O Read
35	-IOWR	I	I/O Write
43	-INPACK	O	Input Port Acknowledge
24	-IOIS16	O	I/O Port is 16 bit
37	-IREQ	O	Interrupt Request
45	-SPKR	O	Audio Digital Waveform
46	-STSCHG	O	Card Status Changed
33	-VS1	O	Voltage Sense 1
40	-VS2	O	Voltage Sense 2
13,38	VCC	-	Supply Voltage
1,50	GND	-	Ground
8,27-32,39 47-49	NC		No Connection

Additional information in accordance with requirements of FCC 15.247 and FCC Public Notice DA 00-705

1. Hopping frequency requirements

The number of hopping frequencies is measured in accordance with FCC Public Notice DA 00-705 and reported the compliance in the test report.

On pseudorandom frequency hopping sequence the following is an example of a 79 hopping sequence in **data transmission mode**:

47, 21, 44, 23, 42, 53, 46, 55, 33, 48, 52, 35, 50, 20, 54, 67, 56, 37, 60, 39, 58, 69, 62, 71, 64, 25, 68, 27, 66, 57, 70, 59, 72, 29, 76, 31, 74, 61, 78, 01, 63, 41, 05, 43, 03, 73, 07, 75, 09, 45, 13, 40, 11, 77, 15, 00, 16, 28, 49, 22, 34, 02, 19, 06, 17, 51, 32, 14, 36, 04, 12, 26, 18, 38, 24, 08, 30, 65, 10

Example of a hopping sequence in **inquiry mode**:

47, 08, 71, 57, 63, 02, 61, 45, 55, 10, 59, 73, 65, 69, 27, 43, 00, 77, 04, 67, 37, 06, 31, 75, 33, 39, 51, 40, 29, 14, 35, 49

Example of a hopping sequence in **paging mode**:

08, 57, 70, 68, 51, 02, 40, 42, 04, 61, 46, 44, 63, 14, 50, 48, 16, 65, 54, 52, 67, 18, 58, 56, 20, 53, 60, 62, 55, 06, 66, 64