



# Macaron N Series

## SM-MSBTF-C01

NFC Controller Module with Integrated Antenna

Datasheet Version 1.2

*Smart Your Life, Approach Your Heart.*



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## Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

### Revision 1.0

Revision 1.0 of this datasheet was published in Jun. 2023. This was the first publication of the document.

### Revision 1.1

Revision 1.1 of this datasheet was published in Sep. 2023. Update card instructions and main board design reference. Add download mode concept.

### Revision 1.2

Revision 1.2 of this datasheet was published in Mar. 2024. Update NFC MODULE OUTLINE on page 18.

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## 1 Product Overview

SM-MSBTF-C01 is full featured NFC controllers designed for integration in portable equipment. It is optimized for low power consumption with fully host controllable power states and for small footprint for portable equipment applications.

The module's compact, flexible design with and exposed pad is optimal for size-sensitive applications, assures robust performance.

The following illustration shows a high-level, generic view of a SM-MSBTF-C01 application.

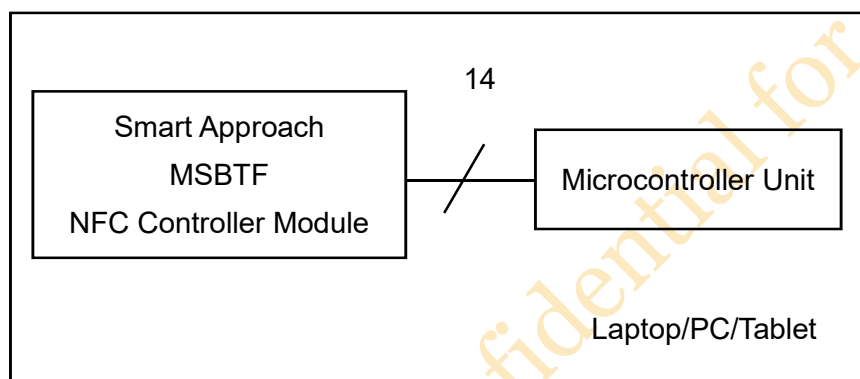


Figure 1 Typical Application

### 1.1 Features

- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated Polling Loop for automatic device discovery
- RF protocols supported
  - ISO/IEC 14443A, ISO/IEC 14443B PICC mode
  - ISO/IEC 14443A, ISO/IEC 14443B PCD mode designed according to NFC Forum digital protocol T4T platform and ISO-DEP
  - FeliCa PCD mode
  - MIFARE PCD encryption mechanism (MIFARE 1K/4K)
  - NFC Forum tags T1T, T2T, T3T, T4T and T5T
  - NFCIP-1, NFCIP-2 protocol
  - NFC Forum certification for P2P, reader and card mode
  - FeliCa PICC mode
  - ISO/IEC 15693/ICODE VCD mode
  - NFC Forum-compliant embedded T4T for NDEF short record

- Supported host interfaces
  - NCI protocol interface according to NFC Forum standardization
  - I2C-bus High-speed mode
- Flexible clock supply concept to facilitate PN7160 integration
  - Internal oscillator for 27.12 MHz crystal connection
  - Integrated PLL unit to make use of device reference clock and facilitate PN7160 integration
- Integrated power management unit
  - Direct connection to a battery (2.3 V to 5.5 V voltage supply range)
  - Support different low-power states configuration: Hard Power-Down state and Standby states activated by firmware
  - Autonomous mode when host is shut down
- Automatic wake-up via RF field, internal timer and I2C-bus interface
- Integrated non-volatile memory to store data and executable code for customization
  - Anti tearing support to recover from tearing events
- Standards compliance
  - NFC Forum Device Requirements
  - NCI 2.0

\*All card types and it's protocol shall follow NXP's and NFC forum recommendation.

Cards that comply with the protocol are subject to testing with the host.

## 1.2 Application

Suggested applications for the SM-MSBTF-C01 module include:

- Mobile devices
- Portable equipment (personal digital assistants, tablet, notebook, wearable)
- Consumer devices
- Smart home gateways

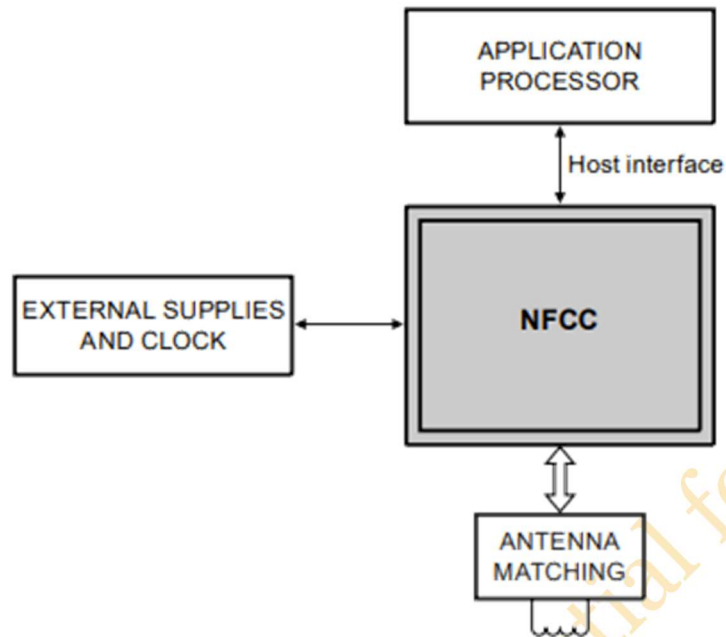


Figure 2 Typical Application II

SM-MSBTF-C01 can be connected on a host controller through I<sup>2</sup>C-bus interfaces. The logical interface towards the host base band is NCI-compliant with additional command set for SA specific product features.

Moreover, SM-MSBTF-C01 provides flexible and integrated power management unit in order to preserve energy supporting Powered by the Field and Power Off mode.

## 2 Functional Descriptions

This section provides detailed information about how SM-MSBTF-C01 module works, what configurations and operational features are available.

The following illustration shows the primary functional blocks of SM-MSBTF-C01 module.

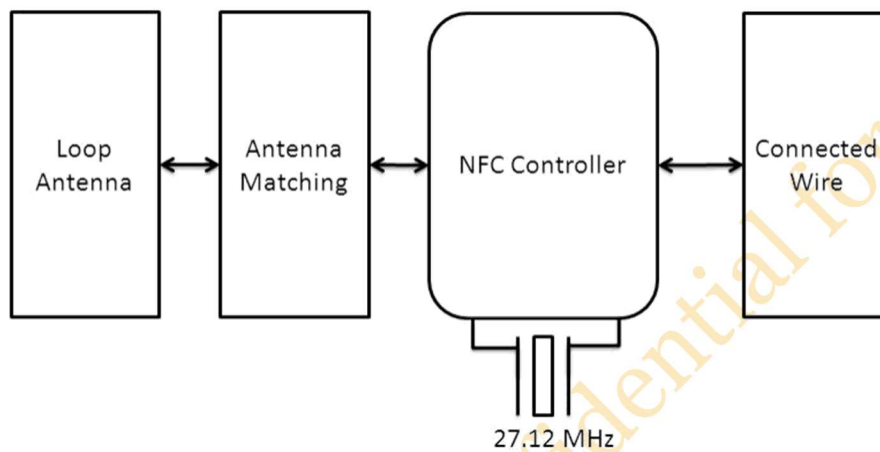
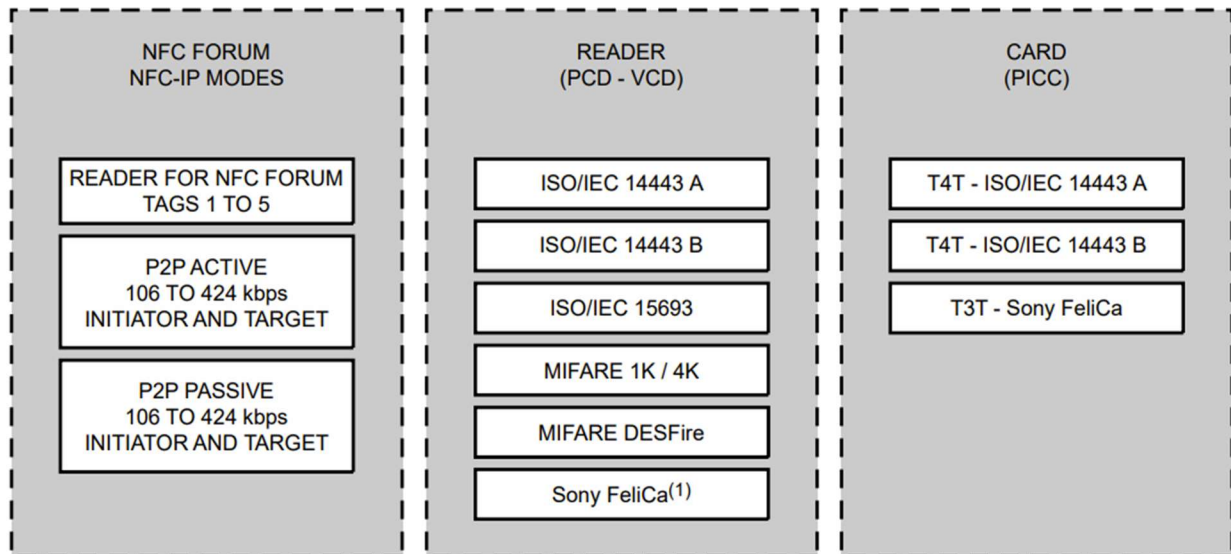


Figure 3 Module Block Diagram

Loop Antenna is Smart Approach customize solution, Antenna size of SM-MSBTF-C01 is 45mm x 35 mm. Antenna matching is also a customize solution. NFC controller includes NXP PN7160 chipset, and has an I<sup>2</sup>C control interface through the connector to mother board.





1. According to ISO/IEC 18092(Ecma 340)standard.
2. PICC only for android HCE.

Figure 4 Transmission Modes

For contactless card functionality, SM-MSBTF-C01 can act autonomously if previously configured by the host in such a manner.

## 2.1 Communication overview for ISO/IEC 14443A / MIFARE Controller

The contactless coprocessor and the on-chip CPU of SM-MSBTF-C01 handle the complete ISO/IEC 14443A/MIFARE RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

### 3 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions. It includes information on the various timing functions of the module.

#### 3.1 Pin Description

The following Table shows the pin description for SM-MSBTF-C01 module.

The connection ground is internally connected and should be connected to GND on the main board as well.

Table 1 Module Pin Description

PIN No.	Name	Description	Power Reference	P/I/O
1	V <sub>BAT</sub>	Battery Supply Voltage	3.3V	P
2	V <sub>BAT</sub>	Battery Supply Voltage	3.3V	P
3	I <sup>2</sup> C_SCL	I <sup>2</sup> C-bus Clock Line	VDD_IO	I
4	I <sup>2</sup> C_SDA	I <sup>2</sup> C-bus Data Line	VDD_IO	I/O
5	IRQ	Interrupt request from module to platform, Normal : Low; Interrupt : High	VDD_IO	O
6	V <sub>EN</sub>	Reset pin input from the host to wake up the device from standby and also to reset the device, Normal : High; Reset : Low	V <sub>BAT</sub>	I
7	DWL_REQ	Firmware download control: Normal : Low; Active : High	VDD_IO	I
8	Reserve2	N.C.	-	-
9	Reserve1	N.C.	-	-
10	MOD_GND	Module Ground	GND	P
11	MOD_GND	Module Ground	GND	P
12	VDD_IO	Pad Supply Voltage	1.8V/3.3V	P
13	VANT	N.C.	-	-
14	MOD_GND	Module Ground	GND	P

#### 3.2 I<sup>2</sup>C Address

SM-MSBTF-C01 I<sup>2</sup>C 7bit address is defined to 0x28. To write data, this module is addressed using 0x50, to read data, this module is addressed using 0x51.

Table 2 I<sup>2</sup>C Address

I <sup>2</sup> C address (R/W=0, write)	I <sup>2</sup> C address (R/W=1, read)
0x50	0x51

### 3.3 Temperature Maximum Ratings

Thermal specifications for this module have been modeled using a two-layer test board.

Table 3 Temperature Maximum Ratings

Symbol	Definition	Value		Units
		Min	Max	
T	Operating Temperature	-25	85	°C
T <sub>s</sub>	Storage Temperature	-40	100	°C

### 3.4 DC Electrical Parameters

DC Electrical specifications for this module have been modeled using a two-layer test board.

Table 4 DC Electrical Specification

Symbol	Definition	Value			Units	Note
		Min	Typ	Max		
V <sub>BAT</sub>	Power Supply	3.1	3.3	5.5	Volts	
I <sub>VBAT</sub>	DC Current			290	mA	(1)

**Note:**

1. continuous total current consumption in PCD mode at V<sub>BAT</sub> = 3.6 V

### 3.5 Antenna Specifications

Antenna specifications for this module have been modeled using a two-layer test board.

Table 5 Antenna Specifications

Item	Value			Unit	Note
	Min	Typ	Max		
<b>DC Resistance</b>	0.5	1	2	$\Omega$	
<b>AC Impedance</b>		50		$\Omega$	
<b>Frequency</b>	13.06	13.56	14.06	MHz	
<b>Q factor</b>	25	30	35		
<b>Antenna Type</b>	FR4 Loop Coil				Add the Ferrite sheet
<b>Size</b>	(45 ±0.3) X (35±0.3)			mm	

### 3.6 Power Consumption

Table 6 Current Consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>I<sub>HPD</sub></b>	Hard power down current	V <sub>BAT</sub> =3.6V, V <sub>EN</sub> =0V	-	10	24	$\mu$ A
<b>I<sub>STBY</sub></b>	Standby state current	V <sub>BAT</sub> =3.6V	-	20	35	$\mu$ A
<b>I<sub>ACT</sub></b>	Active state current	V <sub>BAT</sub> =3.6V	-	4.55	-	mA
<b>I<sub>TVDD</sub></b>	Transmitter supply current	V <sub>BAT</sub> =3.6V	-	240	-	mA

\*Active state : Idle and Listenser modes.

### 3.7 Thermal Protection

Table 7 Thermal Protection

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>OVERTEMP</sub></b>	Temperature protection trigger		-	125	125	$^{\circ}$ C

### 3.8 System power modes

Table 8 System Power Mode Configuration

$V_{BAT}$	VDD_IO	$V_{EN}$	Power mode
Off	X	X	Power Off
On	X	Off	Hard Power Down
On	Off	On	Standby
On	On	On	Active

Note: X: Don't care

Table 9 System Power States

Power State name	Description
<b>Hard Power Down</b>	The MSBTF is supplied by $V_{BAT}$ within its operating range and MSBTF is kept in Hard Power Down ( $V_{EN}$ voltage is kept low by host or SW programming) to have the minimum power consumption. The system mode is in Power Off.
<b>Standby</b>	The MSBTF is supplied by $V_{BAT}$ within its operating range, $V_{EN}$ voltage is high (by host or SW programming) and minimum part of MSBTF is kept supplied to enable configured wake-up sources which allow to switch to Active state; RF field, Host interface (if VDD_IO is high). The system mode is Low-power mode or Full power mode.
<b>Active</b>	The MSBTF is supplied by $V_{BAT}$ within its operating range, $V_{EN}$ voltage is high (by host or SW programming), VDD_IO is high and the MSBTF internal blocks are supplied. 3 sub-modes are defined: Idle, Listener and Poller. The system mode is Full power mode.

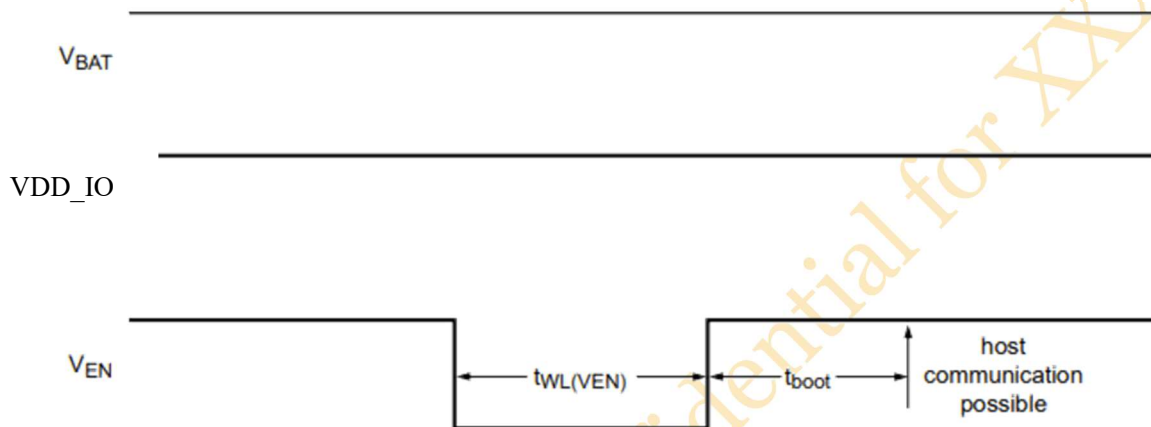
### 3.9 Reset concept

To enter reset, the  $V_{EN}$  voltage shall be set to low (this is also the Hard Power Down state):

Reset means resetting the embedded FW execution and the registers values to their default values. Parts of these default values are defined from EEPROM data loaded values, others are hardware defined.

To get out of reset:

- Pulling  $V_{EN}$  voltage high with  $V_{BAT}$  within its operating range



aaa-024833

Figure 5 Reset via  $V_{EN}$  pin

Table 10 Reset Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{WL(VEN)}$	pulse width VEN LOW	to reset	10	-	-	$\mu s$
$t_{boot}$	boot time		-	-	2.5	ms

### 3.10 Download mode concept

To enter this mode, the pin DWL\_REQ shall be pulled to VDD\_IO before reset via VEN pin is done.

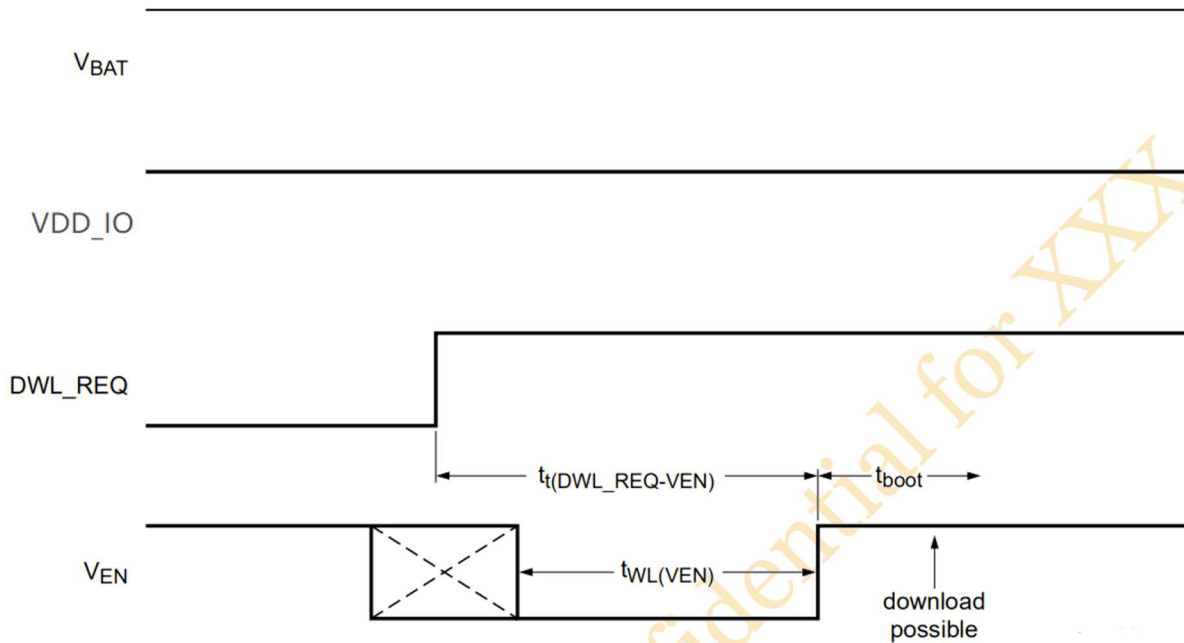


Figure 6 Download mode sequence

Table 11 Download mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{t(DWL\_REQ-VEN)}$	transition time from pin DWL_REQ to pin VEN	DWL_REQ, VEN voltages = HIGH	0	0.5	-	ms

### 3.11 NFC Connection Recommendation

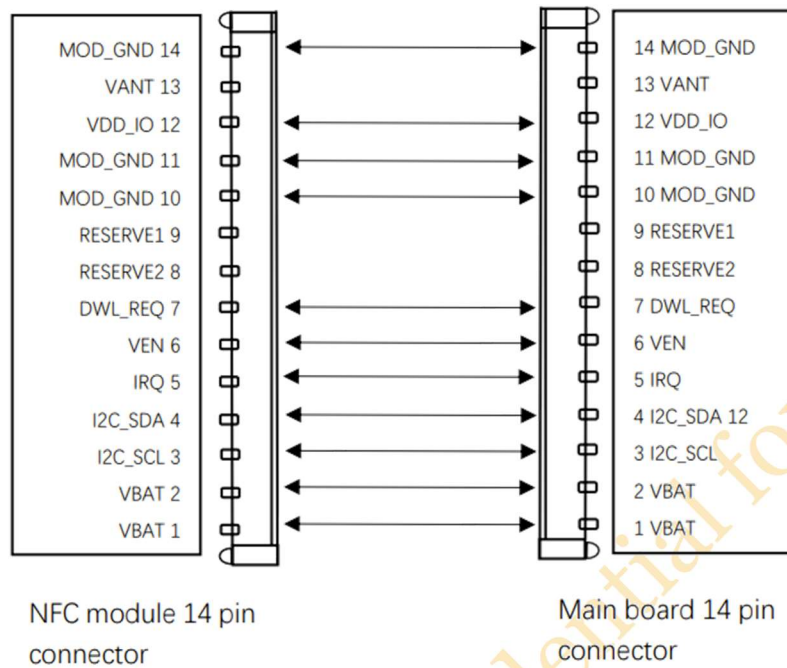
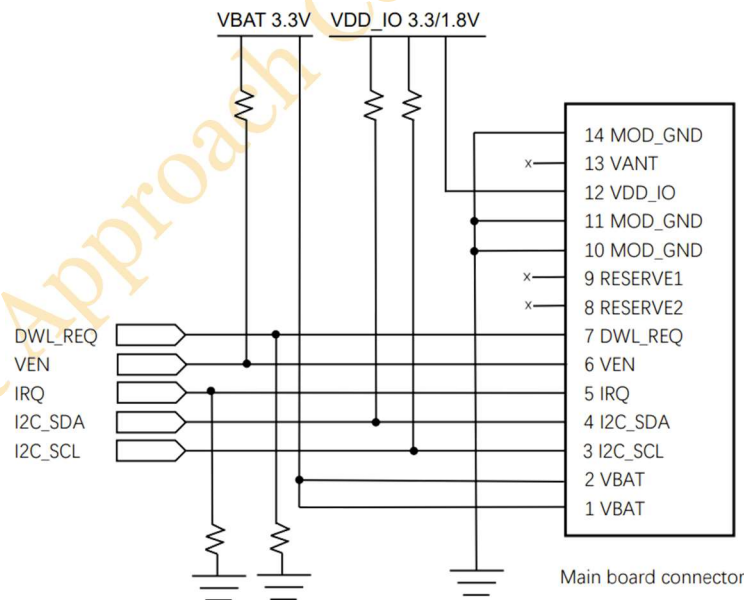


Figure 7 Connection Recommendation

### 3.12 Main Board Design Reference



I2C\_SDA, I2C\_SCL, VEN, DWL\_REQ, IRQ have pull-up or pull-down resistors inside the module, the main board is recommended to reserve the pull-up or pull-down resistors position (not SMD components).

Figure 8 Main Board Design W/O UICC Reference



## 4 Ordering Information

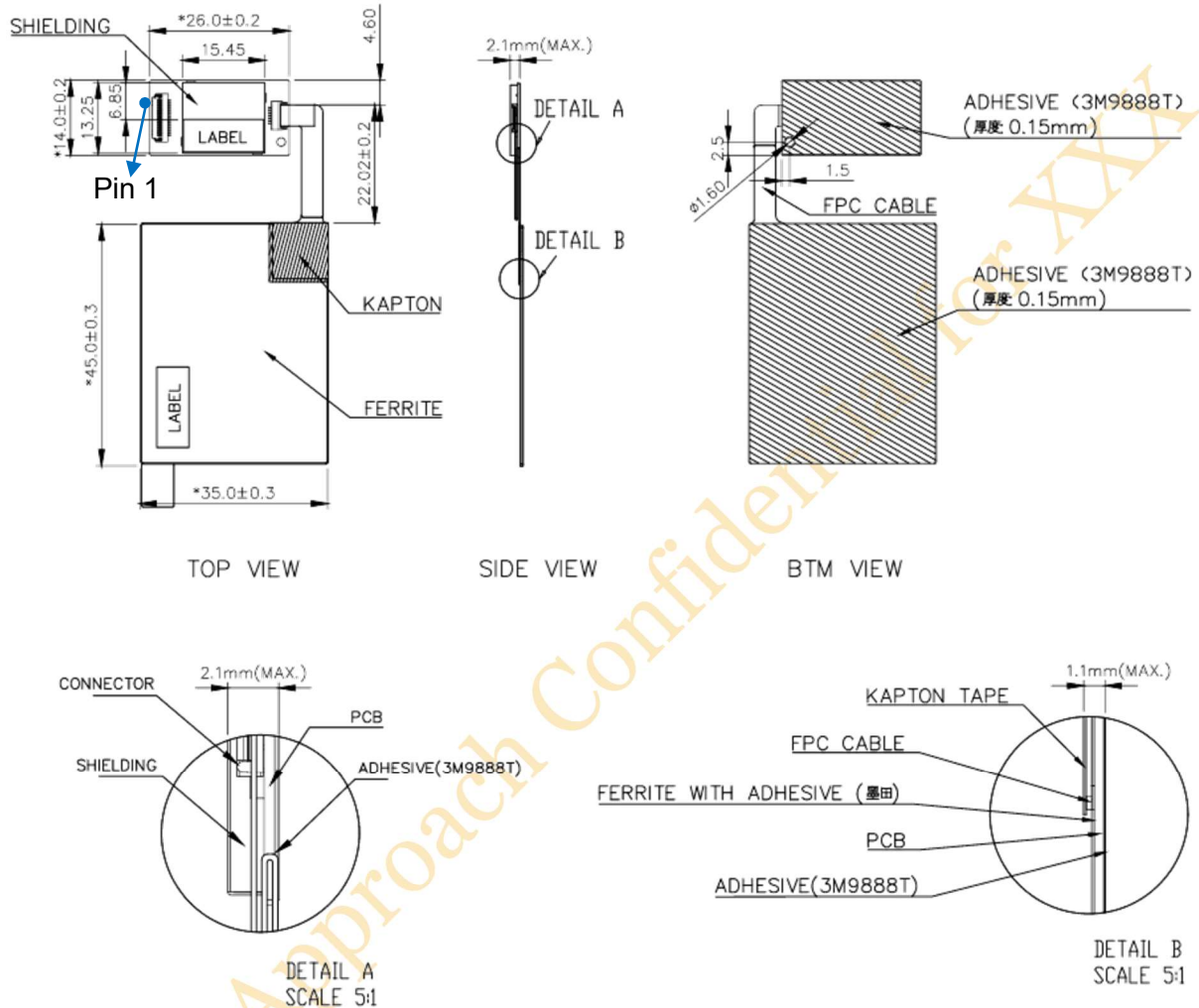
Table 12 Ordering Information Table

Order Number	Descriptions
SM-MSBTF-C01	NFC Macaron Module (NXP PN7160) with Integrated Antenna
Dimension	Module: 71.62 x 35 x 2.1 mm


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## 5 NFC Module Outline

The following illustration shows the package drawing for SM-MSBTF-C01 module. The drawing contains the detail views, dimensions, tolerances and notes.



Mark " \* " is process control dimension.

Mark "  " is FAI control dimension.

Tolerance unless otherwise specified				
Class	A grade	B grade	C grade	D grade
0~10	±0.1	±0.1	±0.2	±1.0
10~50	±0.15	±0.2	±0.3	±2.0
50~100	±0.15	±0.3	±0.3	±2.0
100~250	±0.2	±0.4	±0.5	±3.0
250~500	~	±0.5	±1.0	±3.0
ANGLE	±1/2	±1	~	~

Figure 9 Antenna Module Drawing

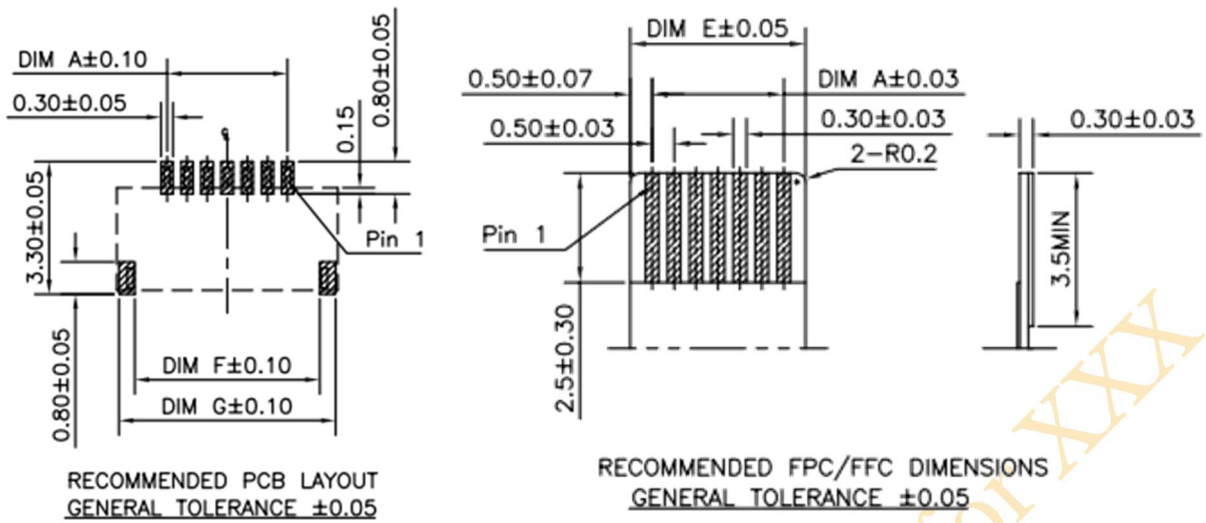


Figure 10 Module FPC Connection Footprint (Button Contact)

CKT	DIM A	DIM B	DIM C	DIM D	DIM E	DIM F	DIM G	DIM H	DIM J	DIM K
04	1.50	4.0	2.57	3.33	2.50	3.10	3.90			
05	2.00	4.5	3.07	3.83	3.00	3.60	4.40			
06	2.50	5.0	3.57	4.33	3.50	4.10	4.90			
07	3.00	5.5	4.07	4.83	4.00	4.60	5.40			
08	3.50	6.0	4.57	5.33	4.50	5.10	5.90		3.0	
09	4.00	6.5	5.07	5.83	5.00	5.60	6.40			
10	4.50	7.0	5.57	6.33	5.50	6.10	6.90			
11	5.00	7.5	6.07	6.83	6.00	6.60	7.40			
12	5.50	8.0	6.57	7.33	6.50	7.10	7.90			
13	6.00	8.5	7.07	7.83	7.00	7.60	8.40			
14	6.50	9.0	7.57	8.33	7.50	8.10	8.90	3.0		2.5
15	7.00	9.5	8.07	8.83	8.00	8.60	9.40			
16	7.50	10.0	8.57	9.33	8.50	9.10	9.90			
17	8.00	10.5	9.07	9.83	9.00	9.60	10.40			
18	8.50	11.0	9.57	10.33	9.50	10.10	10.90		6.0	
19	9.00	11.5	10.07	10.83	10.00	10.60	11.40			
20	9.50	12.0	10.57	11.33	10.50	11.10	11.90			

Figure 11 FPC Wire Dimension