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Declaration

This hard ware " Theory of Operation" high level design document is basically developed for BGAN POCKET SIZE (A5) USER TERMINAL – **Wideye**, **SABRE 1** product was under Inmarsat global PLC, Contract of design & development program with Addvalue Communications.

Where as **SABRE RANGER** is a derivative model from SABRE 1, this document is directly applicable and referred for theory of operation of SABRE RANGER , how ever some of exclusion shall be applied for modules / features like Bluetooth, MMI (man machine Interface) LCD Display, Speaker, Battery Charger.

SABRE RANGER is a Ruggedized BGAN terminal for Remote SCADA applications.

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UT High Level Design Document

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ACRONYMS

ACI	Adjacent Channel Interference
ADC	Analog to Digital Converter
ALC	Automatic Level Control
AUT	Antenna Under Test
AWGN	Additive White Gaussian Noise
AGC	Automatic Gain Control
ASIC	Application Specific Integrated Circuit
BER	Bit Error Rate
BB	Baseband signal processor
BGAN	Broadband Global Area Network
CIC	Cascaded Integrator Comb
CN	Core Network
CORDIC	Coordinate Rotation Digital Computer
CS	Circuit Switched
DAC	Digital to Analog Converter
DDC	Digital Down Converter
DUC	Digital Up Converter
DFT	Discrete Fourier Transform
DD	Decision directed
DA	Data aided
EVM	Error Vector Magnitude
EOF	End Of Frame
FEC	Forward Error Correction
FER	Frame Error Rate
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Arrays
GPS	Global Positioning System
GPRS	General Packet Radio Service
HPA	High Power Amplifier
IF	Intermediate Frequency
I/Q	In-Phase/Quadrature
ISI	Inter-Symbol Interference
IAI-2	Inmarsat Air Interface-2
LEO	Low Earth Orbit
LNA	Low Noise Amplifier
ME	Mobile Equipment
MODEM	Modulator and DEModulator
MCU	MicroControl Unit
MMI	Man Machine Interface
MPU	Micro Processor Unit
MT	Mobile Terminal
NCO	Numerically Controlled Oscillator
NDA	Non-Data Aided
PER	Packet Error Rate
PFD	Power Flux Densities
POST	Power On Self Test

PUT	Pocket User Terminal
PS	Packet Switched
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shifted Keying
RAM	Random Access Memory
RAN	Radio Access Network
RHCP	Right-Hand Circular Polarization
RNS	Radio Network Subsystem
ROM	Read Only Memory
RF	Radio Frequency
ROM	Read Only memory
RRC	Root Raised Cosine
RX	Receiver
SFDR	Spur Free Dynamic Range
SIM	Subscriber Identity Module
SNR	Signal-to-Noise Ratio
SOF	Start Of Frame
TBD	To Be Done/Determined
TDM	Time Division Multiplexing
TDMA	Time Division Multiplexing Access
TE	Terminal Equipment
TX	Transmitter
UICC	Universal Integrated Circuit Card
USIM	Universal Subscriber Identity Module
UT	User Terminal
UW	Unique Word

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1 SYSTEM OVERVIEW

1.1 Introduction

This UT High Level Design Document forms part of the deliverables for the Pocket Size I4 BGAN UT Development Programme Final Design Review (FDR).

Inmarsat plans to introduce a new generation 2-way satellite based data service known as Broadband Global Area Network (BGAN), consisting of new generation satellites, new ground station infrastructure, and new BGAN Modems (UT). Addvalue was awarded a contract to develop and deliver to Inmarsat pre-production Broadband Global Area Network (BGAN) compatible Pocket-size User Terminals (PUT). FDR is one of the early major milestones in the contract.

The objective of this document is to describe the overall BGAN PUT design. This shall lead to the eventual implementation, testing and certification of a pocket size BGAN modem for large volume production at market acceptable cost. As part of the design consideration, the Pocket Size BGAN UT shall be compact in design, light weight, perform reliably and have reasonable battery life during operation.

1.2 Pocket Size BGAN UT

1.2.1 Requirements Specification

The implementation of the Pocket Size BGAN UT is based on the following documents:

- BGAN SDM BASELINE, Release 2.1.0 Dated 28 Feb 2003.
- BGAN UT Product Requirements Specification, Issue 1.2 Dated 11 June 2003

The interface support for Terminal Equipment (TE) includes USB, Bluetooth ready, and RJ11 (phone-jack). Other features include a built-in GPS module for UT positioning, UICC/USIM interface for Network Access Control, Man Machine Interface (MMI via TE) for user configurable, firmware upgradeable and power-on self-test (POST).

1.2.2 System Architecture

The proposed system architecture block diagram is shown in Figure 1. It comprises an Antenna section (BGAN & GPS), an RF section (TX and RX), a Baseband Processing &

Channel Unit, a GPS Module, an Embedded System module, and a Power Unit. Technical details for the various functional blocks are described briefly in the subsequent sections. Further details are available in the UT Hardware Design Document.

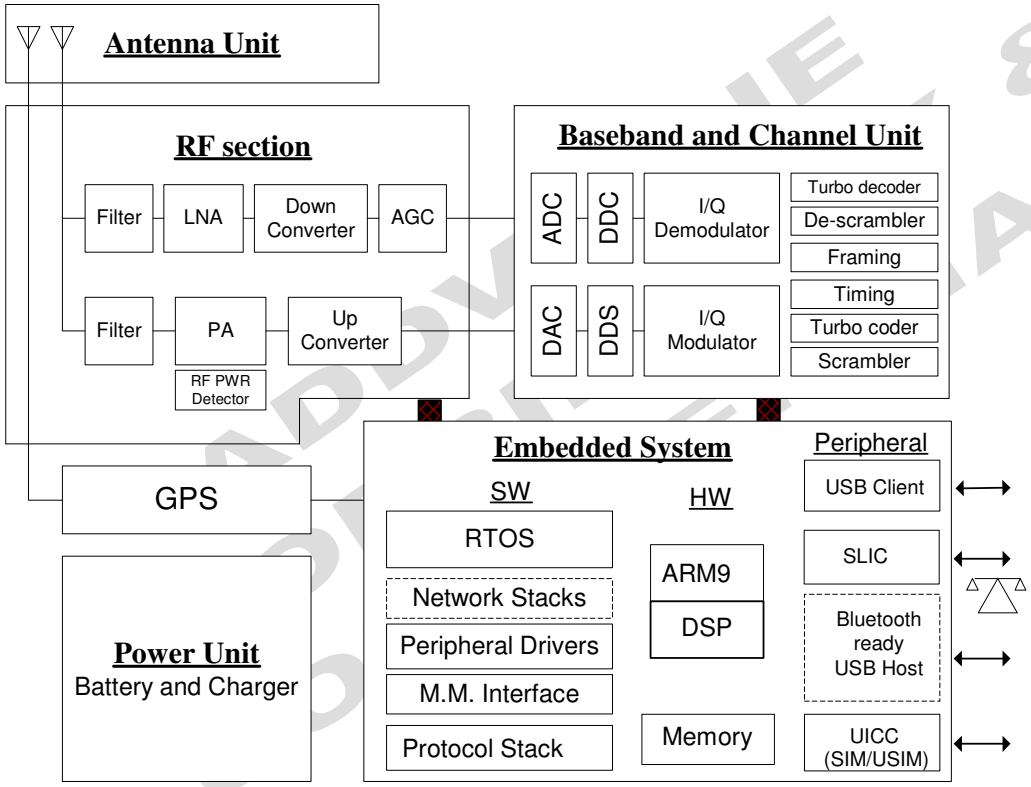

Figure 1: Pocket Size BGAN UT System Architecture Simplified Block Diagram

1.2.3 Components selection & environmental consideration

The UT environmental specification is listed at 0 to 40 degree C. In order to ensure the UT design will meet the environmental specification. The selections of UT components in the design have these specifications, cost and practical considerations in mind.

In the Addvalue UT design, almost all of the semiconductor components selected have temperature range of –40 to +85 degree C. The GPS module is –40 to +55 degree C, Diplexer is –15 to +55 degree C, Battery is –15 to +55 degree C and LCD is 0 to +55 degree C.

The battery is a chemical based component. We can not guarantee the full performance of the UT because the battery power capacity will be reduced at near 0 degree C. Therefore, we have to reduce the UT lower operational temperature range from 0 to +5 degree C when it is powered by battery to ensure full UT performance. The temperature range of 0 to +40 degree C is unchanged when the UT is powered with an external DC power supply.

Beside the battery unit, the LCD unit will be the limiting factor on the environmental operating range of the UT. The power management in the UT will use the information collected from the internal temperature sensor to manage power sequencing, sleep mode behaviors, transmitter duty cycle to reduce the UT power consumption and to ensure user safety, product endurance and the best user experience possible.

2 RF & ANTENNA

2.1 Introduction

The Inmarsat RF transceiver, as shown in Figure 2, consists of the receiver and the transmitter section operating in a frequency range of 1525MHz to 1559MHz and 1626.5MHz to 1660.5MHz respectively. The specification and design guidance for the overall transceiver are described in the UT hardware design document. Along with the proposed design, discrete component selection and measurements results are also included in the UT hardware design document.

The transceiver is expected to operate as a full duplex transceiver. The transceiver shall be able to tune to narrow signaling channel using nominal bandwidth sizes of 10.5KHz, 21KHz, 42KHz, 84KHz and 189KHz wide band traffic channels. The transceiver shall receive a full 200KHz multi-bearer sub-band and from this 200KHz bandwidth pick out narrow channels. Similarly, the transceiver shall have a transmitter capable of burst-to-burst re-tuning inside the assigned 200KHz sub-band.

2.2 Receiver

Dual conversion receiver architecture is chosen as it provides an optimal trade for low cost, interference rejection, and excellent sensitivity for the satellite reception. The Inmarsat receiver spectrum covers from 1525MHz to 1559MHz.

The signal paths originate in the Antenna assembly, which is mounted remotely from the remaining receiver circuitry for best reception. The received signal is initially brought from the Antenna through a shielded RF cable to the RF receiver Unit. In the RF receiver unit, the RF signal is first subjected to a diplexer for isolating the transmitter and also for interference immunity. The signal is then presented to a Low Noise amplifier. This amplified signal is then passed through a 3 pole ceramic filter, which also serves as an image reject filter. The desired signal is boost up and filtered again to improve the gain and noise performance.

The final stage in the front-end receiver is a driver to boost up the signal significantly to ensure sufficient gain before it is presented to the following stage.

The receive signal is then applied to an active double balance mixer with the corresponding Local Frequency (LO) to yield the first Intermediate Frequency (IF) at 248.6MHz. The mixed signal is subsequently applied to a SAW filter to remove the any out of band interference and other intermodulation products generated by the mixer. The 1st 248.6MHz IF signal is then down converted again to the second IF at 10.8MHz by a fixed LO frequency at 237.8MHz. Again the resultant signal is filtered and amplified again. Along the IF chain, ALC circuitries have been strategically placed to keep the signal amplitude consistently before being applied to the Analog-to-Digital converter before going into the baseband. Each of these ALC has a dynamic range of 20dB. Hence the total ALC dynamic range of the whole receiver unit is about 60dB.

2.3 Transmitter

The Inmarsat transmit spectrum covers from 1626.5MHz to 1660.5MHz. Dual up-conversion transmitter architecture is employed for easy filtering.

The signal that originates from the Digital Analog Converter (DAC) output 71MHz.The 71MHz signal is filtered by a SAW filter and amplified before up convert to the second IF frequency at 433.92MHz by a fixed LO frequency at 504.92MHz. The harmonics are filtered by a 433.92MHz SAW filter before up-converting to the desired Inmarsat frequency. A 3-pole ceramic filter further filters the transmitting signal. Finally, the High Power Amplifier (HPA) section will boost the signal. The HPA is a three-stage cascaded amplifier networks based on discrete GaAs FET devices that have superior linearity and high output power. The transmitting signal can be boost up as high as 38dBm to drive the patch antenna for an Effective Isotropic Radiated Power (EIRP) of 10dBW.

2.4 PLL Frequency Synthesizer

The PLL Frequency Synthesizers are responsible for the generation of LO frequencies to both the receiver and transmitter. The PLL Frequency Synthesizers have a common reference clock derived from a 24.192MHz Clipped sine wave TCXO with a frequency stability of +/-2.5ppm. The 237.8MHz and 504.92MHz fixed LO is generated using N-integer PLL Synthesizers responsible for the second stage mixing in the receiver and the first stage mixing in the transmitter. The first stage mixing in the receiver and the second stage mixing in the transmitter derived the desired LO frequencies using two separate N-

fractional PLL Synthesizers. The receive section needs to generate a LO frequency range from 1276.4MHz to 1310.4MHz. The transmit section needs to generate a LO frequency range from 1192.58MHz to 1226.58MHz.

2.5 Frequency plan and spurious consideration

RX frequency	=	1525	~	1559	MHz
TX frequency	=	1626.5	~	1660.5	MHz
RX LO1	=	1276.4	~	1310.4	MHz
TX LO1	=	1192.58	~	1226.58	MHz
TX LO2	=	504.92			MHz
RX LO2	=	237.8			MHz
RX IF1	=	248.6MHz			
RX IF2	=	10.8MHz			
TX IF1	=	433.92MHz			
TX IF2	=	71MHz			

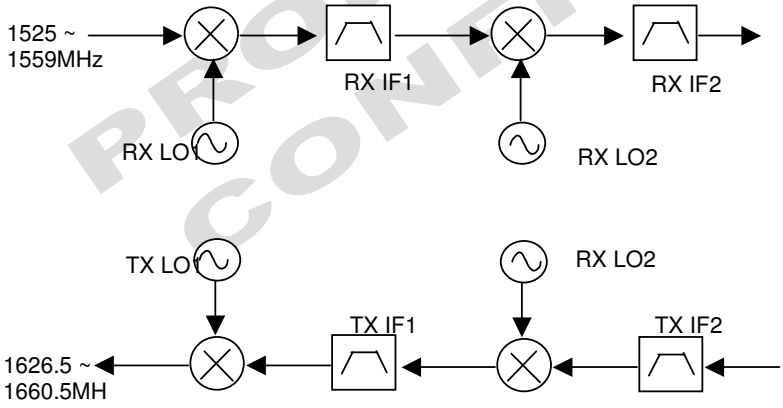

Figure 2: Double Down Conversion Block Diagram

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Harmonics	Ref Clk	TX LO2	RX LO2	RX IF1	RX IF2	TX IF1	TX IF2
Fundamental	**24.192**	**504.92**	**237.8**	**248.6**	**10.8**	**433.92**	**71**
2	48.384	1009.84	475.6	497.2	21.6	867.84	142
3	72.576	1514.76	713.4	745.8	32.4	1301.76	213
4	96.768	2019.68	951.2	994.4	43.2	1735.68	284
5	120.96	2524.6	1189	1243	54	2169.6	355
6	145.152	3029.52	1426.8	1491.6	64.8	2603.52	426
7	169.344	3534.44	1664.6	1740.2	75.6	3037.44	497
8	193.536	4039.36	1902.4	1988.8	86.4	3471.36	568
9	217.728	4544.28	2140.2	2237.4	97.2	3905.28	639
10	241.92	5049.2	2378	2486	108	4339.2	710
11	266.112	5554.12	2615.8	2734.6	118.8	4773.12	781
12	290.304	6059.04	2853.6	2983.2	129.6	5207.04	852
13	314.496	6563.96	3091.4	3231.8	140.4	5640.96	923
14	338.688	7068.88	3329.2	3480.4	151.2	6074.88	994
15	362.88	7573.8	3567	3729	162	6508.8	1065
16	387.072	14642.68	3804.8	3977.6	172.8	6942.72	1136

Table 1: Harmonics table (All in MHz)

		RX		TX		TX		RX	
m	n	mRX LO2 + nRX IF1	mRX LO2 - nRX IF1	mTX LO2 + nTX IF2	mTX LO2 - nTX IF2	mTX LO2 + nRX IF1	mTX LO2 - nRX IF1	mRX LO2 + nTX IF2	mRX LO2 - nTX IF2
1	1	486.4	-10.8	575.92	433.92	753.52	256.32	308.8	166.8
1	2	735	-259.4	646.92	362.92	1002.12	7.72	379.8	95.8
1	3	983.6	-508	717.92	291.92	1250.72	-240.88	450.8	24.8
1	4	1232.2	-756.6	788.92	220.92	1499.32	-489.48	521.8	-46.2
2	1	724.2	227	1080.84	938.84	1258.44	761.24	546.6	404.6
2	2	972.8	-21.6	1151.84	867.84	1507.04	512.64	617.6	333.6
2	3	1221.4	-270.2	1222.84	796.84	1755.64	264.04	688.6	262.6
2	4	1470	-518.8	1293.84	725.84	2004.24	15.44	759.6	191.6
3	1	962	464.8	1585.76	1443.76	1763.36	1266.16	784.4	642.4
3	2	1210.6	216.2	1656.76	1372.76	2011.96	1017.56	855.4	571.4
3	3	1459.2	-32.4	1727.76	1301.76	2260.56	768.96	926.4	500.4
3	4	1707.8	-281	1798.76	1230.76	2509.16	520.36	997.4	429.4
4	1	1199.8	702.6	2090.68	1948.68	2268.28	1771.08	1022.2	880.2
4	2	1448.4	454	2161.68	1877.68	2516.88	1522.48	1093.2	809.2
4	3	1697	205.4	2232.68	1806.68	2765.48	1273.88	1164.2	738.2
4	4	1945.6	-43.2	2303.68	1735.68	3014.08	1025.28	1235.2	667.2
5	1	1437.6	940.4	2595.6	2453.6	2773.2	2276	1260	1118
5	2	1686.2	691.8	2666.6	2382.6	3021.8	2027.4	1331	1047
5	3	1934.8	443.2	2737.6	2311.6	3270.4	1778.8	1402	976
5	4	2183.4	194.6	2808.6	2240.6	3519	1530.2	1473	905
6	1	1675.4	1178.2	3100.52	2958.52	3278.12	2780.92	1497.8	1355.8
6	2	1924	929.6	3171.52	2887.52	3526.72	2532.32	1568.8	1284.8
6	3	2172.6	681	3242.52	2816.52	3775.32	2283.72	1639.8	1213.8
6	4	2421.2	432.4	3313.52	2745.52	4023.92	2035.12	1710.8	1142.8

Table 2: Mixer product output table (All in MHz)

Comments:

1) None of the harmonics of LOs fall into TX and RX frequency band.
2) All IFs have been selected such that their harmonics do not fall into any of the TX and RX frequency band.

Some of the product output from the mixers actually falls within the RX and TX frequency band. However, their signal level should be very weak. To further reduce the effect of these products, low pass filter has been added to LOs to suppress their harmonics level. Special attention will also be given to the PCB layout to avoid cross coupling of such signals into the TX/RX path.

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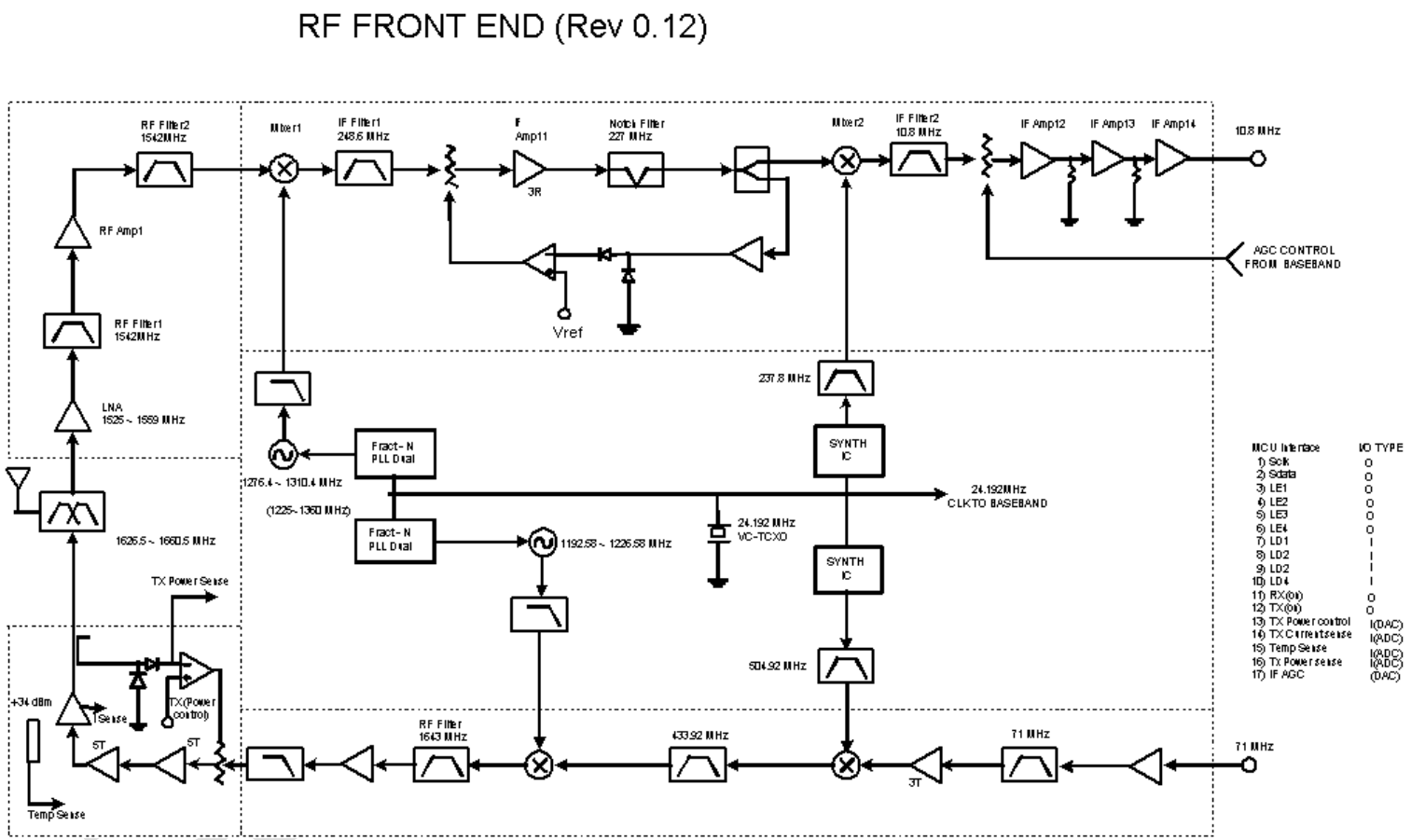

Figure 3: RF Front End Block Diagram

3 BASEBAND PROCESSING & CHANNEL UNIT

3.1 Baseband Processing

3.1.1 Baseband System Overview

The User terminal consists of a satellite MODEM, which allows the users to communicate to the I4 satellite. This MODEM in the user terminal must be working in compliance with the IAI-2 physical layer. The baseband signal processing plays a key role in the satellite MODEM operation.

The objectives of the baseband signal processing system-level design is to trade off between the achievement of the required system PER performance and the low-cost implementation. The baseband signal processor and the channel unit (mainly the turbo encoder/decoder) will be integrated in a FPGA/ASIC to reduce the whole BGAN UT cost. This requires the designers to carefully choose suitable acquisition algorithms and evaluate factors, like the RF transceiver architecture, analog-to-digital conversion scheme, multibearer support, AGC loop, memory usage, and system clock arrangement, etc., in the design considerations.

Structurally, the digital baseband system comprises of the forward link receiving subsystem or demodulator, the return link transmit subsystem or modulator, the baseband system internal control logic, the digital interface to the BGAN UT system microprocessor and the channel code unit system as shown in Figure 4. The UT digital receiver consists of the demodulator and the turbo decoder in the Channel Unit, and the UT digital transmitter consists of the turbo encoder and the modulator. For receiving, the demodulator performs the frame/packet acquisition and demodulation; the channel unit is responsible for turbo-decoding. For transmitting, the modulator performs the signal modulation; the channel unit is responsible for turbo-encoding.

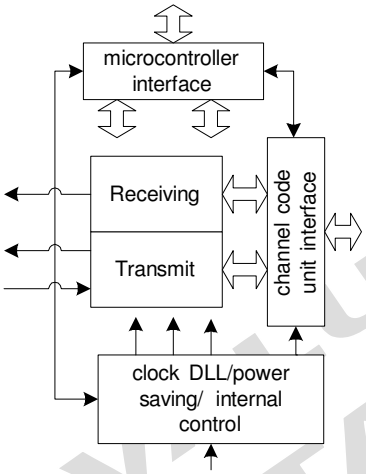

Figure 4: Baseband processor functional block diagram

In the transmit path the baseband processor fetches the turbo-encoded bit stream from the channel code unit and maps them into symbol with either $\pi/4$ QPSK or 16-QAM modulation constellation depending on the bearer type and subtypes. After symbol mapping, both the in-phase and quadrature components of the symbols were filtered by the root-raised cosine filter with $\alpha = 0.25$ at four times of the symbol rate. These band-limited base-band signals are then translated to a certain frequency location in the digital domain from where it will be converted into analog signal and up-converted to the intended RF. The RF signal will be finally radiated through antenna to the I4 satellite.

In the receiving path, the RF signal after the LNA are first down converted to a certain IF by one or more stages of mixing and passband filters. This analog IF signal is converted into digital signal with bandpassing sampling ADC. The IF AGC closed loop maintains the analog signal amplitude before the ADC to be within an appropriate range. After sampling, all the signal processing is converted to the digital domain. The residual carrier offset is removed by multiplying with the output of the numerical controlled oscillators (NCO). The high-rate data samples were then decimated by a CIC filter to be 16X the symbol rate for coarse frequency estimation, and finally the data were decimated to 4X symbol rate for synchronization. With matched filter, using the same set of filters as in the transmission direction, the intersymbol interference (ISI) is reduced. With the

synchronization system, the carrier error and phase error are removed and the true baseband symbol signal were obtained with representation of in-phase and quadrature components and sent to channel coding unit for decoding processing together with the estimated noise variance.

3.1.2 Demodulator

3.1.2.1 Functional Block Diagram

The demodulator architecture depends on the RF transceiver scheme. In this UT transceiver, the RF receiver uses the conventional heterodyne architecture due to its high performance and ease of implementation. Moreover, the BGAN user terminal is required to be multi-mode (different bearer type), and multi-band (multi-bearer). As is well documented, the software-defined radio (SDR) is one of the solutions to meet such application requirements. The UT applies this solution to implement multi-bearer receiving. As a result, the demodulator typically consists of the following processing functions: the analog front-end, the digital down-conversion, the decimation, and the baseband synchronization.

In the analog front-end, a high-performance ADC chip is chosen to convert the analog IF signal to digital data. In the digital down-conversion, the information band is shifted from the IF to the baseband. In the decimation, the highly over-sampled data is decimated to a lower sample rate suitable for baseband signal processing. In the baseband synchronization, the received symbols were qualified in timing and phase. The detailed architecture of UT demodulator is shown in Figure 5.

Thru software-defined radio architecture, the UT demodulator can benefit from the advanced digital signal processing algorithms. That is particularly important for multibearer support and the flexible out-of-band and in-band frequency tuning.

Amongst the four basic demodulator functions, the synchronization processing plays the key role to achieving the required PER performance. In other words, the demodulator capability such as forward bearer acquisition time, the frame detection probability, the receiving robustness in any receiving scenarios, etc, mainly depend on the

synchronization algorithms and their structures. The acquisition capability of a demodulator is one of the most challenging tasks in the UT demodulator implementation.

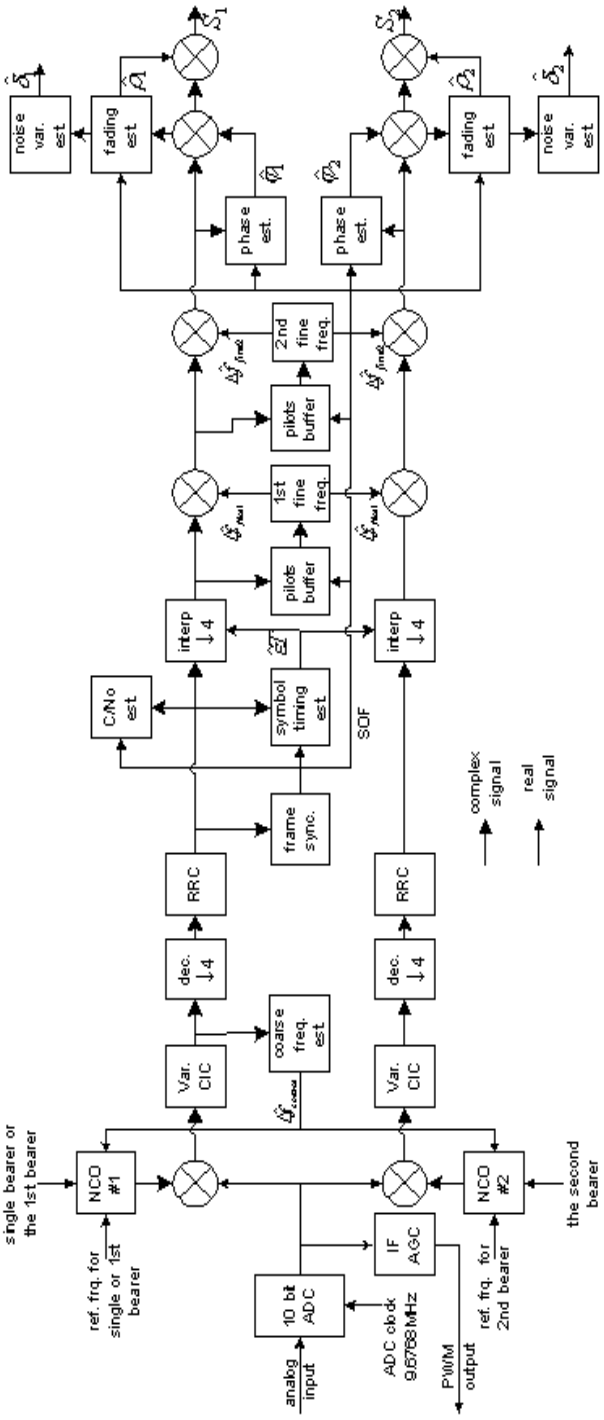

Figure 5: Multi-bearer receiving functional block diagram

At the BGAN's IAI-2 user link side, the I4 satellite continuously illuminates the L-band carrier beam upon a certain region with the Time-Division-Multiplexed (TDM) scheme. All mobile users illuminated in this region can receive the signals from the satellite. As the TDM scheme, a global bearer beam is always being broadcasted on some regions; simultaneously, the regional or spot beams might have been being timing-selectively transmitted to those user terminals already in connection in these regions. The broadcasted global beam carries on the BGAN system information. A UT ready to join the BGAN network system and utilize the service must get the global information first. That is to say, the UT must acquire the global beam bearers before doing anything else. However, the UT does not know the global bearer carrier frequency at power up, so a certain channel frequency estimation processing is needed as shown in Figure 5 before the UT can tune its receiving frequency. In addition to the frequency estimation/tuning, many other synchronization processing such as the frame detection, the symbol timing synchronization, the carrier frequency/phase estimation and correction, etc. are involved in the global bearer acquisition process. This acquisition process is termed "initial" acquisition. The initial acquisition is the first step of the process with which a UT builds its connection to the BGAN network system. This connection building process shouldn't interrupt other UT normal operation.

The TDM scheme also means the forward bearers may change its parameters such as carrier frequency, UW, etc. frame-by-frame during the UT normal operation. As a result, the acquisition will be performed possibly on every subsequent frame. A good synchronization algorithms' structure is that it can complete all the synchronization processing during the time of receiving the UW of this frame. In such ideal case, no frame would be dropped out due to the acquisition time of synchronization processing timing. However, it is very difficult for demodulator to complete all the synchronization processing within a frame's UW for various acquisition scenarios. For example, the forward bearer UW may be changed for the next frame, and this change is not precisely known to the demodulator in advance. Even a little frequency offset leads to symbols loss of synchronization in timing and phase. The PER would increase significantly if the carrier frequency offset were not removed. So the UT demodulator would need to obtain the frequency offset estimate and remove it from the later samples. Any carrier parameters

such as the frequency, the frame timing, and symbol timing etc., changing events at satellite for the next frame would require part or all of the synchronization processing to be activated and any synchronization processing would take a certain time to re-achieve the synchronous status. Until the synchronization status is achieved, the demodulator PER cannot meet the requirement of 1E-3.

The time from the beginning of the first frame where the new parameters are applied till the moment the demodulator achieves the PER of 1E-3 is called acquisition time. The acquisition time for various receiving modes is different. It solely depends on the actual carrier frequency offset value in this mode. Four modes: “initial”, “cold”, “warm”, and “hot”, are classified based on the carrier offset in the SDM V5C1 (rev 2.1)[1]. The actual carrier frequency offset size amongst these modes ranges from about $\pm 9KHz$ to $\pm 1Hz$. The acquisition processing for initial mode has been already mentioned before. The acquisition processing requirement for the other three modes are different from the initial mode.

Whether an acquisition is successful or not is not determined solely by the synchronization algorithms themselves, it depends on the CRC checking by protocol processing where the transmitted PDU data were re-formatted and the CRC received can be checked.

When choosing the demodulator architecture, we must consider each of the synchronization processing algorithm, as well as the structure of these blocks and the sequential order in the whole synchronization system. Those structures that can achieve less acquisition time for all modes will be most suitable for the design.

The architecture shown in Figure 5 highlights the significance of acquisition time of synchronization processing. For example, the frame detection is performed before the symbol timing recovery and carrier frequency and phase recovery. This is because, for each arrived forward frame on the receiver antenna the bearer frame timing could have been changed, the demodulator must look for the new frame timing reference for THIS

[1] “BGAN SDM Vol 5 Chapter 1 Rev 2.1 UT Technical Requirements Specification,” Inmarsat

frame and not the PREVIOUS frame. The start of this frame must be detected first and be made known to the symbol and carrier synchronization processing. The actual symbol timing may not change frame by frame, but the signal processing mechanism must guarantee the symbol timing reference is referred to the SOF of this frame.

3.1.2.2 Synchronization

As mentioned previously, the forward bearer acquisition capability depends on the synchronization algorithms and its structure. In the TDM scheme, some parameters are varied frame by frame. These parameters includes:

1. Carrier frequency offset,
2. The start instant of a frame,
3. The symbol timing
4. The phase (which is always changing symbol by symbol due to phase modulation transmission)

Hence the synchronization system must be able to capture these parameters in order to remove their impact on the demodulator PER. The synchronization will include: carrier frequency synchronization, frame synchronization, symbol timing synchronization, carrier phase recovery. These processing procedures are intrinsically coupled with each other. For example, the carrier frequency error leads to symbol timing synchronization and phase synchronization burden. Joint-parameter estimation algorithm is too complicated for ASIC implementation although its estimation performance is generally better than individual parameter estimation. Hence, the individual parameter estimation is used in the design.

Two kinds of synchronization structures are popularly used: feedback and feedforward. The feedback synchronization algorithms are not suitable for our design because the time taken to achieve acquisition is unacceptable. Moreover, the feedback method leads to the so-called cycle-slip problem, thereby increasing the error rate. Therefore, the feedback synchronization algorithms are inappropriate for UT receiver design of TDM scheme. We use the feedforward synchronization in the UT demodulator. Generally, the feedforward synchronization algorithms include parameter estimators and error removal along the signal path.

There are three types of estimation algorithms: decision-directed (DD), data-aided (DA) and non-data aided (NDA) or blind. Generally, the synchronization acquisition time is determined by the size of the data block or sliding window, which is used for parameter estimator. Amongst these estimators, the NDA algorithms use the largest data block size or sliding data window to achieve the same estimation variance as the other two types of estimators. Therefore, we usually look for any possible DD- or DA- estimators for parameter estimation. In this UT demodulator, the embedded UW and Pilot symbols in the frame can be used in carrier frequency offset and phase estimation. The basic requirement of using UW or pilot-aided estimator is SOF. It means that the frame synchronization must be done before the actual carrier frequency and phase synchronization. However, the frame synchronization can only work well under the small frequency offset situation. For those cases, e.g., "initial" and "cold" modes, where the carrier frequency offset is relatively large in comparison with the errors that the frame synchronization algorithm can tolerate. Therefore, a separate coarse frequency estimator is required before the frame synchronization and this estimator must be NDA-based algorithm.

3.1.3 Modulator

The transmitter is required to output one 5ms or 20 ms burst signal upon the protocol request command. Based on the return link specification, the modulator should be capable of generating the information carrier with burst transmissions using TDMA. The protocol processor schedules the burst transmission. Before each transmission, the bearer type, subtype, symbol rate, and modulation type should be known prior to the burst generation. The different symbol rates and modulations can be specified in the programmable look up table thus allowing different bearers to be supported. After generating the baseband symbol, the modulator will modulate them on a certain carrier signal. The carrier frequency should be able to be tuned with frequency steps of 1.25 KHz with a NCO. The final modulated digital output is converted to an analog signal via a DAC. The turbo encoder output the bit stream to the modulator, and the modulator will map the bit stream into symbols. The RRC filter is used to limit the transmission bandwidth to within the specified bandwidth, the signal output from the RRC filter is at 4X oversample rate. The baseband signals can be outputted to the digital-to-analog-converter before being upconverted to RF band for transmission. However, it is usually upconverted to a

certain carrier in the digital domain for accurate frequency tuning. In this UT, the digital method is used to fulfill the frequency tuning.

The DAC converts the digital IF data into the analog IF signal. With proper IF bandpass filter, a high spectral-purity analog IF signal with limited bandwidth constrained by RRC filter are obtained, and a simple analog upconverter will be used to convert the IF to RF for transmission. This basic functional block diagram of digital modulator is illustrated in Figure 6.

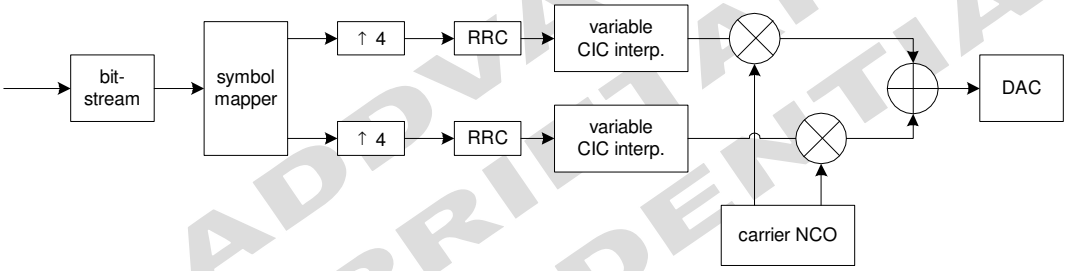

Figure 6: Functional blocks of modulator

An important operation is the interpolation where the low data rate should be raised to the very high data rate, which is defined by the DAC sampling clock. Using the same principle as described in the demodulator, the CIC low pass filter is also used here to perform the interpolation. The sample rate change factor of the CIC interpolator must be variable to support all bearer type. Additionally, a x/SIN(x) filter will be optionally turned on in the hardware depending on the power mask.

3.1.4 Hardware Design

This baseband signal processing is part of the ASIC. The design is going to be done with maximum optimization based on the available hardware resource. Most of the mentioned signal processing circuitries, like the RRC FIR, CIC filters are specifically designed to reuse the hardware resource as much as possible. The power consumption and die size are also the critical implementation consideration.

3.2 Channel Unit

3.2.1 General

3.2.1.1 Introduction

Channel Unit forms part of I4 BGAN PUT design. This functional block is located between I/Q modulation/demodulation and Embedded system as shown in Figure 7. It is part of I4 BGAN PUT physical layer.

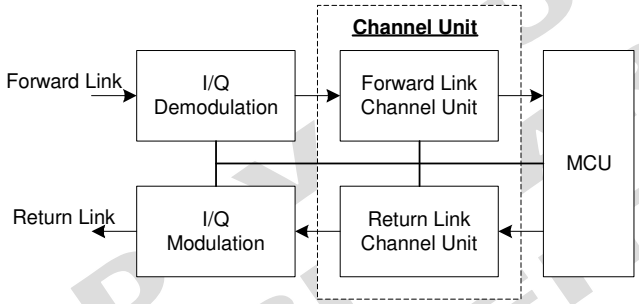

Figure 7: Channel Unit

For the Forward link (modem receiving), the channel unit performs:

- Empty FEC block detection (will be disabled)
- I/Q symbol De-mapping
- Channel de-interleaving and de-puncturing
- Turbo Decoding
- De-scrambling the bit stream

For the Return link (modem transmitting), the channel unit serves:

- Scrambling the bit stream
- Turbo parallel convolutional encoding
- Channel interleaving and puncturing
- Mapping the bit stream into I/Q symbol stream
- Burst formatting and timing control

3.2.1.2 Objective

The design of BGAN PUT Channel unit is in accordance with BGAN SDM Vol.2 Ch.5 Physical Layer Interface, Vol.5 Ch.1 UT Technical Requirement Specification and SDM TTP CDROM.

The Channel unit design will be implemented and verified using FPGA hardware, and subsequently using near-form fit BGAN PUT prototype.

3.2.1.3 Availability and progress

The design of Channel unit include the followings:

1. Channel unit design specification.
2. Floating-point model and simulation of the Turbo encoder/decoder. Both C library and MEX library files should be available, which are used for evaluation of the performance of the system.
3. Fixed-point modeling and simulation of the Turbo encoder/decoder. The model (C library) is used for evaluation of the implementation loss and generating test vectors for hardware design.
4. Forward link and Return link timing plan.
5. Interface to PUT system controller (embedded system).
6. Interface to I/Q modulation and demodulation.
7. Testing plan.
8. Hardware architecture design.

Design work is progressing toward hardware implementation and optimization. An initial HDL channel unit design is available, and it is undergoing simulation and FPGA implementation.

3.2.2 Design Of The Channel Unit

3.2.2.1 Forward Link

The function blocks of the Forward link channel unit are illustrated in Figure 8. The demodulated I/Q symbols are de-mapped, channel de-interleaved and de-punctured into soft-bit systematic code and two Turbo parity codes for Turbo decoding, these codes are stored in X, Y1 and Y2 buffers respectively.

So long the empty block detector does not indicate “empty FEC block”, the Turbo Decoder will decode the FEC block. Turbo Decoder is a key component in the Channel unit: the Log-Map algorithm will be implemented for Turbo codes SISO; a finite state machine controls the iteration of the decoding.

De-scrambled turbo decoded data are presented to embedded system through shared buffer. The MPU reads the FEC block data via DMA controller. The control registers and status registers are accessible by system controller (MPU) under same memory space as in shared buffer.

To cater for bearer and sub-bearer types, the Turbo S-Interleaving LUT and Channel interleaving and Puncturing LUT are generated on the fly. The channel unit generates the S-Interleaving LUT. While the Channel interleaving and Puncturing LUT are generated by the MPU.

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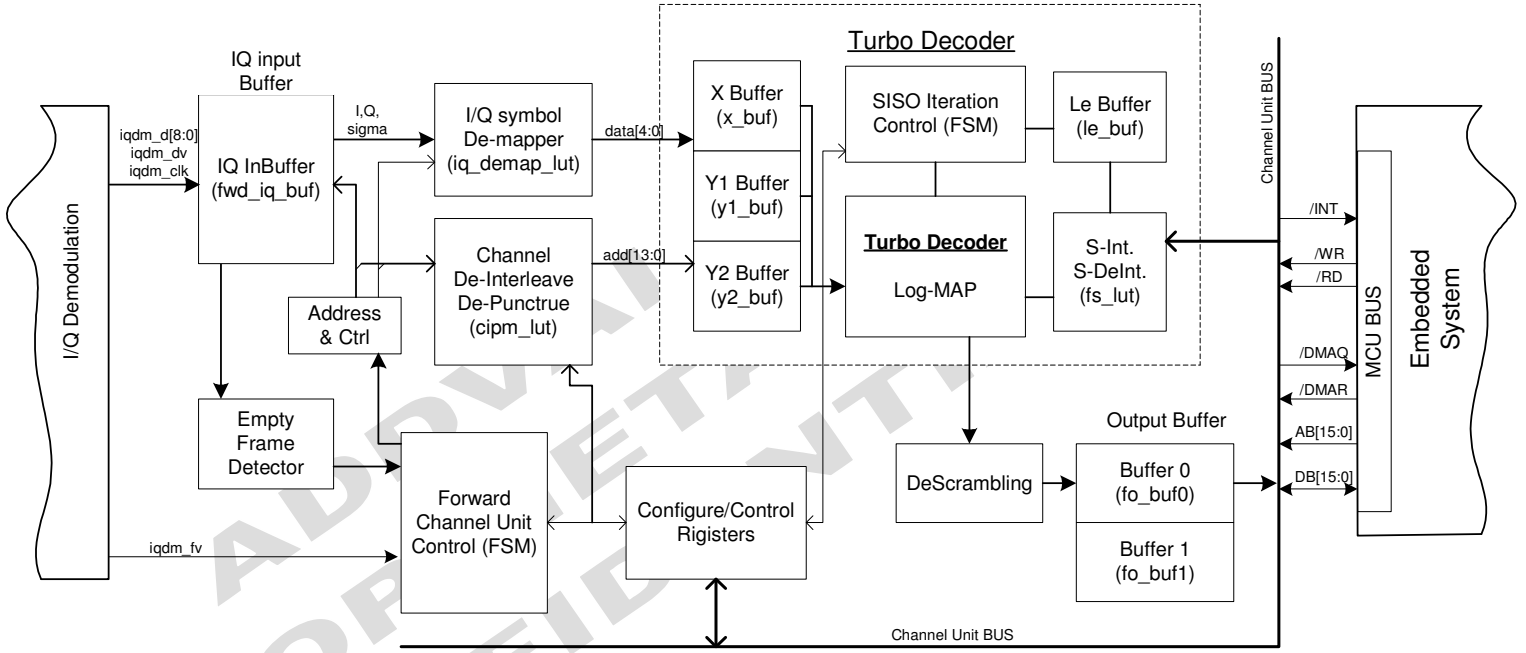


Figure 8: Forward Link Channel Unit

3.2.2.2 Return Link

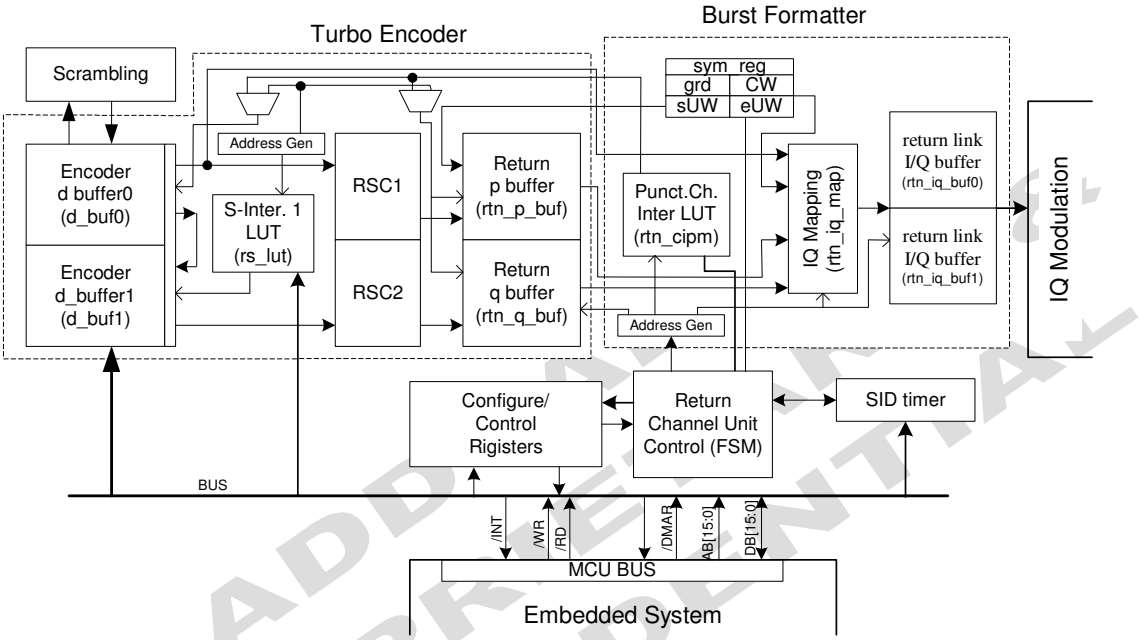


Figure 9: Return Link Channel Unit

The Architecture of Return Link Channel Unit is shown in Figure 9.

The MPU set the configuration registers to configure Return channel unit FSM for various Return Bearer types and sub-types. The S-interleaving LUT and Puncturing and Channel Interleaving LUT are generated by the MPU and loaded into the Return channel unit RAM through DMA interface.

For π/4 QPSK return bearer type, 32 bits Unique Word (UW) goes through RSC to form 32 bits parity UW. 32bit UW plus 1st 8 bits parity UW is used as Start UW of burst frame and 24 bits parity UW is used as End UW. The UW is for Turbo Synchronization. For 16-QAM return bearer, Start UW and End UW are defined and applied in the burst frame.

Return channel unit FSM controls return burst formatting. It adds Guard time, Preamble (CW) symbols and Start UW, End UW to the FEC block and maps into I/Q symbol. For R20T2X bearer type, a burst includes two FEC blocks.

3.2.3 Interfaces Of The Channel Unit

3.2.3.1 General

The block data are exchanged in shared buffers between Baseband and Channel unit, and between Embedded system and Channel unit. Synchronous RAM is used for shared buffer. The direction of data bus and multiplex of address bus are controlled by Channel unit FSM. The parameters, control signals and status of the channel unit are accessed using registers.

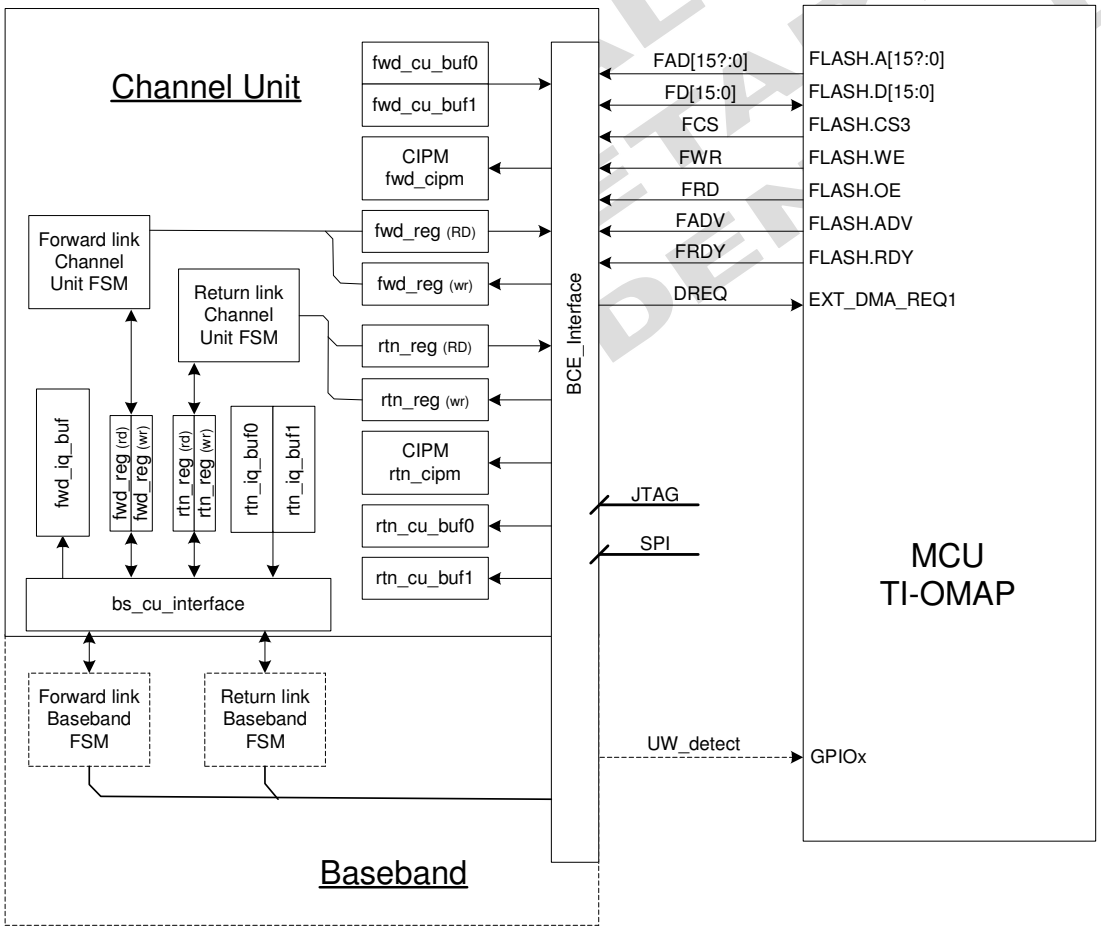


Figure 10: Channel Unit Interfaces

3.2.3.2 Channel Unit to Baseband Processing

3.2.3.2.1 Forward link

A dual-port RAM is used for passing block data from baseband to channel unit.

- Synchronous memory blocks, single port, multiplexed access, sequenced access.
- Baseband writing signals: fwd_iq_ck, fwd_iq_dv, fwd_iq_d[9:0].
- Channel unit reading signals: fwd_iqcu_ck, fwd_iqcu_dv, fwd_iqcu_d[9:0].
- FEC block ready signal: fwd_iq_rdy. Set by baseband, cleared by channel unit.

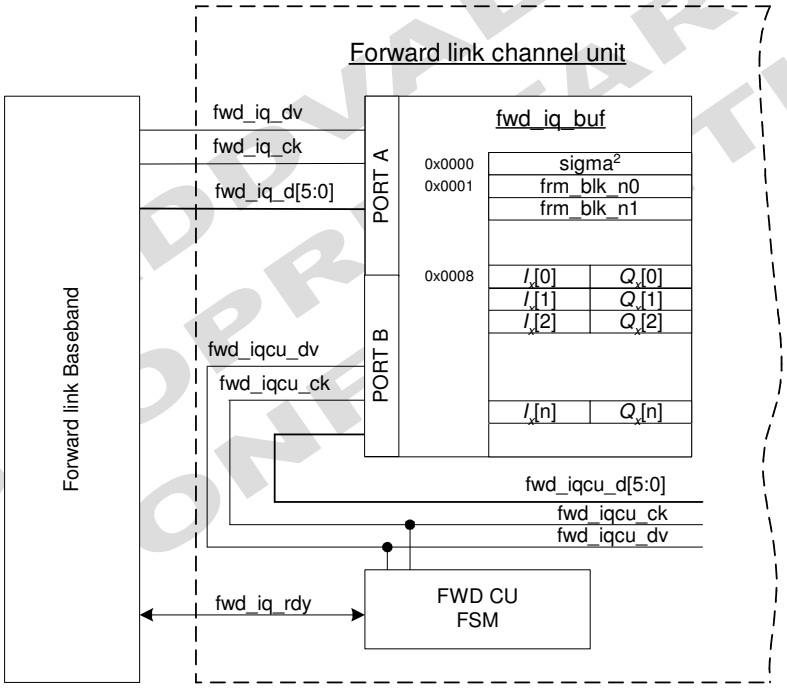


Figure 11: Channel unit I/Q input buffer (forward link)

Channel unit FSM controls the access direction. The Block data contains:

- σ^2,
- Frame No with block No,
- FEC block symbols, etc.

Buffer size: 5992 x 106bits (0x1770, 6 bits). The baseband writing clock is the symbol clock. Channel unit can start reading the buffer once the Turbo decoding is into the 2nd

half of it operation. Even when the reading speed can be fast, the Write flag can be used to slow down the reading speed to avoid over reading.

3.2.3.2.2 Return link

Two pages of shared RAM buffer are used for passing Return link burst to baseband:

- Synchronous RAM, Single port, multiplexed access, two pages toggled.
- Baseband reading, rtn_iq_clk, rtn_iq_dv, rtn_iq_d[3:0].
- Channel unit writing, rtn_iqcu_clk, rtn_iqcu_dv, rtn_iqcu_d[3:0].
- Buffer size: 5088 x 4bits. Two buffers.

As similar as forward link interface to baseband, but two buffers are used in Return link. The buffer contains whole burst symbols.

3.2.3.3 Channel unit to embedded system

The MPU OMAP5910 through EMISF interface to access channel unit and baseband processor as shown on Figure 10. For transferring block data, DMA controller would be used.

The Channel Interleaving and Puncturing LUT (CIPM) are generated on the fly. The C code of the algorithm is available and verified. The required MIP has to be evaluated. The parameters of bearer and sub-bearer type are pre-generated in ".h" file format.

3.2.4 Turbo Codes Encoding/Decoding

3.2.4.1 Design and Simulations

Turbo decoder is a key component in the Channel unit. It not only perform function of channel decoding, it is also a measurement window. The decoder Packet error rate (PER) is used to evaluate the RF, demodulation and system performance, etc. So, it is important to have a perfect turbo decoder.

The design starts with Floating-point simulation of the Turbo decoding algorithm. The Floating-point model will then be used for PUT system simulation, and also as a reference point for Fixed-point simulation.

3.2.4.2 Turbo decoder simulation model

The Turbo coding simulation model is shown on Figure 12. In the modelling, the Ideal I/Q demodulation is assumed; it is for evaluating the Turbo decoder performance only. The noise is added to the I/Q symbol as AWGN channel simulated, that noise variance is derived from specified Es/No.

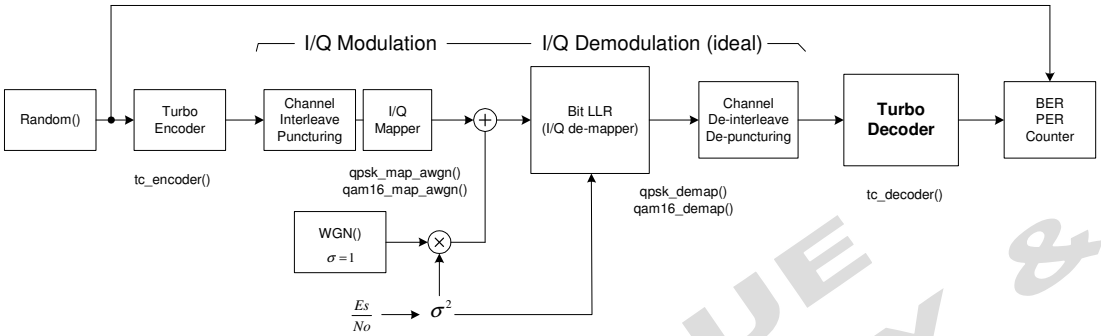


Figure 12: Turbo encoder/decoder float-point model

3.2.5 Hardware Design

Base on fixed-point model, the Turbo decoder algorithm would be easily implemented into hardware. As shown on Figure 13, the SISO consists of LogMAP processor, Le buffer and S-interleaving LUT. The LogMAP processor consists of

- Delta engine,
- Delta store,
- Beta engine,
- Beta store 0/1,
- Alpha engine,
- LLR engine.

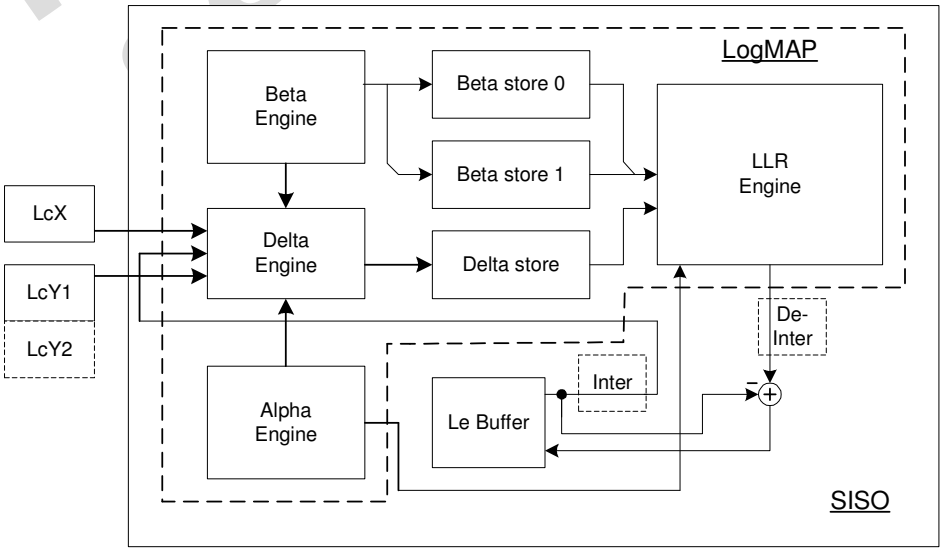


Figure 13: Hardware architecture of Turbo decoder

3.2.6 Conclusion

3.2.6.1 Conclusion for Preliminary Design Review (PDR)

- The Design specification of the channel unit is completed.
- Addvalue's Turbo decoder floating-point model and fixed-point model have been simulated. Both C/C++ library and MEX library are available.
- The loss of fixed-point implementation Turbo decoder is estimated, that is about 0.26dB for bearer F80T4.5XRE. Further optimisation will be continued.
- The test vectors have been captured for hardware development and other testing.
- Testing of Channel unit has been planned.

3.2.6.2 Plan for Final Design Review (FDR)

- Complete hardware RTL design.
- Implement the design in FPGA. Verify the design in the hardware.
- Debug the interfaces with Baseband processing and Embedded system.
- Complete system integration.

3.3 ASIC & DSP Design Considerations

3.3.1 General

3.3.1.1 Introduction

This ASIC design, Baseband and Channel Unit (BCU) chip, is designed specifically for the Inmarsat BGAN Satellite Modem. The BCU chip demodulates sampled IF signals, decodes the Turbo encoded FEC block, de-scrambles and forms data blocks for MPU processing in the Forward Link (Receive). For the Return Link (Transmit), it scrambles the block data; Turbo encodes and modulates it to form the passband signal for transmitting. This document describes the requirements, architecture and other design characteristics of the BCU chip.

3.3.1.2 Architecture of the Chip

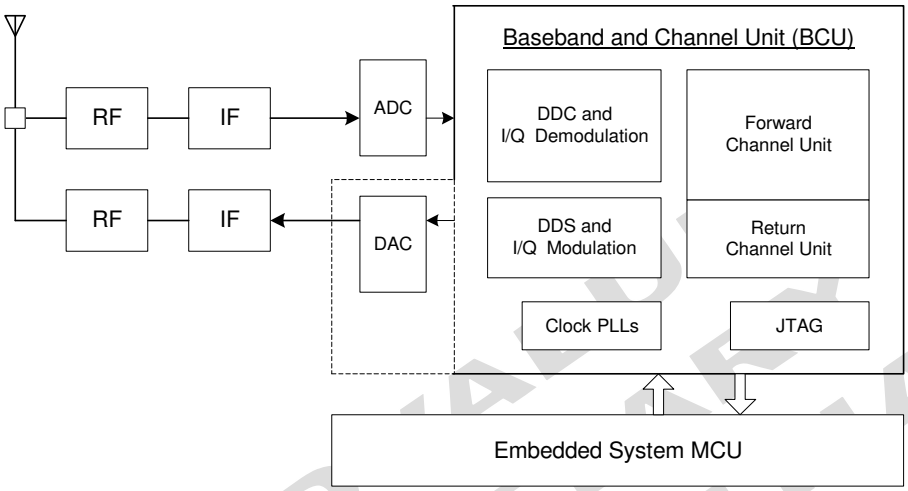


Figure 14: Function Blocks of BCU Chip

As shown in Figure 14, the BCU device consists of:

- DDC (Digital Down Converter) and I/Q Demodulation
- Forward/Return Link Channel Unit
- I/Q Modulation and DDS (Digital Direct Synthesizer)
- CLK PLL and Drive
- JTAG Test port
- DAC

3.3.1.3 Electrical Requirement

This chip will operate at 2.5V +/- 0.2V power supply voltage. The input clock is 40 MHz (TBC). The operating temperature range is between –40 °C and 85 °C.

3.3.1.4 Device Technology and Package type

This chip will be fabricated using the matured 0.35um CMOS technology. Since the Addvalue ASIC is a full digital design and its maximum clock speed is not greater than 100MHz. We do believe the 0.35um technology will offers the most cost effective solution.

A 208-pin PQFP package has been selected for this device. Please refer to Figure 17.

3.3.2 Design Methodology

3.3.2.1 Introduction

As FPGA implementation is a necessary prelude for prototyping the ASIC design, Addvalue will study the design architecture and determine the partitioning of the functional modules to be amalgamated for the FPGA design, which in turn shall be earmarked for ASIC implementation. Partitioning of the FPGAs shall be reviewed and determined at the Preliminary Design Review (PDR). The decision on the types and configuration of ASICs will be reviewed and determined at the Final Design Review (FDR). This will provide ample time for the performance simulation, characterization and evaluation at the FPGA level.

The ASIC development would be separated into 4 stages:

1. Algorithm simulation (floating point and fixed point)
2. Developing FPGA function modules, and Integrating into single FPGA for form fit prototype
3. ASIC development
4. Finalized ASIC

There is a large range of design options available in the ASIC industry for Addvalue to explore and exploit. Addvalue will closely study the various design and economic considerations and make its recommendation on the choice of ASIC options at the Final Design Review (FDR).

3.3.2.2 FPGA Design Flow and Tool

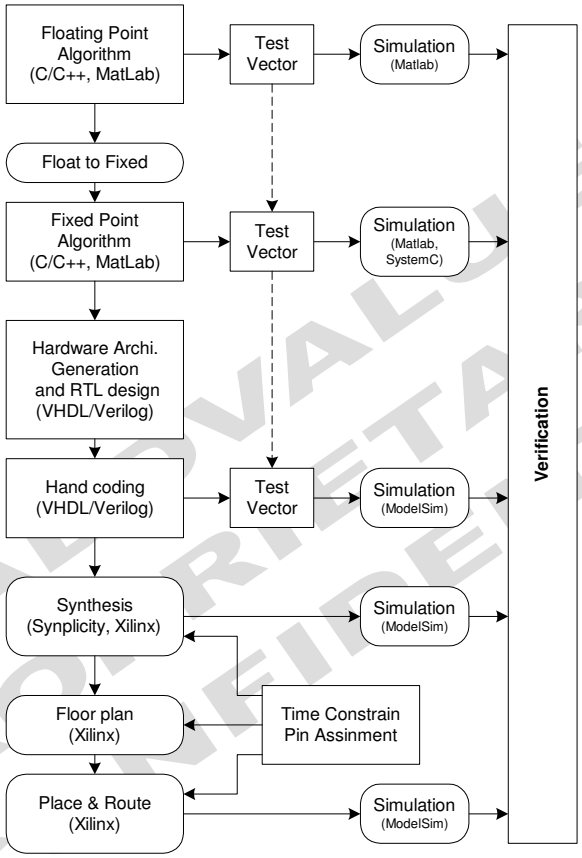


Figure 15: FPGA Design Flow

The Modem physical layer will be implemented in C/C++ and Matlab for both floating point and fixed-point algorithm. Meanwhile, the test vectors and test scenarios would be generated to verify the algorithms.

VHDL/Verilog codes will be developed from fixed-point algorithm. We will use Synopsys/Synplicity and Xilinx synthesis tools to compile the VHDL/Verilog code. ModelSim simulation tool is used for code simulation and post simulation.

For algorithm development and FPGA hardware implementation, Inmarsat BPLT Test Set should be used.

3.3.2.3 ASIC Design Flow and Tool

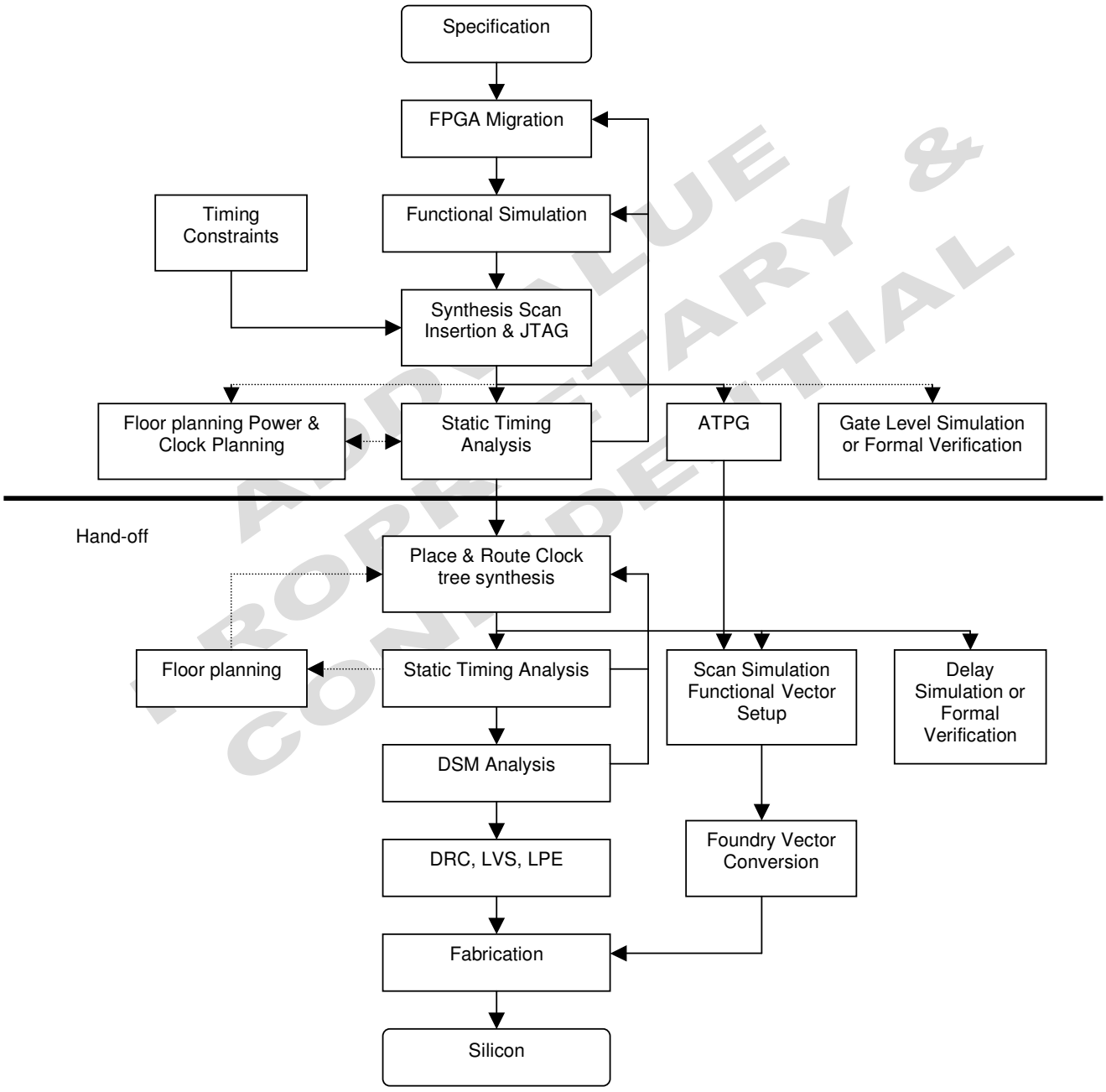


Figure 16: Standard Cell ASIC Design Flow

The ASIC will be developed by porting from the FPGA design, this is an effective way for successful ASIC design. Addvalue will collaborate with ASIC Fab, forges to develop the ASIC for BGAN modem physical layer during the commencement of FPGA migration stage as shown in Figure 16.

The ASIC design will be closely managed from the specification stage onwards to the last silicon stage in accordance with standard ASIC development procedures.

3.3.2.4 FPGA to ASIC migration issues

Addvalue is fully aware of the risk involved with the ASIC development. It is in Addvalue's own interest to ensure the migration of the FPGA to ASIC is done correctly to avoid any pit fall. Issues such as initial FPGA design to match with ASIC vendor's technologies/Library, RTL synthesis, test vectors, design verification and coverage, PCB layout and manufacturing of the final UT must be addressed.

Measures are in place to ensure the transition from FPGA to ASIC impact is minimized. Measures such as pin placements of the ASIC package to ensure easy PCB routing, ASIC functions are compatible to the FPGA to minimize impact of all other UT systems onboard, ease of testing (JTAG and test points/pins) and debug.

Some of these measures have already been implemented into the design during prototyping stage. While others will be implemented during testing and manufacturing.

3.3.3 Device Operation

3.3.3.1 Introduction

This chapter introduces the methods of activating and de-activating BCU chips and selecting a test mode for the device are described.

3.3.3.2 Reset generation

Inside the BCU device, there is power-up reset circuitry. This circuitry provides a clear pulse immediately upon chip power up. After 3 ms the clear pulse goes low and stays low as long as VDD stays high. The output pulse is OR'ed with the complement of the input reset pin, which would set the chip internal, reset signal to "0".

A more detailed implementation of reset generation is to be determined prior to the FDR.

3.3.3.3 Clock Generation

The input clock frequency is 16.8MHz (TBC). The PLL on chip will generate all required frequencies. The clock jitter and phase noise will be greatly concerned later in the design.

3.3.3.4 Estimation of Gate Count

According to preliminary design, the required number of gates and RAM size are listed in Table 3. It is for initial estimation of Die size and ASIC cost. For Turbo Decoder, external RAM is required for buffering.

Item		Gate Count	RAM (bit)
1	DDC, DDS	150,000	30,000
2	I/Q Demodulation, Modulation	120,000	45,000
3	Turbo Decoder, RX Ch Unit	148,000	383,000
4	Turbo Encoder, TX Ch Unit	10,000	169,000
	Total:	428,000	627,000

Table 3: ASIC Gate Count

3.3.3.5 Estimation of the Power Consumption

Total power should be less than 500mw.

3.3.4 Testability

3.3.4.1 Chip Level Testing

Testability at the chip level requires fault verification of all the digital logic. For digital fault coverage testing, the different signal processing sections of the chip are broken into sub-blocks with serial inputs and the use of the test port is provided in the chip requirements document. The following sections describe the types of chip-level tests that will be implemented.

3.3.4.2 Scan Chains

Partial scan chains will be implemented for blocks that are difficult to access through I/O pins such as state machine etc.

3.3.4.3 Built-in Self Test (BIST)

BIST modes will be supported for all memory blocks.

3.3.4.4 Internal Register Access

All internal registers will be accessible via the control/status interface block.

3.3.4.5 IDDQ

IDDQ testing will be performed for pass/fail. Limits will be developed for the IDDQ test.

3.3.4.6 JTAG

A JTAG test port will be provided for board-level scan testing.

3.3.4.6.1 JTAGID

A JTAG ID register will be integrated with JTAG registers for the chip identification.

3.3.4.6.2 JTAG Test Port

The chip will use a JTAG/IEEE 1149.1 standard five-wire test port (TDI, TDO, TCK, TMS, and TRST) for self-test and hardware emulation. An instruction register, a boundary register, a bypass register, and a device identification register will be implemented.

All of the chip's inputs and outputs will be incorporated in a JTAG scan path. The types of boundary-scan cells are input cell, 3-state output cell, bi-directional cell, 3-state control cell, and bi-directional cell.

3.3.5 Pin and Package Information

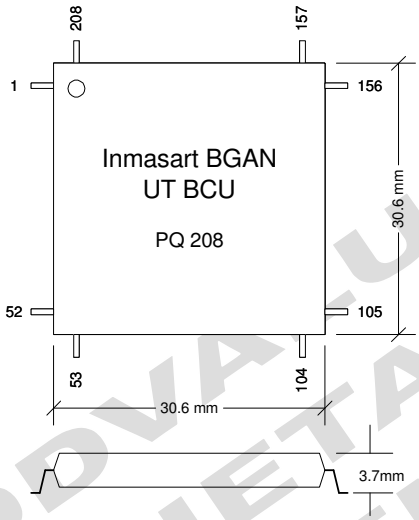


Figure 17: Package Diagram

4 EMBEDDED SYSTEM

The BGAN PUT (Pocket User Terminal) embedded controller features a unique dual core architecture that combines the command and control capabilities of a high performance microprocessor and low power capabilities of a DSP core managed by a RTOS (Real Time Operating System). Added with many integrated on chip peripheral circuits, this reduces external glue logic, power consumption and cuts down on design surface area and costs.

4.1 Targeted Microprocessor - Texas Instrument OMAP 1510

The TI OMAP1510 has a high performance ultra low power 200MHz TMS3320C55x digital signal processor (DSP) core for efficient execution of real time multimedia applications, as well as the TI –enhanced 175MHz ARM 925 processor to run the BGAN protocol stack, command and control functions and user interface applications.

It includes a memory management unit (MMU) for virtual to physical memory translation and task to task memory protection as well as 16KB instruction cache, an 8 KB data cache and a 17 word write buffer. A 1.5 MByte internal SRAM providing a large memory space for on chip data and code storage applications. A two level interrupt handler provides 32 interrupt lines including 13 internal and 19 external interrupts.

Figure 18 is a diagram showing the system architecture of the OMAP1510.

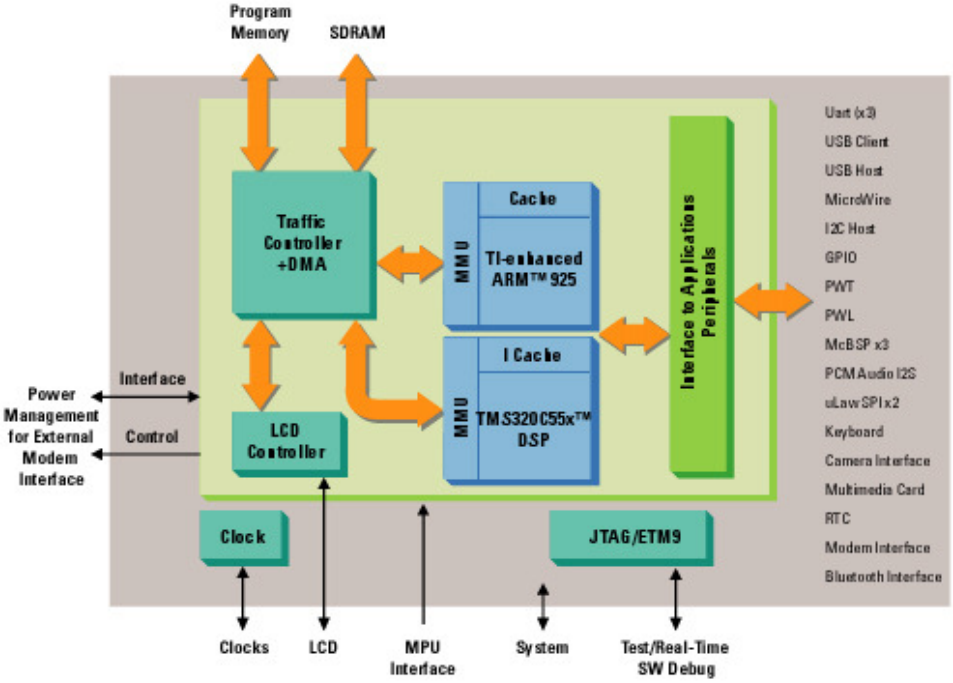


Figure 18: System Architecture of OMAP1510

The OMAP 1510 also includes a wide range of peripheral interfaces such as UART x3, USB Host and USB Client, Microwire, I2C Host, GPIO, PWT (Pulse Width Tone Generator), PWL (Pulse Width Light Modulator), PCM Audio I^2S, Serial Peripheral Interface x2, Keyboard, Camera Interface, SD/MMC (Secure Digital /MultiMedia Card Controller interface), RTC (Real Time Clock), Bluetooth Interface and LCD controller

Figure 19 below shows the peripheral interfaces available for the OMAP1510 and its assignment. Although some of the integrated peripheral circuits like the LCD controller, keyboard, camera interface and SD/MMC will not used in the PUT, these functions allow for future versions of the PUT which might include some human interface features.

BGAN PUT KEY INTERFACES

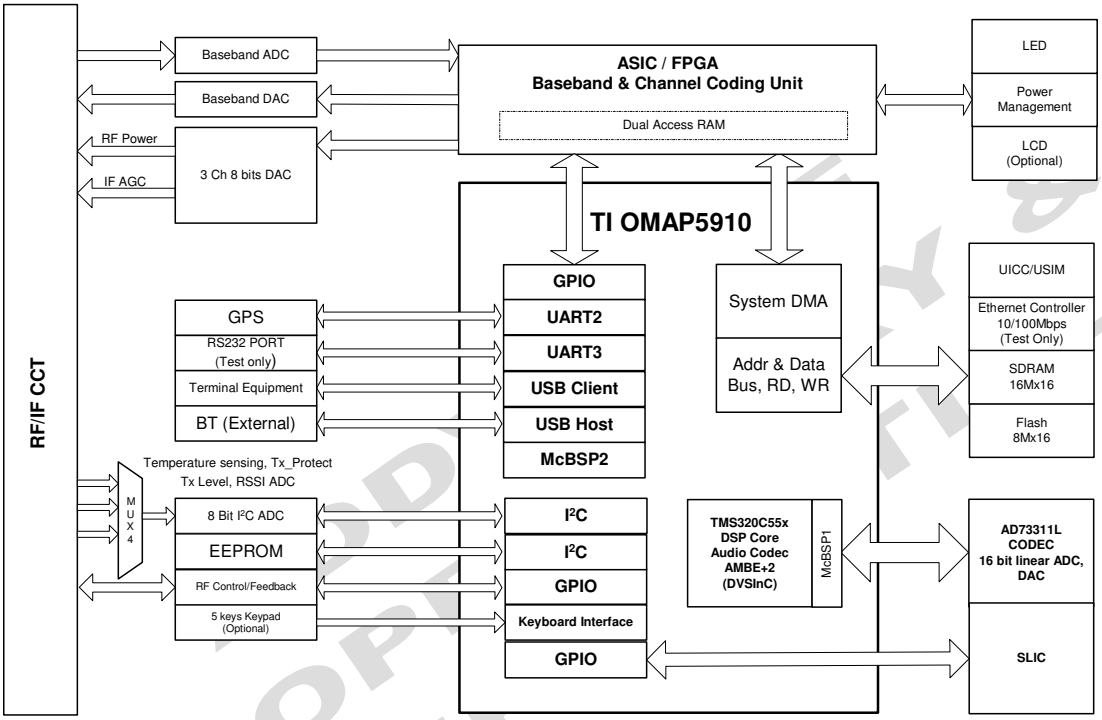


Figure 19: Peripheral interfaces of theOMAP1510

4.2 Real Time Operating System (OS)

VxWorks,® is selected as the RTOS running on top of the OMAP processor. VxWorks,® the run-time component of the Tornado® II embedded development platform, is the most widely adopted real-time operating system (RTOS) in the embedded industry. The VxWorks RTOS comprises the core capabilities of the wind® microkernel along with advanced networking support, powerful file system and I/O management, and C++ and other standard run-time support with more than 320 WindLinkT for Tornado partner companies.

With the selection of VxWorks as the RTOS, more efforts can then be placed on the supervisory control applications development on the PUT.

4.2.1 Standard Peripheral Driver Requirement

The OS and middleware vendor such as GateHouse will supply the following drivers for VxWorks RTOS identified in the system block diagram.

DMA, ARM-DSP Communication Driver, USB Host Controller/Driver, USB Client Controller/Driver, Ethernet IEEE 802.3 Controller/Driver, UART and I^2C Drivers.

4.3 Embedded Function

4.3.1 CPU functions

a) Power On Self Testing (POST)
b) Fault detection and fault recovery.
c) AT Command Handler to handle communication protocol between Terminal Equipment (TE) and Man Machine Interface (MMI).
d) Control and data interface to GPS Module – for retrieving geographical position and supporting antenna alignment to satellite.
e) Bluetooth Host Stack.
f) LAN interface – **For testing only - Ethernet Controller for interface to the BGAN Protocol Tester (BPT)
g) Power Management Control.
h) BGAN Protocol Stack – Manage Circuit Switch and Packet Switch Services between UT and BGAN network.
i) Interface to the UICC or USIM module.
j) Programs Phase Lock Loop (PLL) for channel tuning in both transmitter and receiver channels.
k) Transmitter power level control
l) Supplies parameters for configuring the digital front-end modulation and demodulation section.
m) Configures channel-processing module for channel and FEC decoding.
n) USB Host Controller
o) USB Client

Figure 20 represents the software/firmware functions that will be present in the BGAN PUT.

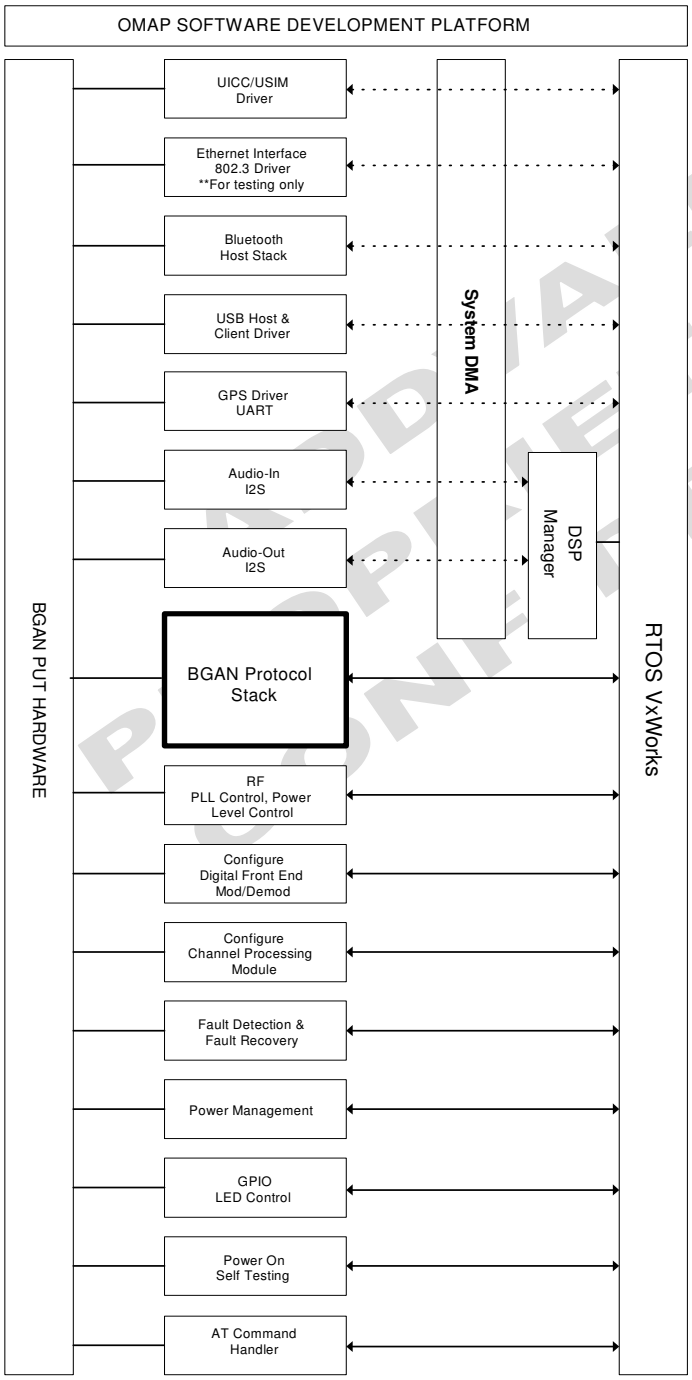


Figure 20: BGAN software components

4.3.2 DSP functions

The DSP will perform the Inmarsat Voice Codec - Using AMBE+2 Vocoder. It is estimated that it will meet the requirement of executing at 40 MIPs.

4.4 Memory Considerations for microprocessor

Table 4 provides an estimate for the FLASH and SRAM memory requirements of the microprocessor.

Function	FLASH Memory	Remarks
Real Time Operating System	800 Kbytes	VxWorks
BGAN Protocol Stack	<1000 Kbytes	(No trace/debug, compiled for ARM)
Interleaver Tables	1.2 Mbytes	
Application Routines	500 Kbytes	
BSP (Board Support Package)	700 Kbytes	
DSP (AMBE+2)	32Kword = 64kbytes	For DSP AMBE+2 Vocoder
Bluetooth Host Stack	300 Kbytes	
Debug Memory	2000 Kbytes	
Boot Code	30 Kbytes	
Total	**6.594 Mbytes**	**External Flash of approximately 8 Mbytes Required**

Table 4: Flash memory requirements

The on chip SRAM of the OMAP1510 is 1.5Mbits. It can be accessed dynamically between the ARM-925 and DSP C55x, and is more than sufficient to cover all the application requirements. The DSP C55x also has its own 80Kword of SRAM that is separate from the available 1.5Mbits. However, the on chip 1.5Mbit SRAM will be dedicated for DSP using an internal memory interface (IMIF).

Function	RAM Memory	Remarks
RTOS (VxWorks)	300KB	
BGAN Protocol Stack	896KBytes (assuming a maximum of 2 PDP context)	Memory usage of BPS with a single PDP context is 512 Kbytes. An additional 384 Kbytes for each subsequent PDP context.
Application Routines	64 KB + 64 KB	A backup of 64 Kbytes is provided
Channel Unit Tables	1.2MB	
Bluetooth Host Stack	30 KB	
DSP AMBE+2 Vocoder	6 KWord	DSP C55x has its own SRAM To reserve 40ms receive schedule jitter buffer and a 40 ms transmit schedule jitter buffer. A 20ms frame is 80 bits of data.
Boot Code	5 KB	
Trace & Debug	2000 KB	
Flash Image	6000 KB	
Total	**10.571 Mbytes**	**Total onboard memory: OMAP 1.5Mbits of on chip RAM and a 16Mx16 external SDRAM**

Table 5: SRAM memory requirements

4.5 GPS Receiver

GPS receiver is used in the PUT to compute the geographic location (latitude and longitude) before establishing a satellite link with right spot beam. A 12-channel GPS receiver (e.g. u-Blox TIM GPS module) is recommended for this purpose. Below are the specifications of GPS module, which is a possible candidate for final selection to be used in the PUT.

Frequency	:	1575.42MHz
Channels	:	12
Accuracy (Position)	:	25 meters (CEP without SA)
Acquisition Rate		
a) Reacquisition	:	0.1 sec., average
b) Hot Start	:	8 sec., average
c) Warm Start	:	38 sec., average
d) Cold Start	:	48 sec., average
Altitude	:	18,000 meters max
Velocity	:	515 meters/sec. max
Power		
a) Supply Voltage	:	+3.3VDC +/-10%
b) Supply Current	:	150mA (typical)
c) Backup Power		+2.5VDC to 3.6VDC

d) Backup Current 10uA (typical)

Electrical Interface	:	Full duplex serial communication, with baud rate selection
Protocol	:	NMEA-0183, version 2.2
Operating Temperature	:	-40 to +85C
Dimension	:	72mm x 42mm x 12mm (L x W x H)
Weight	:	23g
Antenna Connector	:	MCX, R/A MCX, R/A SMA type

A commercially available 12 channel GPS receiver was selected because it has better acquisition time against 8 channel GPS receivers. The interface between the GPS receiver and the microprocessor is a full duplex serial (UART) with selectable baud rate. The data communication protocol used is NMEA. Using this protocol, the GPS receiver can be set to (a) 2D only mode (b) 3D only mode or (c) Auto mode.

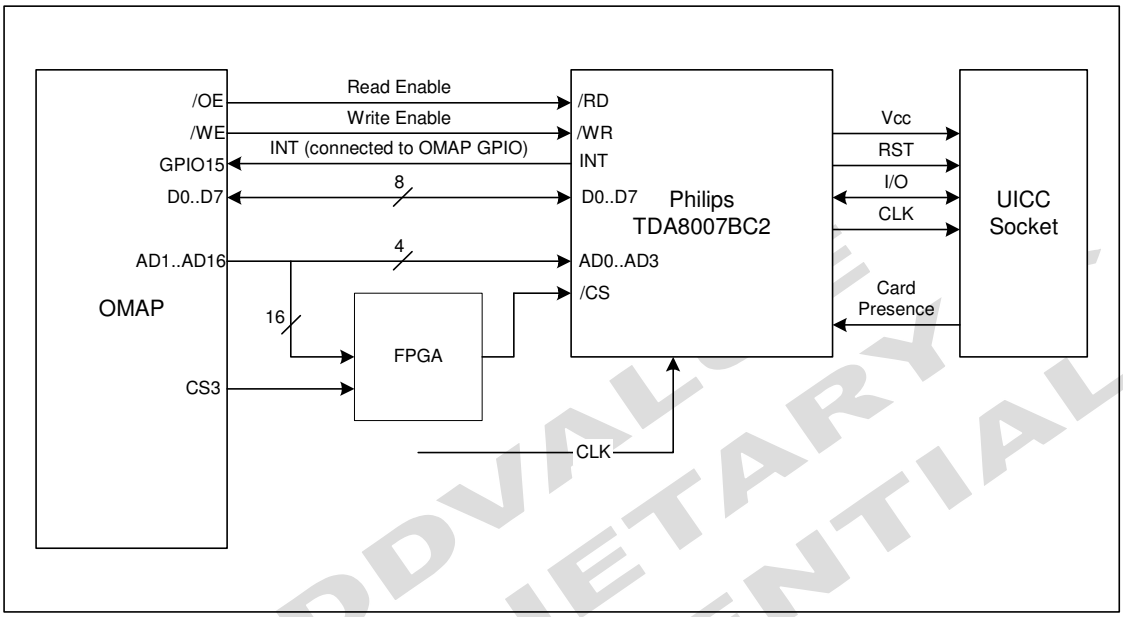
The position accuracy of the GPS receiver is 25 meters, which is well within the PUT requirement (+/- 100m). The GPS receiver can be back-up powered by the battery to avoid cold start. So, except for the first acquisition, subsequent acquisitions will be either warm start or hot start.

4.5.1 GPS Antenna

The GPS receiver to receive GPS signal will use an active antenna. This will be integrated with BGAN satellite antenna. Appropriate filters will be included in the GPS active antenna to suppress the interference from PUT transmission.

4.5.2 UICC/USIM Connection

UICC/USIM is connected to the microprocessor as shown in the figure below. There are four wires connected between the microprocessor and the UICC/USIM for communication and control between USIM and the microprocessor, namely USIM-Vcc (a controlled Vcc by microprocessor), USIM-DATA (bi-directional data line), USIM-RST (USIM reset line) and USIM-CLK (USIM clock input from the microprocessor).



The software implementation related to fetching of UICC/USIM data, de-ciphering and authentication are as per the relevant specifications

4.6 Subscriber Line Interface Circuit (SLIC) For External Telephone Equipment

Similar to a DSL integrated router that Addvalue has developed, The BGAN PUT is required to support telephony functions via external telephone equipment. The purpose of a SLIC module is to provide the necessary network interface functionality to an external telephone device. Commercially available solid-state solutions such as Intersil devices in the HC5517 family will be considered for the BGAN implementation.

The key functions of the SLIC are to provide ringing signal, on hook Maintenance Termination Unit (MTU) voltage to the tip and ring of a telephone line, DC feeding current for off hook operations, and transhybrid balance for 2-wire to 4-wire conversion. The BGAN PUT core processor can control the parameter setting and power on/off of the SLIC module.

4.7 PUT System Integration

The BGAN PUT consists of many sub-systems including software and hardware components. All these sub-systems are to be progressively integrated and tested before getting the whole PUT ready for system testing. This section describes the steps involved in the integration.

The PUT and the host software consists of the following subsystems:

a) Hardware
b) RTOS (VxWorks)
c) Device drivers (device)
d) Physical Layer software
e) BGAN protocol stack
f) Voice Codec
g) Bluetooth (hardware and software)
h) Device drivers (Host)
i) TAFs (Terminal Adaptation Function) for various call and data services
j) PUT Controller Module
k) MMI Interface and Driver

Following are the various steps involved in the integration of PUT.

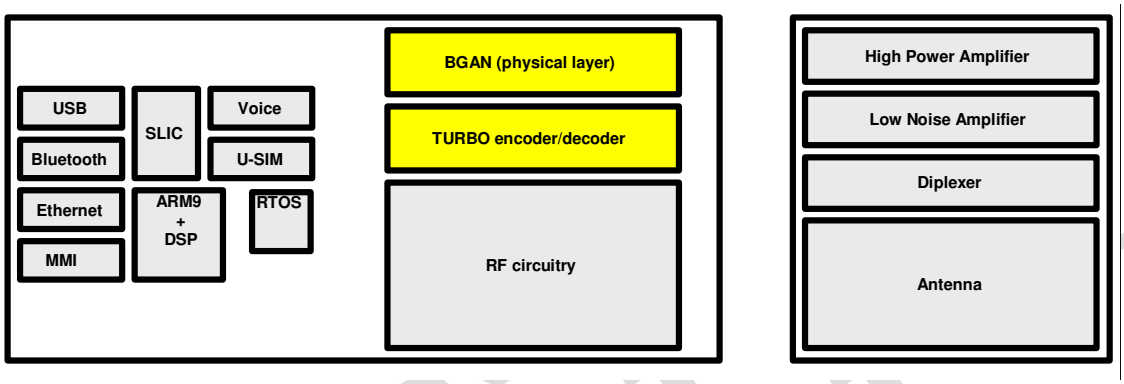
4.7.1 Integration of RTOS with the Hardware

The first step is integrating the RTOS (Vxworks, in this case), into the hardware. This requires developing a BSP (Board Support Package) tailored to meet the PUT hardware. This process will be done with the help of RTOS and the Microprocessor suppliers. Once the BSP is developed, the RTOS will be built for the target hardware using the Development System (Tornado II).

4.7.2 Integration of IAI-2 Physical Layer

After the above steps, IAI-2 physical layer code (FPGA code) is ported into the hardware through one of the physical ports (USB/Ethernet). The Physical layer is then tested for compliance using the BGAN Physical Layer Tester (BPLT), supplied by Inmarsat. This test will cover:

a) Testing of UT transmitter by signal analysis
b) Testing of UT receiver by signal and channel impairments



4.7.3 Integration of BGAN protocol stack

This is the integration of BGAN protocol stack (IAI-2 MAC + Adaptation Layer + UMTS) layer-2 and layer-3 supplied by GateHouse, on top of IAI-2 physical layer integrated earlier. Texas Instrument's OMAP 1510 dual core processor, which has an AMR9 processor and a TMS3320C55x DSP, is used as the engine in this hardware architecture. This processor was selected based on the fact that BGAN protocol stack was tested on a Motorola 68K processor by GateHouse. The processing power of the ARM9 core in OMAP 1510 is much higher than the Motorola 68K processor used by Gatehouse. Hence it can comfortably execute the BGAN protocol stack together with all other device drivers and MMI software.

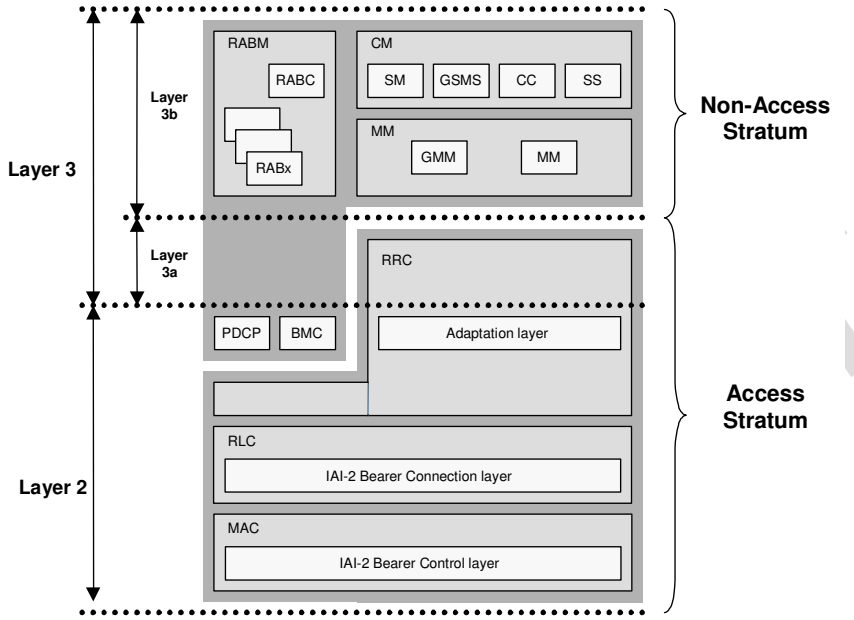
GateHouse shall first port their BPS implementation onto the Innovator board. To test the functionality of the BPS on Innovator board with BPT, a PHY emulator and other BPS interface emulators (UICC I/F, GPS I/F, Ciphering I/F etc), and an AT Command Handler shall also be ported. Basic test scripts shall be used to verify the functionality of BPS. Upon passing all the basic test scripts, this BPS and its test platform shall be delivered to Addvalue for familiarization and for further PUT software development.

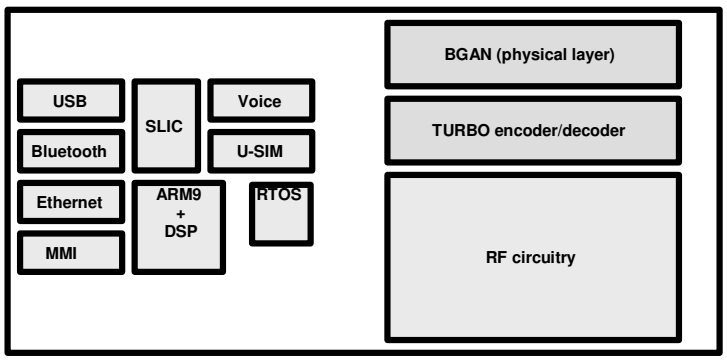
When Addvalue board is ready (with the BSP and VxWorks RTOS), GateHouse shall port the BPS to Addvalue board, together with all the emulator software. Basic test scripts shall be used to verify the functionality of BPS on Addvalue board. Upon passing all the

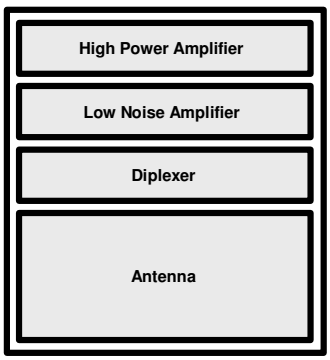
basic test scripts, this BPS and its test platform shall be delivered to Addvalue for porting the actual PHY and BPS interfaces implementation. GateHouse shall support Addvalue in the porting of these actual interfaces.

GateHouse shall continue to test the detailed functionality of the BPS on Addvalue board based on the AL, BCn, BCt and CS User Plane MTRs and test scripts, for the milestone of "PCTA-Pro Testing of BPS on Addvalue H/W".

During these integration, GateHouse will help to ensure that the integration is done smoothly. After integration, testing will be done with BGAN Protocol Tester (BLT) supplied by Inmarsat. The integration testing will be carried out using TTCN test scripts to validate the BGAN protocol stack (layer-2 and layer-3). The BLT operates over Ethernet bypassing the Physical layer to validate only the BGAN protocol stack (layer-2 and layer-3)







4.7.4 Integration of the voice CODEC

DVSI's AMBE+2™ Vocoder source code will be compiled using C55XX DSP compiler and then ported in to the DSP of OMAP1510. The C55xx DSP is source code compatible but not object code compatible to C54xx DSP. Although the cross-compiled code will not be an optimized code, the DSP C55xx has more than 40MIPS to comfortably run the Vocoder algorithm without any performance degradation.

The voice codec will be tested using VCTS (Vocoder test set for the Inmarsat Satellite System) to verify that it conforms to Inmarsat specification. Inmarsat will supply the tester during the integration test.

4.7.5 Integration with MMI and other device drivers

Man Machine Interface (MMI) and all other device drivers required will be integrated after this process and then tested for proper functionality using necessary test stubs and drivers.

4.7.6 Integration with Bluetooth module

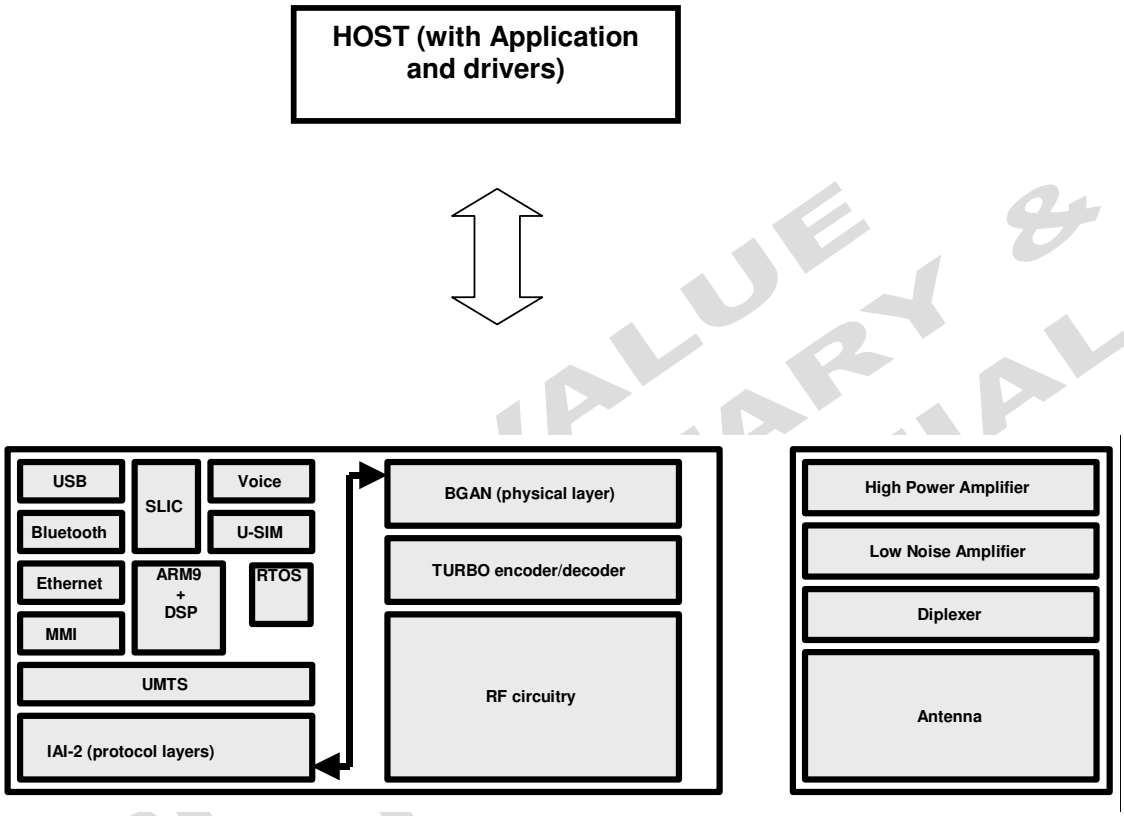
Bluetooth hardware and driver software will be loaded on to the PUT and then the system will be put into Bluetooth Test mode. At this mode, the Bluetooth pre-qualification will be done using Telelogic's Bluetooth Pre-Qaul tester. Final product (PUT) will be tested for BQB qualification at an accredited Bluetooth Test House (e.g. PSB Singapore).

4.7.7 Integration with TAF modules

TAFs for CS and PS services shall be developed based on 3GPP's TE – MT interface (the R Reference Point), and the NAS SAPs. At the same time, the main PUT controller (PUT Control) shall be developed to control various TAFs and to coordinates the access to BGAN services from various TEs.

4.7.8 Integration with Host software

The application software (User Interface) running on the host computer and the host end device drivers will then be loaded on to the host and then the integration test will be carried out with PUT. PUT will be put into local loop-back test mode to do this integration test.



5 BLUETOOTH

Bluetooth is a short-range (10 meters) access technology, with options to extend the range up to 100m, which operates in the 2.4GHz ISM band using frequency hopping spread spectrum technology. The key features of the technology are robustness, low complexity, low power and low cost. It has been designed specifically to operate in noisy frequency environments by incorporating fast acknowledge using shorter packets and frequency-hopping schemes in the radio link to make the link robust.

5.1 Bluetooth Specifications And Profiles

A Bluetooth enabled device has to comply with the Bluetooth Specifications v1.1. Applications that use the Bluetooth link have to use the profiles that have been made available. The Bluetooth Specifications lists the protocols for the core layers of the Bluetooth device. The lower core layers are:

1) Radio
2) Baseband
3) LMP (Link Manager Protocol)
4) HCI (Host Controller Interface)

The higher core layers are:

1) L2CAP (Logical and Link Control and Adaptation Protocol)
2) RFCOMM
3) SDP (Service Discovery Protocol)

The Core layers of Bluetooth are used by all the applications via the profiles. These core layers form the common data and physical link to the external devices. The profiles form the services that the Bluetooth device is able to provide to external devices or for use by applications within the device.

The profiles have been developed to describe how implementations of user models are to be accomplished. The user models describe a number of user scenarios where Bluetooth performs the radio transmission. The profile defines options in each protocol that is mandatory for use with the profile. It also defines the parameter ranges for each protocol. The profile concept is aimed at reducing the risk of interoperability problems between

different manufacturers' products. A Bluetooth profile may have dependencies on other profiles as well if it re-uses parts of that profile either implicitly or explicitly. The profiles of interest in this project are listed below:

1) GAP (Generic Access Profile).
2) SDAP (Service Discovery Application Profile)
3) SPP (Serial Port Profile).
4) DUN (Dial-Up Networking) Profile
5) CTP (Cordless Telephony Profile)

5.2 Bluetooth Protocol Architecture

The

Figure 21 pictorial view of the Bluetooth protocol architecture shows how different profiles interact with one another as well as with the core layers.

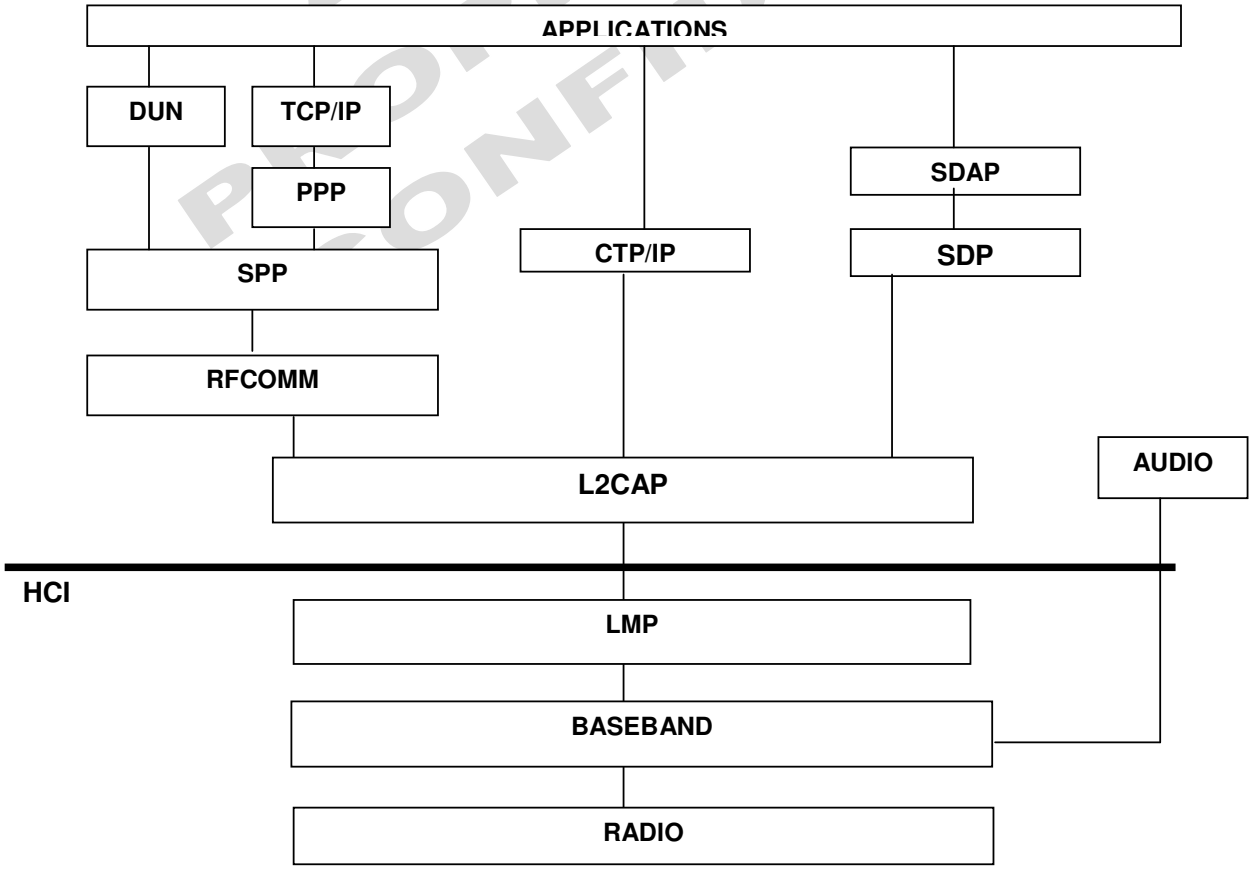


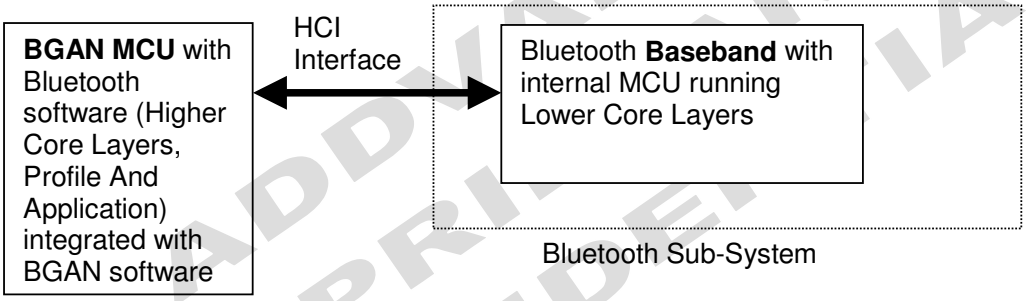
Figure 21: Bluetooth Specification Protocol Stack

5.3 Bluetooth Software Development

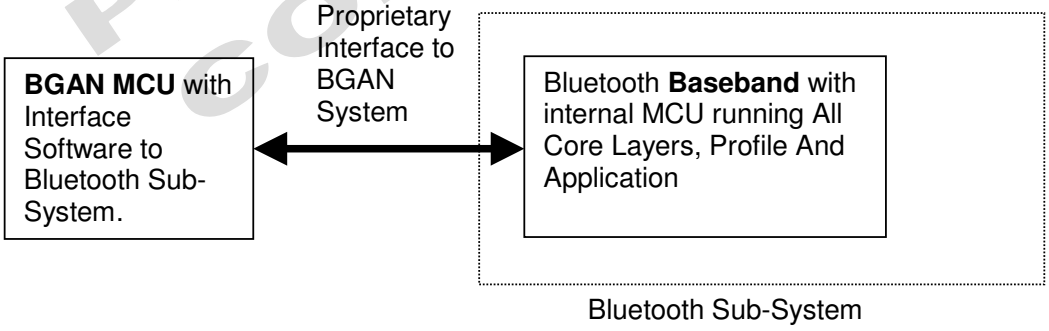
In general, the Bluetooth IC manufacturers develop the lower layer core stack for their chipsets. Hence, lower layer protocols do not need further development. The interface to the lower layer protocol will be done through the HCI layer.

There exists two ways of implementing the Bluetooth subsystem:

1) Running the higher layer protocol on a separate MCU



2) Running the higher layer protocol within the same MCU as the lower layer protocols.



The first method removes the necessity of integration of the higher layer stack from the lower layers The higher layer can be developed independently from the lower layers and the interface to the lower layers will be through the standard HCI interface. The drawback is however the need to integrate the higher layer protocol and profile layers to the BGAN software. The Bluetooth software will also require some processing time for its own functions. The Bluetooth higher layers will also have to share RAM and ROM with the BGAN software as well.

The second method calls for the integration of the higher layer stack with the lower layer. This uses the MCU that is already present in the Bluetooth IC. The resources of RAM/ROM may come from only the IC if there is enough resource to support both the higher and lower layers of the protocol.

To support BGAN PUT applications, the higher layer BGAN core stack of L2CAP/RFCOMM/SDP will be employed. This protocol stack has been fully developed. In addition, application profiles required in the BGAN PUT include SPP, GAP, SDAP and DUN. SPP, GAP and SDP have already been developed. DUN is currently under development.

5.4 Bluetooth Access Option

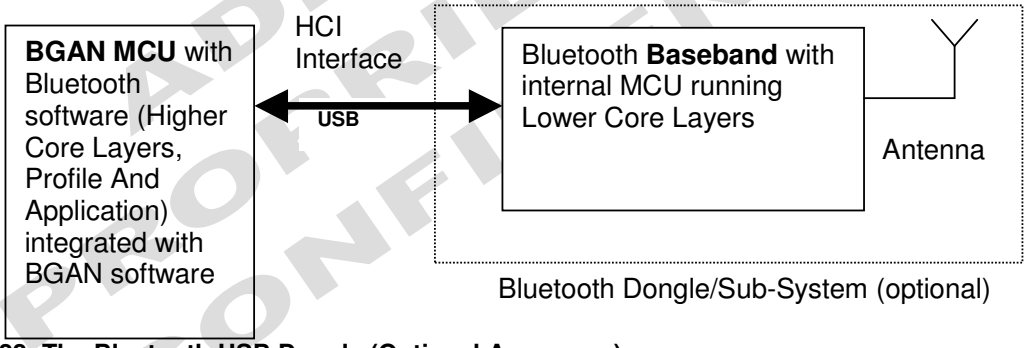


Figure 22: The Bluetooth USB Dongle (Optional Accessory)

The BGAN PUT shall be made 'Bluetooth Ready' which means that the Bluetooth Host protocol stack including all the necessary application profiles will be embedded into the PUT. A user should plug in a compatible external USB dongle, if he/she wants to have Bluetooth access to the PUT. The Figure 22 above illustrates the external Bluetooth dongle, which can be connected via the USB host port to the PUT. This will be an optional accessory to the BGAN PUT to make it "Bluetooth Enabled".

5.5 Bluetooth Hardware Development

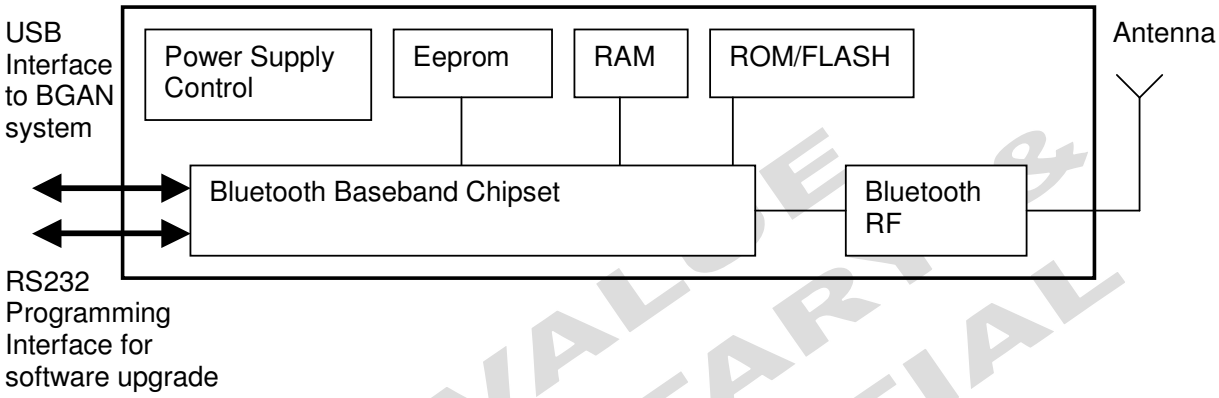


Figure 23: The Bluetooth Hardware System

The Bluetooth module will consist primarily of the Bluetooth Baseband Chipset and the Bluetooth RF chipset. External components will largely be the RAM, ROM and EEPROM. RAM and ROM will be required if the selected Bluetooth Baseband is unable to support the code size or ram requirements of the protocol stack. The Flash is recommended for the code as this will allow software upgrades to be easily done. The EEPROM will be of a small capacity for maintaining Bluetooth device information and registrations of other Bluetooth devices. This may not be required if the Flash is used instead of the ROM. The Power Supply Control is used to regulate power for the Bluetooth module including a power down mode.

The chipsets that are being considered for implementation are tentatively CSR, Philips, and Silicon Wave. Addvalue has already worked with these vendors and is also the Design House for these vendors. Current completed designs use Philips and Conexant chipset while Silicon Wave and CSR solutions are under development.

6 POWER MANAGEMENT

Since the BGAN Pocket UT is required to be portable, it is well understood that it has to be battery powered. When powered from the internal battery, the PUT can operate in the ambient temperature range of 5°C ~ +40°C, while powered from an external power supply, the PUT can operate in the ambient temperature range of 0°C ~ +40°C. This chapter describes the system power supply block diagram, the choice of batteries, charging circuit design, the DC/DC converters, the external power adapter as well as the external automotive power adapter.

6.1 Block Diagram:

Figure 24 shows the System power supply block diagram.

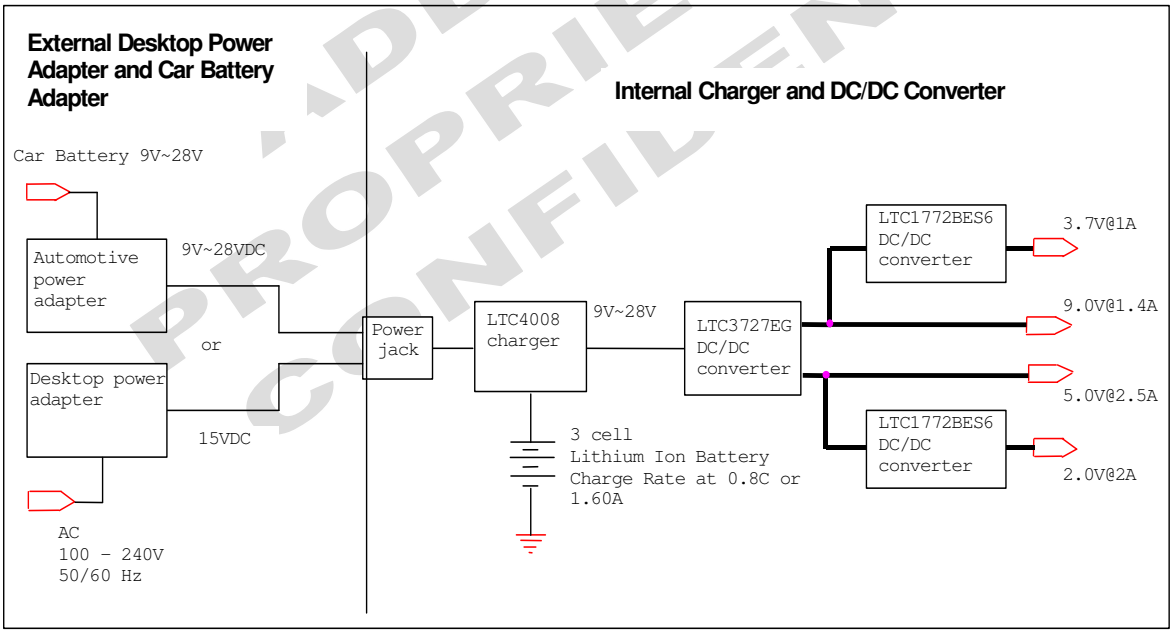


Figure 24: System Power Supply Block Diagram

Using only a single power jack, the BGAN PUT can power-up by using either the external power adapter from an AC mains power source or the external automotive power adapter from a car battery source.

From an AC mains power source, the external power adapter output is 15Vdc. From a car battery source, the output voltage is slightly lower than the input voltage because of a protection circuit that protects the BGAN PUT from voltage surges during car ignition.

Regardless of the power source, the charger will start to charge the battery when a power source is detected. When an external power source is available, the system is powered by this external source. However, when the charger module detects that, the external source is unavailable or removed, the battery is switched in to supply the system power.

The 9V~28V output of the external power adapters will pass through the charger as the system output voltage, and will become the input voltage of the LTC3727, a dual-output DC/DC converter. The outputs of the LTC3727 are 9V/1.4A and 5V/2.5A. The 9V/1.4A will also become an input to another DC/DC converter, which is an LTC1772, which will have an output of 3.7/1A. The 5V/2.5A will also become an input to another LTC1772 DC/DC converter, which will have an output of 2V/2A.

6.2 Battery Pack

Currently, Lithium-Ion battery is the most commonly used type of battery in high-end portable and handheld devices. Due to its high volume production, the cylindrical type “18 x 65” battery is relatively cheap compared to the other battery types such as prismatic cells. After evaluating several makes of batteries we selected a battery pack using GP1865L200 cells from GP batteries. The battery pack consists of three cylindrical battery cells connected in series and a protection circuit. The protection circuit has the following features:

a) **Over Charge Protection:** The over charge limit per cell is 4.35V ± 0.05V.When battery cells, reach this limit, protection circuit will immediately act causing termination of charge to battery pack.

b) **Over Discharge Protection:** The over discharge release voltage per cell is 3.00V ± 0.15V. When battery cells reach this limit, protection circuit will act immediately causing battery pack to terminate discharge.

c) **Over Current Protection:** The over discharge current limit is 6.5 ± 1.0A. When battery reaches this limit, protection circuit will act immediately causing battery pack to terminate discharge.

d) **Short Circuit Protection:** In the event of a short-circuit, an LR4-450 polyswitch will trip to a high resistance state once a fault current has been applied to the device.

6.3 Battery Charger

The battery pack can be charged using an external power source. It could be an AC wall adapter or an external automotive adapter.

The battery charger design is based on the LTC4008 Li-Ion battery charger controller from Linear Technologies. The LTC4008 is a constant-current/constant-voltage charger controller. Charging current is programmable with a sense resistor and programming resistor to ±4% typical accuracy. In our design, the charging current is programmed at 1.60A or 0.8C (80% of charge rate). An external sense resistor programs the supply current for the external adapter. This will monitor the total current drawn from the input source, and automatically reduces battery charging current, preventing overload of the input supply. Battery temperature is monitored by an external thermistor to prevent charging outside the acceptable temperature range.

A severely depleted battery is charged at 10% of maximum charging current as a form of battery conditioning. The charging current will be switched to a high rate after the battery reached a “safe” voltage (2% below the norminal voltage). Charging time for a severely depleted battery is approximately 150 minutes or less than 3 hours.

A new PUT will not be necessarily charged at 10% of the maximum charge rate. The charger will charge the battery at 10% of the charge rate only when it detects that the battery voltage falls below the minimum voltage required to safely charge the battery to

full rate. As long as the battery stays below the "safe" voltage, the charger will remain charging the battery at 10% rate until it reaches the "safe" voltage to do so.

For an ex-factory PUT, it is recommended to condition its battery pack by charging it for a recommended period of time (usually > than 3 hours) before its first use.

6.4 System Power Supply

A fully charged battery pack should have approximately 12.55V ±0.15V. As the system needs power supply at various voltages, the battery voltage will be converted using DC/DC converters. There are three DC/DC converters used in the system. A single LTC3727EG that supplies 9V/1.4A and 5V/2.5A and two LTC1772 that supplies 3.7V/1A and 2V/2A respectively.

The LTC3727EG is a high efficiency, 2-phase synchronous step-down switching regulator. It brings considerable benefits of 2-phase operation to portable applications. With 2-phase operation, the two channels of the dual switching regulator are operated 180 degrees out of phase. This effectively interleaves the current pulses drawn by switches, greatly reducing the overlap time where they add together. This will result into a significant reduction of total RMS input current, which in turn reduces shielding requirements for EMI and improves real world operating efficiency.

The LTC1772 is a constant frequency current mode step-down DC/DC controller providing excellent AC and DC load and line regulation. It provides ±2.5% output voltage accuracy and consumes only 270uA of quiescent current. The LT1772 is also configured for Burst Mode operation, which enhances efficiency at low output current. To further maximize the life of a battery source, the external P-channel MOSFET is turned on continuously in dropout (100%dutycycle). In shutdown, the device draws a mere 8uA.

Figure 25 shows the estimated current consumption by major sub-systems in the BGAN PUT.

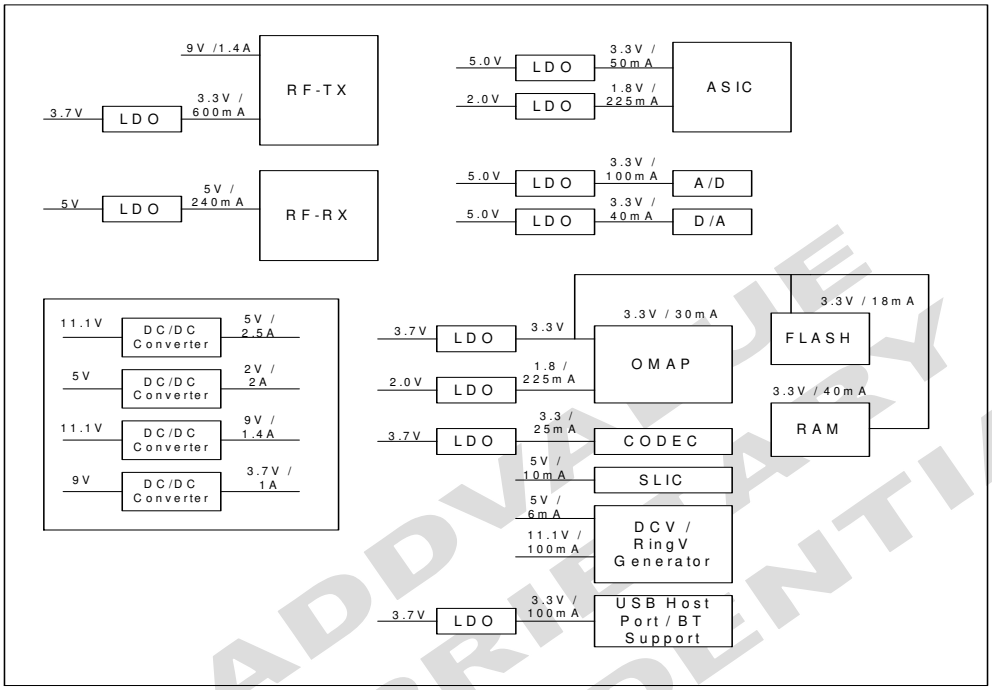


Figure 25: BGAN PUT Power Distribution

6.5 External Desktop Power Adapter

The desktop power adapter is a DSA-0421S-15 switching power supply manufactured by Dee Van Enterprises Co., Ltd. This unit is used to power-up the PUT from the AC mains. The adapter has the following protection features:

a) **Primary (Input) Protection:** An internal fuse on the AC input line is provided.

b) **Secondary (Output) Protection:**

i. **Over Current Protection*:*** 6.0A maximum with auto recovery function.

ii. **Over Voltage Protection:** If an overvoltage fault occurs on the adapter output, the adapter will shutdown before the output exceeds 18.9V.

iii. **Short Circuit Protection:** The adapter will protect itself, and shutdown, if a short circuit is placed between the DC output and the Ground. This condition will cause no damage to the adapter.

Table 6 is the AC wall power supply adapter specification.

	Parameter	Specification
1	Input voltage	90VAC ~ 264VAC
2	Input Frequency	47Hz ~ 63Hz
3	Input Current	1.2A max
4	Inrush current	No damage shall occur and the input fuse shall not blow up.
5	Power efficiency	Will not be less than 80% at nominal input voltage and full load condition
6	Output Voltage	+15V
7	Maximum Load Current	2.8A
8	Minimum Load Current	0.0A
9	Maximum Output Power	42W
10	Total Output Regulation	±5%
11	Operating Temperature	0°C ~ +40°C
12	Dimension	101 (L) x 56 (W) x 33.5 (H) mm
13	Weight	270 gms

Table 6: External Desktop Power Adapter Specification

6.6 Power sequencing

In order to protect the complex and high power RF circuits onboard of the PUT unit, a power-sequencing scheme will be employed during the power up stage.

Power sequencing is done by the ASIC/FPGA. It will ensure a fail-safe power on reset for the system and protect high power RF circuits from damage. The added benefit will be lower power usage and longer battery life.

6.7 External Automotive Power Adapter (Optional Accessory)

The external automotive power adapter is a device to be used by the BGAN PUT to power up from a car battery source. The external automotive power adapter also features a protection circuit to protect the PUT against voltage surges during car ignition.

7 MECHANICAL

7.1 Background

Based on User Terminal Product Requirements Specification, the Pocket-size User Terminal (PUT) shall be a single physical unit complete with a built-in BGAN antenna. This unit shall also comply with IP44 standard protected against splashing water and solid foreign objects of 1.0mm diameter and greater, as the operating environment is expected to be outdoor or semi-outdoor. Size and weight constraint need to be considered for better portability. The following summarizes some of the studies and findings.

7.2 ME Conceptual Design

1. The BGAN PUT size is estimated to be around 235mm x 150mm x 35mm (ME-5) or 252mm x 160mm x 44mm (ME-12). The modem should be functional both indoor and outdoor.
2. The modem base unit has adjustable feet that provide positioning angle to be at 0° to 85° maximum from horizontal position in order to received signal from satellite at certain geographic location. Refer to Appendix 2.
3. Light color is applied to the case surface to reduce sun light absorption and resultant heating.
4. The Top and Bottom Housing are molding with PC material that can withstand rugged outdoor usage. O-ring gasket will be added on the enclosure in order to meet IP44 standard, no cooling fan can be added.
5. Heat sink radiation fin is added on the top surface for more efficient heat dissipation through natural convection.
6. The product total weight is expected to be around 955g. The weight breakdown is as following:
    a) Top Housing : 100g
    b) Bottom Housing : 130g
    c) Heat Sink : 130g
    d) Antenna PCB and GPS : 100g
    e) RF module : 175g
    f) Base-band PCB : 150g
    g) Battery pack : 150g
    h) Diplexer : 20g

It is slightly lighter than previous estimation, as we have changed the Bottom Housing from die casting to plastic housing. ME design is done by using pro-e 3D solid modeling, that is capable to check geometric and interference in order to minimize tooling tweak.

7. ME design for ESD proof concept that complies to CE or UL standard.
8. Refer to Appendix 1 for the ME conceptual design.
9. Number of modular socket available:
    a) Power jack – one piece
    b) RJ11 – one piece
    c) USB client – one piece
    d) USB host – one piece (for optional external BT dongle)
    e) RJ45 – one piece (for testing stage only, and will be removed on the final product)
10. Battery weight to be located at the bottom side, when PUT is swiveled to an angle of 85°, the centre of gravity will be towards the battery side, hence it won't be topple easily.

7.3 ID Conceptual Design

1. The desired BGAN PUT shape and size should be handy and easy to be carried around.
2. The PUT should be working in indoor or outdoor environment.
3. The ID should be ergonomics, sleek and rugged to be used indoor and outdoor.
4. A list of proposed ID is available from the UT Hardware Design Document. Appendix 2 shows the ID with an adjustable stand to position itself at the optimum angle with respect to the satellite position. Two dummy mockup had been fabricated for marketing review.
5. LED assignment as following:(quantity and assignment to be confirmed by Inmarsat)
    a. Power
    b. Low Batt
    c. Bluetooth Active
    d. GPS status
6. A compass will be mounted on the housing for direction indication.

8 VOICE CODEC

Voice codec (Vocoder) forms part of BGAN UT design. This section provides an overview on the design and implementation of BGAN UT Vocoder. It also covers the design of an echo canceller that complies with the ITU-T G.168 document. The TMS320C55x™ DSP will perform the BGAN Voice Codec - AMBE+2™ Vocoder and Echo Canceller. Other functional blocks of Voice Codec includes the RJ11 connector, SLIC hybrid circuit, ADC/DAC codec as shown in Figure 26.

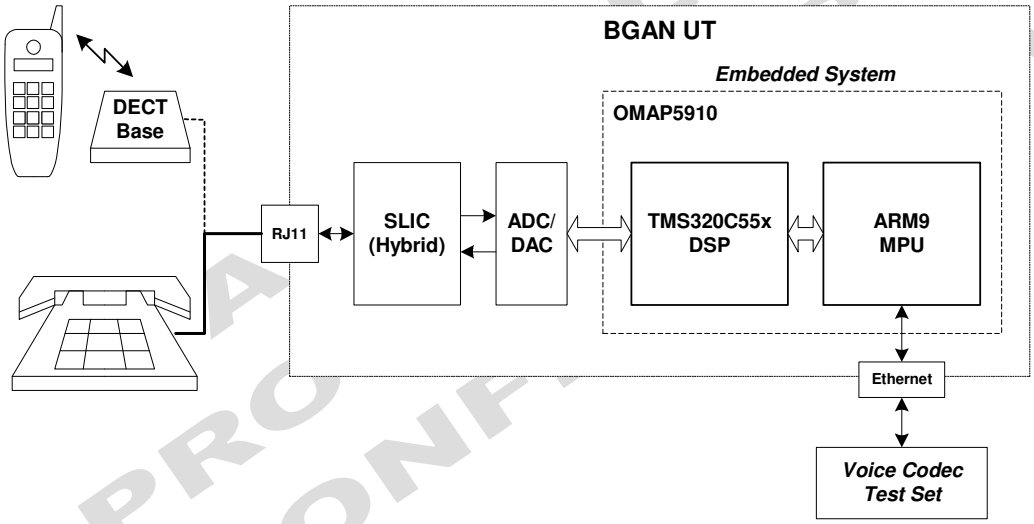


Figure 26: Voice Codec Unit

At the initial stage, DVSI's AMBE+2™ Vocoder will be implemented on TMS320VC5510 DSP Starter Kit (DSK) module. The Spectrum Digital TMS320VC5510 DSK is used as the development platform. The Vocoder will be tested using DVSI's Voice Codec Test Set (VCTS) provided by Inmarsat.

Eventually, AMBE+2™ Vocoder and Echo Canceller will be implemented and run on the DSP core Texas Instruments (TI) TMS320C5510™ within the OMAP5910. AD73311L from Analog Devices was chosen for the CODEC design. The OMAP Innovator platform could be used to test out the performance of the C55x DSP at the final integration testing with BGAN Protocol Stack (BPS).

8.1 DESIGN OF AMBE+2™ VOICE CODEC

This chapter section describes the Digital Voice System, Inc.'s (DVSI) 4.0 kbps AMBE+2™ Vocoder. DVSI's AMBE+2™ Vocoder is based on a generalized version of the MBE speech model used in DVSI's previous IMBE™ and AMBE® speech coders. Digital speech is input to the encoder in 10ms segments. Each segment or subframe of speech is analyzed to estimate a set of generalized MBE model parameters including a fundamental frequency, a set of voicing parameters and a set of spectral magnitudes. The MBE model parameters for two consecutive subframes are grouped together to form a 20ms frame, and the model parameters for both subframes in the frame are then jointly quantized. A single parity bit is added to the quantized bits and resulting 80 bits are output as the encoded bits for each 20ms frame of speech.

At the receiving end, the decoder a receiver receives a frame of 80 encoded bits and decodes the MBE model parameters for both subframes. The parity bit is checked and if a parity error is detected then a frame repeat is applied to the frame to reduce the perceived effect of any bit errors. The decoded MBE model parameters for each subframe are used to synthesize a 10ms segment of speech. This is performed for both subframes in the frame to produce the decoder speech output for the frame. A block diagram of DVSI's AMBE+2™ Vocoder is shown in Figure 27.

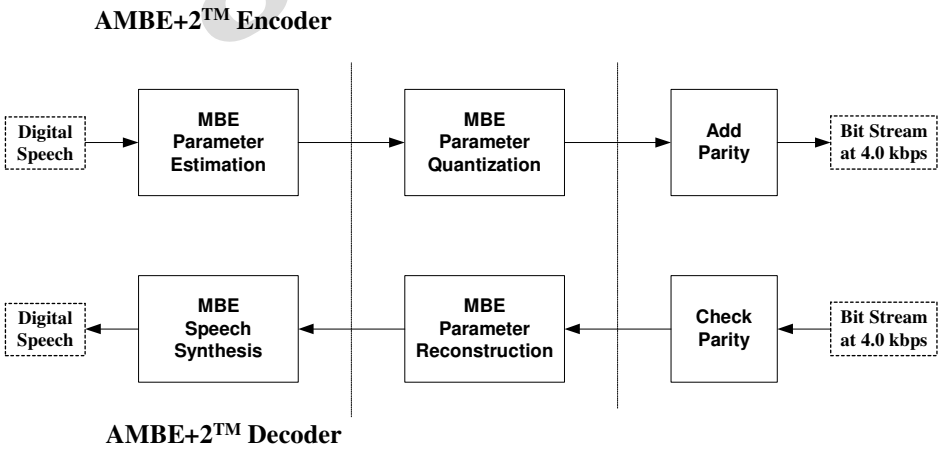


Figure 27: DVSI AMBE+2™ Vocoder Block Diagram

DVSI's AMBE+2™ Vocoder also includes a number of advanced features. These include such as noise suppression, adaptive voice activity detection (VAD) and comfort noise insertion (CNI), tone detection, transmission and regeneration of DTMF, North American call progress and single tones, and channel error mitigation.

8.2 ECHO CANCELLER

Echo Canceller (EC) system, which is part of the BGAN Voice Codec, is implemented in Texas Instruments TMS320C55x DSP together with DVSI's AMBE+2™ Vocoder. We have designed an FIR Echo Canceller based on a similar implementation found in the document of Texas Instruments' Digital Signal Processing Solutions: Digital Voice Echo Canceller with TMS32020 [SPRA129]. We have derived and ran simulation based on some algorithms in the document.

In the design, EC consists of 3 major signal-processing functions; they are an adaptive filter, near-end speech detection and residual echo suppressor. The signal processing flow diagram for a single-channel digital voice echo canceller is shown in Figure 28.

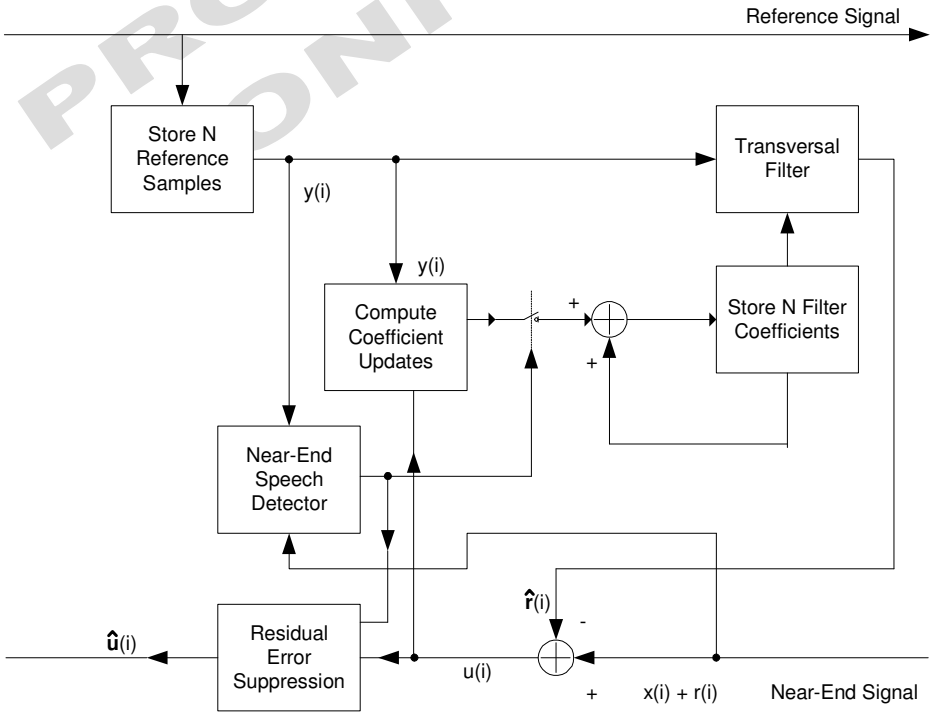


Figure 28: Signal Processing for a Digital Voice Echo Canceller

8.2.1 Performance Requirements

Echo cancellers have the following fundamental requirements:

- Rapid convergence when speech is incident in a new connection
- Low-return echo level during single-talking (i.e., echo-return loss enhancement)
- Slow divergence when there is no signal
- Rapid return of the echo level to residual if the echo path is interrupted
- Little divergence during double-talking

The ITU-T G.165/G.68 recommendation specifies echo canceller performance requirements with band-limited white noise (300 – 3400 Hz) test signals at the near-end and far-end input signal ports. The test has incorporated an adaptive echo canceller in all speech modes in order to effectively eliminate local acoustic and electronic echo (the latter mainly from the 2-wire to 4-wire converter (hybrid) when routing via the 2-wire port).

Digital voice echo canceller products are typically designed to accommodate circuits with tail delays of 16 ms or more and circuits with echo-return loss levels greater than 3 dB to 6 dB. Typical digital voice echo canceller product specifications can be found in ITU-T G.165/G.168 recommendation documents.

Furthermore, in EC design, the coefficient update process dominates the computational requirement and efficiency of DSP realizations. The DSP efficiency and speed, in turn, determines the maximum number of echo canceller taps that can be achieved with the processor.

8.3 Processing Requirements (MIPS)

The total peak MIPS requirements for this vocoder are estimated as follows:

- AMBE+2™ Encoder 29.0 MIPS
- AMBE+2™ Decoder 15.6 MIPS
- Echo Canceller 15.0 MIPS
- Total 59.6 MIPS

When designing the Vocoder, the encoder processing load is significantly higher in the second subframe of the each frame than in the first subframe, while the decoder

processing load is significantly higher in the first subframe of each frame than in the last subframe. This imbalance is the result of the channel processing done over the entire frame, which must be performed in the last encoder subframe and first decoder subframe. The echo canceller MIPS requirement is estimated to be 10 MIPS for each channel with 32 ms echo path, 15 MIPS for 64 ms echo path.

8.4 AD/DA Converter

Analog Devices AD73311L is a 16-bit ADC channel and a 16-bit linear DAC channel. Each channel provides 70 dB SNR over a voiceband signal bandwidth. The gains of ADC and DAC channels are programmable over 38 dB and 21 dB ranges respectively. A serial port (SPORT) allows easy interfacing of single or cascaded devices to industry standard DSP engines like TI C55xx DSP.

The CODEC operates at an 8 ksamples/sec rate (sampling period of 125 microseconcds) at both the digital input and digital output. The TI DSP on OMAP is responsible for initializing and controlling this CODEC.

8.4.1 Digital Interfacing

AD73311L is interfaced to the TMS320VC5510™ DSP via McBSP1. The software developed reads 160 samples (20 ms) continuously from AD73311L. Figure 29 shows the connection between the C55xx DSP and the AD73311L.

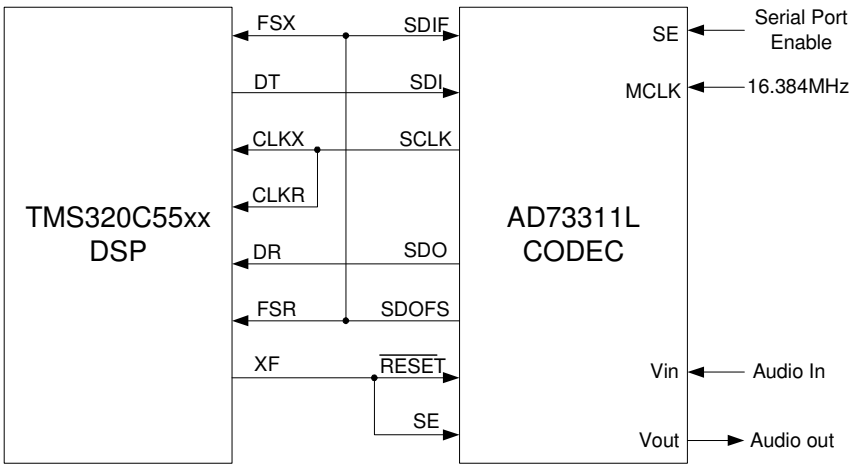


Figure 29: Connections between C55xx and AD73311L

8.5 SLIC circuit

A SLIC performs a 2-wire to 4-wire conversion of the analog signal. The 2-wire circuit is the balanced line going to the subscriber loop (the TIP/RING), while the 4-wire circuit is the audio signal going to and from the AD73311L voice codec.

The Intersil ISL5585DIM SLIC circuit was selected for this design. It belongs to a 3.3V ringing SLIC Family for Voice over Broadband (VoB) as shown in Figure 30. It is used to support POTS in short and medium loop length, wireless and wireline voice over broadband applications. ISL5585DIM chip is also capable of operating with 100V ringing battery supply, which translates directly to the amount of ringing voltage supplied to subscriber. With the high operating voltage, subscriber loop lengths can be extended to 500Ω (i.e. 5,000 feet) and beyond.

At absolute maximum ratings, TA = 250, the maximum supply voltages, Vcc, is -0.5V to +7V and VCC to VBH is 110V. The maximum TIP/RING negative voltage pulse is between VBH to 15V and the minimum TIP/RING positive voltage pulse is +8V. When under operating conditions, the positive power supply is +3.3V ±10% and low battery power supply, VBL, ranged from -16V to -52V ±5%. Lower voltage is suggested. The high batter power supply voltage, VBH, is from VBL to -85V ±10%.

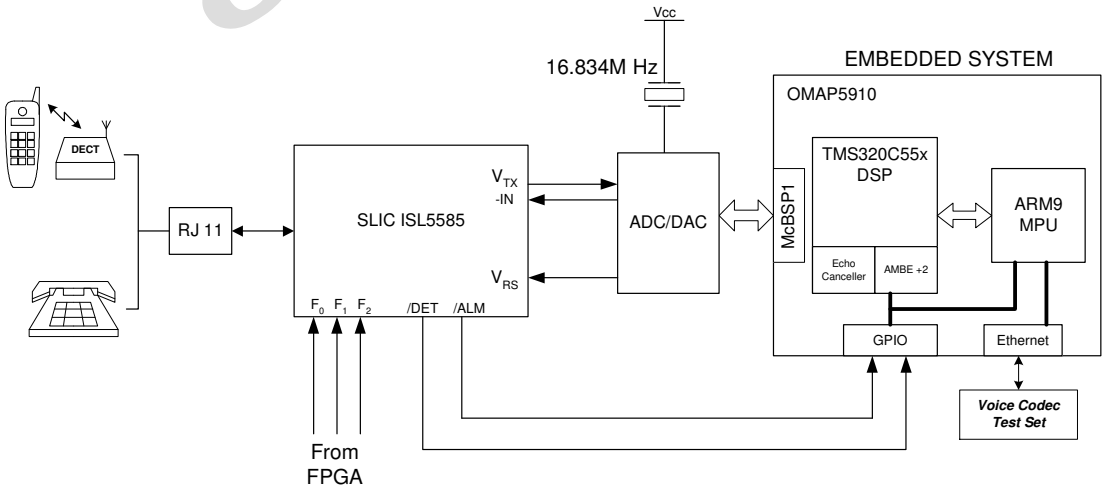


Figure 30: SLIC circuit block diagram

In addition, other key features across the product also include: low power consumption, ringing using sinusoidal waveforms, robust auto detection mechanisms for when subscribers go on or off hook, and minimal external discrete application components.

8.6 Voice Codec Test Set Protocol

This section describes the planning and development of Voice Codec Test Set (VCTS) protocol to be used for Vocoder terminals testing.

The VCTS protocol developed to meet the test requirements for Vocoder terminals. These requirements include all digital bit-exact test and conformance test using the digital and analog interfaces on the terminal. The test set uses Ethernet as a control channel to configure the terminal under test for requirements testing and as a digital interface for voice and channel data. DVSI's Voice Code Data Sets (VCDS) is part of VCTS. The VCTS protocol implements this control and data interface shall meet the specification of special protocol designed by DVSI for testing the Vocoder.

Figure 31 below is a typical setup for Ethernet interface testing.

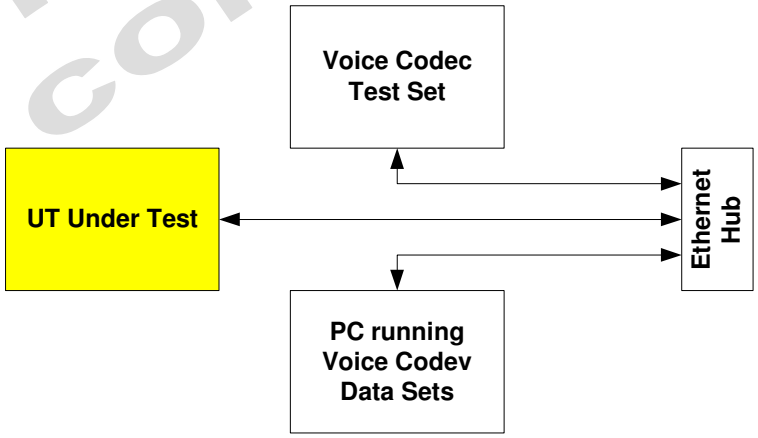


Figure 31: Test setup support Ethernet interface

Taking into consideration of time consumption to develop such Ethernet testing protocol specified by DVSI, alternative option also been planned to replaced such testing protocol interface software development. Ethernet communication interface daughter card developed by Windmill Innovations™ that support Texas Instruments C5510™ DSK is a ready to use dual 100BaseTx Daughter Board. The daughter card comes with configurable DIP switches and a RJ-45 media connector, which is compatible with the DVSI Net-2000™ Voice Coder Unit.

9 QUALITY ASSURANCE PLAN

The BGAN A5 PUT will be designed and produced using ISO9001 practice. The device is design with a proposed Mean Time Between Failure (MTBF) of 10,000 hours of operation or equivalent to 2 year of customer warranty.

This prediction may be used as a tool to compare the inherent reliability of this device to similar ones (if any), and does not claim to represent accurate expected field performance.

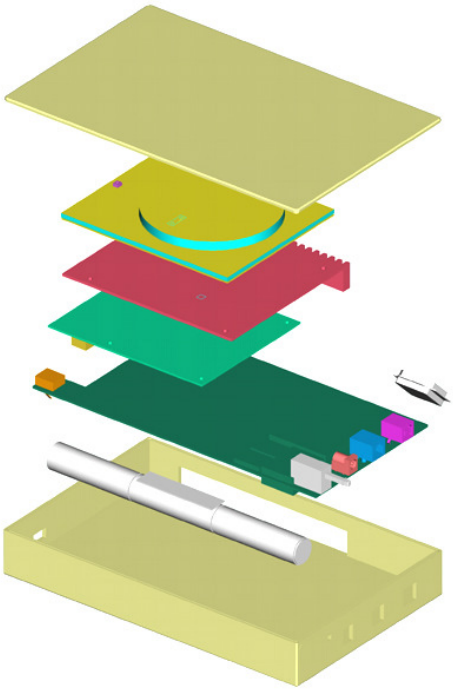
The reliability of the device will be predicted as per MIL-HDBK-217F, “Parts Count Reliability Prediction” standard or equivalent or other standards specified/recommended by Inmarsat.

Mechanical and enclosure for the device shall be designed to meet IP65 rating and environmental condition defined by Inmarsat in their product definition to meet environmental reliability requirements.

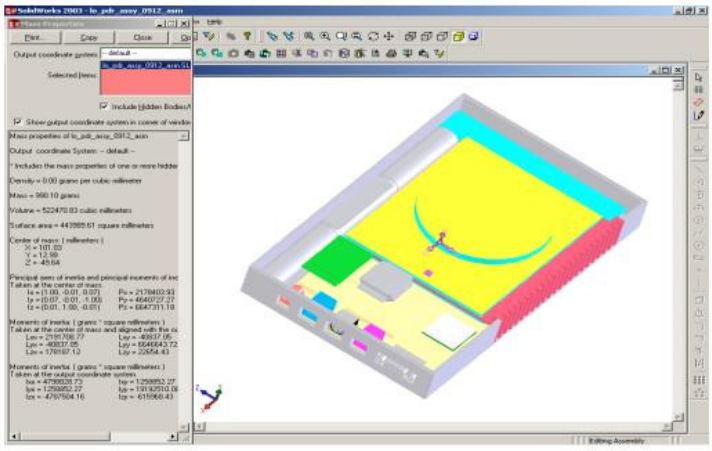
For the reliability testing for all the device configurations shall be follow the MIL-STD-810E / NEMA spec.

Quality assurance practice shall be applied to component selection during design phase. Quality control shall be applied during manufacturing of the device to ensure the PUT will meet all the required standards.

Appendix 1: Mechanical Concept Design



Centre of Gravity



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Appendix 2: Fully Closed Position with mounting & Standing Angle: 0° to 85°