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~~1.2.2~~1.1.1 System Architecture

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The proposed system architecture block diagram is shown in Figure 1~~Figure 1Figure 1Figure 1Figure 1Figure 1~~. It comprises an Antenna section (BGAN & GPS), an RF section (TX and RX), a Baseband Processing & Channel Unit, a GPS Module, an Embedded System module, and a Power Unit with power up sequencing scheme for high power RF circuit protection. High-level internal and external interfaces are shown in . Technical details for the various functional blocks are described in the subsequent sections.

Field Code Changed

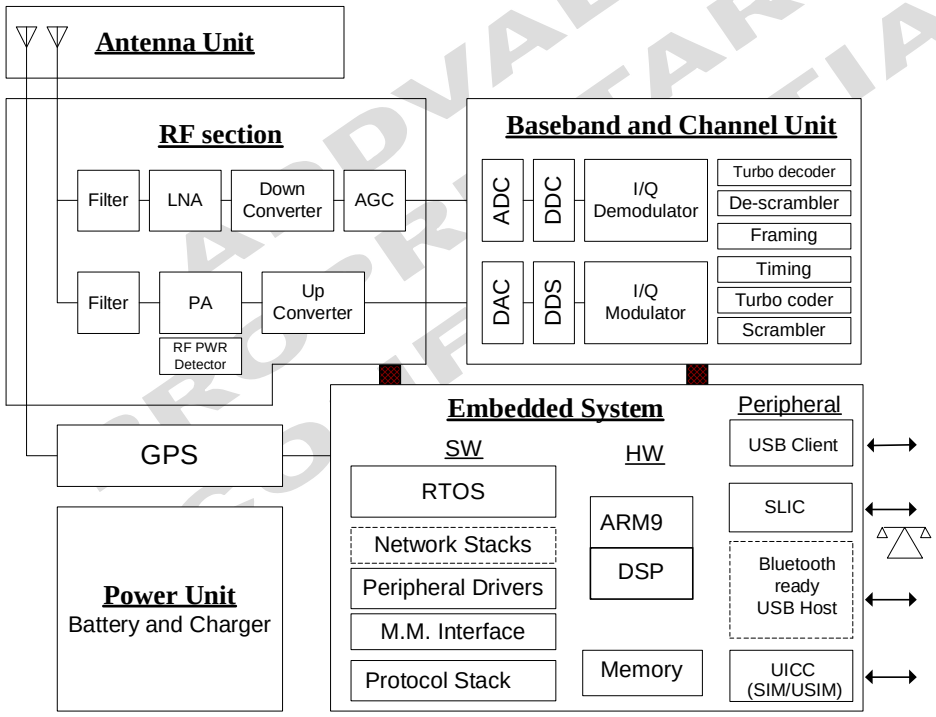

Figure 1: Pocket Size BGAN UT System Architecture Simplified Block Diagram

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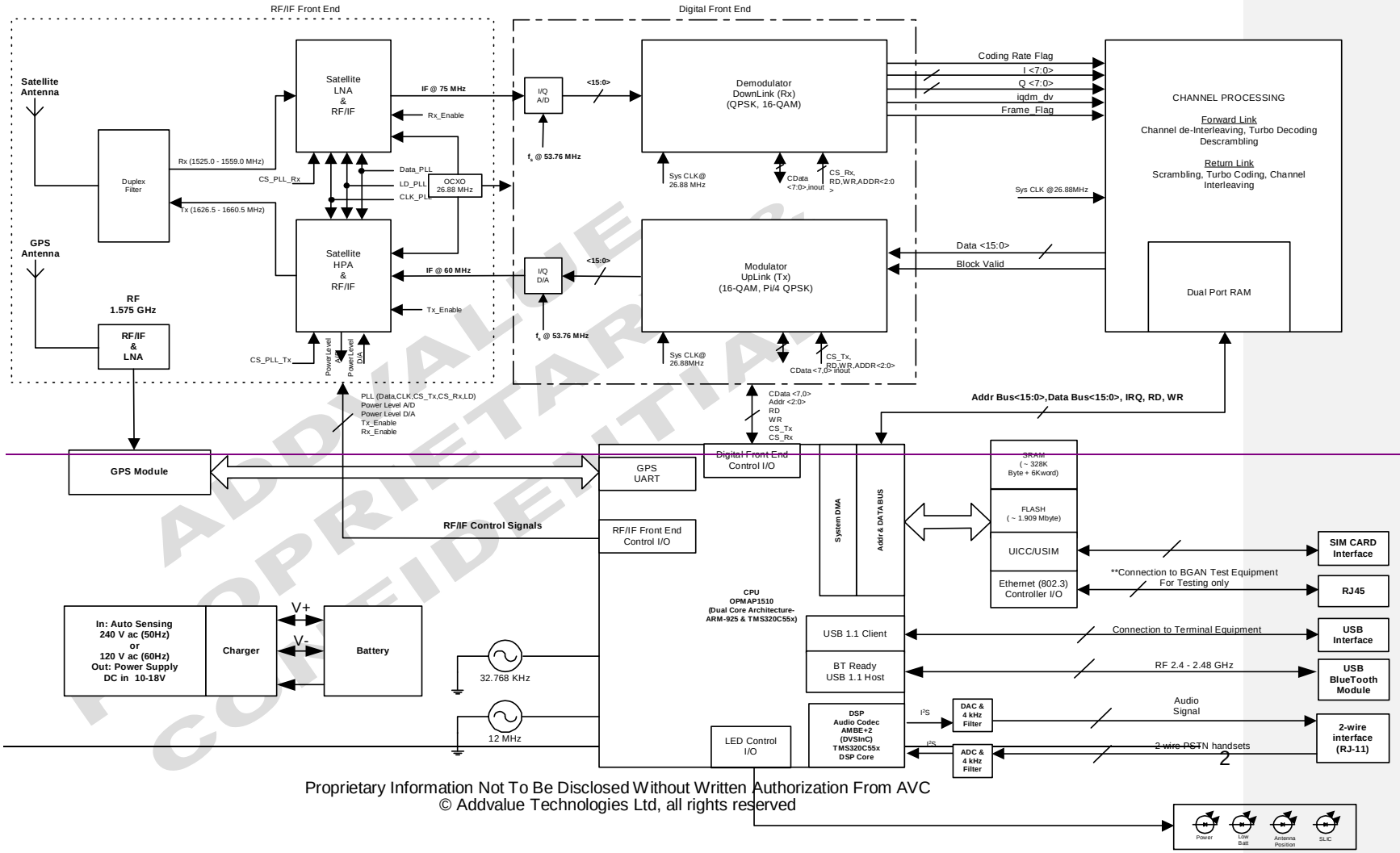

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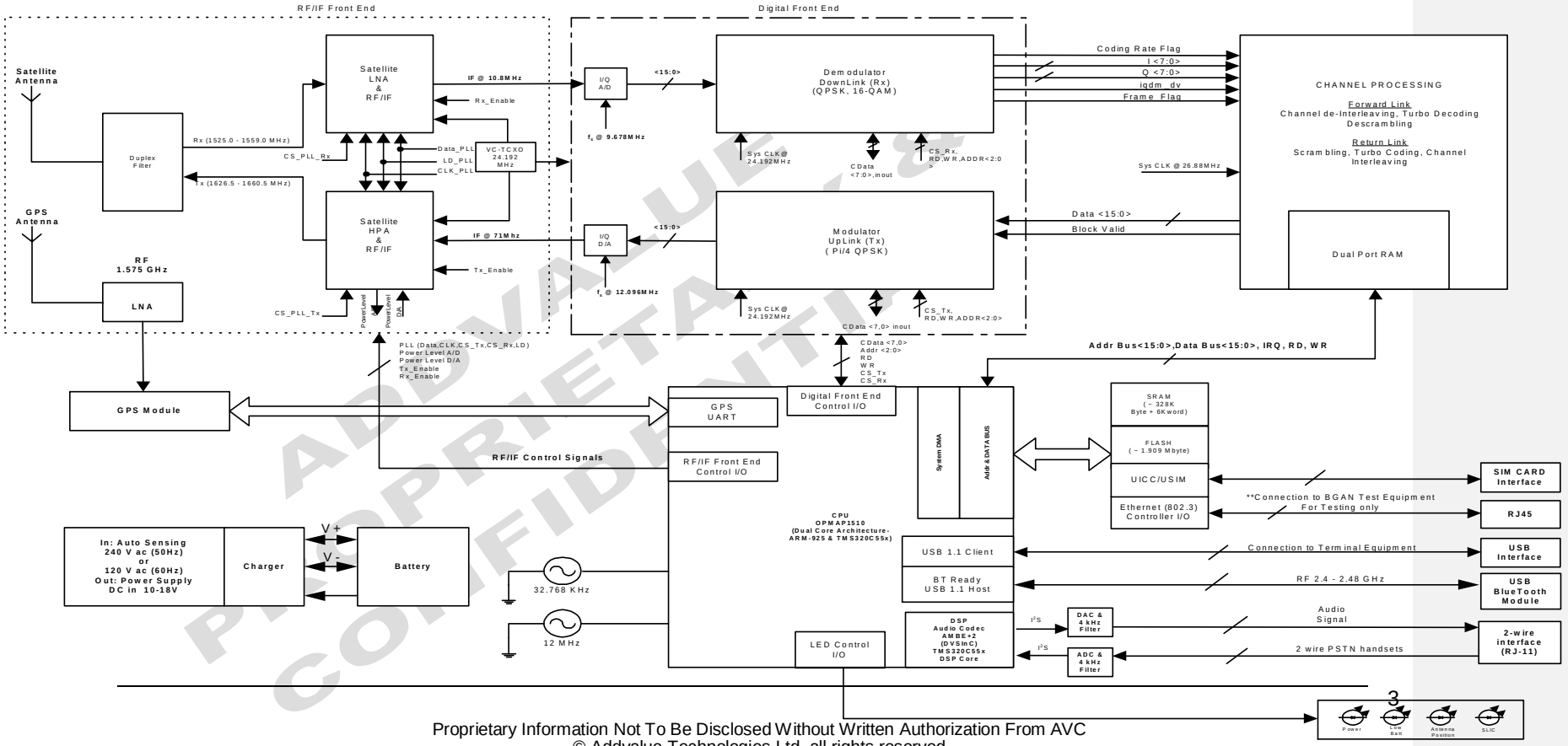
~~**Figure 2: Pocket Size BGAN UT System Architecture**~~

Figure 2~~3~~: Pocket Size BGAN UT System Architecture



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