

TZ150

Change History			
DATE	Version	Description	Designer
05/03/2004	0.1	Initial schematic received	
05/13/2004	0.2	<p>Page2 Remove U2, R20, C21, add decap for CPU power.</p> <p>Page3 Pull-up PCI req, PCI Int, pull-down MIIA-RXERR U1_E1, no stuff for R39, R40, stuff R42, R41, connect MIIC_RXERR U1_A2, pull-down SDR_CLK_IN, use serial termination resistors, no FB. add FB for switch add GPIO for WLAN.</p> <p>Page4 Remove 56TSOP flash, add GPIO pull-up/down.</p> <p>Page5 No FB for SDR CLK, add decap for SDR power, add serial termination for SDR control/address, add RC termination for SDR data, specify SDR serial termination placement</p> <p>Page6 connect miniPCI chassis to net_gnd, add 5V decap, add serial resistor to IDSEL, add 0.001uf decap, disconnect miniPCI audio ground</p> <p>Page7 Add FB to 1.8 AVCC, remove NRESET, replace FB with resistor, connects PMEXR U10_66, add serial termination for MII, stuff option for PS0/PS1, pull-down U10_1, U10_120 serial to gND, use LED5 for WAN</p> <p>Page8 WAN as NIC, LAN as HUB connection, RX->RD & TX->TD</p> <p>Page9 Use 2 LED for Link/Act and Speed, remove PPPoE and add WLAN Link/Act, add LED color text.</p>	G Tsang

Change History			
DATE	Ver.	Description	PCB number
2004/04/21	0.1	Initial schematic	4900PK00A
2004/05/17	0.2	<p>Page2 1. Remove U2, R20, C21 2. add decap for CPU power.</p> <p>Page3 1. Pull-up PCI req, PCI Int. 2. Connect MIIC_RXERR U1_A2. 3. Add FB for switch add GPIO for WLAN.</p> <p>Page4 1. Add GPIO pull-up/down.</p> <p>Page5 1. Add serial termination for SDR control/address, add RC termination for SDR data.</p> <p>Page6 1. Connect miniPCI chassis to net_gnd, add 5V decap. 2. disconnect miniPCI audio ground</p> <p>Page7 1. Add FB to 1.8 AVCC 2. Connects PMEXR U10_66 3. Add serial termination for MII 4. Use LED5 for WAN</p> <p>Page9 1. Use 2 LED for Link/Act and Speed, remove PPPoE and add WLAN Link/Act, add LED color text.</p>	

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Change History			
DATE	Version	Description	Designer
05/21/2004	0.3	<p>Page3 Add GPIO for SPI select, pull-down SDR_CLK_IN, add PCI add PCI separated clock PCI_CLK_OUT_USB for USB.</p> <p>Page4 Add RC termination for ELB bus on flash. Suggest to remove 56TSOP flash.</p> <p>Page6 No stuff resistor for PCI_PAR, add RC termination option PCI bus control/AD.</p> <p>Page7 Add SPI select from GPIO, re-arrange SPI bus. Suggest to fix KS8995XA symbol.</p> <p>Page8 Request to make change for connection WAN as NIC.</p> <p>Page9 No stuff for inverter, provide individual power for USB no stuff option for 5V fuse, PCI_CLK_OUT_USB from CPU.</p> <p>Page10 Re-arrange Link/Act for green LED, Speed for yellow LED, correct LED color text.</p>	G Tsang
05/25/2004	0.4	<p>Page3 Adds 56 Ohm in serial with U25_9 & U25_10 and 0 Ohm in serial with U25_7 & U25_8. We may need to stuff 1000 Ohm @100 MHZ FB later for test.</p> <p>Page4 Only ELB_AD14, AD15, AD18, AD20, AD21, AD22 and control signals ELB_OE, RW, CSA, CSB for stuff option (NU) RC termination. Adds STmicro M29DW323D and M29D640D for Flash reference.</p>	G Tsang
2004/08/03	1.0	1.0 is the same as 0.5	
2004/09/01	1.1	Remove R219 and install R48	

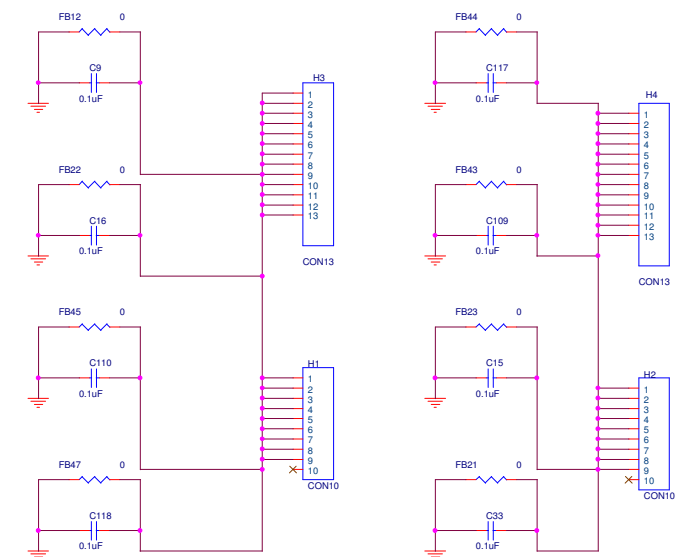
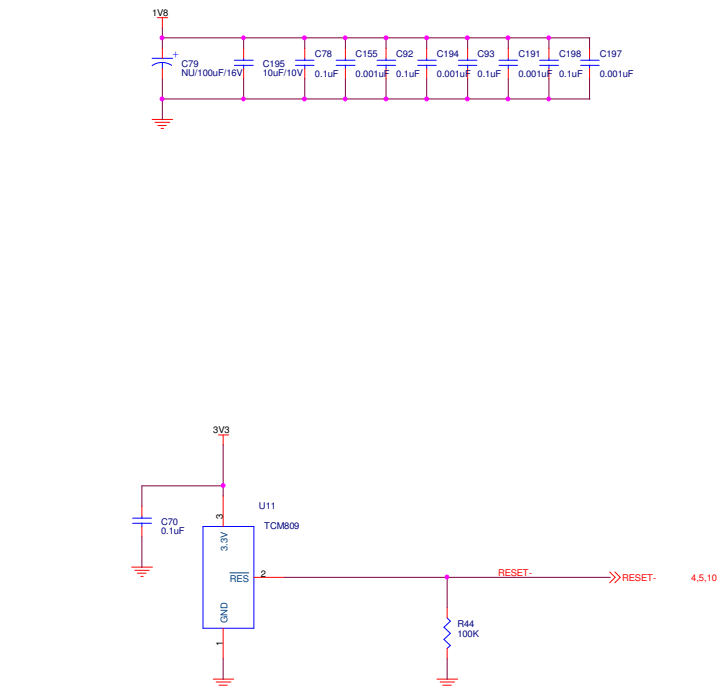
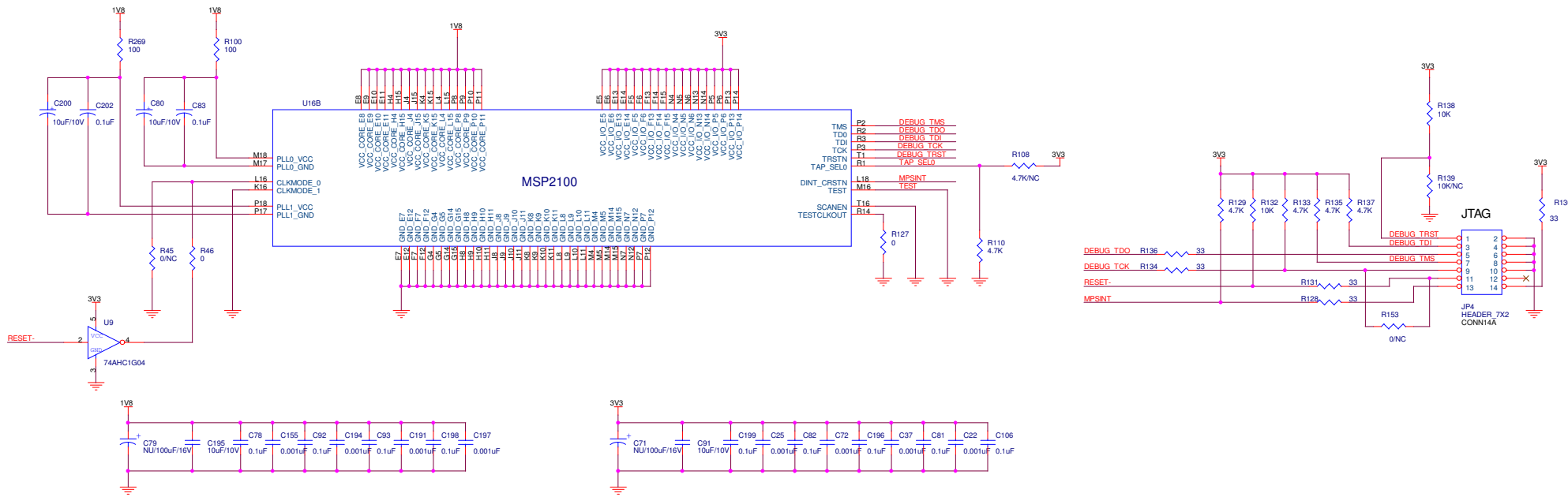
Change History			
DATE	Ver.	Description	PCB number
2004/05/24	0.3	<p>Page3 1. Add GPIO for SPI select. 2. Pull-down SDR_CLK_IN. 3. Add PCI separated clock PCI_CLK_OUT_USB for USB. 4. Add RS232 for debug port</p> <p>Page4 1. Add RC termination for ELB bus on flash. 2. Remove 56TSOP flash.</p> <p>Page6 1. No stuff resistor for PCI_PAR. 2. Add RC termination option PCI bus control/AD.</p> <p>Page7 1. Add SPI select from GPIO, re-arrange SPI bus. 2. Fix KS8995XA symbol.</p> <p>Page8 1. Make change for connection WAN as NIC.</p> <p>Page9 1. Remove inverter, provide individual power for USB. 2. PCI_CLK_OUT_USB from CPU.</p> <p>Page10 1. Re-arrange Link/Act for green LED, Speed for yellow LED, correct LED color text.</p>	
2004/05/26	0.4	<p>Page3 1. Adds 56 Ohm in serial with U25_9 & U25_10 and 0 Ohm in serial with U25_7 & U25_8. 2. Stuff R37, R38, no stuff for R40, R41.</p> <p>Page4 1. Remove terminator resistors for ELB_OE, RW, and else, because they are also terminated in PCI. 2. Adds STmicro M29DW323D and M29D640D for Flash reference. 3. Remove resistors reserved for Intel A3 Flash. 4. Use 12V81.66A switching power adaptor. 5. Use a 5X2 pin header as the debug port.</p>	
2004/07/29	0.5	1. Add MX29LV320ATTC and MX29LV640TTC for reference.	4900PK00B
2004/08/03	1.0	1.0 is the same as 0.5	
2004/09/01	1.1	Remove R219 and install R48	

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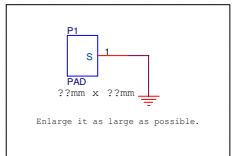
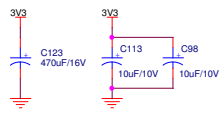
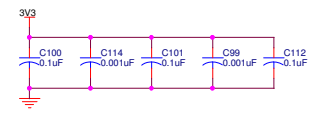
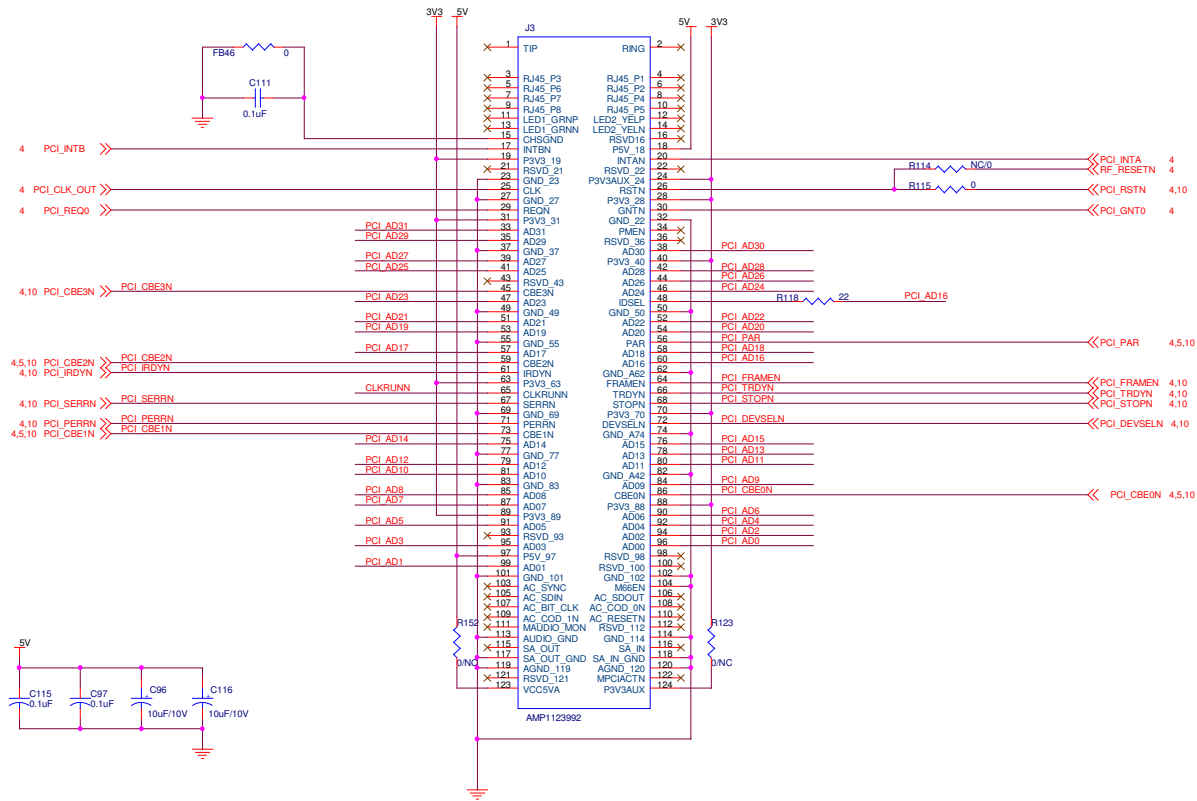
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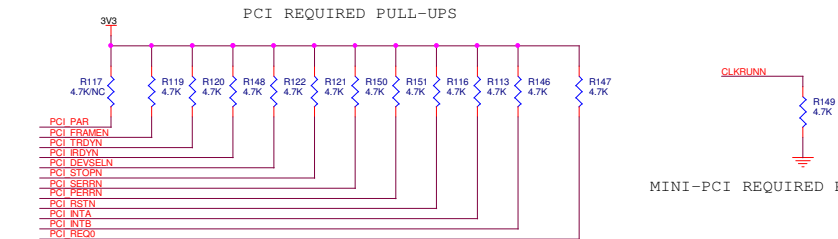
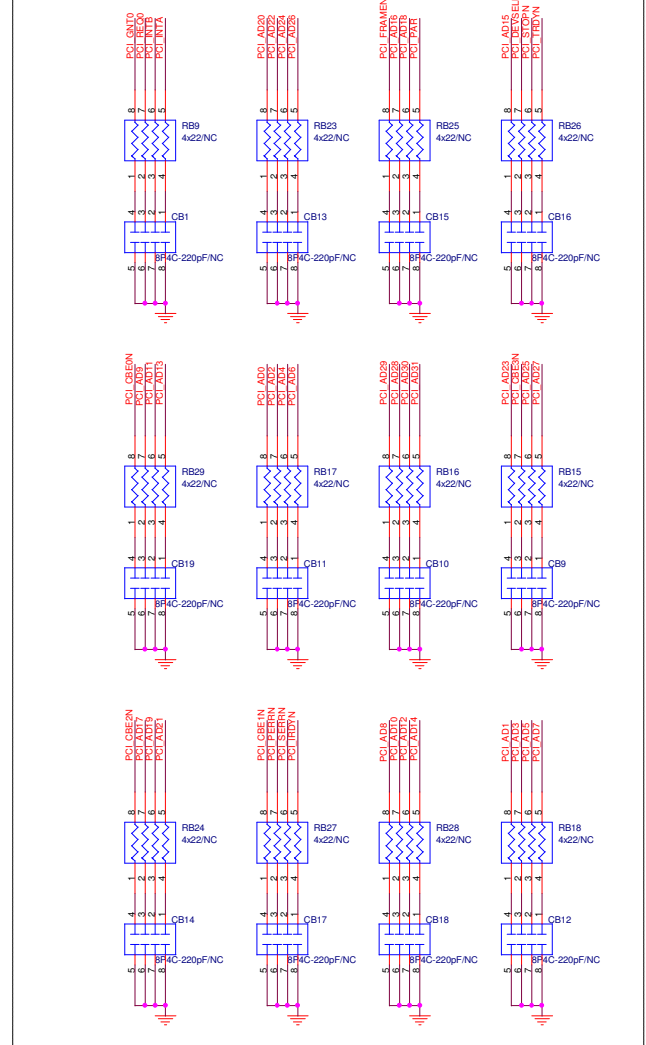
HI~H4: Mounting Hole

4.5.10 PCI_AD[31:0]

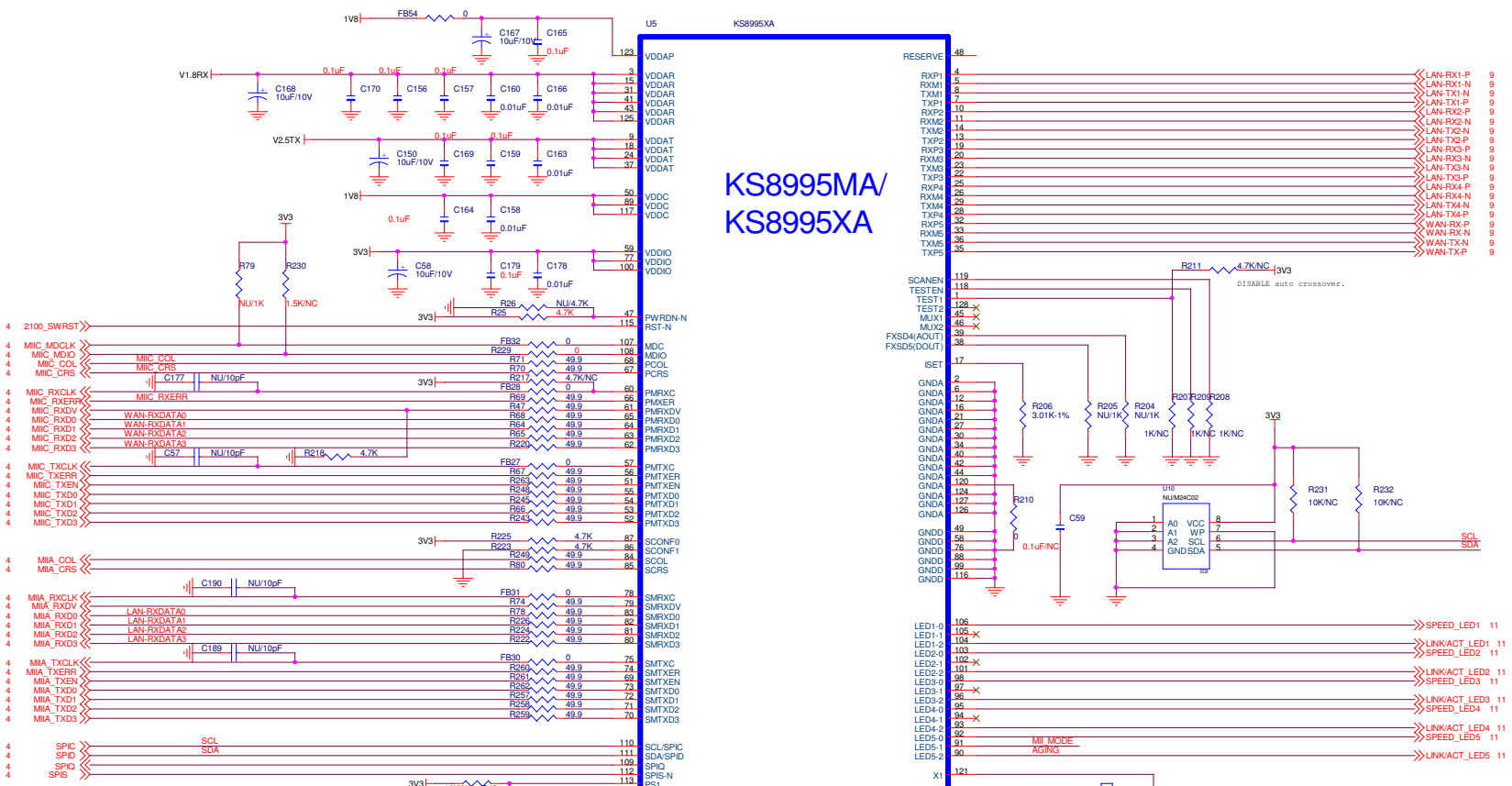
MINI-PCI CONNECTOR



RC termination for PCI bus, place end of the PCI bus

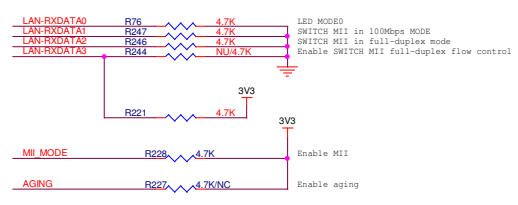
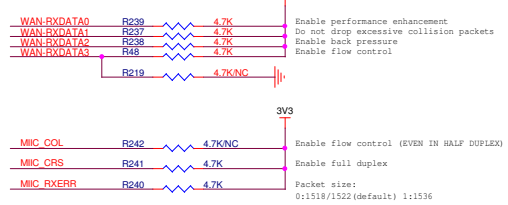


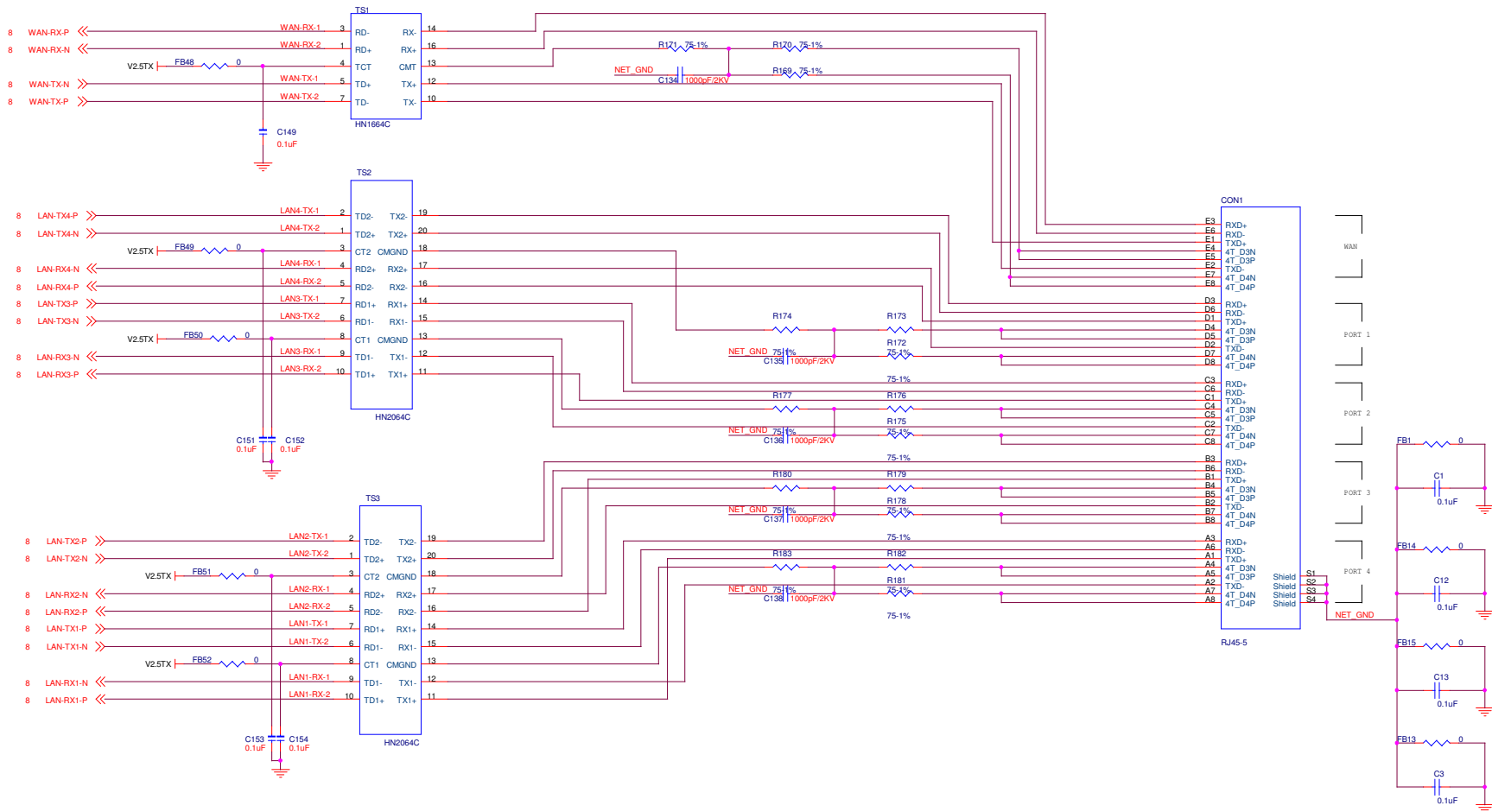
KS8995MA/ KS8995XA



PS[1..0] are internal weak pull down
SPI is only used
in KS8995M

PS[1..0]	Bus config
00	I2C master mode for EEPROM
01	Reserved
10	SPI slave mode for CPU
11	Factory test mode



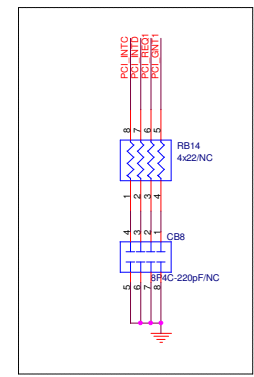
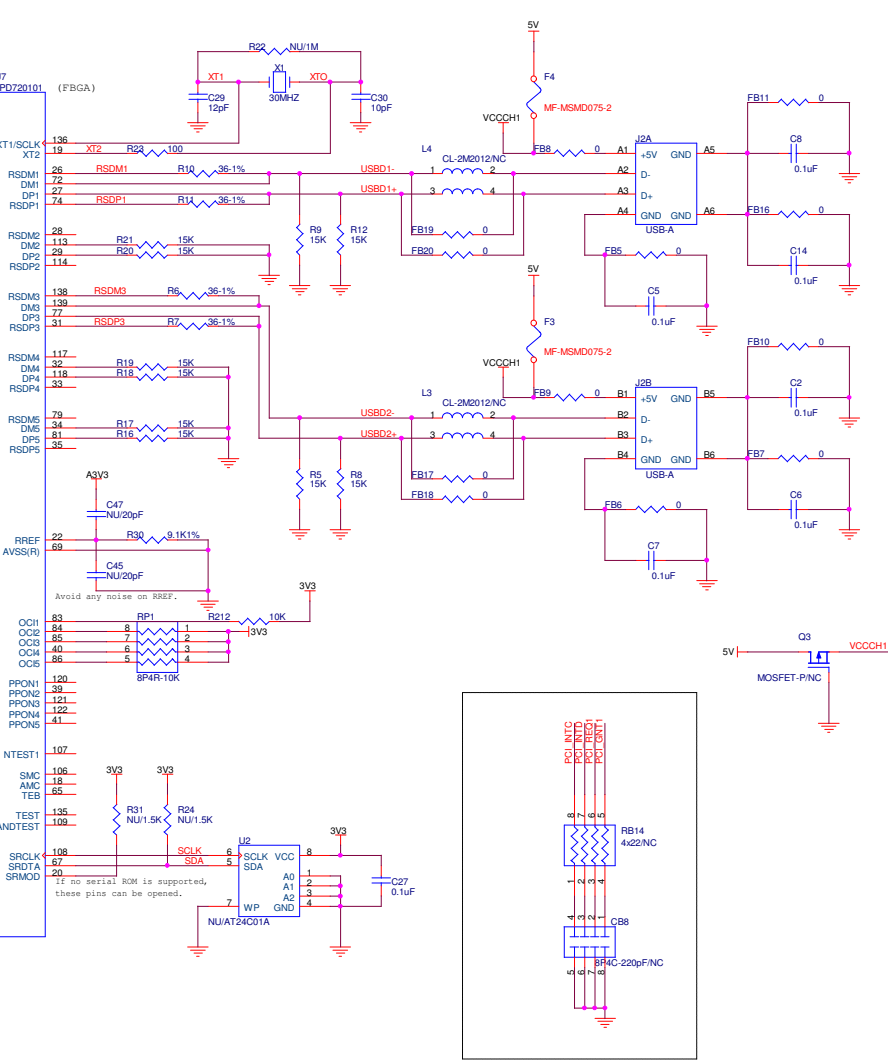
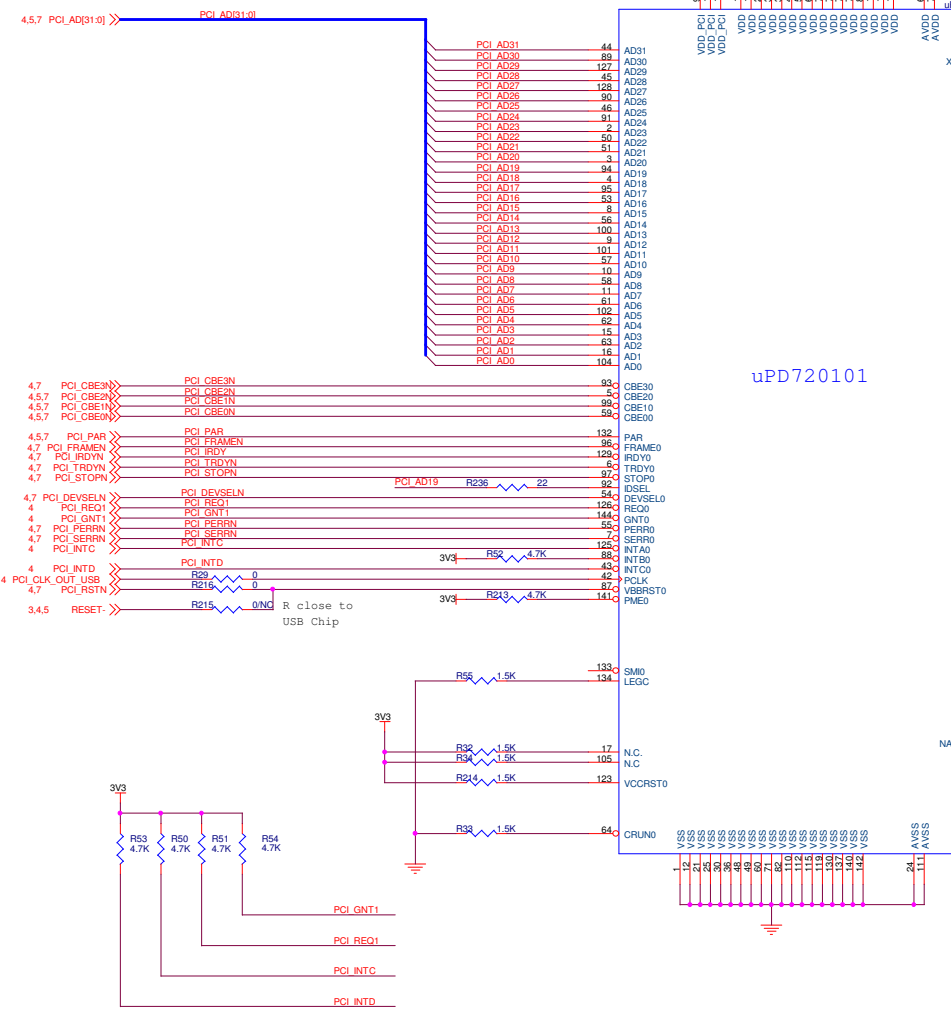
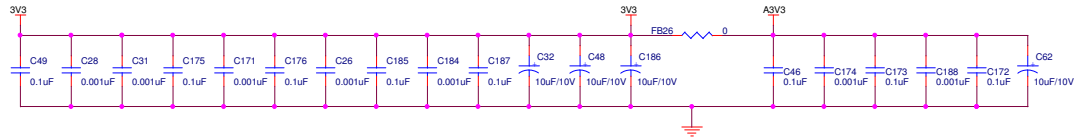


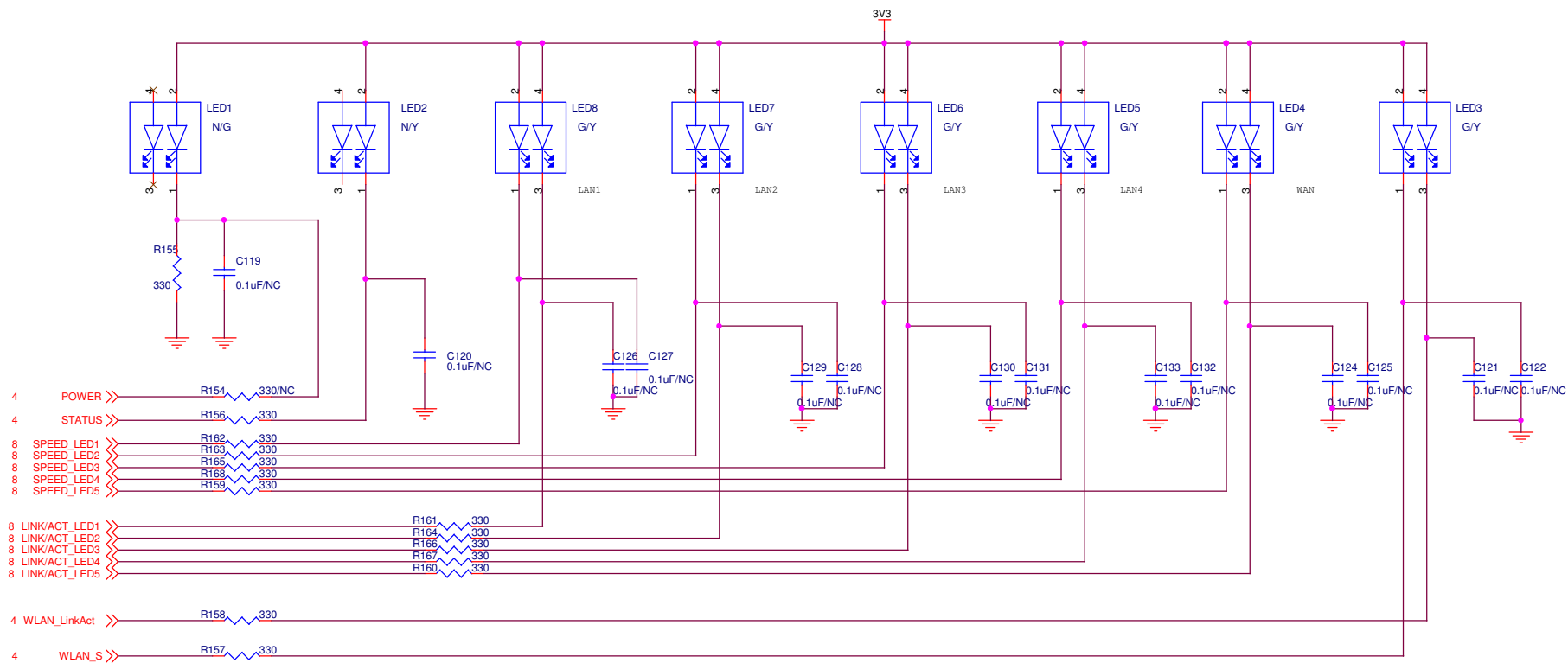
WAN-TX-1	R195	49.9-1%
WAN-TX-2	R187	49.9-1%
WAN-RX-1	R185	49.9-1%
WAN-RX-2	R184	49.9-1%
LAN4-TX-1	R189	49.9-1%
LAN4-TX-2	R188	49.9-1%
LAN4-RX-1	R190	49.9-1%
LAN4-RX-2	R191	49.9-1%
LAN3-TX-1	R193	49.9-1%
LAN3-TX-2	R192	49.9-1%
LAN3-RX-1	R194	49.9-1%
LAN3-RX-2	R195	49.9-1%
LAN2-TX-1	R197	49.9-1%
LAN2-TX-2	R196	49.9-1%
LAN2-RX-1	R198	49.9-1%
LAN2-RX-2	R199	49.9-1%
LAN1-TX-1	R201	49.9-1%
LAN1-TX-2	R200	49.9-1%
LAN1-RX-1	R202	49.9-1%
LAN1-RX-2	R203	49.9-1%
	C140	0.1uF
	C139	0.1uF
	C141	0.1uF
	C142	0.1uF
	C143	0.1uF
	C144	0.1uF
	C145	0.1uF
	C146	0.1uF
	C147	0.1uF
	C148	0.1uF

USB trace


- Keep traces of USB bus D+ and D- in the same length.
- Achieve 90 ohm differential characteristic impedance.
- Maintain parallelism between D+ and D-.
- Locate Rs resistor (R50 - R59) nearby Host controller.
- Do not route USB2.0 D+ and D- over the power plane split.
- Do not route USB2.0 D+ and D- over the other high frequency signals.
- It is preferred to route USB2.0 D+ and D- over ground layer.
- It is preferred to route USB2.0 D+ and D- using single layer.

For more detail, see design guideline in design kit.





		WAN	LAN [PORT 1 - PORT 4]					Wireless LAN
TOP	Green	Link - Solid	Link - Solid	Link - Solid	Link - Solid	Link - Solid	Power	Link - Solid
PIN 3 & 4	LED	Act - Flashing	Act - Flashing	Act - Flashing	Act - Flashing	Act - Flashing		Act - Flashing
PIN 1 & 2	Yellow	Speed - 10BT / OFF	Speed - 10BT / OFF	Speed - 10BT / OFF	Speed - 10BT / OFF	Speed - 10BT / OFF	Status	Wi-Fi Sec
BOTTOM	LED	Speed - 100BT / ON	Speed - 100BT / ON	Speed - 100BT / ON	Speed - 100BT / ON	Speed - 100BT / ON		TBD


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Title: **TZ150 - LED display**

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