Revision January 20, 2009

Application

- IEEE802.11 b/g Wireless Local Area Networks
- IEEE802.11n Wireless Local Area Networks
- TDMA Packet Protocol Radios
- 2.4GHz ISM Wireless System

RT2720 is a monolithic SiGe RF IC that integrates half-duplex direct-conversion radio transceivers designed for IEEE802.11 b/g/n WLAN systems or other wireless LAN applications operating in 2.4GHz (low-band) ISM bands.

The IC has one transmit channel and two concurrent receive channels. The receivers achieve low noise figure, high input sensitivity, high linearity, and high output power while consuming low dc power. The two receive channels are designed to improve robustness and to receive two data streams during receive operation. Each receive path features a gain selectable, low-noise amplifiers (LNA), followed by RF-to-baseband I/Q demodulators, discrete-step variable-gain amplifiers and integrated channel-selection filters. The transmit chain includes integrated reconstruction filters, a baseband-to-RF I/Q modulator, discrete-step variable-gain amplifiers for power-level control, and pre-drivers for external power amplifiers. The modulator and demodulator are driven by internal VCO. The VCO is phase-locked by an internal 3-wire-interfaced PLL. The bandwidth of the integrated channel-selection filters and the reconstruction filters can be programmed to narrow-band (10MHz) and wide- band (20MHz). Their bandwidth is calibrated by an internal autonomous calibration circuit. To help IQ mismatch calibration, a baseband transmit-to-receive loopback feature is provided. A crystal oscillator using external crystal and three low dropout regulators (LDO) are also integrated.

The RT2720 is housed in a 68-pin 8x8mm^2 leadless QFN package well suited for PCMCIA, MiniPCI, PCI, USB boards or embedded applications. It is designed to work seamlessly with RT2860 and RT2880 baseband/Mac IC.

Features

- A single-chip transceiver
- 2.4 GHz bands
- Low noise figure
- High linearity
- Low power consumption
- Integrated channel-selection filters
- Integrated reconstruction filters
- Power management/standby mode
- Integrated low dropout regulators
- Single supply 3.0 to 3.6V operation

Rx

- Icc.....129 mA
- Receiver Sensitivity (54Mbps)..... -73 dBm
- Receiver DSB Noise Figure..... 6 dB
- Input IP3 (High Gain) .....-20 dBm
- Input IP3 (Low Gain) ..... 12 dBm
- Input P1dB (High Gain)..... -30 dBm
- Input P1dB (Low Gain)..... 2 dBm
- VGA Gain Control Range..... 62 dB

Tx

- Icc..... 104mA
- Output Power (OFDM)..... 6 dBm
- Output Noise Floor.....-141dBm/Hz
- Output P1dB.....14 dBm
- VGA Gain Control Range..... 15 dB

Sleep

- Icc.....<1uA

Order Information

Part Number	Temp Range	Package
RT2720L	-10~85 ^{0}C	68Ld QFN

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Functional Block Diagram

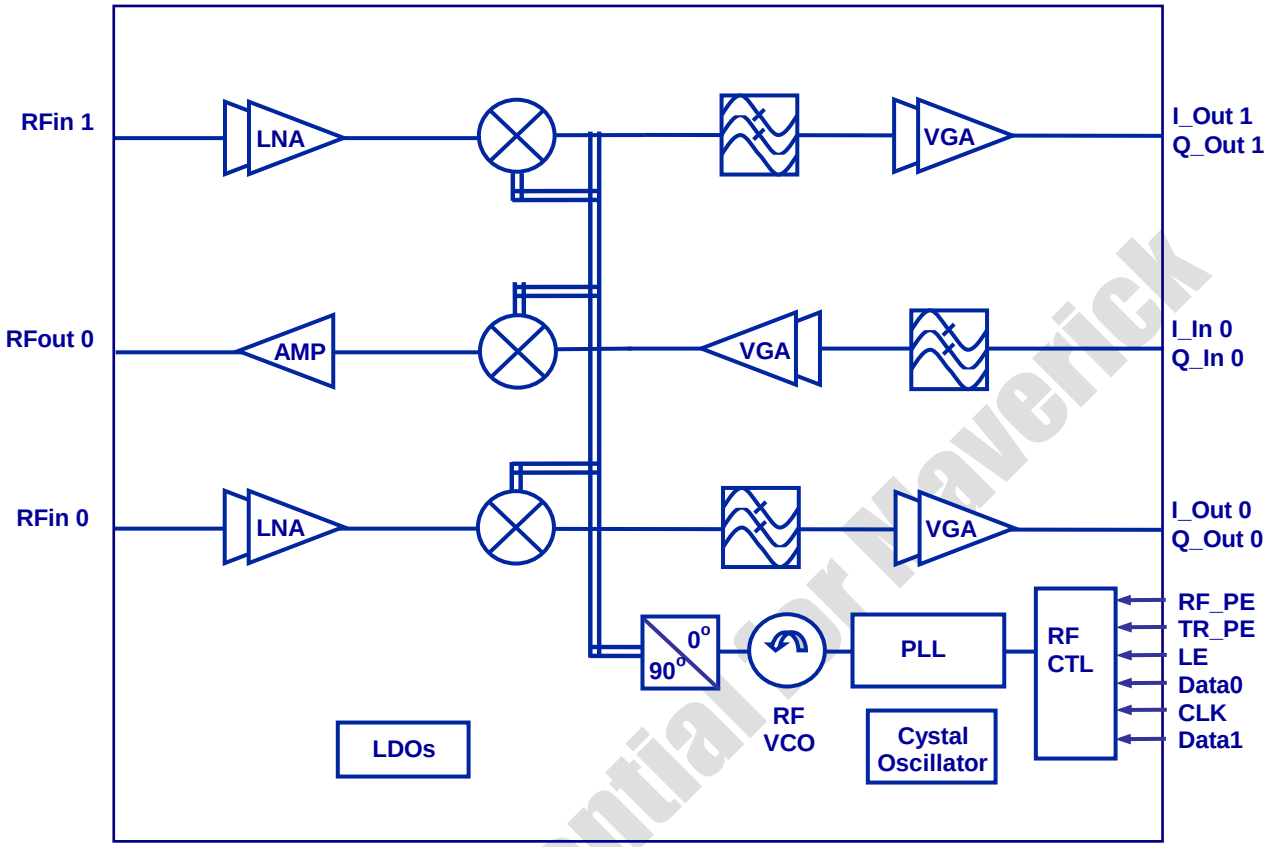

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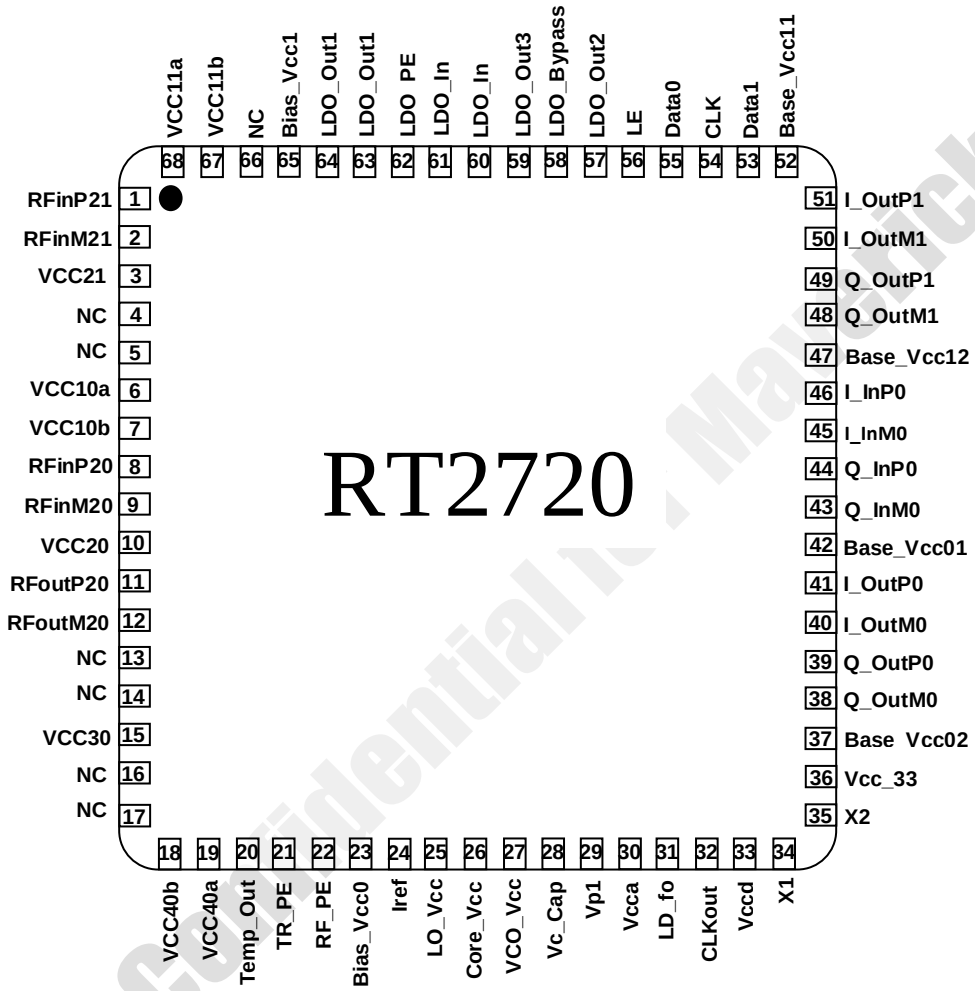
Table of Content

1. Pin Description

1.1 Pinout of RT2720 QFN68 8x8mm²



1.2 Pin Description of RT2720

Pin	Name	Description
1	RFinP21	Rx RF input of channel 1.
2	RFinM21	
3	VCC21	Power supply for RF circuits of channel 1.
4	NC	Not connected.
5	NC	
6	VCC10a	Power supply for low-band IF circuits of channel 0.
7	VCC10b	Power supply for low-band LO buffers of channel 0.
8	RFinP20	Rx RF input of channel 0.
9	RFinM20	
10	VCC20	Power supply for low-band RF circuits of channel 0.
11	RFoutP20	Tx RF output.
12	RFoutM20	
13	NC	Not connected.
14	NC	
15	VCC30	Power supply for high-band RF circuits of channel 0.
16	NC	Not connected.
17	NC	
18	VCC40b	Power supply for high-band LO buffers of channel 0.
19	VCC40a	Power supply for high-band IF circuits of channel 0.
20	Temp_Out	Temperature reference voltage output (proportional to absolute temperature).
21	TR_PE	Rx and Tx enable control. Refer to Operation Mode in Section 3.
22	RF_PE	
23	Bias_Vcc0	Power supply for bandgap reference circuit of channel 0.
24	Iref	200mA reference current output.
25	LO_Vcc	Power Supply for LO buffer.
26	Core_Vcc	Power supply for internal VCO.
27	VCO_Vcc	Power supply for internal VCO.
28	Vc_Cap	Control voltage for internal VCO.
29	Vp1	PLL charge pump power supply.
30	Vcca	Power Supply for prescaler of PLL.
31	LD_fo	Synthesizer lock detect, programmable or reference divider output.
32	CLKout	Crystal oscillator output.
33	Vccd	Power supply for digital CMOS divider of PLL.
34	X1	Crystal inputs or external crystal oscillator input.
35	X2	
36	Vcc_33	Power supply for control registers.
37	Base_Vcc02	Power supply for baseband circuits of channel 0.
38	Q_OutM0	Baseband Q differential output of channel 0.
39	Q_OutP0	
40	I_OutM0	Baseband I differential output of channel 0.
41	I_OutP0	
42	Base_Vcc01	Power supply for baseband circuits of channel 0.
43	Q_InM0	Baseband Q differential input of channel 0.
44	Q_InP0	
45	I_InM0	Baseband I differential input of channel 0.
46	I_InP0	
47	Base_Vcc12	Power supply for baseband circuits of channel 1.
48	Q_OutM1	Baseband Q differential output of channel 1.
49	Q_OutP1	

Pin	Name	Description
50	I_OutM1	Baseband I differential output of channel 1.
51	I_OutP1	
52	Base_Vcc11	Power supply for baseband circuits of channel 1.
53	Data1	Serial data input for channel 1. Clocked on the rising and falling edges of CLK.
54	CLK	Serial data input clock. Up to 60MHz.
55	Data0	Serial data input for channel 0 and PLL programming.
56	LE	Serial data latch enable control.
57	LDO_Out2	LDO output (supply up to 10mA).
58	LDO_Bypass	LDO bypass capacitor for noise filtering.
59	LDO_Out3	LDO output (supply up to 18mA).
60	LDO_In	Power supply for LDO.
61	LDO_In	Power supply for LDO.
62	LDO_PE	LDO enable control.
63	LDO_Out1	LDO output (supply up to 180mA).
64	LDO_Out1	LDO output (supply up to 180mA).
65	Bias_Vcc1	Power supply for bandgap reference circuit of channel 1.
66	NC	Not connected
67	VCC11b	Power supply for LO buffers of channel 1.
68	VCC11a	Power supply for IF circuits of channel 1.

2 Maximum Ratings and Operating Conditions Absolute Maximum Ratings

Supply Voltage 3.6V
Vcc to Vcc Decouple..... –0.3 to +0.3V
Any GND to GND..... –0.3 to +0.3V

2.2 Thermal Information

Thermal Resistance (Typical, Note 1.) . JA (° C/W) QFN Package.....28.4°C /W
Maximum Junction Temperature (Plastic Package) .....125°C
Maximum Storage Temperature Range ..... –40 °C to 125 °C
Maximum Lead Temperature (Soldering 10s)..... 260°C

2.3 Operating Conditions

Temperature Range ..... -10 to 85°C
Supply Voltage Range..... 2.7V to 3.3V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:
JA is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.

2.4 DC Electrical Characteristics

(Ta=25 C, VCC = 3 V, Unless otherwise specified.)

Transceiver (two transmit channels and three receive channels)

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	Vcc		2.7		3.3	V
Receive total supply current (2 receivers, excluding VCO and crystal oscillator)	Icc	Low Band		123		mA
Internal VCO			5		11	mA
Transmit total supply current (1 transmiters, excluding VCO and crystal oscillator)	Icc	High Power		98		mA
		Mid Power		78		
		Low Power		68		
Crystal Oscillator				3		mA
Current Reference Output	Iref		180	200	220	μA
Temperature Reference Output	Temp_Out	Temperature = 25°C		0.9		V
		Temperature Coefficient		2.62		mV/°C
Control Logic Input Voltage	VIH VIL	High level Low level	0.7*Vcc		 0.3*Vcc	V V
Control Logic Input Current	IHL		-10		10	μA
Power down current	IPD	RF_PE=0, TR_PE=0, OSC_en=0		1		μA
TX/RX Power down speed					1	μs
RX/TX, TX/RX Switching Speed					1	μs

Low Dropout Regulators (LDO)

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage	LDO_In		3		3.6	V
Output Voltage				2.85		V
Quiescent Current				1		mA
Output Current		LDO_Out1			180	mA
		LDO_Out2			10	
		LDO_Out3			18	
Control Logic Input Voltage	LDO_PE	High level Low level	0.7*LDO_In		0.3*LDO_In	V
Control Logic Input Current			-10		10	μA
Power down current		LDO_PE=0		1		μA

2.5 AC Electrical Characteristics

2.5.1 Receiver (each channel)

f_{RF} = 2437MHz, $f_{baseband}$ = 5MHz, Unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Unit
RF Frequency Range		2400		2500	MHz
Conversion Voltage Gain (AGC code = 11111)	LNA_Gain0 = 1, LNA_Gain1 = 1	86	90	94	dB
	LNA_Gain0 = 0, LNA_Gain1 = 1		73		
	LNA_Gain0 = 1, LNA_Gain1 = 0		58		
Gain Variation over RF Frequency	LNA_Gain0 = 1, LNA_Gain1 = 1				dB
Baseband Output Amplitude (Pin = -90 dBm, AGC code = 11111)	LNA_Gain0 = 1, LNA_Gain1 = 1		300		mV
	LNA_Gain0 = 0, LNA_Gain1 = 1		42		
	LNA_Gain0 = 1, LNA_Gain1 = 0		7.5		
Double-Sideband Noise Figure	LNA_Gain0 = 1, LNA_Gain1 = 1 AGC code = 11111		6		dB
Input P1dB	LNA_Gain0 = 1, LNA_Gain1 = 1	-32	-30	-28	dBm
	LNA_Gain0 = 0, LNA_Gain1 = 1	-15	-13	-11	
	LNA_Gain0 = 1, LNA_Gain1 = 0	0	2	4	
LNA Gain Switching Time	RF to Baseband output			0.15	μs
LO Leakage	RF input				dBm

2.5.2 Baseband Receive Filter and Output Buffer (common for low-band and high-band receivers)

fbaseband = 5MHz, after filter self-calibration, Unless otherwise specified.

Parameters	Conditions		Min	Typ	Max	Unit
Output P1dB	Differential	common-mode voltage=1.5		1.4		V
		common-mode voltage=0.6		0.8		
Baseband Filter Bandwidth	1dB upper bandwidth	narrow band		10.1		MHz
		wide band		21.4		
	3dB upper bandwidth	narrow band		10.5		
		wide band		23		
	1dB lower bandwidth			126		kHz
	3dB lower bandwidth			40		
Baseband Filter Rejection	25 MHz	narrow band		35		dB
	50MHz	narrow band		75		
		wide band		33.5		
	100 MHz	wide band		72		
Baseband Output Amplitude	Within 0.3 – 9.5 MHz	narrow band		1		dB

Ripple	Within 0.3 - 19 MHz	wide band		1.8		
Baseband Output Group Delay Ripple	Within 0.3 – 9.5 MHz	narrow band		212		ns
	Within 0.3 - 19 MHz	wide band		215		
IQ Gain Matching					0.2	dB
IQ Phase Matching					1	degree
Rx AGC Gain Control Step	5-bit control = 32 levels			2		dB/step
	Additional gain (using PLL register)			10.7		dB
Rx AGC Gain Settling Time	Including DC offset cancellation				0.4	μs
Baseband Output Common-Mode Voltage			1.4	1.5	1.6	V
			0.55	0.6	0.65	
Baseband Output DC Offset	Differential				40	mV
Baseband Output Impedance	Differential			500		Ω
Baseband Output External Load	Single-ended		15 5		 18	kΩ pF
	Differential		8 2.5		 9	kΩ pF

2.5.3 Transmitter

f_{RF} = 2437MHz, $f_{baseband}$ = 5MHz, Unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Unit
RF Frequency Range		2400		2500	MHz
Output Power (OFDM)	Vin(rms)=0.15V, ALC Code = 1001		4		dBm
			1		
			-3		
Output Power (CCK)	Vin(rms)=0.3V, ALC Code = 1001		10		dBm
			7		
			3		
Output Power Variation over RF Frequency					dB
Output P1dB			13.5		dBm
			11		
			6.5		
ACPR (OFDM)	Pout=-6dBm, OFDM, 10MHz offset		-48	-45	dBc
Output Noise Floor	Pout=-6dBm, ALC Code = 1001		-141		dBm/Hz
LO Suppression	Pout=-6dBm	35	40		dBc
Carrier Suppression		30	35		dBc
Single-Sideband Suppression	$2f_{LO} - f_{RF}$	35	40		dBc
Tx ALC Gain Control Step	5-bit control = 32 levels		0.5		dB/step

2.5.4 Baseband Transmit Filter (common for both low-band and high-band transmitters)

$f_{baseband}$ = 5MHz, with filter self-calibration, Unless otherwise specified.

Parameters	Conditions		Min	Typ	Max	Unit
Input P1dB	Differential Amplitude			0.48		V
Baseband Filter Bandwidth	1dB upper bandwidth	narrow band		10.3		MHz
		wide band		19.7		
	3dB upper bandwidth	narrow band		12.3		

		wide band		23.5		
Baseband Filter Rejection	20 MHz	narrow band		13.2		dB
	30 MHz	narrow band		23.6		
		wide band		7.5		
	50 MHz	narrow band		37.5		
		wide band		20		
	100 MHz	wide band		40		
Baseband Filter Amplitude Ripple	Within 0.3 - 9.5 MHz	narrow band		0.8		dB
	Within 0.3 - 19 MHz	wide band		1		
Baseband Filter Group Delay Ripple	Within 0.3 - 9.5 MHz	narrow band		13		ns
	Within 0.3 - 19 MHz	wide band		7		
IQ Gain Matching					0.2	dB
IQ Phase Matching					1	degree
Baseband Input Common-Mode Voltage			2.3	2.4	2.5	V
Baseband Input Impedance	Differential			190		Ω

2.5.5 RF VCO

Parameters	Conditions		Min	Typ	Max	Unit
Phase Noise at Transmit RF output	VCO only Offset = 100 KHz	Low-Band		-100		dBc/Hz
		High-Band		-95		
Integrated phase noise at RF output	PLL locked 10kHz - 10MHz	Low-Band		0.5		degree
		High-Band		1.0		
Tuning Sensitivity	Vc = 1.2V to 1.5V	Low-Band	80		123	MHz/V
		High-Band	88		164	

2.5.6 PLL

Parameters	Conditions	Min	Typ	Max	Unit
Operating frequency		2412	-	2484	MHz
Reference Oscillator Frequency	No load or loaded on X2		40	50	MHz
Reference Oscillator Sensitivity		0.5			Vpp
Phase Detector Frequency				50	MHz
Charge Pump Supply Voltage		2.7	-	3.6	V

3 Operation Mode

Mode	RF_PE	T/R_PE	EN (serial bus)	Status
PLL Disable State	x	x	0	Inactive PLL, active serial interface, disabled PLL registers.
Power Down State	0	0	1	Inactive PLL, active serial interface, register in save mode
PLL Active State	0	1	1	Inactive Tx and Rx. Active PLL and serial interface.
Receive State	1	1	1	Active Rx and PLL
Transmit State	1	0	1	Active Tx and PLL

Note:
1. PLL_PE is controlled via the PLL serial interface. The actual synthesizer control is a logic AND function of PLL_PE and the result of the logic OR function of RF_PE and T/R_PE

4 PLL FUNCTIONAL DESCRIPTIONS

Serial Data Input

Serial data is entered using three pins, Data, Clock, and CE pins. Serial data of binary data is entered through Data pin.
On a rising edge of clock, one bit of serial data is transferred into the shift register. On a rising edge of load enable signal, the data stored in the shift register is transferred to one of registers depending upon the control bit data setting.

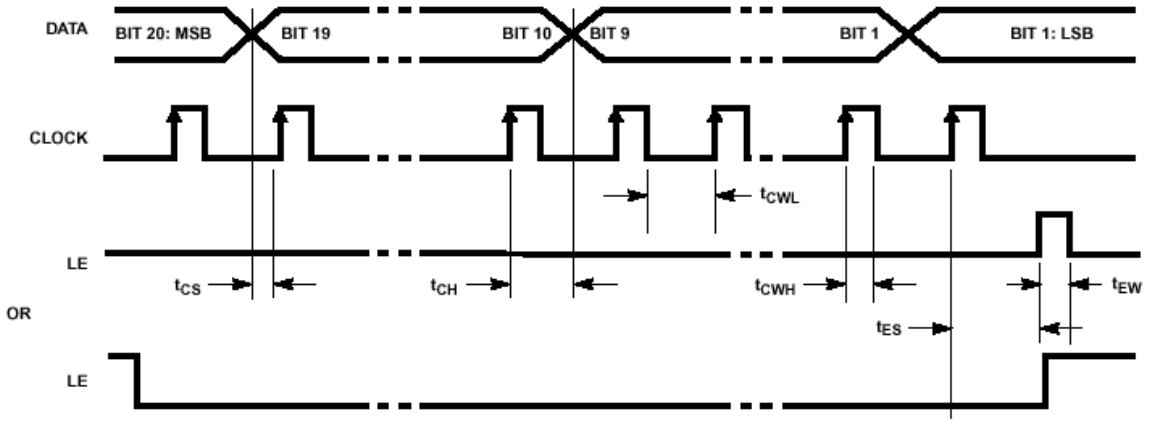


FIGURE 1. SERIAL DATA INPUT TIMING

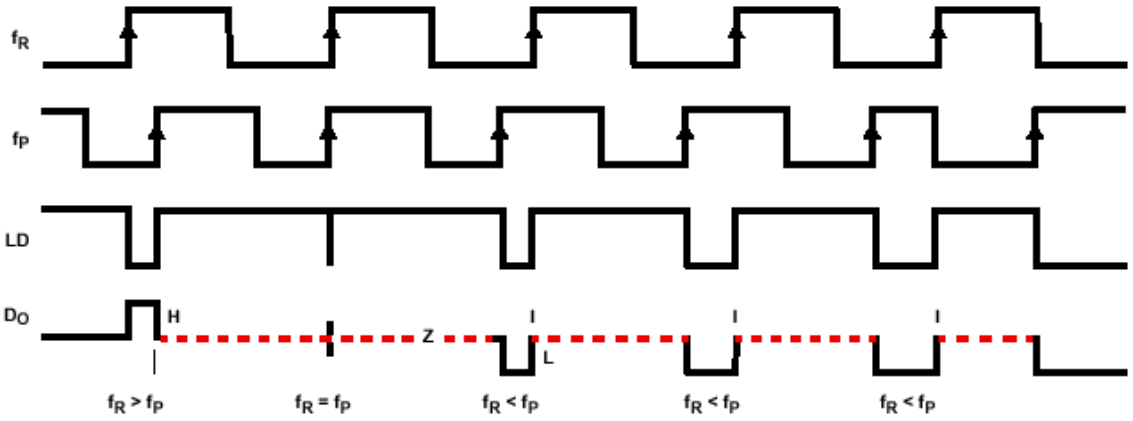
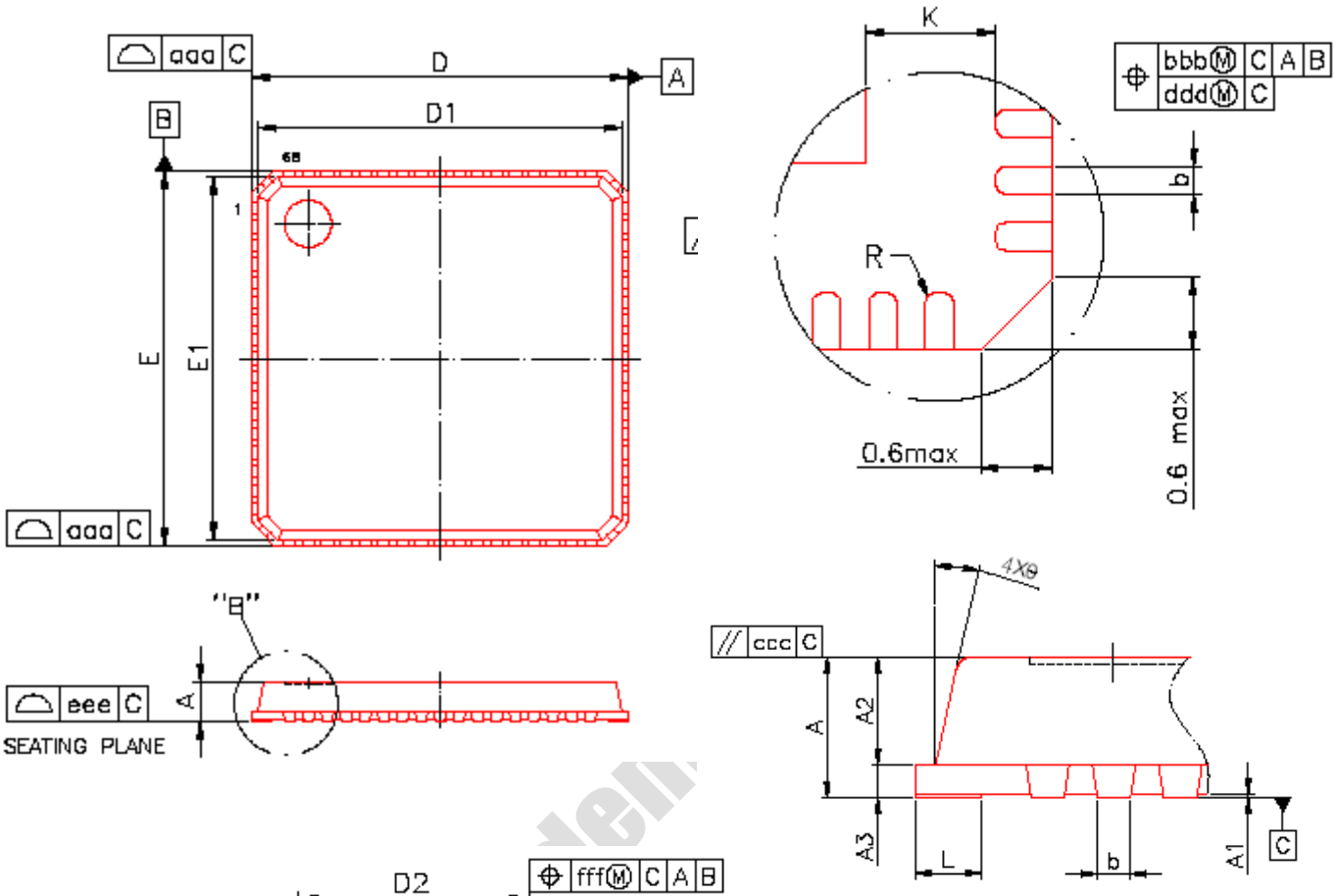
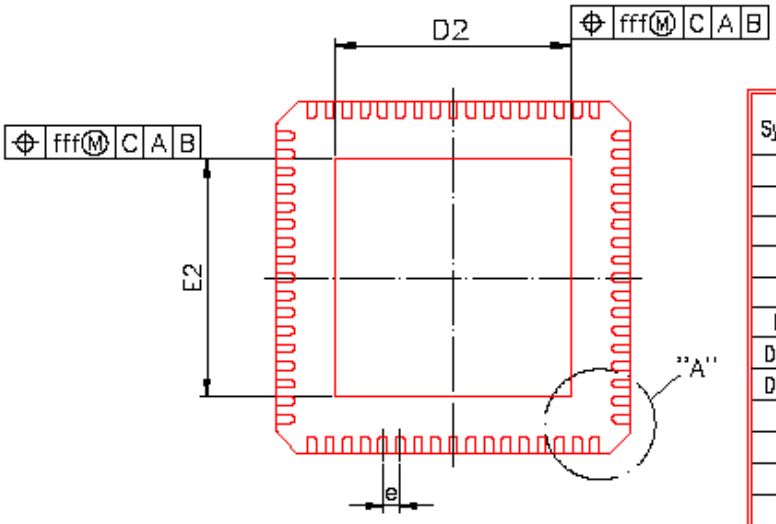


FIGURE 2. PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS

5 Package Physical Dimension

5.1 QFN 68L (8x8x0.9mm)





Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.80	0.024	0.026	0.031
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	8.00 BSC			0.315 BSC		
D1/E1	7.75 BSC			0.305 BSC		
D2/E2	5.20	5.35	5.50	0.205	0.211	0.217
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.075	---	---	0.003	---	---
K	0.20	---	---	0.008	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

6 Revision History

Rev	Date	From	Description
0.8	7/10/06	K. Fong	Create objective spec from RT2850B
0.9	7/26/06	D. Lo	Modify PLL registers.
1.0	7/28/06	K. Fong	Update package and pin info.
1.1	1/31/07	D. Lo	Preliminary data sheet
3.0	1/20/09	Allie Hsieh	Revise Maximum Junction Temperature