IEEE Draft P802.3af/D3.1

Supplement to
Information technology—
Telecommunications and information exchange between systems—
Local and metropolitan area networks—
Specific requirements—
Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications

Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)

Sponsor

LAN MAN Standards Committee
of the
IEEE Computer Society

Changes to ANSI/IEEE Std 802.3-2000, Clause 1

EDITORIAL NOTES - This supplement is based on the current edition of IEEE Std 802.3, 2000. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of IEEE P802.3af.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions.

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 3.1, June 2002	Inclusion in Working Group recirculation ballot draft.

1.1 Normative references

1.2 Definitions

Insert the following definitions at the end of section 1.4, the definitions must be renumbered appropriately after insertion.

1.2.1 Midspan: A location in a link segment that is distinctly separate from the MDIs.

1.2.2 Link Section: The point-to-point medium connection between an PD and a PSE.

1.3 Abbreviations

Insert the following item alphabetically in section 1.5.

PD	Powered Device
PSE	Power Sourcing Equipment
SELV	Safety Extra Low Voltage

Changes to ANSI/IEEE Std 802.3-2000, Clause 22

EDITORIAL NOTES - This supplement is based on the current edition of IEEE Std 802.3, 2000. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of IEEE P802.3af.

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Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 1.0, December 2001	Initial draft for review.
Draft 3.1, May 2002	Inclusion in Working Group recirculation ballot draft.

22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.2.4 Management functions

Change the third paragraph of this subclause as follows:

The MII basic register set consists of two registers referred to as the Control register (Register 0) and the Status register (Register 1). All PHYs that provide an MII shall incorporate the basic register set. All PHYs that provide a GMII shall incorporate an extended basic register set consisting of the Control register (Register 0), Status register (Register 1), and Extended Status register (Register 15). The status and control functions defined here are considered basic and fundamental to 100 Mb/s and 1000 Mb/s PHYs. Registers 2 through ~~10~~12 are part of the extended register set. The format of Registers 4 through 10 are defined for the specific Auto-Negotiation protocol used (Clause 28 or Clause 37). The format of these registers is selected by the bit settings of Registers 1 and 15.

Change the last Table 22-6 as follows:.

Table 22–6—MII management register set

Register address	Register name	Basic/Extended	
		MII	GMII
0	Control	B	B
1	Status	B	B
2,3	PHY Identifier	E	E
4	Auto-Negotiation Advertisement	E	E
5	Auto-Negotiation Link Partner Base Page Ability	E	E
6	Auto-Negotiation Expansion	E	E
7	Auto-Negotiation Next Page Transmit	E	E
8	Auto-Negotiation Link Partner Received Next Page	E	E
9	MASTER-SLAVE Control Register	E	E
10	MASTER-SLAVE Status Register	E	E
11	PSE Control register	E	E
12	PSE/PD Status register	E	E
~~11~~13 through 14	Reserved	E	E
15	Extended Status	Reserved	B
16 through 31	Vendor Specific	E	E

22.2.4.3 Extended capability registers

Change the first paragraph of this subclause as follows:

In addition to the basic register set defined in 22.2.4.1 and 22.2.4.2, PHYs may provide an extended set of capabilities that may be accessed and controlled via the MII management interface. Eleven~~Nine~~ registers have been defined within the extended address space for the purpose of providing a PHY-specific identifier to layer management, and to provide control and monitoring for the Auto-Negotiation process.

Add the following two new subclauses after subclause 22.2.4.3.8, renumber current subcluse 22.2.4.3.9 to be subcluse 22.2.4.3.11.

22.2.4.3.9 PSE Control register (Register 11)

Register 11 provides control bits that are used by a PSE. See 33.6.1.1.

22.2.4.3.10 PSE/PD Status register (Register 12)

Register 12 provides status bits that are supplied by a PSE and PD. See 33.6.1.2.

Changes to ANSI/IEEE Std 802.3-2000, Clause 30

EDITORIAL NOTES - This supplement is based on the current edition of IEEE Std 802.3, 2000 as modified by Draft 5.0 of IEEE P802.3ae, 10Gb/s Ethernet. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of IEEE P802.3af.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions.

Editors' Notes: *To be removed prior to final publication.*

References:

None.

Definitions:

1.4.??? Mid-Span PSE group: A PSE or collection PSE's that can be related to the logical arrangement of PSEs within a Mid-Span PSE.

Abbreviations:

None.

Revision History:

Draft 1.0, July 2001	Initial draft for review. This draft is based on the IETF Power Ethernet (DTE Power via MDI) MIB of June 2001 and the notes from the Management Ad Hoc meeting held 8th January (http://www.ieee802.org/3/af/public/documents/management_ad_hoc_report.pdf) at the IEEE P802.3af January 2001Interim meeting in Irvine, CA.
Draft 1.1, August 2001	Updates based. Change the enmeration "auto" and "off" to "enable" and "disable" in the attribute aPSEAdminState. Change attribute to read-only and add acPSEAdminControl. Add the acPSEAdminControl action to control the aPSEAdmin-State attribute. Add additional enumerations to aPSEPowerDetectionStatus Add new attributes aPSEPowerVoltageStatus and aPSEPower-Classification and new action acPSEPowerVoltageStatusClear.
Draft 3.1, May 2002	Draft 3.0 Working Group Ballot comments. Add oMidSpan and oMidSpanGroup managed Object Classes. Remove acPSEPowerCurrentStatusClear action and add aPSE-UnderCurrentCounter & aPSEOverCurrentCounter attributes.

30. 10 Mb/s, 100 Mb/s, 1000 Mb/s and 10 Gb/s Management

30.1 Overview

Change the first paragraph of this subclause as follows:

This clause provides the Layer Management specification for DTEs, repeaters, and MAUs based on the CSMA/CD access method. The clause is produced from the ISO framework additions to Clause 5, Layer Management; Clause 19, Repeater Management; and Clause 20, MAU Management. It incorporates additions to the objects, attributes, and behaviors to support 100 Mb/s, 1000 Mb/s and 10 Gb/s, full duplex operation, MAC Control, ~~and~~ Link Aggregation and DTE Power via MDI.

30.1.1 Scope

Change the first paragraph of this subclause as follows:

This clause includes selections from Clauses 5, 19, and 20. It is intended to be an entirely equivalent specification for the management of 10 Mb/s DTEs, 10 Mb/s baseband repeater units, and 10 Mb/s integrated MAUs. It also includes the additions for management of MAC Control, DTEs and repeaters at speeds greater than 10 Mb/s, embedded MAUs~~, and~~ /PHYs and DTE Power via MDI. Implementations of management for DTEs, repeater units, and embedded MAUs should follow the requirements of this clause (e.g., a 10 Mb/s implementation should incorporate the attributes to indicate that it is not capable of 100 or 1000 Mb/s operation~~;~~; half duplex DTE should incorporate the attributes to indicate that it is not capable of full duplex operation, etc.).

30.1.2 Relationship to objects in IEEE 802.1F

Change the second paragraph of this subclause as follows:

oMidSpan

This object class is mandatory and shall be implemented as defined in IEEE 802.1F. This object is bound to oMAC-Entity, oRepeater, oMidSpan and oMAU as defined by the NAMEBINDINGs in 30A.10.1. Note that the binding to oMAU is mandatory only when MII is present. The Entity Relationship Diagrams, figures 30–3 and 30–4, shows these bindings pictorially.

30.2.2.1 Text description of managed objects

Insert the following text immediately after the description of oWIS:

oMidSpan

The top-most managed object class of the Mid-Span PSE containment tree shown in Figure 30–4. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this standard.

oMidSpanGroup

The MidSpanGroup managed object class is a view of a collection of PSEs.

oPSE

The managed object of that portion of the containment tree shown in

Figure 30–3 and Figure 30–4. The attributes and actions defined in this subclause are contained within the oPSE managed object.

oPD

The managed object of that portion of the containment tree shown in Figure 30–3. The attributes and actions defined in this subclause are contained within the oPD managed object.

30.1.4 Management model

Change the second last paragraph of this subclause as follows:

The above items are defined in 30.3, 30.4, 30.5, 30.6, 30.7, ~~and~~ 30.8, 30.9 and 30.10 of this clause in terms of the template requirements of ISO/IEC 10165-4: 1991.

30.2.3 Containment

Change the first paragraph of this subclause as follows:

A containment relationship is a structuring relationship for managed objects in which the existence of a managed object is dependent on the existence of a containing managed object. The contained managed object is said to be the subordinate managed object, and the containing managed object the superior managed object. The containment relationship is used for naming managed objects. The local containment relationships among object classes are depicted in the entity relationship diagrams, Figure 30–3 and Figure 30–4. ~~This~~ These figures shows the names of the object classes and whether a particular containment relationship is one-to-one or one-to-many. For further requirements on this topic, see IEEE Std 802.1F-1993.

Change the Figure 30-3 as follows:

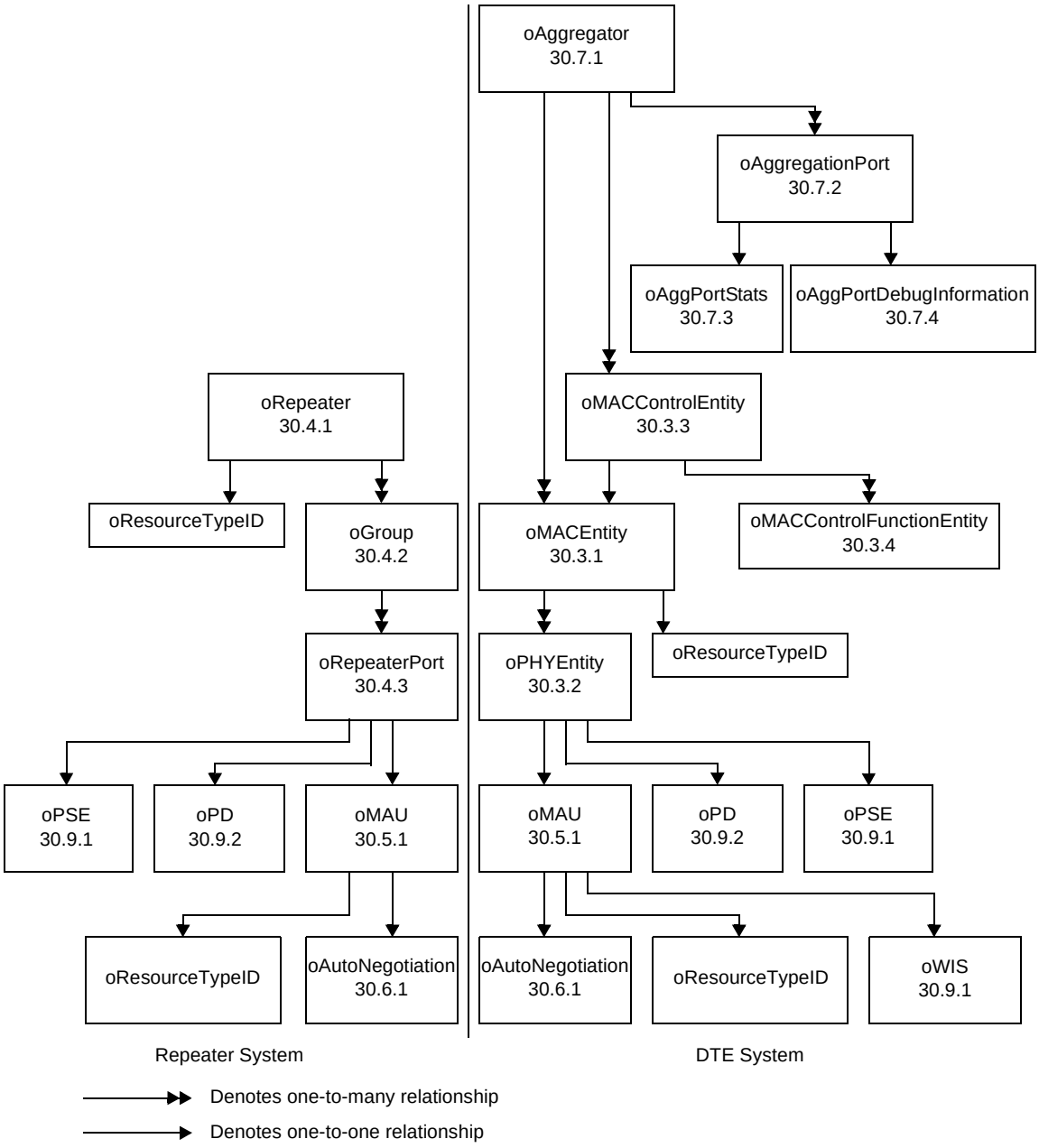


Figure 30–3—Repeater and DTE System eEntity relationship diagram

Add new Figure 30-4 as follows:

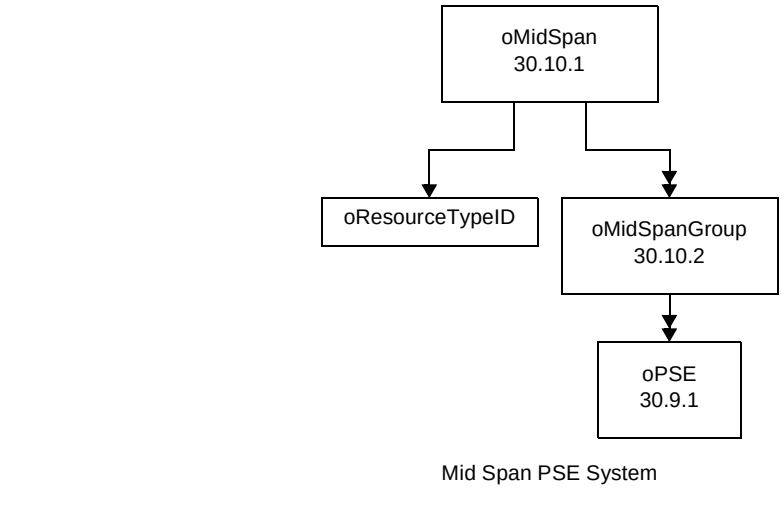


Figure 30–4—Mid-Span PSE system entity relationship diagram

30.2.5 Capabilities

Change the first paragraph of this subclause as follows:

This standard makes use of the concept of *packages* as defined in ISO/IEC 10165-4: 1992 as a means of grouping behaviour, attributes, actions, and notifications within a managed object class definition. Packages may either be mandatory, or be conditional, that is to say, present if a given condition is true. Within this standard *capabilities* are defined, each of which corresponds to a set of packages, which are components of a number of managed object class definitions and which share the same condition for presence. Implementation of the appropriate basic and mandatory packages is the minimum requirement for claiming conformance to IEEE 802.3 Management. Implementation of an entire optional capability is required in order to claim conformance to that capability. The capabilities and packages for IEEE 802.3 Management are specified in Tables 30–1, 30–2, ~~and~~ 30–3 and 30–4.

Insert the following paragraph at the end of this subclauses:

For Mid-Span PSE management, the Basic Capability shall be implemented in its entirety. All attributes and actions are notifications.

Insert the following new table after Table 30-3

Table 30–4—PSE and PD Capabilities

			PSE Basic Package (Mandatory)	PSE Recommended Package (Optional)	PD Basic Package (Mandatory)	PD Recommended Package (Optional)	Basic Capability (Mandatory)
oResourceTypeID managed object							
aResourceTypeIDName	ATTRIBUTE	GET					X
aResourceInfo	ATTRIBUTE	GET					X
oMidSpan managed object class (30.10.1)							
aMidSpanID	ATTRIBUTE	GET					X
aMidSpanGroupCapacity	ATTRIBUTE	GET					X
aMidSpanGroupMap	ATTRIBUTE	GET					X
nMidSpanGroupMapChange	NOTIFICATION						X
oMidSpanGroup managed object class (30.10.2)							
aMidSpanGroupID	ATTRIBUTE	GET					X
aPSECapacity	ATTRIBUTE	GET					X
aPSEMap	ATTRIBUTE	GET					X
nPSEMapChange	NOTIFICATION						X
oPSE managed object class (30.9.1)							
aPSEID	ATTRIBUTE	GET	X				
aPSEAdminState	ATTRIBUTE	GET	X				
aPSEPowerPairsControlAbility	ATTRIBUTE	GET		X			
aPSEPowerPairs	ATTRIBUTE	GET-SET		X			
aPSEPowerDetectionControl	ATTRIBUTE	GET-SET		X			
aPSEPowerDetectionStatus	ATTRIBUTE	GET		X			
aPSEPowerClassification	ATTRIBUTE	GET		X			
aPSEPowerCurrentStatus	ATTRIBUTE	GET		X			
aPSEUnderCurrentCounter	ATTRIBUTE	GET		X			
aPSEOverCurrentCounter	ATTRIBUTE	GET		X			
acPSEAdminControl	ACTION			X			
oPD managed object class (30.9.2)							
aPDID	ATTRIBUTE	GET			X		
aPDPowerStatus	ATTRIBUTE	GET				X	
Common Attributes Template							
aCMCounter	ATTRIBUTE	GET		X			

Insert the following new table after subclause 30.8

30.9 Management for Power Sourcing Equipment (PSE) and Powered Device (PD)

30.9.1 PSE managed object class

This subclause formally defines the behaviours for the oPSE managed object class, attributes and actions.

30.9.1.1 PSE attributes

30.9.1.1.1 aPSEID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aPSEID is assigned so as to uniquely identify a PSE among the subordinate managed objects of the containing object.;

30.9.1.1.2 aPSEAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

enable	PSE functions enabled
disable	PSE functions disabled

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of the PSE functions. An interface which can provide the PSE functions specified in Clause 33 will be enabled to do so when this attribute has the enumeration “enable”. When this attribute has the enumeration “disable” the interface will act as it would if it had no PSE function. The operational state of the PSE function can be changed using the acPSEAdminControl action. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Power Enable bit specified in 33.6.1.1.5.;

30.9.1.1.3 aPSEPowerPairsControlAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
Indicates the ability to control which PSE Pinout Alternative (see 33.2.1) is used for PD detection and power. When “true” the PSE Pinout Alternative used can be controlled through the aPSEPowerPairs attribute. When “false” the PSE Pinout Alternative used cannot be controlled through the aPSEPowerPairs attribute. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Pair Control Ability bit specified in 33.6.1.2.6;

30.9.1.1.4 aPSEPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

signal	PSE Pinout Alternative A
spare	PSE Pinout Alternative B

BEHAVIOUR DEFINED AS:

A read-write value that identifies the supported PSE Pinout Alternative specified in 33.2.1. A GET operation returns the PSE Pinout Alternative in use. A SET operation changes the PSE Pinout Alternative used to the indicated value only if the attribute aPSEPowerPairsControlAbility is "true". If the attribute aPSEPowerPairsControlAbility is "false" a SET operation has no effect.

The enumeration "signal" indicates that PSE Pinout Alternative A is used for PD detection and power. The enumeration "spare" indicates that PSE Pinout Alternative B is used for PD detection and power. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the detection status bits specified in 33.6.1.2.5.;

30.9.1.1.5 aPSEPowerDetectionControl

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

auto	PD detection normal
test	PD detection test mode

BEHAVIOUR DEFINED AS:

A read-write value that identifies the current mode of operation of the PD Detection function specified in 33.2.6. A GET operation returns the mode of operation of the PD Detection function. A SET operation changes the mode of operation of the PD Detection function to the indicated value.

The enumeration "auto" indicates that the PD Detection function is enabled. The enumeration "test" indicates that the PD Detection function is enabled, however, power shall not be supplied if a valid PD is detected. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Detection Control bits specified in 33.6.1.1.2.;

30.9.1.1.6 aPSEPowerDetectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

disabled	PD detection disabled
searching	PD detection searching
detected	Valid PD detected but power not supplied
deliveringPower	Valid PD detected and power supplied
fault	PD detection fault detected
invalidPD	Invalid PD detected
test	PD detection test mode
unknown	unknown PD detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 33.2.6.

The enumeration "disabled" indicates that the PD Detection function has been disabled. The enumeration "searching" indicates that the PD Detection function is enabled and is searching for a valid PD. The enumeration "detected" indicates that the PD Detection function has detected a valid PD but the PSE is not supplying power. The enumeration "deliveringPower" indicates that the PD Detection function has detected a valid PD and the PSE is supplying power. The

enumeration “fault” indicates that the PD Detection function has detected a PD Detection fault. Faults detected are vendor specific. The enumeration “invalidPD” indicates that the PD Detection function has detected an invalid PD. The enumeration “test” indicates that the PD Detection function has been placed in test mode. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Detection Status bits specified in 33.6.1.2.5.;

30.9.1.1.7 aPSEPowerClassification

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

class0	Class 0 PD
class1	Class 1 PD
class2	Class 2 PD
class3	Class 3 PD
class4	Class 4 PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the PD Class of a detected PD as specified in 33.2.7. The value is only valid while a valid PD is being detected, as indicated by the attribute aPSEPowerDetectionStatus reporting the enumeration “detected” or “deliveringPower”.

If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PD Class bits specified in 33.6.1.2.4.;

30.9.1.1.8 aPSEPowerCurrentStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

ok	current normal
underCurrent	undercurrent condition has been detected
overCurrent	overcurrent condition has been detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Power Supply function specified in 33.6.1.1.

The enumeration “ok” indicates neither an undercurrent nor an overcurrent condition has been detected. The enumeration “underCurrent” indicates an undercurrent condition has been detected. The enumeration “overCurrent” indicates an overcurrent condition has been detected.

An undercurrent condition is detected when the current drawn from the PSE at the MDI is less than Off-mode current 2 for a duration greater than Under load time limit. An overcurrent condition is detected when the current drawn from the PSE at the MDI is greater than the Overload current limit for a duration greater than Overload time limit. The values Overload current limit, Overload time limit, Off-mode current 2 and Under load time limit are specified in Table 33-5. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Undercurrent and Overcurrent bits specified in 33.6.1.2.3 and 33.6.1.2.2.;

30.9.1.1.9 aPSEUnderCurrentCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second

BEHAVIOUR DEFINED AS:

Counts the number of times that the aPSEPowerCurrentStatus attribute changes from any enumeration to the enumeration “underCurrent ”.;

30.9.1.1.10 aPSEOverCurrentCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 20 counts per second

BEHAVIOUR DEFINED AS:

Counts the number of times that the aPSEPowerCurrentStatus attribute changes from any enumeration to the enumeration “overCurrent ”.;

30.9.1.2 PSE actions

30.9.1.2.1 acPSEAdminControl

ACTION

APPROPRIATE SYNTAX:

Same as aPSEAdminState

BEHAVIOUR DEFINED AS:

This action provides a means to alter aPSEAdminState.

30.9.2 PD managed object class

This subclause formally defines the behaviours for the oPD managed object class and attributes.

30.9.2.1 PD attributes

30.9.2.1.1 aPDID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aPDID is assigned so as to uniquely identify a PD among the subordinate managed objects of the containing object.;

30.9.2.1.2 aPDPowerStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

off	PD not receiving Power
receivingPower	PD receiving Power

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the Power Pair Status bits specified in

33.6.1.2.7.

The enumeration “off” indicates that the PD is drawing a current less than the minimum value of I_{Port} as specified in Table 33–13. The enumeration “receivingPower” indicates that the PD is drawing a current greater than the minimum value of I_{Port} as specified in Table 33–13. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Power Pair Status bits specified in 33.6.1.2.7.;

30.10 Layer management for Mid-Span Power Sourcing Equipment (PSE)

30.10.1 Mid-Span PSE managed object class

This subclause formally defines the behaviours for the oMidSpan managed object class, attributes and notifications.

30.10.1.1 Mid-Span PSE attributes

30.10.1.1.1 aMidSpanID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMidSpanID is assigned so as to uniquely identify a Mid-Span PSE among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2: 1992 [SMI], Definition of management information).;

30.10.1.1.2 aMidSpanGroupCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aMidSpanGroupCapacity is the number of Mid-Span PSE groups that can be contained within the Mid-Span PSE. Within each managed Mid-Span PSE, the Mid-Span PSE groups are uniquely numbered in the range from 1 to aMidSpanGroupCapacity.

Some Mid-Span PSE groups may not be present in a given Mid-Span PSE instance, in which case the actual number of Mid-Span PSE groups present is less than aMidSpanGroupCapacity. The number of Mid-Span PSE groups present is never greater than aMidSpanGroupCapacity.;

30.10.1.1.3 aMidSpanGroupMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
A string of bits which reflects the current configuration of units that are viewed by Mid-Span PSE group managed objects. The length of the bitstring is “aMidSpanGroupCapacity” bits. The first bit relates to Mid-Span PSE group 1. A “1” in the bitstring indicates presence of the Mid-Span PSE

group, “0” represents absence of the Mid-Span PSE group.;

30.10.1.2 Mid-Span PSE notifications

30.10.1.2.1 nMidSpanGroupMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the Mid-Span PSE group structure of a Mid-Span PSE. This occurs only when a Mid-Span PSE group is logically removed from or added to a Mid-Span PSE. The nMidSpanGroupMapChange notification is not sent when powering up a Mid-Span PSE. The value of the notification is the updated value of the aMidSpanGroupMap attribute.;

30.10.2 Mid-Span PSE Group managed object class

This subclause formally defines the behaviours for the oMidSpanGroup managed object class, attributes, actions, and notifications.

30.10.2.1 Mid-Span PSE Group attributes

30.10.2.1.1 aMidSpanGroupID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A value unique within the Mid-Span PSE. The value of aMidSpanGroupID is assigned so as to uniquely identify a Mid-Span PSE group among the subordinate managed objects of the containing object (oMidSpan). This value is never greater than aMidSpanGroupCapacity.;

30.10.2.1.2 aPSECapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aMidSpanGroupPSECapacity is the number of PSEs contained within the Mid-Span PSE group. Valid range is 1-1024. Within each Mid-Span PSE group, the PSEs are uniquely numbered in the range from 1 to aMidSpanGroupPSECapacity. Some PSEs may not be present in a given Mid-Span PSE group instance, in which case the actual number of PSEs present is less than aMidSpanGroupPSECapacity. The number of PSEs present is never greater than aMidSpanGroupPSECapacity.;

30.10.2.1.3 aPSEMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:

A string of bits that reflects the current configuration of PSE managed objects within this Mid-Span PSE group. The length of the bitstring is "aMidSpanGroupPSECapacity" bits. The first bit relates to PSE 1. A "1" in the bitstring indicates presence of the PSE, "0" represents absence of the PSE.;

30.10.2.2 Mid-Span PSE Group notifications

30.10.2.2.1 nPSEMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the PSE structure of a Mid-Span PSE group. This occurs only when a PSE is logically removed from or added to a Mid-Span PSE group. The nMidSpanPSEMapChange notification is not sent when powering up a Mid-Span PSE. The value of the notification is the updated value of the aMidSpanPSEMap attribute.;

Changes to ANSI/IEEE Std 802.3-2000, Annex 30A and 30B

EDITORIAL NOTES - This supplement is based on the current edition of IEEE Std 802.3, 2000 as modified by Draft 5.0 of IEEE P802.3ae, 10Gb/s Ethernet. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3af.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions.

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 1.1, December 2001	Initial draft for review.
Draft 3.1, May 2002	Draft 3.0 Working Group Ballot related comments. Add oMidSpan and oMidSpanGroup managed Object Classes. Remove acPSEPowerCurrentStatusClear action and add aPSE-UnderCurrentCounter & aPSEOverCurrentCounter attributes.

Annex 30A

(normative)

GDMO specification for 802.3 managed object classes

Editor's Note: *to be removed prior to final publication.*
Any values of OBJECT IDENTIFIER required to complete these GDMO definition will be allocated when this draft is issued for Sponsor ballot.

Change the first paragraph of this annex as follows:

This annex formally defines the protocol encodings for CMIP and ISO/IEC 15802-2: 1995 [ANSI/IEEE Std 802.1B and 802.1k, 1995 Edition] for the IEEE 802.3 Managed Objects using the templates specified in ISO/IEC 10165-4: 1992. The application of a GDMO template compiler against 30A.1 to ~~30A.15~~30A.19 will produce the proper protocol encodings.

30A.10.1 ResourceTypeID, formal definition

Insert the following paragraph at the end of this subclauses:

nbResourceTypeID-midSpan **NAME BINDING**

SUBORDINATE OBJECT CLASS “IEEE802.1F”:oResourceTypeID;
NAMED BY SUPERIOR OBJECT CLASS oMidSpan AND SUBCLASSES;
WITH ATTRIBUTE aMidSpanID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) ResourceTypeID-midSpan(??)};

Insert the following subclauses after subclause 30A.15.2:

30A.16 PSE managed object class

30A.16.1 PSE, formal definition

oPSE **MANAGED OBJECT CLASS**

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;

CHARACTERIZED BY
pPSEBasic PACKAGE
ATTRIBUTES aPSEID GET,
aPSEAdminState GET;
;
;
CONDITIONAL PACKAGES
pPSERecommended PACKAGE
ATTRIBUTES aPSEPowerPairsControlAbility GET,
aPSEPowerPairs GET-REPLACE,
aPSEPowerDetectionControl GET-REPLACE,

```
                                    aPSEPowerDetectionStatus    GET,
                                    aPSEPowerClassification     GET,
                                    aPSEPowerCurrentStatus      GET,
                                    aPSEUnderCurrentCounter     GET,
                                    aPSEOverCurrentCounter      GET;
            ACTIONS                 acPSEAdminControl;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30) package(4)
                                    pseRecommendedPkg(??)};
            PRESENT IF              The recommended package is implemented;
    REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            managedObjectClass(3) pseObjectClass(??)};

nbPSE-repeaterName          NAME BINDING

    SUBORDINATE OBJECT CLASS        oPSE;
    NAMED BY SUPERIOR OBJECT CLASS  oRepeaterPorts AND SUBCLASSES;
    WITH ATTRIBUTE                  aPSEID;
    REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            nameBinding(6) pse-repeaterName(??)};

nbPSE-dteName               NAME BINDING

    SUBORDINATE OBJECT CLASS        oPSE;
    NAMED BY SUPERIOR OBJECT CLASS  oPHYEntity AND SUBCLASSES;
    WITH ATTRIBUTE                  aPSEID;
    REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            nameBinding(6) pse-dteName(??)};

nbPSE-midSpanName           NAME BINDING

    SUBORDINATE OBJECT CLASS        oPSE;
    NAMED BY SUPERIOR OBJECT CLASS  oMidSpanGroup AND SUBCLASSES;
    WITH ATTRIBUTE                  aPSEID;
    REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            nameBinding(6) pse-midSpanName(??)};
```

30A.16.2 PSE attributes

```
aPSEID                      ATTRIBUTE

    WITH ATTRIBUTE SYNTAX           IEEE802Dot3-MgmtAttributeModule.OneOfName;
    MATCHES FOR                     EQUALITY;
    BEHAVIOUR                       bPSEID;
    REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            attribute(7) pseID(???)};

bPSEID                      BEHAVIOUR

    DEFINED AS              See “BEHAVIOUR DEFINED AS” in 30.9.1.1.1;
```

aPSEAdminState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PortAdminState;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pseAdminState(???)};

bPSEAdminState **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.2;

aPSEPowerPairsControlAbility **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PairCtrlAbility;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEPowerPairsControlAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) psePowerPairsControlAbility(???)};

bPSEPowerPairsControlAbility **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.3;

aPSEPowerPairs **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PSEPowerPairs;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEPowerPairs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) psePowerPairs(???)};

bPSEPowerPairs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.4;

aPSEPowerDetectionControl **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.DetectControl;
MATCHES FOR EQUALITY, ORDERING **????**;
BEHAVIOUR bPSEPowerDetectionControl;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) psePowerDetectionControl(???)};

bPSEPowerDetectionControl **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.5;

aPSEPowerDetectionStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.DetectStatus;

MATCHES FOR EQUALITY;
BEHAVIOUR bPSEPowerDetectionStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) psePowerDetectionStatus(???)};

bPSEPowerDetectionStatus BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.9.1.1.6;

aPSEPowerClassification ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PowerClass;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEPowerClassification;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) psePowerClassification(???)};

bPSEPowerClassification BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.9.1.1.7;

aPSEPowerCurrentStatus ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.CurrentStatus;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEPowerCurrentStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) psePowerCurrentStatus(???)};

bPSEPowerCurrentStatus BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.9.1.1.8;

aPSEUnderCurrentCounter ATTRIBUTE

WITH ATTRIBUTE SYNTAX aCMCounter;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEUnderCurrentCounter;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pseUnderCurrentCounter(???)};

bPSEUnderCurrentCounter BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.9.1.1.9;

aPSEOverCurrentCounter ATTRIBUTE

WITH ATTRIBUTE SYNTAX aCMCounter;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEUnderCurrentCounter;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pseOverCurrentCounter(???)};

bPSEOverCurrentCounter **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.1.10;

30A.16.3 PSE actions

acPSEAdminControl **ACTION**

BEHAVIOUR bPSEAdminControl;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) PSEAdminControl(??)};

bPSEAdminControl **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.1.2.1;

30A.17 PD managed object class

30A.17.1 PD, formal definition

oPD **MANAGED OBJECT CLASS**

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;
CHARACTERIZED BY
pPDBasic PACKAGE
ATTRIBUTES aPDID GET;
;
;
CONDITIONAL PACKAGES
pPDRecommended PACKAGE
ATTRIBUTES aPDPowerStatus GET;
REGISTERED AS
{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) pdRecommendedPkg(??)};
PRESENT IF The recommended package is implemented;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) pdObjectClass(??)};

nbPD-repeaterName **NAME BINDING**

SUBORDINATE OBJECT CLASS oPD;
NAMED BY SUPERIOR OBJECT CLASS oRepeaterPorts AND SUBCLASSES;
WITH ATTRIBUTE aPDID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) pd-repeaterName(??)};

nbPD-dteName **NAME BINDING**

SUBORDINATE OBJECT CLASS oPD;
NAMED BY SUPERIOR OBJECT CLASS oPHYEntity AND SUBCLASSES;

WITH ATTRIBUTE aPDID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) pd-dteName(??)};

30A.17.2 PD attributes

aPDID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bPDID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pdID(???)};

bPDID **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.2.1.1;

aPDPowerStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PowerStatus;
MATCHES FOR EQUALITY, ORDERING **????**;
BEHAVIOUR bPDPowerStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pdPowerStatus(???)};

bPDPowerStatus **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.9.2.1.2;

30A.18 Mid-Span managed object class

oMidSpan **MANAGED OBJECT CLASS**

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;
CHARACTERIZED BY
midSpanBasic PACKAGE
ATTRIBUTES aMidSpanID GET,
aMidSpanGroupCapacity GET,
aMidSpanGroupMap GET;
NOTIFICATIONS nMidSpanGroupMapChange;
;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) midSpanObjectClass(??)};

nbMidSpanName **NAME BINDING**

SUBORDINATE OBJECT CLASS oMidSpan;
NAMED BY SUPERIOR OBJECT CLASS “ISO/IEC 10165-2 ”:system AND SUBCLASSES;
WITH ATTRIBUTE aMidSpanID;

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) midSpanName(??)};

nbMidSpanMonitor NAME BINDING

SUBORDINATE OBJECT CLASS "IEEE802.1F ":oEWMAMetricMonitor;
NAMED BY SUPERIOR OBJECT CLASS "ISO/IEC 10165-2 ":system AND SUBCLASSES;
WITH ATTRIBUTE aScannerId;
CREATE WITH-AUTOMATIC-INSTANCE-NAMING;
DELETE ONLY-IF-NO-CONTAINED-OBJECTS;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) midSpanMonitor(??)};

30A.18.1 Mid-Span PSE attributes

aMidSpanID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bMidSpanID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) midSpanID(???)};

bMidSpanID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.10.1.1.1;

aMidSpanGroupCapacity ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY,ORDERING;
BEHAVIOUR bMidSpanGroupCapacity;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) midSpanGroupCapacity(???)};

bMidSpanGroupCapacity BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.10.1.1.2;

aMidSpanGroupMap ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
MATCHES FOR EQUALITY;
BEHAVIOUR bMidSpanGroupMap;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) midSpanGroupMap(???)};

bMidSpanGroupMap BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.10.1.1.3;

30A.18.2 Mid-Span PSE notifications

nMidSpanGroupMapChange **NOTIFICATION**

BEHAVIOUR bMidSpanGroupMapChange;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10)midSpanGroupMapChange(???)};

bMidSpanGroupMapChange **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.10.1.2.1;

30A.19 Mid-Span managed object class

oMidSpanGroup **MANAGED OBJECT CLASS**

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;
CHARACTERIZED BY
midSpanBasic PACKAGE
ATTRIBUTES aMidSpanGroupID GET,
aPSECapacity GET,
aPSEMap GET;
NOTIFICATIONS nPSEMapChange;
;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) midSpanGroupObjectClass(??)};

nbMidSpanGroupName **NAME BINDING**

SUBORDINATE OBJECT CLASS oMidSpanGroup;
NAMED BY SUPERIOR OBJECT CLASS oMidSpan AND SUBCLASSES;
WITH ATTRIBUTE aMidSpanGroupID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) midSpanGroupName(??)};

30A.19.1 Mid-Span PSE Group attributes

aMidSpanGroupID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bMidSpanGroupID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) midSpanGroupID(???)};

bMidSpanGroupID **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.10.2.1.1;

aPSECapacity **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY,ORDERING;
BEHAVIOUR bPSECapacity;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pseCapacity(???)};

bPSECapacity **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.10.2.1.2;

aPSEMap **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
MATCHES FOR EQUALITY;
BEHAVIOUR bPSEMap;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pseMap(???)};

bPSEMap **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.10.2.1.3;

30A.19.2 Mid-Span PSE Group notifications

nPSEMapChange **NOTIFICATION**

BEHAVIOUR bPSEMapChange;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10)pseMapChange(???)};

bPSEMapChange **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.10.2.2.1;

Annex 30B

(normative)

GDMO and ASN.1 definitions for management

30B.2 ASN.1 module for CSMA/CD managed objects

Insert the following ASN.1 definitions into the ASN.1 module, in appropriate alphabetic sequence:

```
CurrentStatus :: = ENUMERATED {
    ok                  (0),    -- current normal
    underCurrent        (1),    -- under current detected
    overCurrent         (2),    -- over current detected
    both                (3)     -- underand over current detected
    }

DetectControl ::= ENUMERATED {
    auto                (0),    -- PD detection normal
    test                (1)     -- PD detection test mode
    }

DetectStatus :: = ENUMERATED {
    disabled            (0),    -- PD detection disabled
    searching           (1),    -- PD detection searching
    detected            (2),    -- Valid PD detected but power not supplied
    deliveringPower     (3),    -- Valid PD detected and power supplied
    fault               (4),    -- PD detection fault detected
    invalidPD           (5),    -- Invalid PD detected
    test                (6)     -- PD detection test mode
    }

PairCtrlAbility ::=BOOLEAN

PDPowerPairs ::= ENUMERATED {
    signal              (0),    -- PD Pinout Mode A
    spare               (1),    -- PD Pinout Mode B
    both                (2)     -- PD Pinout Mode A and B
    }

PowerClass :: = ENUMERATED {
    class0              (0),    -- Class 0 PD
    class1              (1),    -- Class 1 PD
    class2              (2),    -- Class 2 PD
    class3              (3),    -- Class 3 PD
```

```
        class4              (4)     -- Class 4 PD
        }


    PowerStatus :: = ENUMERATED {
        off                 (0),    -- PD not receiving Power
        receivingPower      (1)     -- PD receiving Power
        }


    PSEPowerPairs ::= ENUMERATED {
        signal              (0),    -- PSE Pinout Alternative A
        spare               (1)     -- PSE Pinout Alternative B
        }
```

33. Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)

33.1 Overview

This clause defines an optional power sublayer for use with existing physical layers as defined in Clauses 14, 25 and 40. This additional sublayer allows data terminal equipment to draw power from the same generic cabling as that used for data transmission. This clause is optional only in the sense that systems may or may not employ powering via the MDI. All implementations of the twisted-pair link shall be compatible at the MDI. Designers are free to implement circuitry within the PD and PSE (in an application-dependent manner) provided the MDI specifications are met.

DTE powering is intended to provide a 10BASE-T, 100BASE-TX or 1000BASE-T device with a simple interface to both the data it requires and the power to process these data. In a single link, the user will both power and link devices that are compliant. To this end, this clause specifies:

a) a power source to add power to the 100 Ω balanced cabling system,
b) the characteristics of a powered device's load on the power source and the structured cabling,
c) a protocol allowing for detecting a device that requires power, and
d) optionally, a method to classify devices based on their power needs.

The importance of item "c" above should not be overlooked. Given the large number of legacy devices (both 802.3 and other types of devices) that could be connected to a 100 Ω balanced cabling system, and the possible consequences of powering such devices, the protocol to distinguish compatible devices and non-compatible devices should not be undervalued.

This clause differentiates between the two ends of the link, defining the power sourcing equipment (PSE) and the powered device (PD) as separate but intimately related devices. The reader is advised that while each device is defined separately, they can only truly be understood by learning both.

33.1.1 Terminology

Without regard to this clause's name "DTE Power via MDI", any device which contains an MDI compliant with Clause 14, Clause 25 and / or Clause 40, and sinks and / or sources power in accordance with the specifications of this clause shall be permitted.

33.1.2 Goals and Objectives

Power via MDI, as described in this clause, provides the following:

Power - Powered Devices designed to the standard and within its range of available power may require no additional connection other than the MDI to obtain power and data for operation.

Safety - Power Sourcing Equipment designed to the standard will not introduce non-SELV (safety extra low voltage) power into the wiring plant.

Compatibility - Clause 33 utilizes the existing MDIs of 10BASE-T, 100BASE-TX, and 1000BASE-T without modification and adds no significant requirements to the cabling. The use of other 802.3 MDIs is considered beyond the scope of this specification.

Simplicity - The powering system described here is no more burdensome on the end users than the requirements of 10BASE-T, 100BASE-TX, or 1000BASE-T.

33.1.3 Relationship of Power via MDI in the IEEE 802.3 Architecture

Power via MDI comprises an optional sublayer between the Physical Layer and the Medium in the OSI Reference Model and the CSMA/CD layer architecture. Figure 33–1 depicts the positioning of the Power via MDI sublayer in the case of the PD.

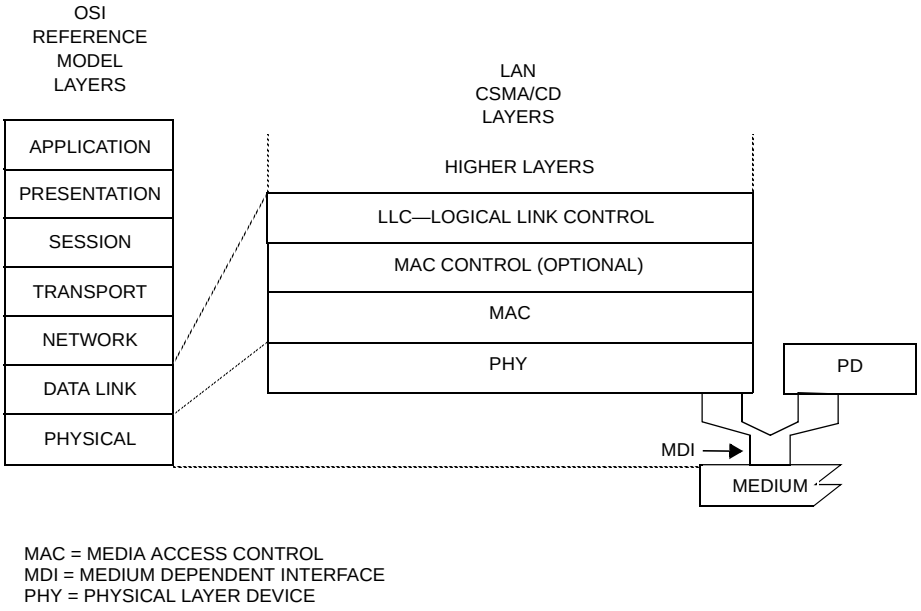


Figure 33–1—DTE Power via MDI Powered Device (PD) relationship to the ISO/IEC Open Systems Interconnect (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

Figure 33–2 and Figure 33–3 depict the positioning of the Power via MDI sublayer in the cases of the end-point PSE and the midspan PSE, respectively.

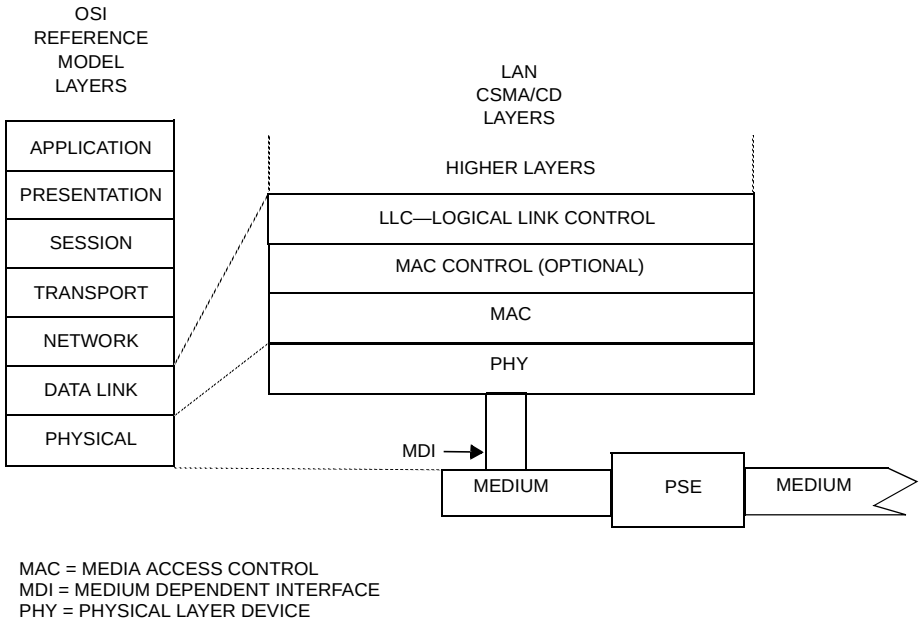


Figure 33–2—DTE Power via MDI Midspan Power Sourcing Equipment (PSE) relationship to the ISO/IEC Open Systems Interconnect (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

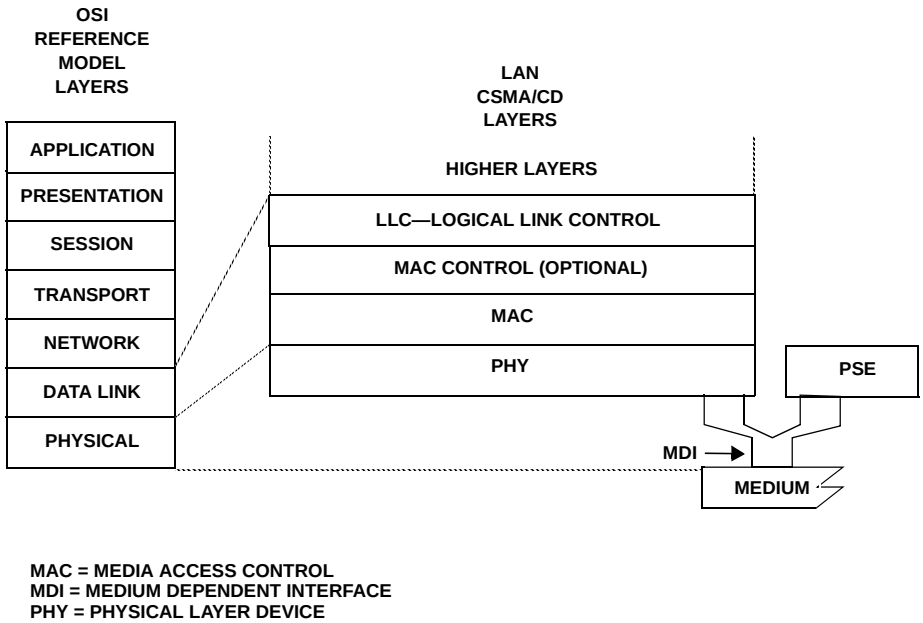


Figure 33–3—DTE Power via MDI Endpoint Power Sourcing Equipment (PSE) relationship to the ISO/IEC Open Systems Interconnect (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

33.2 Power sourcing equipment

Power sourcing equipment (PSE), as the name implies, is the equipment that provides the power to the link section. The PSE's main functions are to search the link segment for a PD, detect a PD, optionally classify the PD, supply power to the link segment, monitor the power on the link segment, and remove power from the link segment.

A PSE is electrically specified at the point of the physical connection to the cabling. Characteristics such as the losses due to overvoltage protection circuits, power supply inefficiencies, etc., after the MDI connector are not accounted for in this specification.

For the purposes of this document, a single MDI is discussed. Where specific requirements of multiple MDIs are stated, requirements are to be extended to all ports of a multi-port PSE.

33.2.1 MDI pin assignments

A PSE device may provide power via one of two valid four-wire connections. In each four-wire connection, the two wires associated with a pair carry the same nominal current in each conductor. The diagram Figure 33–4, in conjunction with Table 33–1, illustrates the valid alternatives.

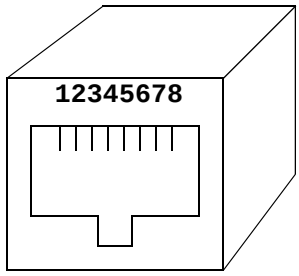


Figure 33–4—PD and PSE eight-pin modular jack

For the purposes of data transfer, the type of PSE data port is relevant to the far end PD and in some cases to the cabling system between them. Therefore, alternative A matches the positive voltage to the TD pair. Automatically-configuring MDI/MDI-X PSEs are assigned the polarity choice associated with MDI-X configurations. Alternative B does not have such an association.

A PSE shall implement alternative A, or alternative B, or both. The ordering of the alternatives should not be construed as a preference of implementation. Implementers are free to implement either alternative or both. While a PSE may be capable of both alternative A and alternative B, PSEs shall not operate both alternative A and alternative B on the same link segment simultaneously.

33.2.2 PSE location

PSEs may be placed in two locations with respect to the link segment, either coincident with the MDI or midspan. PSEs that are coincident with the MDI are said to be "Endpoint PSE". PSEs which are located midspan are said to be "Midspan PSE". The requirements of this document shall apply equally to Endpoint and Midspan PSE unless the requirement contains an explicit statement that it applies to only one implementation.

Endpoint PSEs may support either alternative A or B, or both, as described in 33.2.1. Endpoint PSEs can be compatible with 10BASE-T, 100BASE-TX or 1000BASE-T.

Table 33–1—PSE Pinout Alternatives

Conductor	Alternative A MDI-X or Auto-MDI-X	Alternative A MDI	Alternative B All
1	Negative V_{Port}	Positive V_{Port}	
2	Negative V_{Port}	Positive V_{Port}	
3	Positive V_{Port}	Negative V_{Port}	
4			Positive V_{Port}
5			Positive V_{Port}
6	Positive V_{Port}	Negative V_{Port}	
7			Negative V_{Port}
8			Negative V_{Port}

Midspan PSEs shall use alternative B as described in 33.2.1. Midspan PSEs are limited to operation with 10BASE-T and 100BASE-TX systems. Operation of Midspan PSEs on 1000BASE-T systems is considered beyond the scope of this standard.

33.2.3 PSE state diagram

The state diagram of the PSE is shown in Figure 33–5.

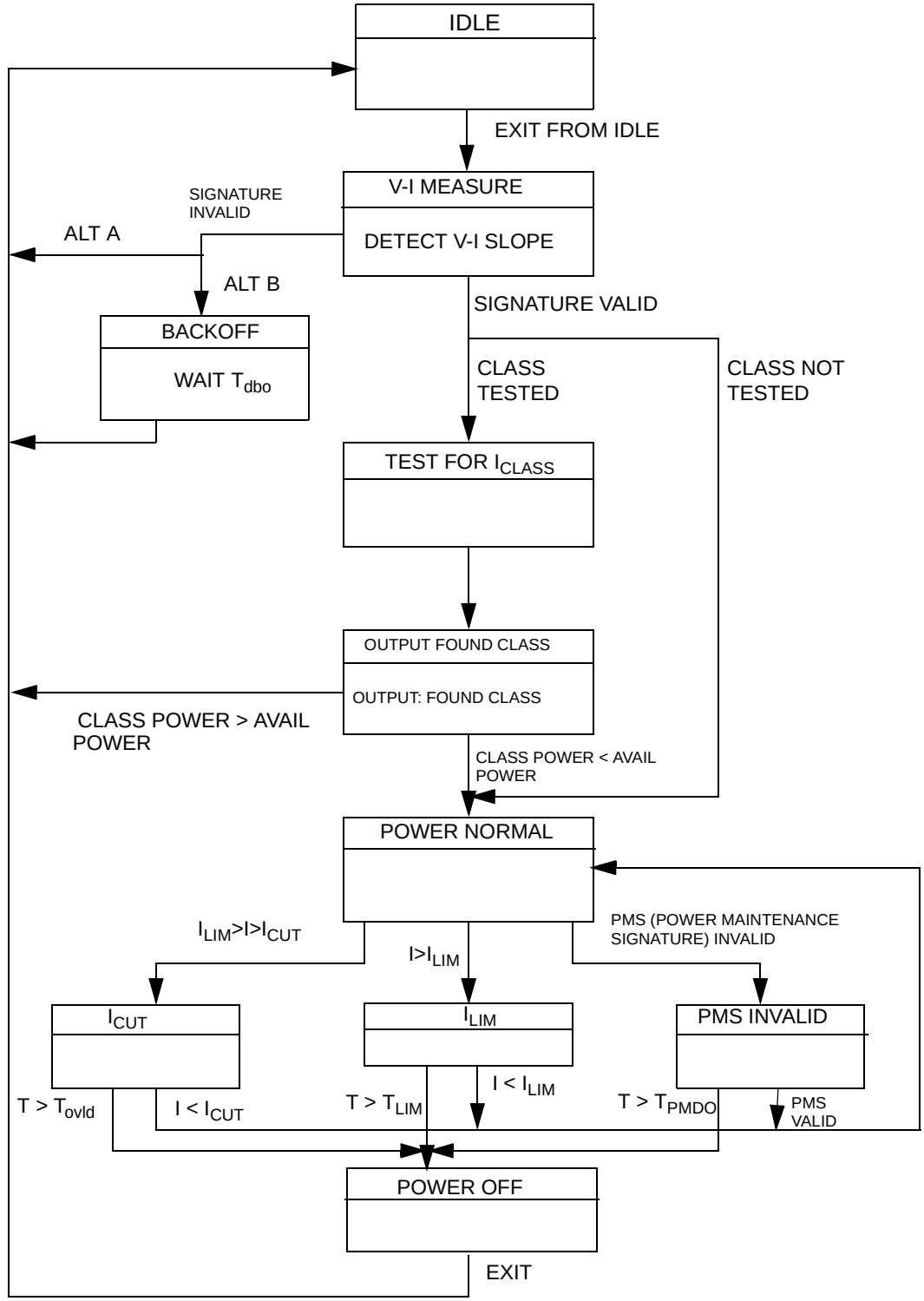


Figure 33–5—PSE state diagram

33.2.4 PD detection

The PSE shall not apply operating power to the MDI until it has successfully detected a PD requesting power as described in this section.

The PSE is not required to probe the link segment in order to detect a PD that presents a valid signature. For any number of reasons the PSE may not be attempting to detect a PD for a period of time. This period of time is implementation dependent. Also, a PSE may successfully detect a PD, but may then not power the detected PD.

PD detection shall operate without regard to data link status. Power may be requested by a PD that is already operating the link segment for data communications, or may be requested by a PD that is not yet operational.

33.2.5 PSE validation circuit

The PSE shall detect the PD by probing via the PSE MDI interface. The Thevenin equivalent of the detection circuit is shown in Figure 33–6. PSE requirements are stated for a Thevenin circuit only; they may be transformed via circuit theory into other circuit parameters in specific implementations.

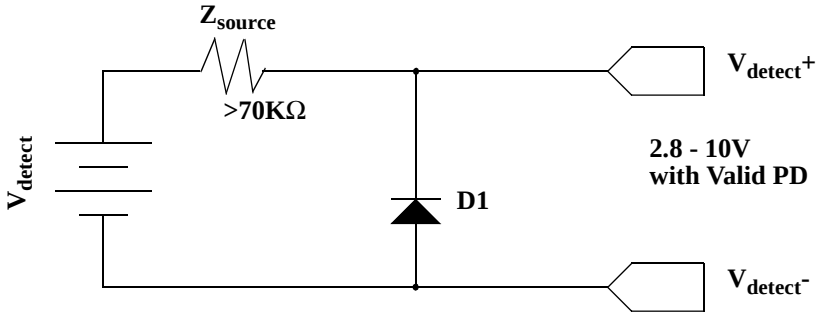


Figure 33–6—PSE detection source

A functional equivalent of the detection circuit that has no source impedance limitation, but restricts the PSE detection circuit to the first quadrant, is shown in Figure 33–7.

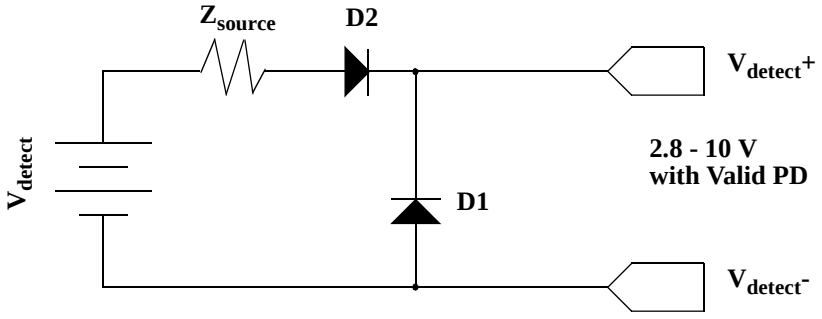


Figure 33–7—Alternative PSE detection source

In Figure 33–6 and Figure 33–7, diode D1 protects the PSE against reversed voltages when two PSE devices are connected together.

The open circuit voltage shall be less than 30 V. The short circuit current shall be less than 5 mA. Output capacitance shall be as specified in Table 33–5. The PSE shall exhibit Thevenin equivalence to one of the detection circuits shown in Figure 33–6 or Figure 33–7 in all detection states.

33.2.5.1 Detection probe requirements

The detection voltage V_{detect} shall create a voltage of 2.8 to 10 V with a valid PD signature connected. The PSE shall make at least two measurements with V_{detect} values that will create at least a 1 V difference between the two measurements at the port.

The PSE shall control the slew rate of the probing detection voltage when switching between detection voltages to be lower than 0.1 V/μs.

33.2.6 PSE detection of PDs

The polarity of V_{detect} shall match the polarity of V_{Port} as defined in 33.2.1.

33.2.6.1 Detection Criteria

The PSE probes the link segment in order to detect a valid PD signature. A PSE shall accept as a valid signature a link segment with all of the following characteristics:

a) 19 KΩ - 26.5 KΩ DC resistance between powering pairs,
b) no more than 120 nF of capacitance,
c) tolerate a voltage offset of up to 2.0 VDC in the signature characteristics, and
d) tolerate a current offset of up to 12 μA in the signature characteristics.

33.2.6.2 Rejection Criteria

The PSE shall reject link segments as having an invalid signature, when those link segments exhibit any of the following characteristics:

a) less than 15 KΩ DC resistance between powering pairs, or
b) more than 33 KΩ DC resistance between powering pairs, or
c) more than 10 μF capacitive load.

33.2.6.3 Other Criteria

The PSE shall turn on power only on the same pairs as those used for detection.

Note: The PSE is not required to power the link segment, nor is it required to inspect the link segment for a valid PD. A PSE may detect PDs and not power them once detected, or it may stop interrogating the link segment at any time.

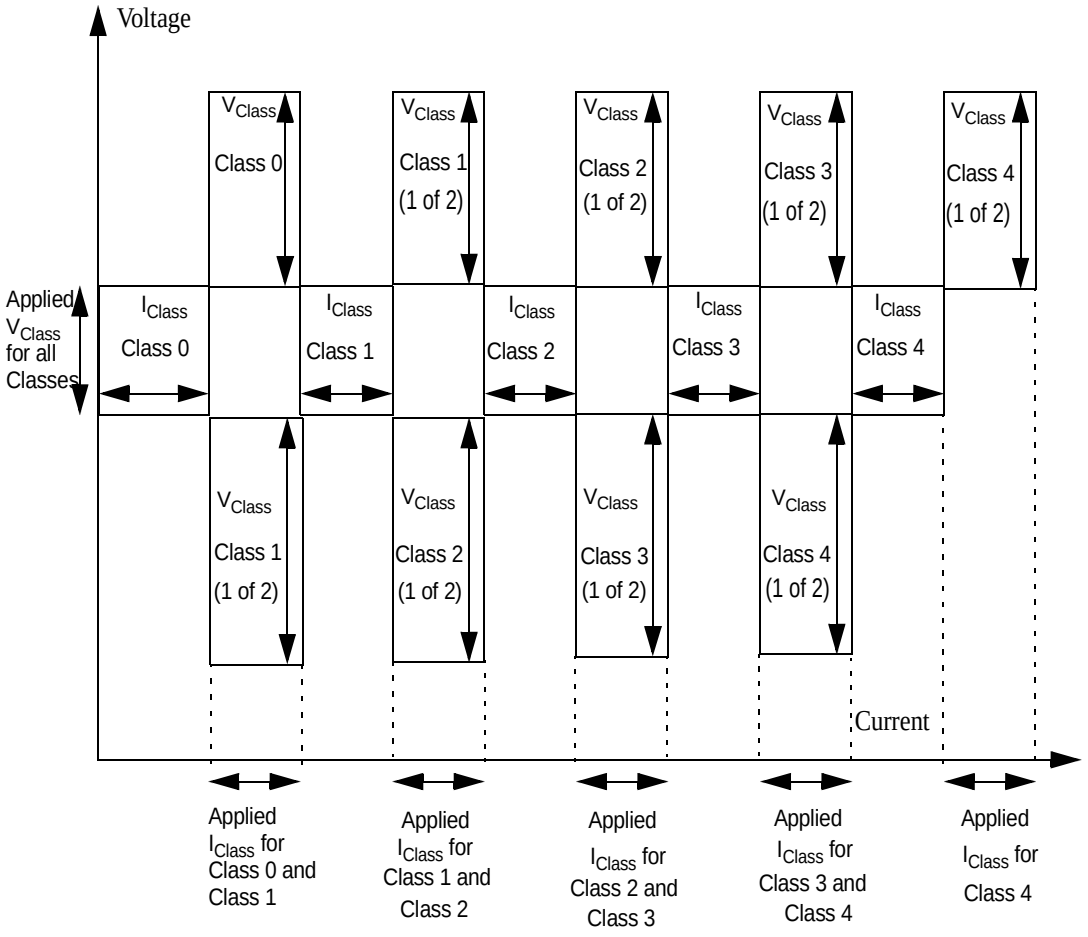
33.2.7 PSE detection of Class 1-4 PDs

The PSE may optionally classify PDs, and PDs may provide information, to allow features such as load management to be implemented. If a PSE successfully completes detection of a PD, and the PSE does not classify the PD in Class 1, 2, 3, or 4, then the PSE shall assign the PD to Class 0.

A successful classification of a Class 1-4 PD requires:

a) Successful PD detection, and subsequently,
b) Successful Class 1-4 classification.

A PSE may classify a Class 1-4 PD by either applying voltage and measuring current or by applying current and measuring voltage, as shown in Figure 33–8.



APPLIED VOLTAGE METHOD:
Apply V_{Class}
Measure I_{Class}
Only one measurement necessary for classification

APPLIED VOLTAGE METHOD:
Apply I_{Class}
Measure V_{Class}
Multiple measurements may be necessary for classification

Figure 33–8—Classification I-V template

33.2.7.1 PD Classes

PDs may provide information that would allow a PSE to classify their power requirements. The classifications are listed in Table 33–2.

Table 33–2—Power Classifications

Class	Usage	Maximum power levels at output of PSE	Maximum power levels at input of PD
0	Default	15.4 Watts	0.44 - 12.95 Watts
1	Optional	4.0 Watts	0.44 - 3.84 Watts
2	Optional	7.0 Watts	3.84 - 6.49 Watts
3	Optional	15.4 Watts	6.49 - 12.95 Watts
4	Optional - Reserved for future use	Treat as Class 0	Not allowed - Reserved for future use

Note: Column four of Table 33–2 is provided for ease of reference. Refer to 33.3.3.1 for specific information.

Class 4 is reserved for future use. PSE detection of a Class 4 PD should use Class 0 power values.

33.2.7.2 PSE classification - measured current method

If the measured current method is used, the PSE shall provide V_{Class} between 15 and 20 volts, limited to 100 mA or less to the MDI with the same polarity as defined for V_{Port} in 33.2.1 and with specifications defined in Table 33–5. The PSE shall measure the current I_{Class} and classify the PD based on the observed current according to Table 33–3.

Table 33–3—PD classification - measured current method

Measured Current I_{Class}	Classification
Less than 5 mA	Class 0
8 - 13 mA	Class 1
16 - 21 mA	Class 2
25 - 31 mA	Class 3
35 - 43 mA	Class 4
47 - 100 mA	PSE may default to Class 0 or not power the PD

33.2.7.3 PSE classification - measured voltage method

If the measured voltage method is used, the PSE shall provide I_{Class} which shall be limited to less than 47 mA with V_{Class} limited to less than 30 volts with the same polarity as defined for V_{Port} in 33.2.1 with specifications defined in Table 33–5. The PSE shall measure the voltage V_{Class} and classify the PD based on the observed voltage according to Table 33–4. For Class 1-4, the measured voltage shall meet the requirement in each of the two current ranges.

Table 33–4—PD classification - measured voltage method

Classification Current I_{Class}	Measured Classification Voltage V_{Class}	Classification
5 - 8 mA	> 20 V	Class 0
5 - 8 mA	< 15 V	Class 1
13 - 16 mA	> 20 V	
13 - 16 mA	< 15 V	Class 2
21 - 25 mA	> 20 V	
21 - 25 mA	< 15 V	Class 3
31 - 35 mA	> 20 V	
31 - 35 mA	< 15 V	Class 4
43 - 47 mA	> 20 V	
43 - 47 mA	< 15 V	PSE may default to Class 0 or not power the PD

Voltage measurements from several applied currents may be necessary to classify the PD.

33.2.8 Detection and classification timing

If a PSE is going to apply power, it shall be within T_{tot} after the start of a detection / classification cycle.

PSEs may operate where the ability to meet the T_{tot} turn on is not possible, such as during start up, oversubscription of available power, etc. No specification is made for detection of or application of operational power to PDs for PSEs in these other modes.

Detection and classification timing shall meet the specifications in Table 33–5.

The PSE shall turn on power after a valid detection in less than 400 ms, if power is to be applied.

33.2.8.1 Detection backoff and retry

It is possible that two separate PSEs, one which implements alternative A and one which implements alternative B, may be attached to the same link segment. In such a configuration, and without any backoff algorithm, the multiple PSEs may prevent each other from ever detecting a valid PD by interfering with the detection process of the other.

After a PSE that is performing detection using alternative B fails to detect a valid PD signature, the PSE shall back off no less than T_{dbo} before attempting another detection. During this backoff, the PSE shall not apply a voltage greater than 2.8 V. During this detection backoff, the PSE is exempted from the overall detection timing specified in 33.2.8. A PSE that is performing alternative B detection may exit from backoff mode within one cycle.

Optionally, if the PSE that is performing detection using alternative B detects an open circuit (a resistance greater than 500 KΩ) on the link segment, then that PSE need not perform the detection backoff.

The maximum detection cycle time for a PSE that is performing alternative A detection is 1s. A PSE that is performing alternative A detection is not subject to the detection backoff nor is it exempt from the T_{tot} timing of 33.2.8.

33.2.9 Power Supply Output

The PSE shall provide power to the MDI in conformance with Table 33–5.

Table 33–5—PSE output requirements

Item	Parameter		Unit	Min	Max	Notes
1	Output voltage	V_{Port}	VDC	44	57	See Note for Item 1
2	Load regulation		VDC	44	57	See Note for Item 2
3	Power feeding ripple and noise:					
	f < 500Hz		V_{pp}		0.5	See Note for Item 3
	500Hz - 150kHz		V_{pp}		0.2	
	150KHz-500KHz.		V_{pp}		0.15	
	500KHz-1MHz		V_{pp}		0.05	
4	Maximum output current in normal powering mode at PSE min output voltage.	I_{Port_max}	mAdc	350		See Note for Item 4
5	Output current in startup mode	I_{Inrush}	mA	400	450	For duration of 50ms min, Duty cycle = 5% min.
6	a) Power off mode current 1	I_{Min1}	mA	0	5	PSE disconnects for $t > T_{PMDO}$
	b) Power off mode current 2	I_{Min2}	mA	5	11	PSE may or may not disconnect for $t > T_{PMDO}$

Table 33–5—PSE output requirements

Item	Parameter		Unit	Min	Max	Notes
7	PD power maintenance request drop out time limit	T_{PMDO}	ms	300	400	See Note for Item 7
8	Overload current detection range	I_{CUT}	mA	350	400	See Note for Item 8
9	Overload time limit	T_{ovld}	ms	50	75	See Note for Item 9
10	Output current – at short circuit condition	I_{LIM}	mA	400	450	See Note for Item 10
11	Short circuit duration	T_{LIM}	ms	50	75	See Note for Item 11
12	Turn on rise time	T_{Rise}	µs	15		From 10% to 90% of V_{Port}
13	Turn off time	T_{Off}	ms		500	Discharge time from V_{Port} to 2.8VDC
14	Continuous Output Power	P_{Port}	W	15.4		Over the range of output voltage. Averaged over 1sec.
15	Current imbalance	I_{imb}	mA		8mA	See Note for Item 15
16	Power turn on time	T_{pon}	ms		400	See Note for Item 16
17	Detection backoff time	T_{dbo}	s	1		PSE detection backoff time limit
18	Output capacitance during detection mode	C_{out}	nF		520	
19	Detection timing	T_{det}	ms		500	Time to complete detection of a PD
20	Classification timing	T_{pdc}	ms	10	75	Time to classify the PD
21	Total detection and power on	T_{tot}	s		1	The sum of T_{det} max, T_{pdc} max and T_{pon} max

NOTES for Table 33-5:

Note for Item 1: Inclusive of line and temperature variations; voltage potential measured between any conductor of one power pair and any conductor of the other power pair.

Note for Item 2: From 0.44W to 15.4W load step. Load rate of change 35mA/µs max. Voltage transients as a result of the load changes are limited to 3.5V/µs max.

Note for Item 3: Common mode and/or differential noise pair to pair values.

a) From 0.44 - 15.4 W at operating V_{Port}.
b) The limits are meant to ensure data integrity. To meet EMI standards, lower values may be needed.
c) For higher frequencies see 33.4.5 and 33.4.6.

Note for Item 4: For I_{Port_max}:

a) I_{Port_max} for V_{Port} > 44V is I_{Port_max} = 15.4 W / V_{Port}.
I_{Port_max} is guaranteed by PSE in order to ensure 15.4 W min output power.

b) Ripple current content (I_{ac}) superimposed on the dc current level (I_{dc}) is allowed if the total current (I_{rms}) is 350mA max for a total output power of 15.4W.
For $V_{Port} > 44V$, $I_{rms\_max} = 15.4\ W/V_{Port}$.
c) The PSE should support the following AC current waveform parameters:
1) Ipeak = 0.4 A minimum for 50 ms and 5% duty cycle minimum.
For $V_{Port} > 44V$, $Ipeak = 17.6W/V_{Port}$.
2) The RMS, DC and ripple current are related by the following equation: $I_{rms}^2 = I_{dc}^2 + I_{ac}^2$

Note for Item 7: For T_{PMDO}:
a) The PSE will not remove power if the PD maintenance signal is absent for less than 300ms duration.
b) The PSE will remove power if the PD maintenance signal is absent for a duration equal to or greater than 400ms.
c) If 300ms<tx<400ms and t<tx, where tx is the time threshold for a disconnect decision, the PSE may or may not remove power from the port.
d) If 300ms<tx<400ms and t>tx, where tx is the time threshold for a disconnect decision, the PSE will remove power from the port.
e) See Figure 33–18 for timing relationships.

Note for Item 8: After time duration of T_{ovld} the PSE shall disconnect the power from the port.

Note for Item 9: If $350mA < I_{CUT} < 400mA$ for $50ms < T_{ovld} < 75ms$, the PSE shall disconnect the port.

Note for Item 10: Max. value of the port current during short circuit condition.
The power shall be disconnected from the port within $T_{LIM.}$
Max. value applies over operating voltage range as specified in Item 1.

Note for Item 11: If short circuit condition is detected, the power will be disconnected from the port within $T_{LIM.}$

Note for Item 15: Current imbalance between the two conductors of a power pair over the current load range.
Note: This is inclusive of the current imbalance requirements of the implemented MDI - this is not an additional current imbalance.

Note for Item 16: PSE power up time for a PD after completion of detection and optional classification.

END of Notes for Table 33-5.

In order to prevent the potential for oscillation the output impedance of the PSE power supply should be less than 300 milliohms at any frequency lower than 100 kHz.

Editor's Note: *To be removed prior to final publication.*

This should refer to an Annex if a practical test methodology can be devised.

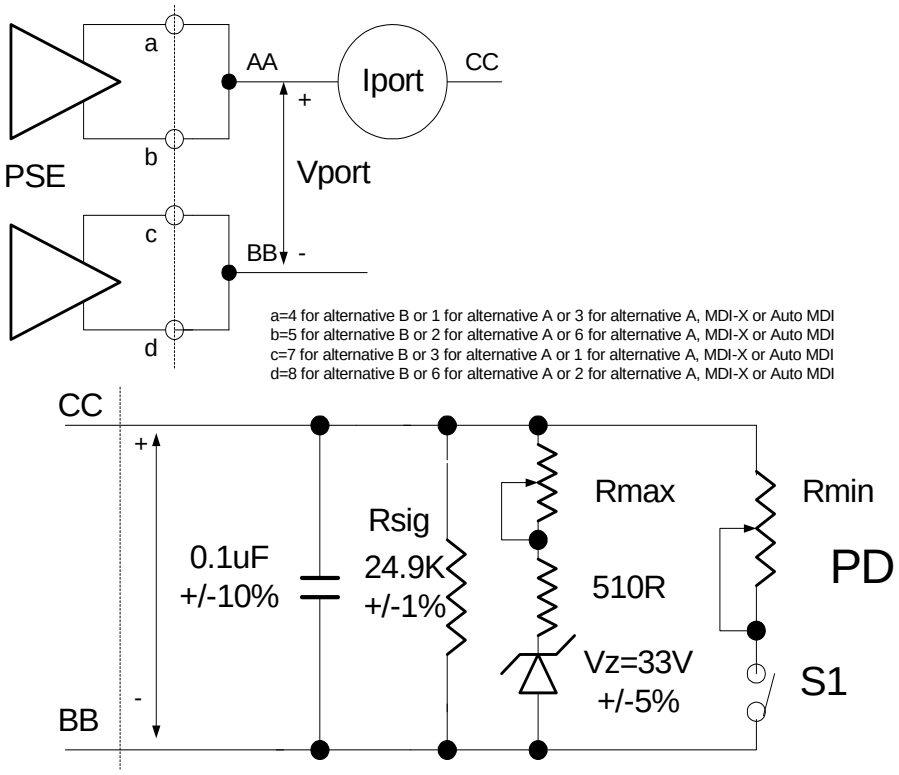
Regardless of the requirements stated here, the PSE shall comply with applicable local and national codes related to safety.

33.2.9.1 Test Procedure PSE-1 (output polarity, output voltage, and continuous output power)

Test Procedure PSE-1 is used for testing:

a) output voltage polarity (Table 33–1),
b) V_{Port} (Table 33–5, item 1),
c) I_{Port_max} (Table 33–5, item 4, including note a)), and
d) P_{Port} (Table 33–5, item 14).

Test Procedure PSE-1 uses Test Configuration PSE-A as shown in Figure 33–9.



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

$$R\min < \frac{Vport^2}{15.5 - Vport * Iport\_\min}$$

$$44V \le Vport \le 57$$

Figure 33–9—Test configuration PSE-A

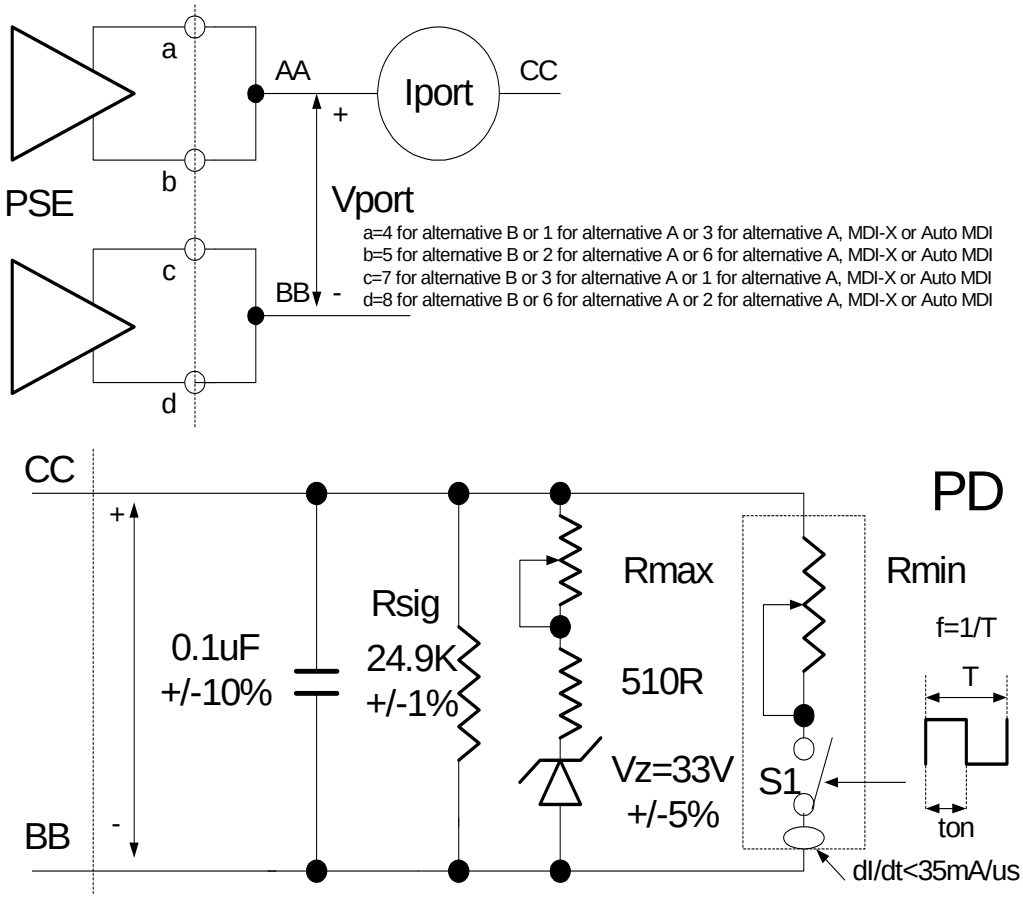
Test Procedure PSE-1 is as follows:

1) Wait 1 s min and measure V_{Port} at Rmax (S1 open).
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Wait 1 s min and measure V_{Port} at Rmin (S1 closed).
   Rmin is adjusted to have a total load of 15.4W min.

33.2.9.2 Test Procedure PSE-2 (load regulation)

Test Procedure PSE-2 is used for testing load regulation, i.e., voltage transients during load changes (Table 33–5, item 2).

Test Procedure PSE-2 uses Test Configuration PSE-B as shown in Figure 33–10



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

$$R\min < \frac{Vport^2}{15.5 - Vport * Iport\_\min}$$

$$44V \le Vport \le 57$$

Figure 33–10—Test configuration PSE-B

Test Procedure PSE-2 is as follows:

1) Wait 1 s min and measure V_{Port} at Rmax (S1 open).
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Wait 1 s min and measure V_{Port} at Rmin (S1 closed).
   Rmin is adjusted to have a total load of 15.4W min.
3) Change load from Rmax to Rmin and from Rmin to Rmax at f = 10Hz,
   duty cycle (ton/T) = 0.5 +/- 20%, while monitoring V_{Port}.

33.2.9.3 Test Procedure PSE-3 (ripple and noise)

Test Procedure PSE-3 is used for testing ripple and noise (Table 33–5, item 3).

Test Procedure PSE-3 uses Test Configuration PSE-A as shown in Figure 33–9.

Test Procedure PSE-3 is as follows:

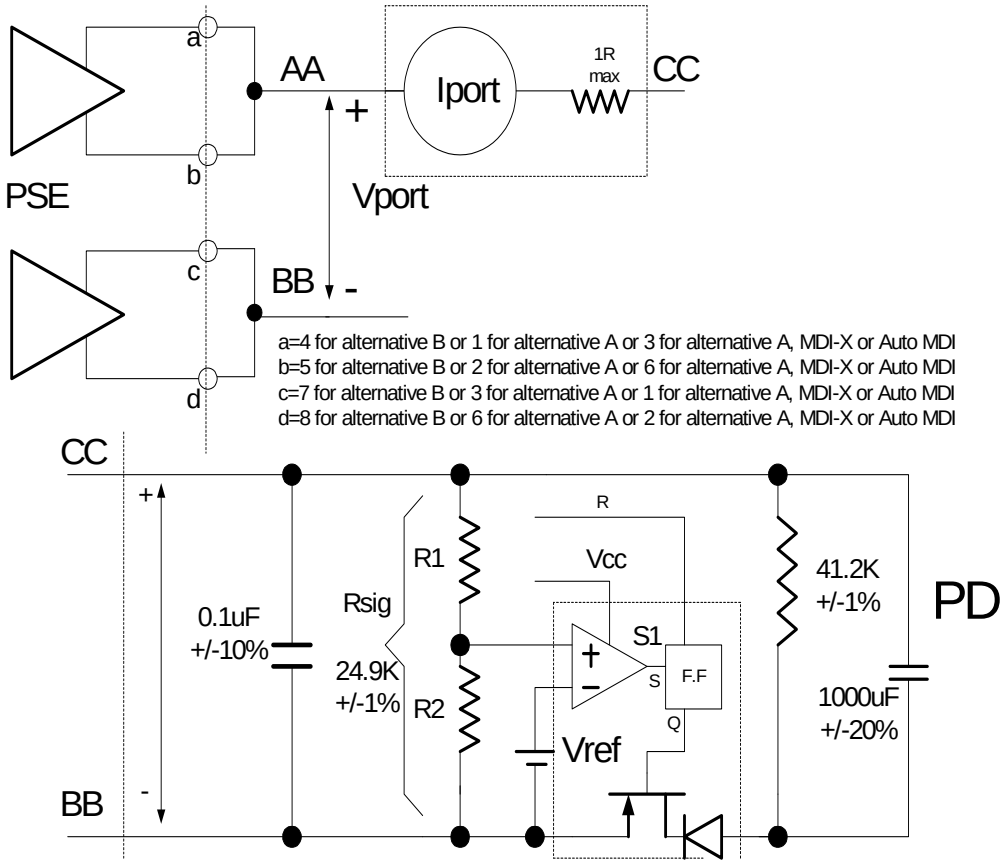
1) Wait 1 s min and measure V_{Port} at Rmax (S1 open).
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Wait 1 s min and measure V_{Port} at Rmin (S1 closed).
   Rmin is adjusted to have a total load of 15.4W min.
3) Measure V_{Port} ac noise and ripple at Rmax (S1 open) and at Rmin (S1 closed) by using spectrum analyzer or equivalent equipment.

33.2.9.4 Test Procedure PSE-4 (output current in startup mode)

Test Procedure PSE-4 is used for testing:

a) I_{Inrush} (Table 33–5, item 5) and
b) T_{LIM} (Table 33–5, item 11).

Test Procedure PSE-4 uses Test Configuration PSE-C as shown in Figure 33–11



Test setup principles:

1. S1 function is to connect a large capacitive load when the port voltage exceeds 42V.
2. S1 shall be designed to allow the transition from OFF to ON with less than 50us.
3. The capacitive load value designed to force a short circuit condition for more than 75ms.
4. Test can be repeated only if the voltage across the capacitive load is less than 0.7V and S1 was reset.

Figure 33–11—Test configuration PSE-C

Test Procedure PSE-4 is as follows:

1) Wait 1 s min and measure V_{Port} at Rmax (S1 open).
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Wait 1 s min and measure V_{Port} at Rmin (S1 closed).
   Rmin is adjusted to have a total load of 15.4W min.

3) Verify that I_{Port} is within limits shown in Figure 33–12.

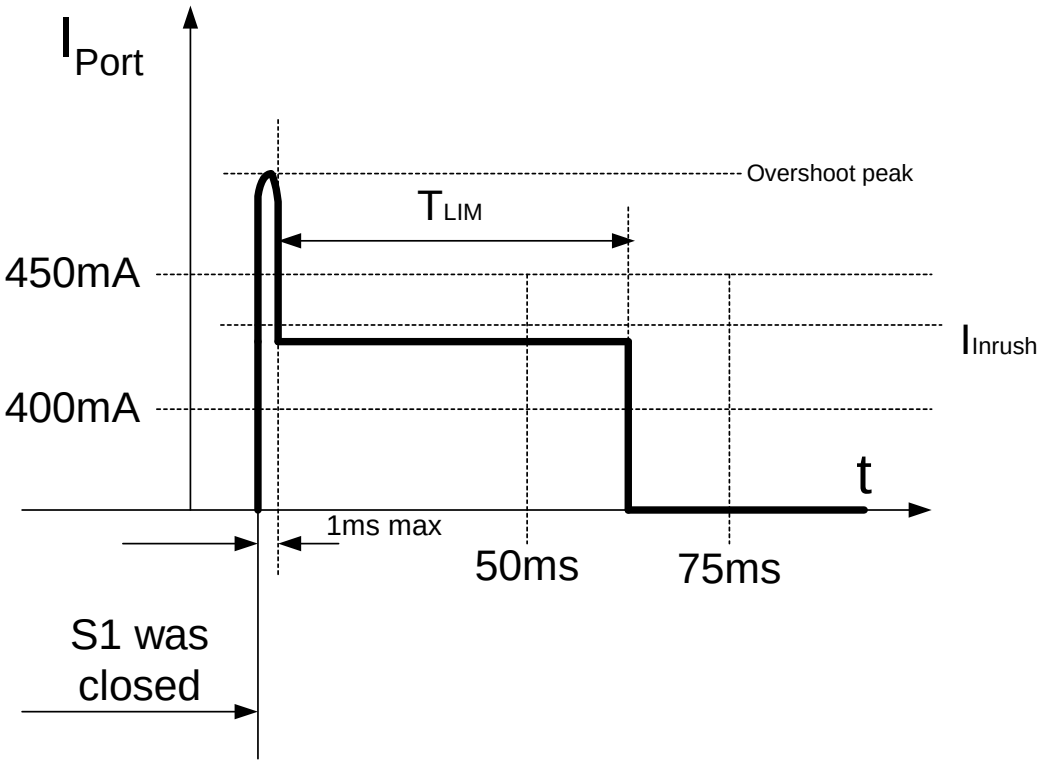


Figure 33–12—Output current in startup mode

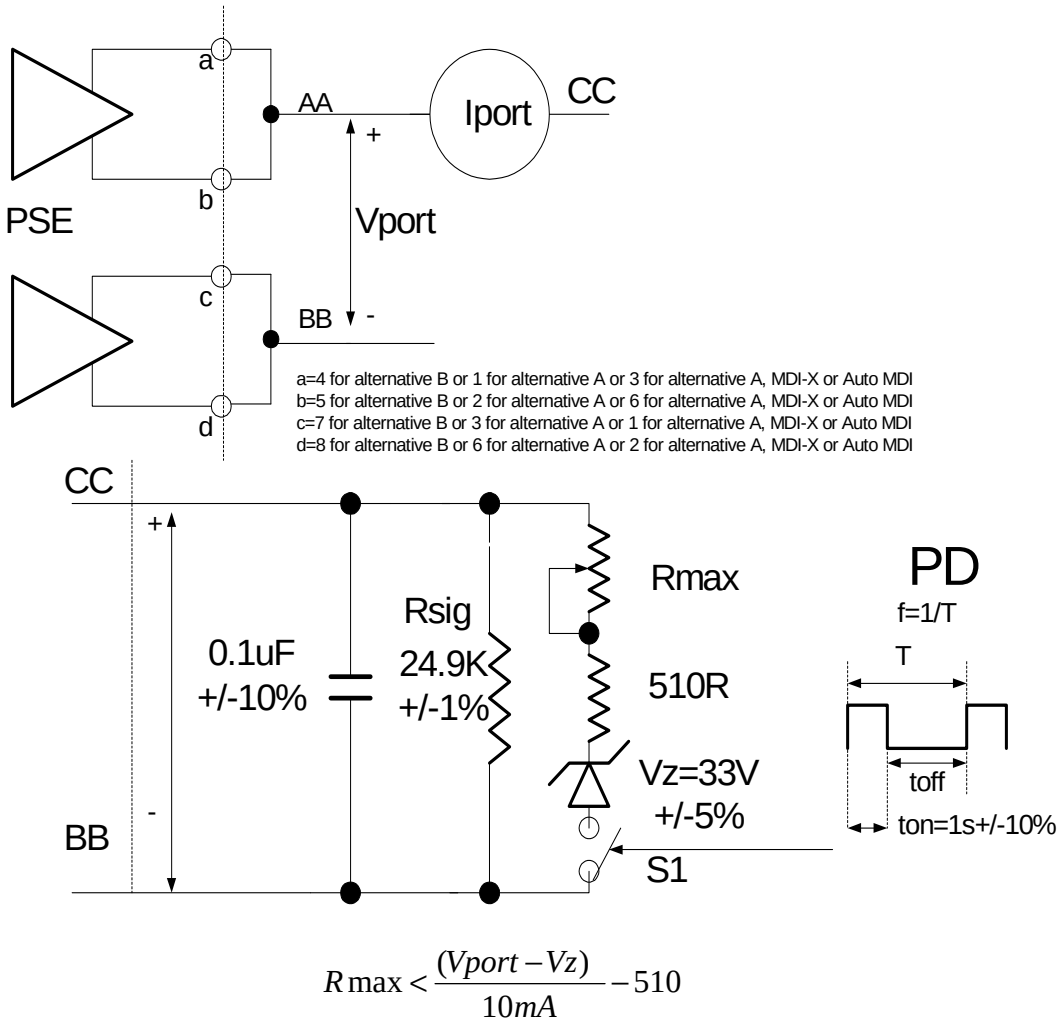
33.2.9.5 Test Procedure PSE-5 (power off mode current)

Test Procedure PSE-5 is used for testing:

a) I_{Min1} (Table 33–5, item 6a) and
b) T_{PMDO} (Table 33–5, item 7)

when using option a) in 33.2.11.

Test Procedure PSE-5 uses Test Configuration PSE-D as shown in Figure 33–13.



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

Figure 33–13—Test configuration PSE-D

Test Procedure PSE-5 is as follows:

1) Wait 1 s min and measure V_{Port} at Rmax (S1 closed).
   Verify that 44V <= V_{Port} <= 57V.
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Increase Rmax and verify that the power is removed from the port by verifying that V_{Port} decreases by 1V at I_{Port} >= 5mA.
3) Repeat step 1.
4) Adjust S1 control to: S1 off time 299.0 ms.
   Verify that V_{Port} is stable and within its initial values (i.e., power is not removed from the port).
5) Adjust S1 control to: S1 off time 400.0 ms.
   Verify that power is removed from the port within 400 ms max of the first cycle from the time that S1 was opened.

33.2.9.6 Test Procedure PSE-6 (overload current detection range and overload timings)

Test Procedure PSE-6 is used for testing:

a) I_{CUT} (Table 33–5, item 8) and
b) T_{ovld} (Table 33–5, item 9).

Test Procedure PSE-6 uses Test Configuration PSE-B as shown in Figure 33–10.

Test Procedure PSE-6 is as follows:

1) Set Rmax (S1 open) and Rmin (S1 closed).
   (Rmax is adjusted to generate I_{Port} min = 10mA.)
   Verify that 44V <= V_{Port} <= 57V.
2) Close S1. Decrease Rmin slowly until power is removed from the port and note the actual value of I_{CUT}. (Power is removed when V_{Port} decreases by 1V from its initial value and I_{Port} is reduced to less than 5mA.)
3) Verify that $(15.4/V_{Port}) < I_{CUT} < 400mA$.
4) Repeat step 1.
   Adjust S1 control to: $I_{Port} > I_{CUT}$. S1 on time: 50.0 ms.
   Verify that power is not removed from the port.
   Adjust S1 control to: $I_{Port} > I_{CUT}$. S1 on time: 75.0 ms.
   Verify that power is removed from the port.

The relationships between overload detections and timings are shown in Figure 33–14.

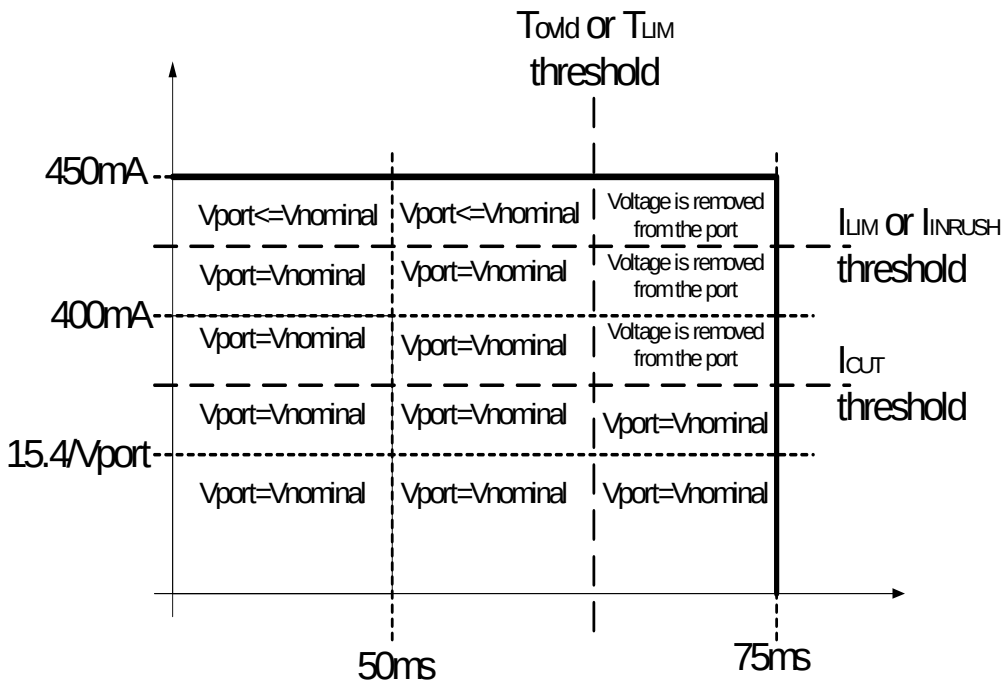


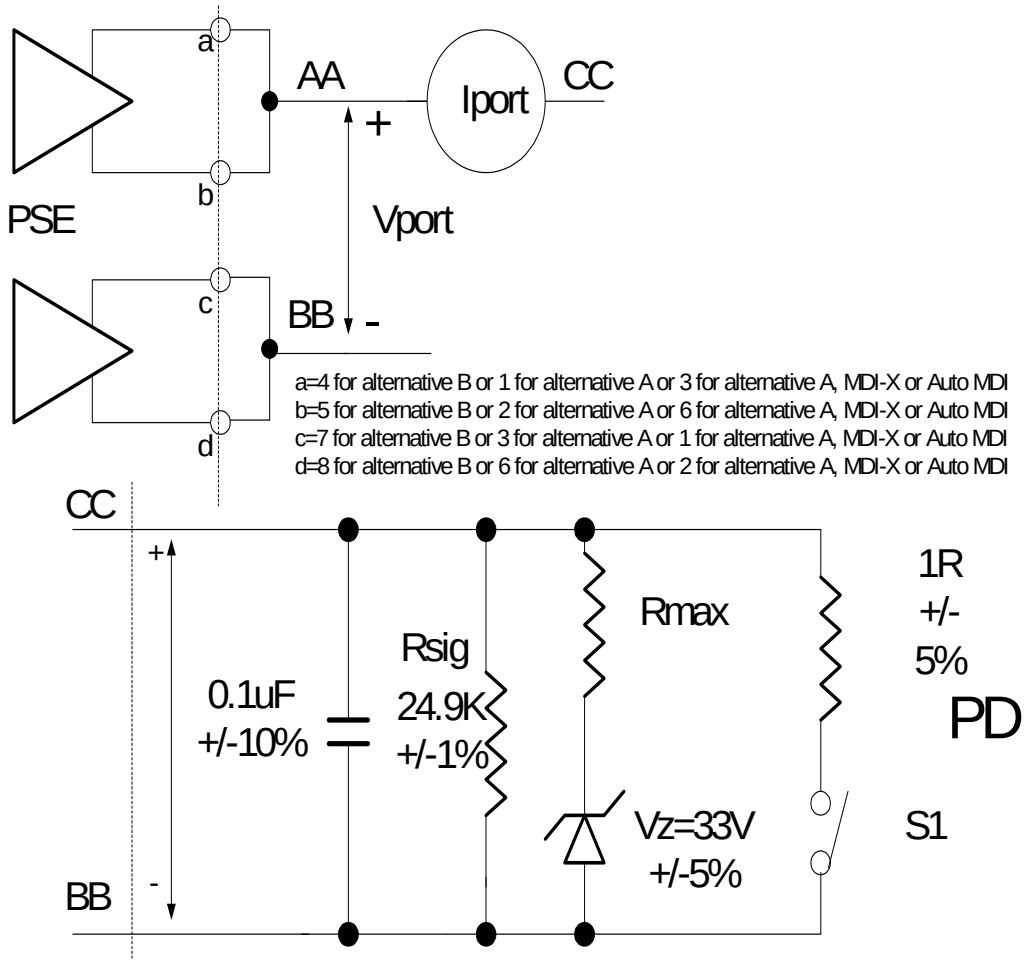
Figure 33–14—Overload detection and timings

33.2.9.7 Test Procedure PSE-7 (short circuit current and timing)

Test Procedure PSE-7 is used for testing:

a) I_{LIM} (Table 33–5, item 10) and
b) T_{LIM} (Table 33–5, item 11).

Test Procedure PSE-7 uses Test Configuration PSE-E as shown in Figure 33–15.



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

Figure 33–15—Test configuration PSE-E

Test Procedure PSE-7 is as follows:

1) Wait 1 s min and measure V_{Port} at Rmax (S1 open).
   Rmax is adjusted to generate I_{Port} min = 10mA.
   Verify that 44V < V_{Port} < 57V.
2) Close S1 and observe I_{Port} .

3) Verify that I_{Port} is within limits shown in Figure 33–16.

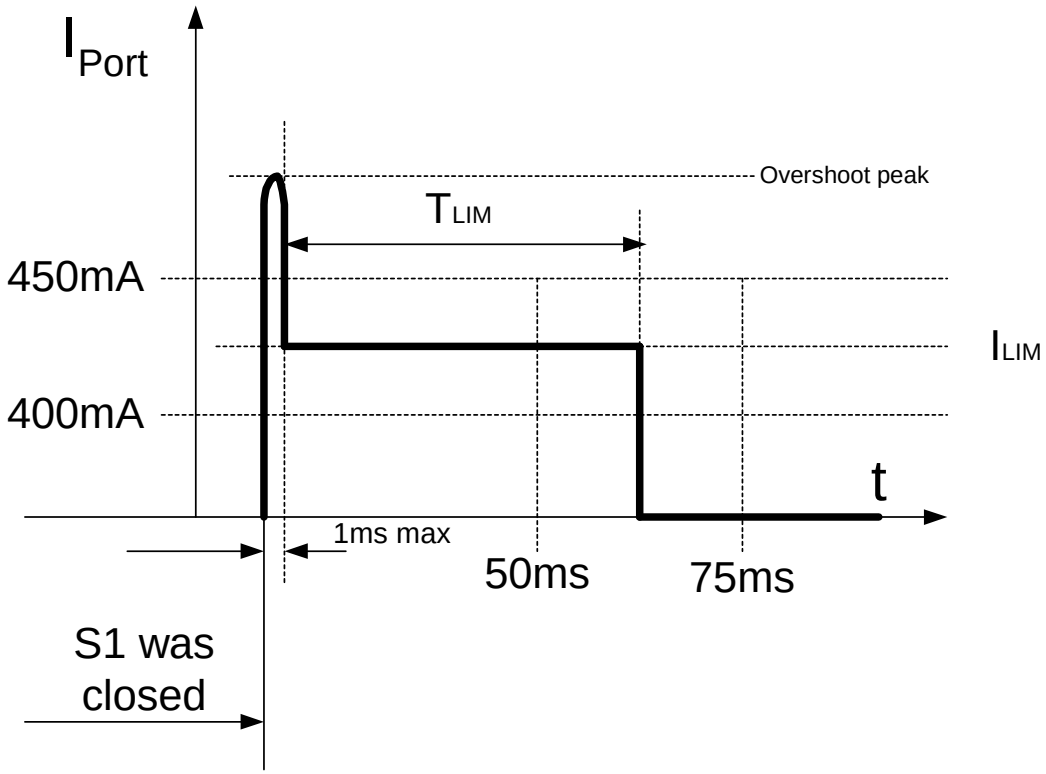


Figure 33–16—Output current at short circuit

33.2.9.8 Test Procedure PSE-8 (turn on rise time)

Test Procedure PSE-8 is used for testing T_{Rise} (Table 33–5, item 12).

Test Procedure PSE-8 uses Test Configuration PSE-A as shown in Figure 33–9.

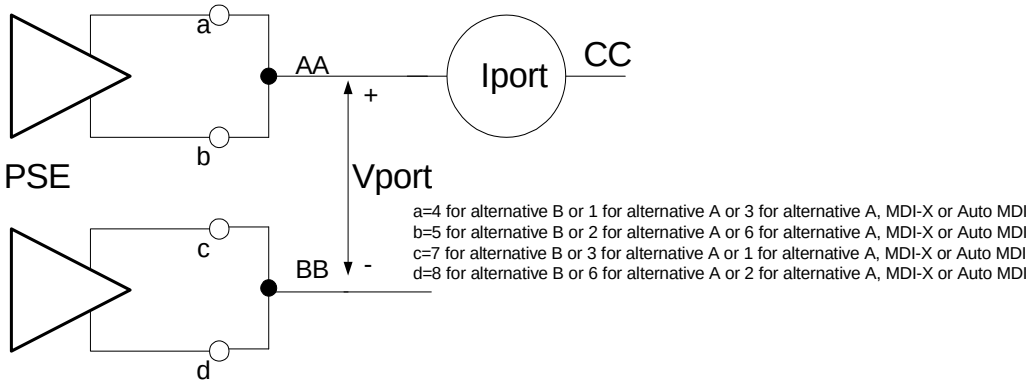
Test Procedure PSE-8 is as follows:

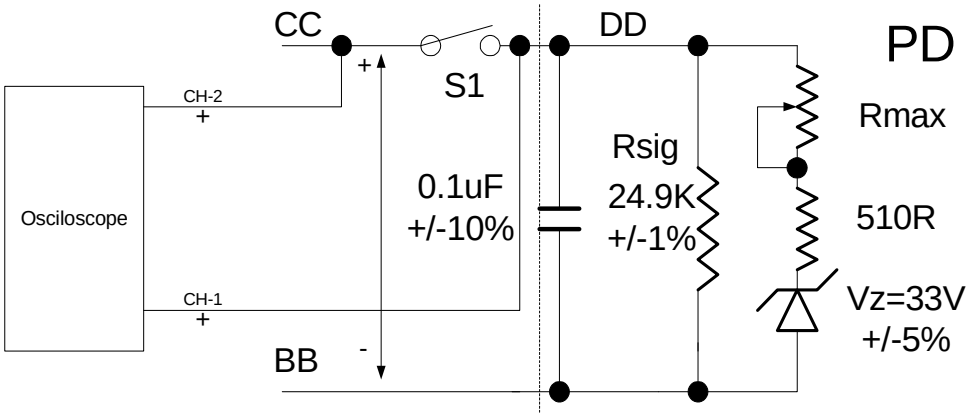
1) Measure V_{Port} at Rmax (S1 open).
   Rmax is adjusted to generate I_{Port} min = 10mA.
   Measure rise time from 10% of V_{Port} to 90% of V_{Port}.
   See Figure 33–19.
2) Measure V_{Port} at Rmin (S1 closed).
   Rmin is adjusted to have a total load of 15.4W min.
   Measure rise time from 10% of V_{Port} to 90% of V_{Port}.
   See Figure 33–19.

33.2.9.9 Test Procedure PSE-9 (turn off time)

Test Procedure PSE-9 is used for testing T_{Off} (Table 33–5, item 13).

Test Procedure PSE-9 uses Test Configuration PSE-F as shown in Figure 33–17.





$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

$$44V \le Vport \le 57$$

Figure 33–17—Test configuration PSE-F

Test Procedure PSE-9 is as follows:

1) Measure V_{Port} at Rmax (S1 closed).
   Rmax is adjusted to generate I_{Port} min = 10mA.
2) Monitor V_{Port} at PSE side (CC) and at PD side (DD).
   Disconnect PD load by turning off S1 at T_0.
   Use CH-1 as the trigger signal for measuring the timings.
   Verify that V_{Port} has not changed during the first 300 ms (T_1) from T_0.
   Verify that power is removed from the port within 400 ms (T_2) from T_0.

Verify that V_{Port} is less than 2.8Vdc within 500 ms max from tx.
The turn off timing relationships are illustrated in Figure 33–18.

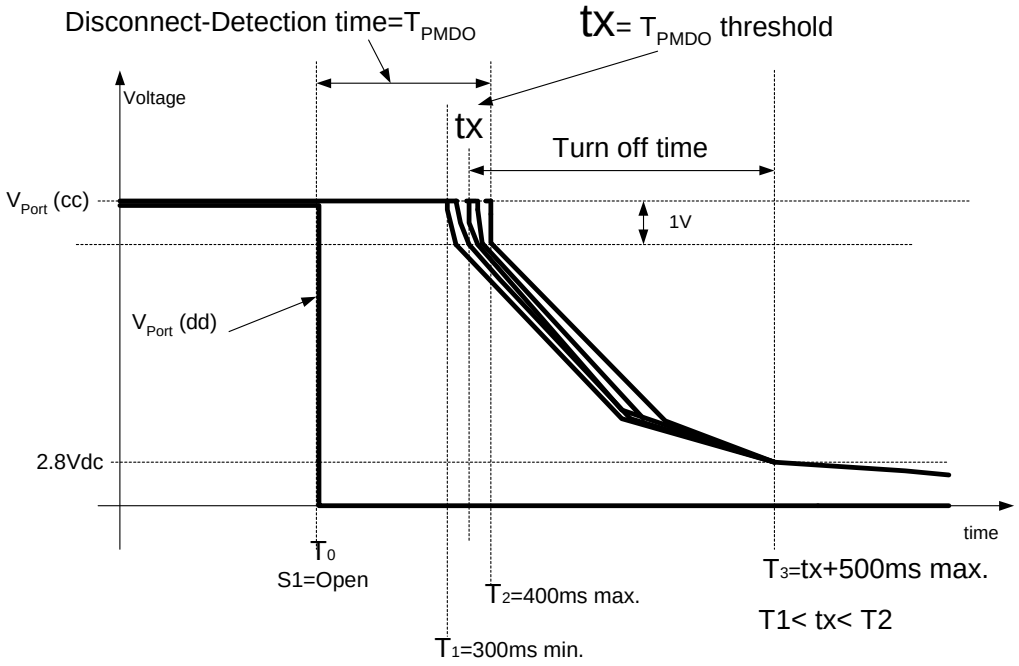


Figure 33–18—Turn off timing relationships

33.2.9.10 Test Procedure PSE-10 (turn on, detection, classification and total cycle times)

Test Procedure PSE-10 is used for testing:

a) T_{pon} (Table 33–5, item 16),
b) T_{det} (Table 33–5, item 19),
c) T_{pdc} (Table 33–5, item 20), and
d) T_{tot} (Table 33–5, item 21).

Test Procedure PSE-10 uses Test Configuration PSE-F as shown in Figure 33–17.

Test Procedure PSE-10 is as follows:

1) Wait 1s min and measure V_{Port} at Rmax (S1 closed).
Rmax is adjusted to generate I_{Port} min = 10mA.

2) Open S1. Repeat step 1 and monitor the events vs. timings as illustrated in Figure 33–19.

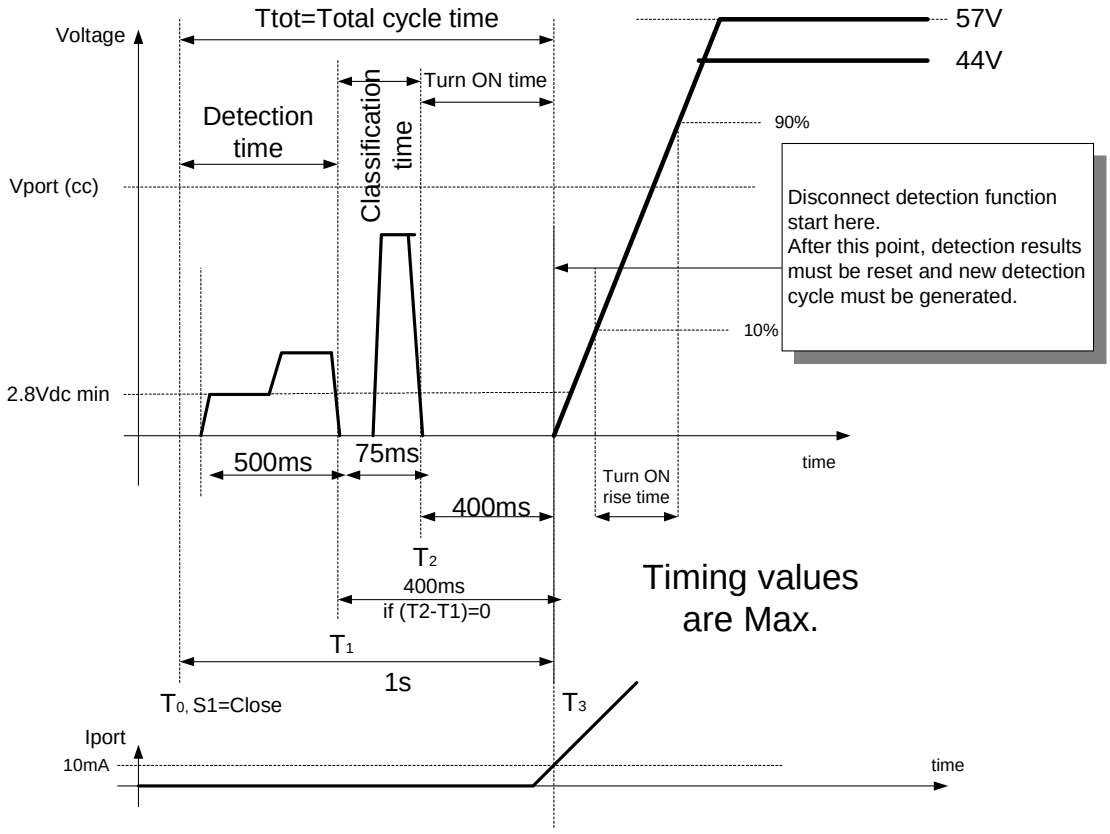
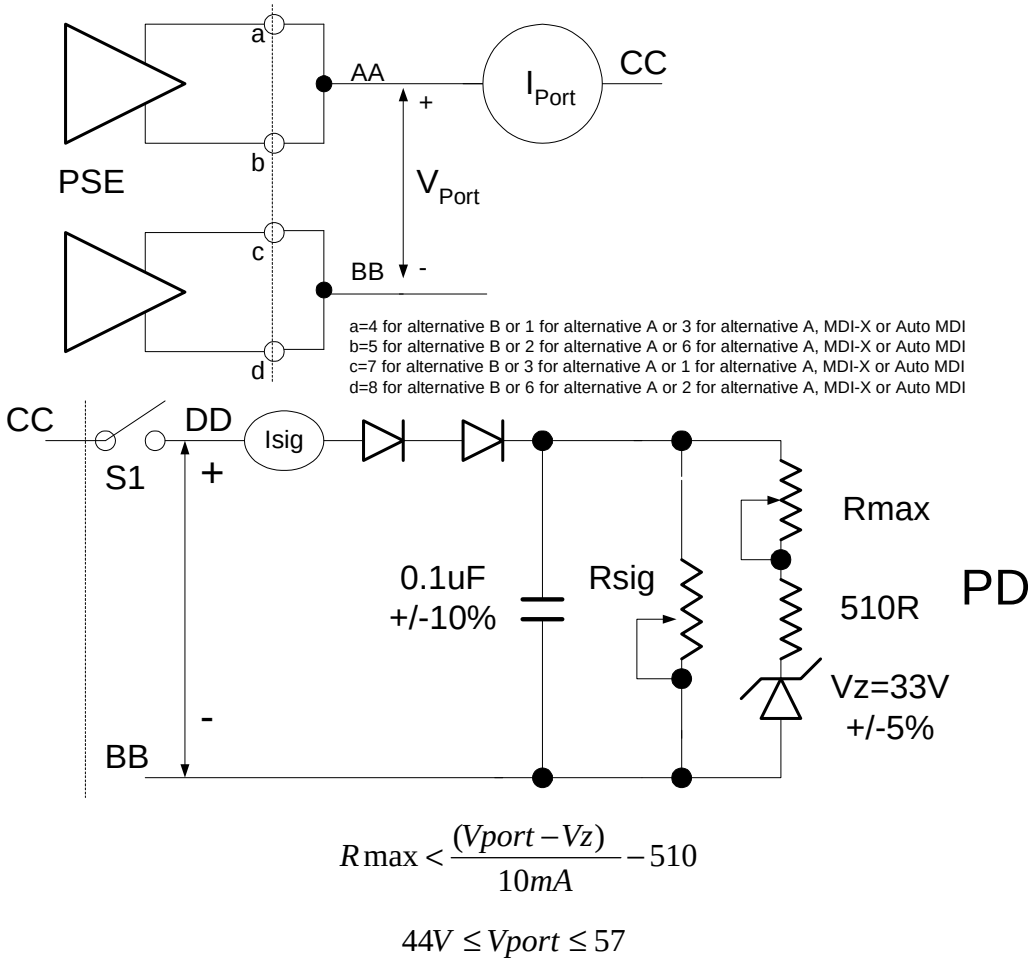


Figure 33–19—Detection, classification, turn on, and total cycle timing relationships

33.2.9.11 Test Procedure PSE-11 (detection backoff time)

Test Procedure PSE-11 is used for testing T_{dbo} (Table 33–5, item 17).

Test Procedure PSE-11 uses Test Configuration PSE-G as shown in Figure 33–20.



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

$$44V \le Vport \le 57$$

Figure 33–20—Test configuration PSE-G

Test Procedure PSE-11 is as follows:

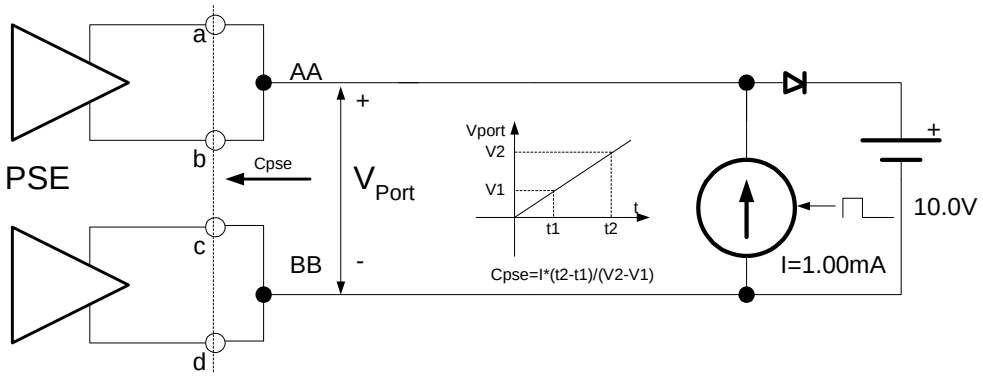
1) Set Rsig to 24.9KΩ+/-1%. Close S1.
   Measure V_{Port} at Rmax.
   Rmax is adjusted to generate $I_{Port}\,\min = 10\text{mA}$ at V_{Port}.
2) Open S1.
   Connect V1 = 2.9V+/-0.1Vdc source between points DD and BB. Record Isig1.
   Connect V2 = 3.9V+/-0.1Vdc source between points DD and BB. Record Isig2.
   Adjust Rsig until (V2-V1)/(Isig2-Isig1)=34KΩ+/-1%.
   Close S1.
   Verify that V_{Port} is less than 2.8V for 2s minimum.
3) Open S1.
   Connect V1 = 2.9V+/-0.1Vdc source between points DD and BB. Record Isig1.
   Connect V2 = 3.9V+/-0.1Vdc source between points DD and BB. Record Isig2.
   Adjust Rsig until (V2-V1)/(Isig2-Isig1)=510KΩ+/-1%.

Close S1.
Verify that V_{Port} voltages and timings are as defined in Figure 33–19.

33.2.9.12 Test Procedure PSE-12 (port capacitance during detection)

Test Procedure PSE-12 is used for testing C_{out} (Table 33–5, item 18).

Test Procedure PSE-12 uses Test Configuration PSE-H as shown in Figure 33–21.



a=4 for alternative B or 1 for alternative A or 3 for alternative A, MDI-X or Auto MDI
b=5 for alternative B or 2 for alternative A or 6 for alternative A, MDI-X or Auto MDI
c=7 for alternative B or 3 for alternative A or 1 for alternative A, MDI-X or Auto MDI
d=8 for alternative B or 6 for alternative A or 2 for alternative A, MDI-X or Auto MDI

Figure 33–21—Test configuration PSE-H

Test Procedure PSE-12 is as follows:

1) Set PSE port to Off mode.
   Connect switched current source I to the PSE port.
   The current source voltage is clamped to 10V.
   Calculate port capacitance by using the equation specified in Figure 33–21.
2) Accurate LCR meter can be used as an alternative. Test voltage should be less than 0.5Vpp.

33.2.10 Power supply allocation

A PSE shall not initiate power provision to a link if the PSE is unable to provide the maximum power level requested by the PD based on the PD's classification.

If, after powering, the system determines that the attached PD requires less power than required by its classification, the system may use the additional information in its power allocation algorithm. The mechanism for obtaining the additional information is not specified.

If the system implements a power allocation algorithm, no additional behavioral requirement is placed on the system as it approaches or reaches its maximum power subscription. Specifically the interaction between one PSE and another PSE in the same system is beyond the scope of this standard.

Table 33–6—PSE port parameters for AC disconnect-detection function

Item	Parameter	Symbol	Unit	Min	Max	Notes
1	Pulse parameters					
	Port disconnect probing ac voltage when PD is disconnected	V_open	V_{pp}	Recommended min value above $1V_{pp}$ to overcome noise and ripple issues.	0.1*Vdc	Include noise, ripple, etc.
	AC probing signal frequency	F_p	Hz	5	500	
	AC probing signal slew rate	SR	V/µs		0.1	
2	AC source output impedance					
	Source output resistance of the AC probing signal	R_sac	KΩ	5		
	PSE port impedance during resistor detection when measured from the link to the PSE port	R_rev	KΩ	70		May be redundant.
3	PSE port voltage during ac disconnect detection					
	Port ac voltage when PD is connected		V_{pp}		0.5	May be redundant.
	Port voltage when PD is disconnected	V_{Port}	V_p		60	
4	Disconnect detection thresholds					
	Disconnect detection time	T_{PMDO1}	ms	300	400	May be redundant.
5	AC power maintenance signature					
	"Shall not remove power from the port"	Z_{ac1}	KΩ		(33)	
	"Shall remove power from the port"	Z_{ac2}	KΩ	(500)		

33.2.11 PSE power removal

The PSE will monitor the link segment and shall disconnect the power from a port when a PD is removed or no longer maintains the power maintenance signature.

The PSE shall monitor either A or B or both components of the power maintenance signature. The PSE removes power if it detects either:

a) The dc current is less than specified at Table 33–5 item 6 or
b) The ac impedance is higher than specified in Table 33–6

The PSE shall remove power from the link segment within the limits of T_{PMDO} as specified in Table 33–5.

33.2.11.1 Test Procedure PSE-13 (ac disconnect pulse parameters)

Test Procedure PSE-13 is used for testing:

a) $V_{\_close}$ (AC voltage when PD is connected),
b) $V_{\_open}$ (Table 33–6, item 1),
c) F_p (Table 33–6, item 1),
d) SR (Table 33–6, item 1),
e) T_{PMDO1} (Table 33–6, item 4) when using option b) in 33.2.11,
f) V_p (Table 33–6, item 3), and
g) Z_{ac1} and Z_{ac2} (Table 33–6, item 5).

Test Procedure PSE-13 uses Test Configuration PSE-I as shown in Figure 33–22.

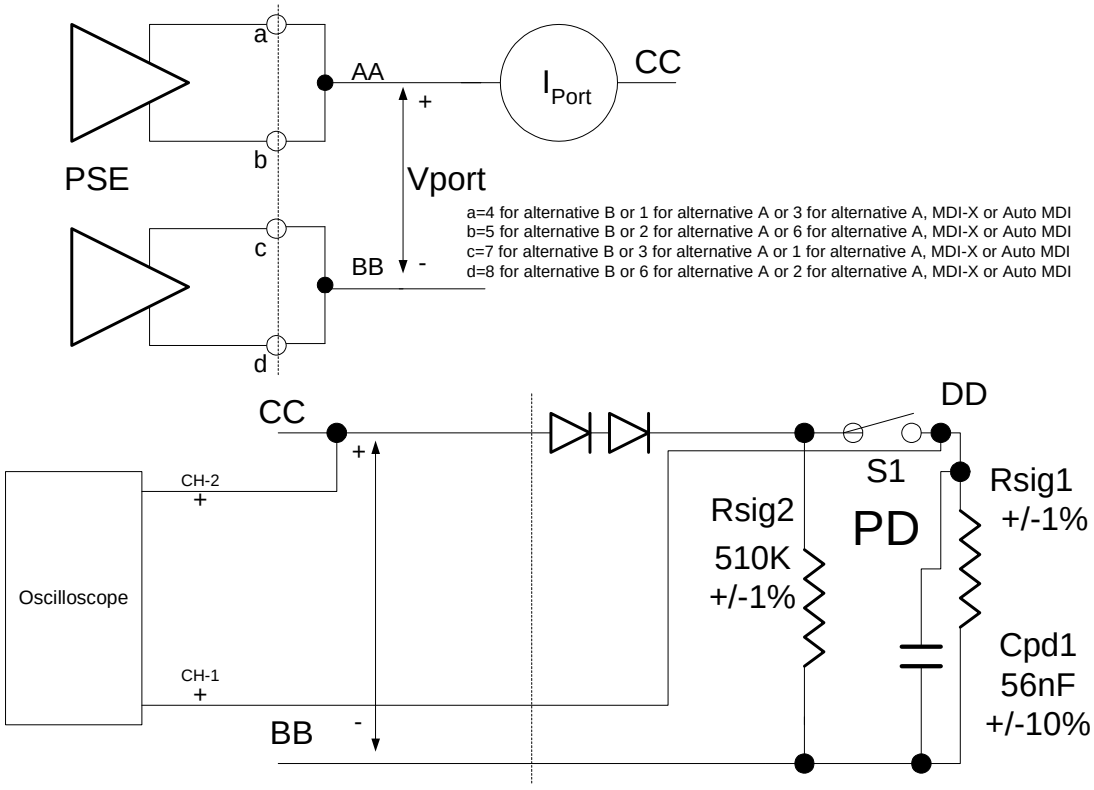


Figure 33–22—Test configuration PSE-I

Test Procedure PSE-13 is as follows:

1) Set Rsig1 value to have total of 26.25KΩ with Rsig2 =510 KΩ and S1 closed.
   Measure V_{Port} and verify that 44V <= V_{Port} <=57 and $V_{\_close}$ <0.5Vpp.
2) Monitor V_{Port} at PSE side (CC) and at PD side (DD).
3) Disconnect PD by turning off S1 at T_o.
   Use CH-1 as the trigger signal for measuring the timings.
4) Verify that power is not removed during the first 300ms (T_1) from T_o.

5) Verify that power is removed from the port within 400ms (T_2) max from T_o. (power is removed when V_{Port} has dropped by 1V min)
6) Measure $V_{\_open}$, F_p and SR. Refer to Figure 33–23.

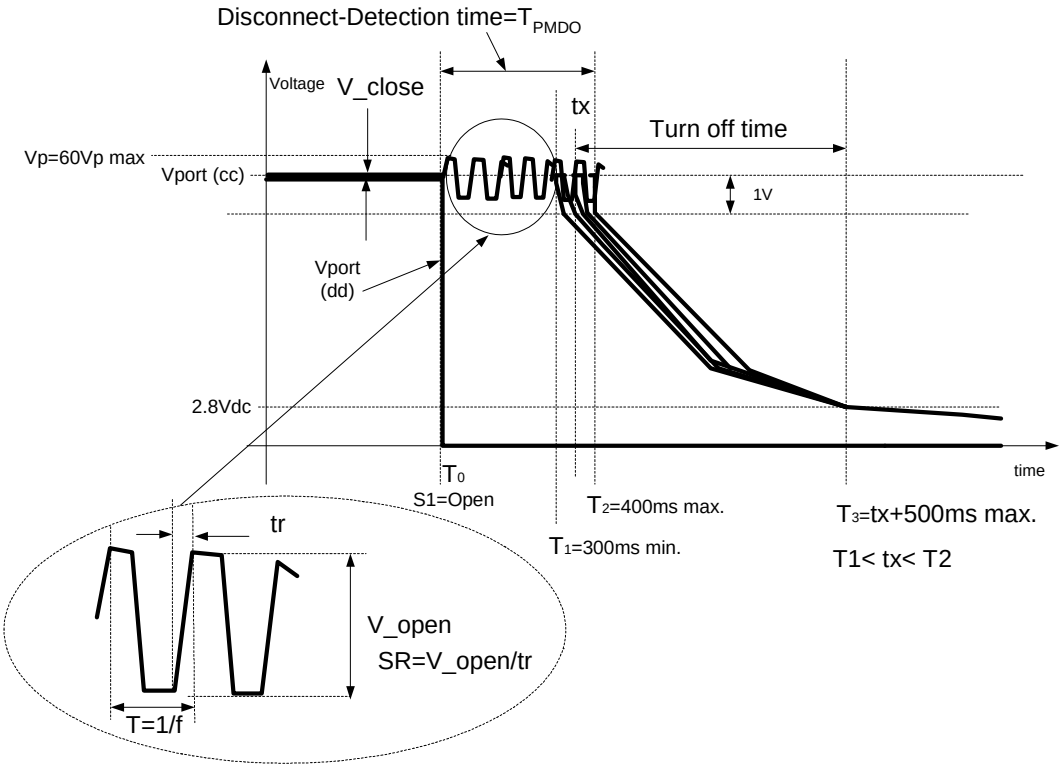


Figure 33–23—AC disconnect timing relationships

33.2.11.2 Test Procedure PSE-14 (port impedance)

Test Procedure PSE-14 is used for testing:

a) $R_{\_sac}$ (Table 33–6, item 2),
b) $R_{\_rev}$ (Table 33–6, item 2),
c) Z_{source} (Figure 33–6 and Figure 33–7), and
d) Detection short circuit (33.2.5).

Test Procedure PSE-14 uses Test Configuration PSE-J as shown in Figure 33–24.

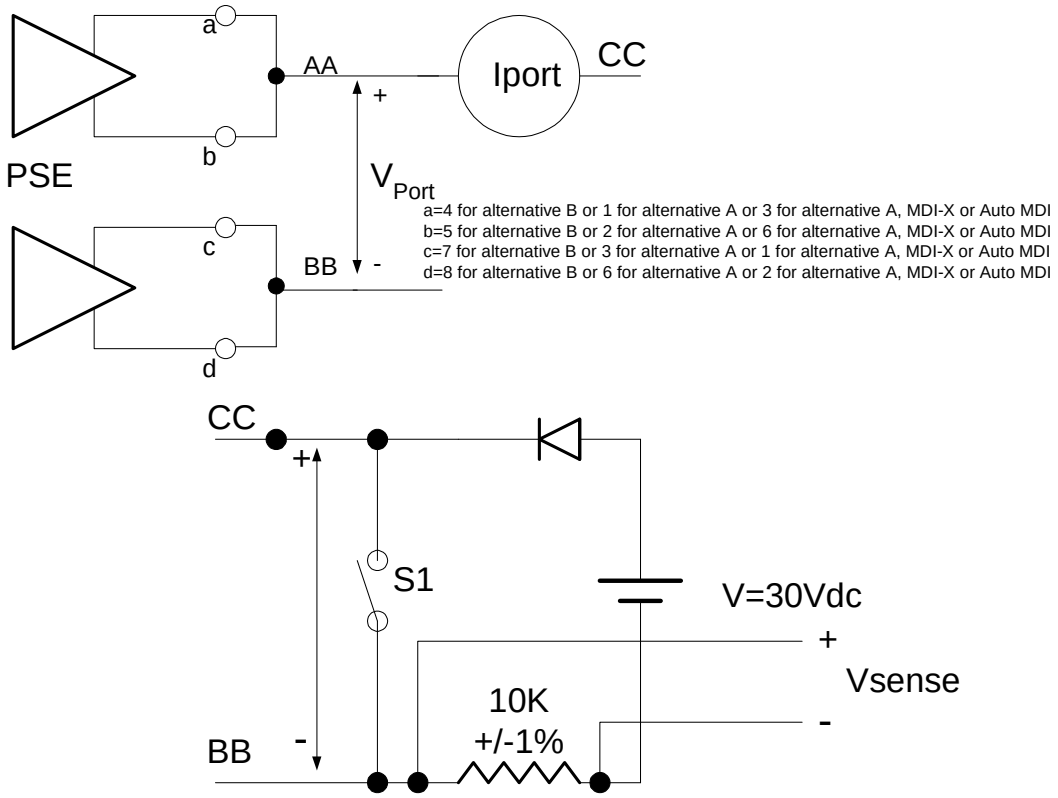


Figure 33–24—Test configuration PSE-J

Test Procedure PSE-14 is as follows:

1) Set S1 = close. Monitor I_{Port} and verify that I_{Port} is less than 5mA over 2s period. (Ignore results of first 1ms).
2) Record V_{-open} and its frequency F_p from Test Procedure PSE-13 and calculate Ix[mApp]=V_{-open}/5.
3) Verify that I_{Port} at frequency Fp is less than Ix over 2s period. (Ignore results of first 1ms).
4) Set S1 = open.
5) Verify that Vsense<3.625Vp ((30V-1V)*10K/80K) over 2s period. (Ignore results of first 26ms (5*10K*0.52µF).

33.3 Powered Devices

For the purposes of Clause 33, a PD is a device that is either drawing power or requesting power by participating in the PD detection algorithm. A device that is capable of becoming a powered device may or may not have the ability to draw power locally and, if doing so, may or may not require power from the MDI. PD capable devices that are neither drawing nor requesting power are also covered in this clause.

A PD is specified at the point of the physical connection to the cabling. Characteristics such as the losses due to voltage correction circuits, power supply inefficiencies, separation of internal circuits from external ground or other characteristics induced by circuits after the MDI connector are not specified. Limits specified for the PD are specified at the MDI, not at any point internal to the PD, unless specifically stated.

33.3.1 PD MDI

The PD shall be capable of accepting power on either of two sets of MDI conductors. Without implying a preference, the two conductor sets are named Mode A and Mode B. In each four-wire connection, the two wires associated with a pair are at the same nominal voltage. The diagram Figure 33–4 in conjunction with Table 33–7 illustrates the two power modes.

The PD shall not source power on its MDI.

PDs that implement only Mode A or Mode B are specifically not in compliance with this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not in compliance with this standard.

However, power draw at the MDI aggregate is specified in 33.3.5, and the PSE requirement not to supply both will remain.

Table 33–7—PD Pinout

Conductor	Mode A MDI	Mode A MDI-X	Mode B All
1	Negative V_{Port}	Positive V_{Port}	
2	Negative V_{Port}	Positive V_{Port}	
3	Positive V_{Port}	Negative V_{Port}	
4			Positive V_{Port}
5			Positive V_{Port}
6	Positive V_{Port}	Negative V_{Port}	
7			Negative V_{Port}
8			Negative V_{Port}

The PD may be implemented to be insensitive to the polarity of the power supply, however, the PD shall be able to operate in at least one of the PD mode A columns and the PD mode B column in Table 33–7.

Note the sensitivity of the power to the interface type in Mode A. If the twisted pair interface is implemented as an MDI per Clause 14, the wire pair (1,2) is at a lower potential than the wire pair (3,6). If the interface is implemented as an MDI-X per Clause 14, the wire pair (1,2) is at a higher potential than the wire pair (3,6).

A PD that implements Auto-MDI-X shall be polarity insensitive.

33.3.2 PD state diagram

The state diagram of the PD is shown in Figure 33–25.

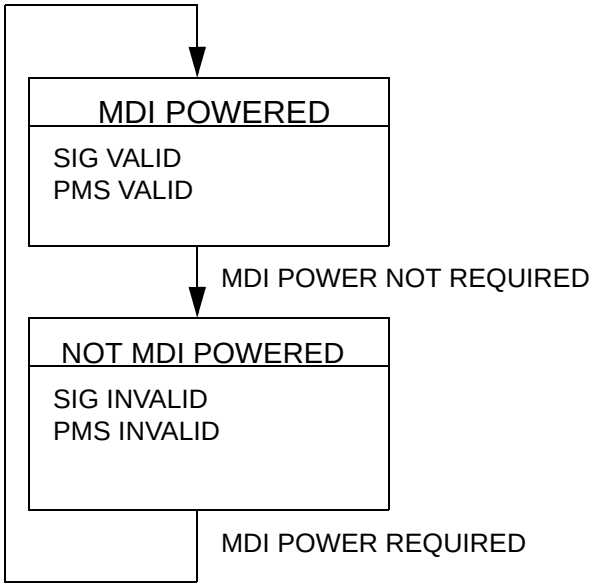


Figure 33–25—PD state diagram

33.3.3 PD detection signature

If a PD will accept power via MDI, but is not powered via MDI, then it shall present a valid detection signature at the MDI between Positive V_{Port} and Negative V_{Port} of PD mode A and between Positive V_{Port} and Negative V_{Port} of PD mode B as defined in 33.3.1.

A PD shall present an non-valid detection signature at the MDI between Positive V_{Port} and Negative V_{Port} of PD mode A and between Positive V_{Port} and Negative V_{Port} of PD mode B as defined in 33.3.1 while it is in a mode where it will not accept power via MDI.

When a PD becomes powered via the MDI, it shall present a non-valid detection signature on the set of pairs from which is it not drawing power.

The valid PD detection signature shall have the characteristics of Table 33–8.

Table 33–8—Valid PD detection signature characteristics, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
V-I Slope (at any 1V or greater chord)	2.7 - 10.1V	23.75	26.25	KΩ
V offset			1.9	V
I offset			10	µA
Input capacitance	2.7 to 10.1 V	0.05	0.11	µF
Input inductance	2.7 to 10.1 V		100	µH

V-I slope is the effective resistance calculated from the two voltage/current measurements made during the detection process.

$$\text{V-I slope} = (V_2-V_1)/(I_2-I_1) \quad (33–1)$$

Where (V_1, I_1) and (V_2, I_2) are measurements made at the PD port.

The PD current shall monotonically increase with voltage at all voltages below 28V.

A non-valid detection signature shall have one or both of the characteristics in Table 33–9.

Table 33–9—Non-valid PD detection signature characteristics, measured at PD input connector

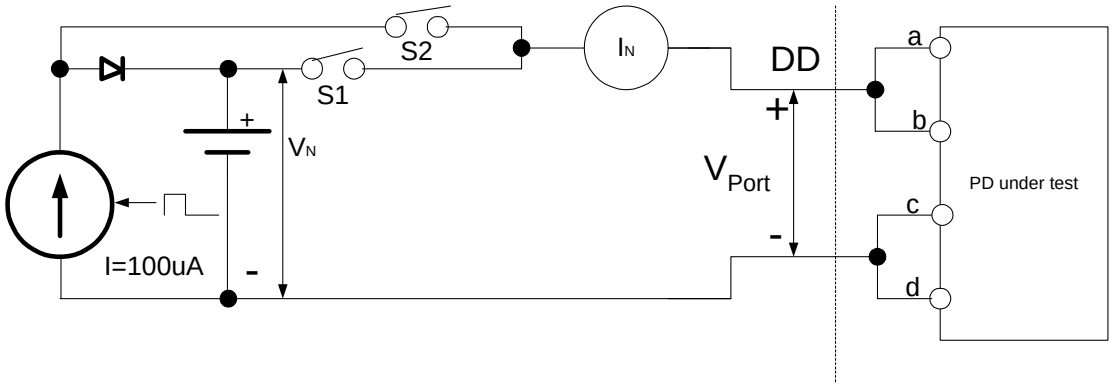
Parameter	Conditions	Range of Values	Unit
V-I Slope	V < 10.1V I < 500µA	Either greater than 45 or less than 12	KΩ
Input Capacitance	V < 10.1V	Greater than 10	µF

33.3.3.1 Test Procedure SIG-1 (PD signature characteristics)

Test Procedure SIG-1 is used for testing:

a) V-I slope (Table 33–8),
b) V offset (Table 33–8), and
c) Input capacitance (Table 33–8).

Test Procedure SIG-1 uses Test Configuration SIG-A as shown in .Figure 33–26



a=4 for alternative B or 1 for alternative A, MDI-X or 3 for alternative A, MDI or Auto MDI-X
b=5 for alternative B or 2 for alternative A, MDI-X or 6 for alternative A, MDI or Auto MDI-X
c=7 for alternative B or 3 for alternative A, MDI-X or 1 for alternative A, MDI or Auto MDI-X
d=8 for alternative B or 6 for alternative A, MDI-X or 2 for alternative A, MDI or Auto MDI-X

Figure 33–26—Test configuration SIG-A

Test Procedure SIG-1 is as follows:

1) Set S1 to ON. Set S2 to OFF. Limit the current of V_N to between 4 and 5 mA.
2) Change V_N from 2.70V to 10.1V in steps of 0.370V and measure I_N for each V_N value.
3) Calculate $Rsig_N = (V_{N+1} - V_N)/(I_{N+1} - I_N)$.
4) Verify that 23.75KΩ<=RsigN <= 26.25KΩ.
   Note: The concept of this setup is to measure the equivalent Rsig as seen at the PD port and includes all possible errors caused by series diode drops (V offset) and component accuracy.
   Psig is calculated with a minimum of two measurements to simulate PSE operation.
5) Change V_N from 0.00V to 2.70V in steps of 0.20V and measure I_N.
6) Plot the results of I_N vs V_N from steps 1 and 5 and find V offset. See Figure 33–27.
7) Set S1 to OFF. Set S2 to ON. Set V_N to 10.0V.
8) Activate the switched current source.
   Note: The concept of this setup is to calculate the capacitance value by ramping the capacitance voltage with a constant current source and using the equation I*t=V*C. This method is useful when series diodes are present.
9) Calculate the port capacitance by using the equation specified in Figure 33–28.
10) An accurate LCR meter can be used as an alternative. The test voltage should be less than 0.5Vpp.
11) Verify that the PD port capacitance is between 50nF and 110nF.

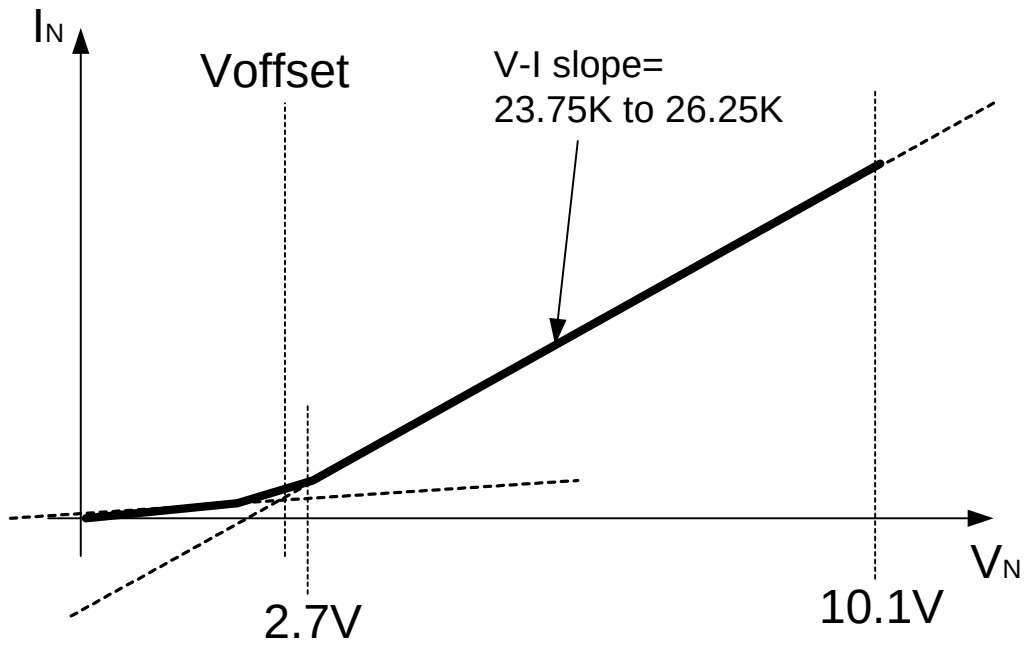
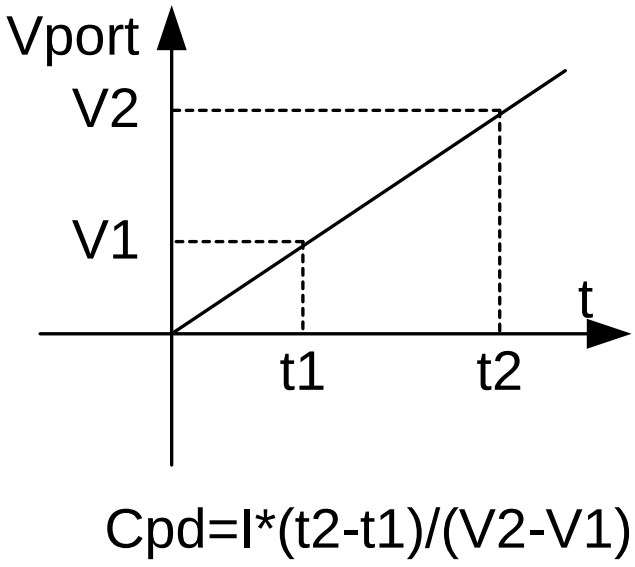


Figure 33–27—Signature voltage offset



Cpd=I*(t2-t1)/(V2-V1)

Figure 33–28—Signature input capacitance

33.3.4 PD Classifications

A PD may be classified by the PSE based on the classification information provided by the PD. The intent of PD classification is to provide information about the maximum power required by the PD during operation. Class 0 is the default for PDs and requires no more than a signature resistor. However, to improve power management at the PSE, the PD can provide a signature for Class 1 to 3.

The PD is specified based on power. The classification of the PD is the maximum power that the PD will draw across all input voltages and operational modes.

If the PD is designed to return a Class 1 to 3 classification, the selection shall be designed in accordance with the maximum power draw as specified by Table 33–10.

Table 33–10—PD Power Classification

Class	Usage	Maximum power used by the PD
0	Default	0.44 - 12.95 Watts
1	Optional	0.44 - 3.84 Watts
2	Optional	3.84 - 6.49 Watts
3	Optional	6.49 - 12.95 Watts
4	Not Allowed	Reserved for Future Use

Note: Class 4 is defined but is reserved for future use. Class 4 can not be returned by a compliant PD.

In addition to a valid detection signature, PDs that implement classification shall provide both the current characteristics and the voltage characteristics of a classification signature as specified in Table 33–11 and

Table 33–11—Classification signature, current characteristics, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
Current for Class 0	15V - 20V	0	4	mA
Current for Class 1	15V - 20V	9	12	mA
Current for Class 2	15V - 20V	17	20	mA
Current for Class 3	15V - 20V	26	30	mA
Current for Class 4	15V - 20V	36	42	mA

Table 33–12. A PD that implements classification shall present one and only one set of classification characteristics during classification and the classification shall be the same for both modes of PSE classification.

Table 33–12—Classification signature, voltage characteristics, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
Voltage for Class 0	5 to 8 mA	21		V
Voltages for Class 1	5 to 8 mA	10	14	V
	13 to16 mA	21		V
Voltages for Class 2	13 to 16 mA	10	14	V
	21 to 25 mA	21		V
Voltages for Class 3	21 to 25 mA	10	14	V
	31 to 35 mA	21		V
Voltages for Class 4	31 to 35 mA	10	14	V
	43 to 47 mA	21		V

Note: In Table 33–12 the voltage is limited by the source to 28V.

33.3.5 PD power

The power supply of the PD shall operate within the characteristics in Table 33–13.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the MDI.

Table 33–13—PD power supply limits

Item	Parameter		Unit	Min	Max	Notes
1	Input voltage	V_{Port}	Vdc	36	57	Includes loss in the cabling plant
2	Input Average Power	P_{Port}	W	$P_{Port\,1}$	12.95	See Note for Item 2
3	Port capacitance during operation	C_{Port}	µF	5	See note	See Note for Item 3
4	Ripple and noise, < 500Hz		V_{PP}		0.5	See Note for Item 4
	Ripple and noise, 500Hz - 150KHz		V_{PP}		0.2	
	Ripple and noise, 150KHz - 500KHz		V_{PP}		0.15	
	Ripple and noise, 500KHz - 1MHz		V_{PP}		0.05	
5	a) Input current in normal powering mode at PD min. input voltage V_{Port} = 37V.	I_{Port}	mADC	10	350	See Note for Item 5a
	b) Input current range in startup mode	I_{Inrush}	mA		400	See Note for Item 5b
6	a) PD Power supply turn on voltage	V_{On}	Volts		42	See Note for Item 6
	b) PD power supply turn off voltage	V_{Off}	Volts	30		

NOTES for Table 33-13

Note for Item 2: For P_{Port}:

a) Averaged over 1 second
$P_{Port1} = V_{Port} * I_{Port}$
measured when the PD is fed by 44V to 57V with 20Ω in series
I_{Port} =10mA min. for C_{port} < 180µF.

b) I_{Port} = 10mA * C_{port} [µF] /180 for C_{port} > 180µF

c) The minimum power is provided only for ease of reference, the minimum PD current draw (Table 33–13, Item 5a) and the V_{Port} are the governing values.

Note for Item 3:
While there is no max capacitance, the PD max input capacitor value and its circuitry will be designed in such a way that when a PD is connected to a PSE through series resistance of 0.1Ω to 20Ω and PSE voltage is changed from 44V to 57V, the peak current will be 0.4A max for a max duration of 50ms. Input capacitance of 180µF or less require no special input considerations.

Note for Item 4:
Output noise at the input terminals of the PD. Common mode and/or differential noise pair-to-pair values.

a) For all operating voltages in the range defined by item 1, and over the range of input power of the device.
b) The limits meant to ensure data integrity. To meet EMI standards, lower values may be needed.

Note for Item 5a: For I_{Port}:

a) I_{Port} maximum current will be equal to $12.95W/V_{Port}$ for $V_{Port} > 37V$
b) Ripple current content (I_{ac}) superimposed on the DC current level (I_{dc}) is allowed if the total current (I_{rms}) is 350mA max for a total input power of 12.95W. For $V_{Port}>37V$, $I_{rms}max=12.95/V_{Port}$ [Arms]
c) The AC current waveform parameters are limited to the following numbers:
I_p=0.4A max for 50ms max and 5% duty cycle max. For $V_{Port}>37V$, $Ip=14.4/V_{Port}$ [Ap].
The RMS, DC and ripple current are bounded by the following equation: $I_{rms}^2 = I_{dc}^2 + I_{ac}^2$.

Note for Item 5b: For I_{Inrush}:

a) I_{Inrush} is limited by the PSE for a duration of 50ms if $C_{port} < 180\mu F$ as specified in Table 33–5
b) I_{nrush} shall be limited by the PD if $C_{port} > 180\mu F$.
c) 10mA minimum current must be maintained when measured when the PD is fed by 44V to 57V with 20Ω in series.

Note for Item 6:
The PD will turn on at voltages <=42V and turn off at voltages >=30V when it is fed by a 44V-57V voltage source connected through 20Ω series resistor.
The PD should turn on and off without startup oscillation and within the first trial at any load value.

END of Notes for Table 33-13

In order to prevent the potential for oscillation, the input impedance of the PD power supply should be greater than 30 Ω at any frequency lower than the crossover frequency of the PD power supply feedback loop.

Editor's Note: *To be removed prior to final publication.*

This should refer to an Annex if a practical test methodology can be devised.

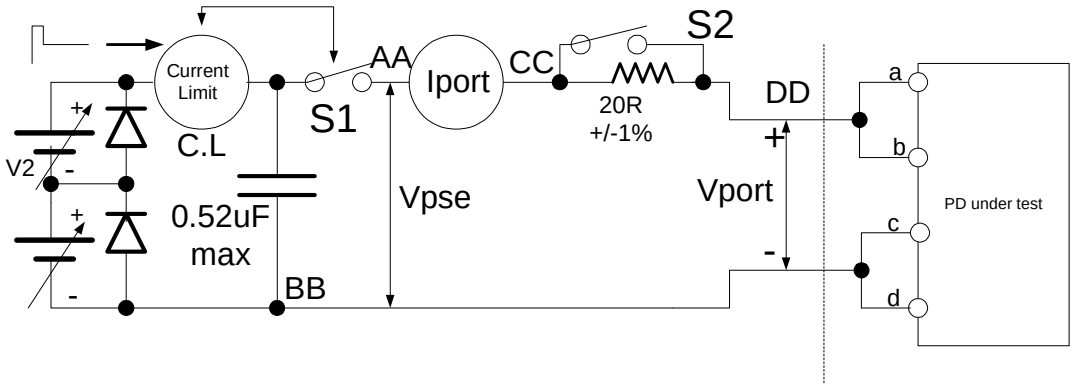
33.3.5.1 Test Procedure PD-1 (all parameters)

Test Procedure PD-1 is used for testing:

a) V_{Off} (Table 33–13, item 6b),
b) V_{On} (Table 33–13, item 6a),
c) I_{Inrush} at Vpse=44Vdc (Table 33–13, item 5b),
d) T_{Inrush} at Vpse=44Vdc (Table 33–13, item 5b),
e) I_{Inrush} at Vpse=57Vdc (Table 33–13, item 5b),
f) T_{Inrush} at Vpse=57Vdc (Table 33–13, item 5b),
g) I_{Port} (max average input current during normal powering mode at V_{Port}=37Vdc) (Table 33–13, item 5a),
h) P_{Port} (max input power at 37Vdc) (Table 33–13, item 2),

i) Max input peak current at V_{Port}=37Vdc and max load (Table 33–13, item 2),
j) I_{Port} (max average input current during normal powering mode at V_{Port}=57Vdc) (Table 33–13, item 5a),
k) P_{Port} (max input power at 57Vdc) (Table 33–13, item 2),
l) Max input peak current at V_{Port}=57Vdc and max load (Table 33–13, item 2),
m) I_{Port} (min input current at V_{Port}=37Vdc) (Table 33–13, item 5a),
n) I_{Port} (min input current at V_{Port}=57Vdc) (Table 33–13, item 5a),
o) Polarity insensitivity when PD implements Auto-MDI-X (33.3.1), and
p) PD false underload timing limitations (Table 33–13, item 2 note b).

Test Procedure PD-1 uses Test Configuration PD-A as shown in Figure 33–29.
C.L is a controlled current limit device with two threshold settings, CL1 and CL2.
CL1 and CL2 are time-limited to TCL1 and TCL2.
If I_{Port} >=CL1 for t>TCL1, then S1 is opened and test is failed.



a=4 for alternative B or 1 for alternative A, MDI-X or 3 for alternative A, MDI or Auto MDI-X
b=5 for alternative B or 2 for alternative A, MDI-X or 6 for alternative A, MDI or Auto MDI-X
c=7 for alternative B or 3 for alternative A, MDI-X or 1 for alternative A, MDI or Auto MDI-X
d=8 for alternative B or 6 for alternative A, MDI-X or 2 for alternative A, MDI or Auto MDI-X

Figure 33–29—Test configuration PD-A

Test Procedure PD-1 is as follows:

1) Set S1 to OFF. Set S2 to ON. Set V1 to 30.0V. Set CL1=CL2=1.0A.
2) Set S1 to ON. Wait 1s and verify that I_{Port}< 1.14mA(=30V/26.25KΩ)
3) Set S1 to OFF. Set S2 to OFF. Set V1 to 44.0V. Set V2=0.0V. Set CL1=CL2=0.4A,TCL1=50ms, CL2=350.0mA and TCL2=5s. Set PD for max load mode.
4) Set S1 to ON.
5) Record the following parameters: I_{Inrush}, T_{Inrush}, V_{on}. See Figure 33–30.
6) Set S1 to OFF.
7) Set V1 to 57.0V. Set S1 to ON and record the following parameters: I_{Inrush}, T_{Inrush}, V_{on}. See Figure 33–30.

8) Set S2 to ON. Set V1 = 37.0V, V2 = 0.0V, CL1 = 0.4A, TCL1=50ms, CL2=350.0mA and TCL2=5s. Set PD for max load mode.
9) Wait 1s and record Iport_dc and Iport_ac parameters. See Figure 33–30.
10) Set V1=57V and repeat steps 8,9.
11) Set S2 to ON. Set V1 = 30.0V, V2 = 0.0V, CL1 = 0.4A, TCL1=50ms, CL2=350.0mA and TCL2=5s. Set PD for max load mode.
12) Increase V1 until PD power supply turns ON. Verify that V1<=Von.
13) Set S1 to OFF. Set S2 to ON. Set V1 = 37.0V, V2 = 0.0V, CL1 = 0.4A, TCL1=50ms, CL2=350.0mA and TCL2=5s. Set PD for min load mode.
14) Set V1=57.0V. Verify that I_{Port}>= 10mA.
15) If the PD implements Auto-MDI-X, repeat steps 3, 4, and 5, and verify PD operation with reverse polarity connection.
16) Set V1=44V and V2=13V. Set PD to its minimum operating load.
17) Wait 1s until I_{Port} is stable.
18) Set S3 to OFF and monitor I_{Port}. Verify that I_{Port} is less than 10mA for only T_{UNLD}<290ms.
    If I_{Port} is not less than 10mA for any time duration, then timing requirement is ignored.
    See Figure 33–31.
19) Set S1 to OFF. Verify that I_{Port} <1.14mA at V_{Port} >30.0V. Verify that V_{Port} is less than 2.8V within 0.5s max from the time S1 was turned OFF.
    If this requirement can not be met, PD vendor shall specifically define the time required to wait after PD disconnection for reconnection to the MDI port. In any case, this time shall not be more than 5s.
20) To verify PD input capacitance during normal operating mode:
    Set S1 to OFF. Set S2 to ON. Set V1=57.0V, V2=0.0V, CL1=CL2=1.0A,TCL1=TCL2=10s. Set PD for constant load.
21) Set S1 to ON.
22) Wait 1s and measure I_{Port}.
23) Set S1 to OFF while monitoring V_{Port}. Measure the time duration, Tdrop for V_{Port} to drop from 57.0V to 56.0V.
    Calculate C=I_{Port} *Tdrop/1V. Verify that 5µF<C<180µF.
24) If C>180µF, set CL1=CL2=1.0A, TCL1=TCL2=5s.
    Repeat all tests regarding inrush current limitation and verify that inrush current is limited by the PD to 0.4A max.

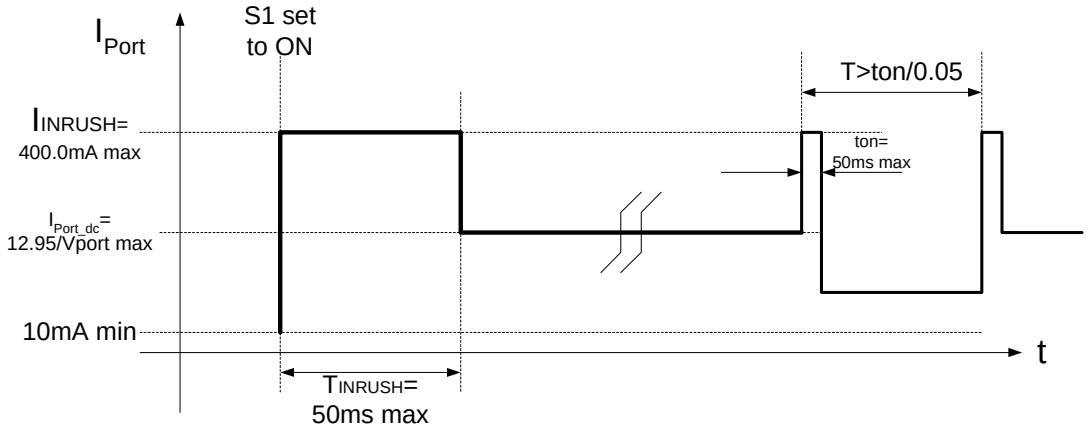


Figure 33–30—PD inrush current timing

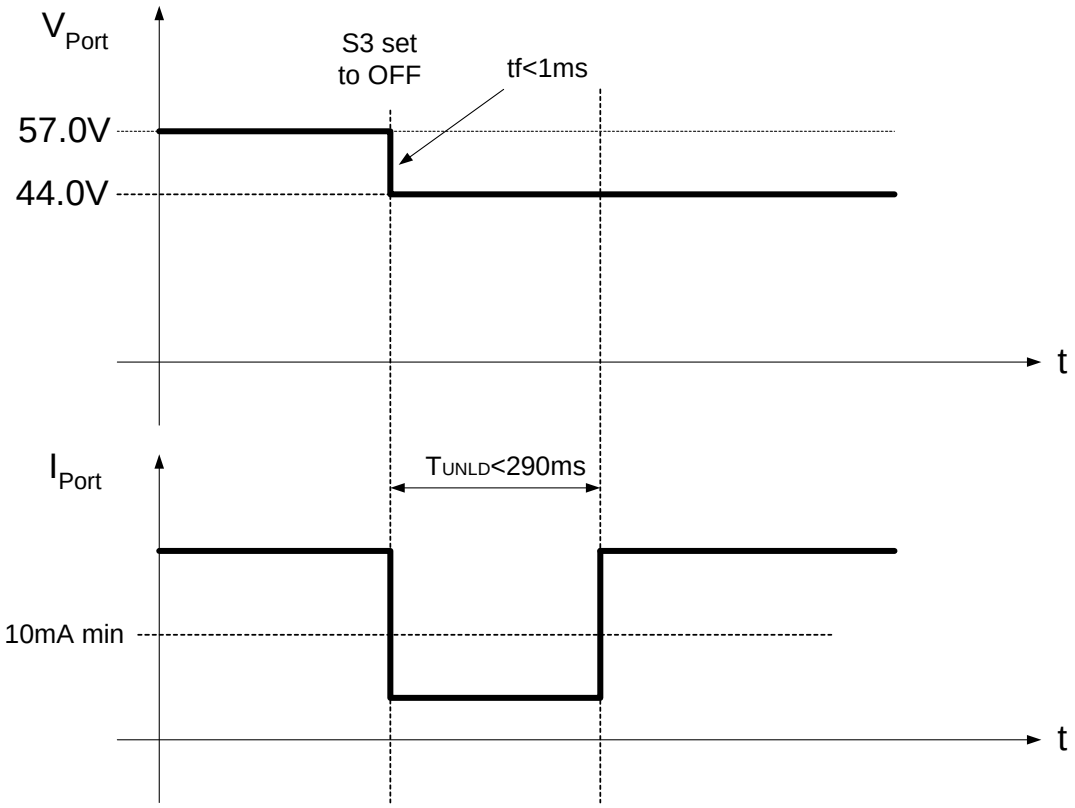


Figure 33–31—PD underload timing

33.3.6 PD power maintenance signature

In order to maintain power, the PD shall provide a valid power maintenance signature at the MDI. The power maintenance signature shall be both:

a) Current draw equal or above the minimum current draw as specified in Table 33–14
b) Ac input impedance equal to or below the max impedance defined in Table 33–14.

Table 33–14—PD power maintenance signature

Item	Parameter	Symbol	Unit	Min	Max	Notes
1	Input current	I_{in}	mA	10		
2	Input resistance	R_{pd_d}	KΩ		26.25	
3	Input capacitance	C_{pd_d}	µF	0.05		

A PD that does not maintain any one of:

a) The minimum input current as defined in Table 33–14 and
b) A max ac input impedance as specified by Table 33–14

may be disconnected from power within the limits of T_{PMDO} as specified in Table 33–5.

Powered PDs which no longer require power shall remove both components a and b of the power maintenance signature.

33.4 Electrical Specifications

This section defines the electrical specifications for both the PSE and PD. The specifications apply at the cabling side of the mated connection where power is supplied or received. When specified as an operating condition, the requirements apply without regard to the state of data transmission.

The requirements of 33.4 are consistent with the requirements of the PHYs of 10BASE-T, 100BASE-TX and 1000BASE-T. With the exception of 33.4.4, Resistance balance, no margins have been added, removed, tightened, or relaxed for Clause 33.

33.4.1 Isolation

The PSE or PD shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 Vrms at 50-60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950.
b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC 60950, during the test. The resistance after the test shall be at least 2MΩ, measured at 500 Vdc.

33.4.1.1 Electrical isolation environments

There are two electrical power distribution environments to be considered that require different electrical isolation properties.

Environment A - When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.

Environment B - When a LAN crosses the boundary between separate power distribution systems or the boundaries of a single building.

The device containing either a PSE or a PD shall comply with applicable local and national codes related to safety. See IEC 60950.

33.4.1.1.1 Environment A requirements

Attachment of network segments via network interface devices (NIDs) that have multiple instances of a twisted pair MDI requires electrical isolation between each segment and the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the basic MAU/PHY/medium standard. (See 14.3.1.1, TP-PMD, and 40.6.1.1.) Multiple instances of PSE and/or PD shall meet or exceed the isolation requirement of the MAU/PHY with which they are associated.

A multi-port NID complying with Environment A requirements does not require electrical power isolation between link segments

33.4.1.1.2 Environment B requirements

The attachment of network segments, which cross environment A boundaries, requires electrical isolation between each segment and all other attached segments and also the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the basic MAU/PHY/medium standard. (See 14.3.1.1, TP-PMD, and 40.6.1.1.) Multiple instances of PSE and/or PD shall meet or exceed the isolation requirement of the MAU/PHY with which each is associated.

The requirements for interconnected electrically conducting link segments that are partially or fully external to a single building environment may require additional protection against lightning strike hazards. Such requirements are beyond the scope of this standard.

It is recommended that the above situation be handled by the use of a non electrically conducting link segment (see Clause 15, 26 or 38).

33.4.2 Fault tolerance

Each wire pair of the PSE or PD shall, under all operating conditions, withstand without damage the application of short circuits of any wire to any other wire within the 4-pair cable for an indefinite period of time. The magnitude of the current through such a short circuit shall not exceed I_{limmax}.

Each wire pair shall withstand without damage a 1000V common-mode impulse applied at Ecm of either polarity (as indicated in Figure 33–32). The shape of the impulse shall be 0.3/50 µs (300 ns virtual front time, 50 µs virtual time or half value), as defined in IEC 60060, where Ecm is an externally applied AC voltage as shown in Figure 33–32.

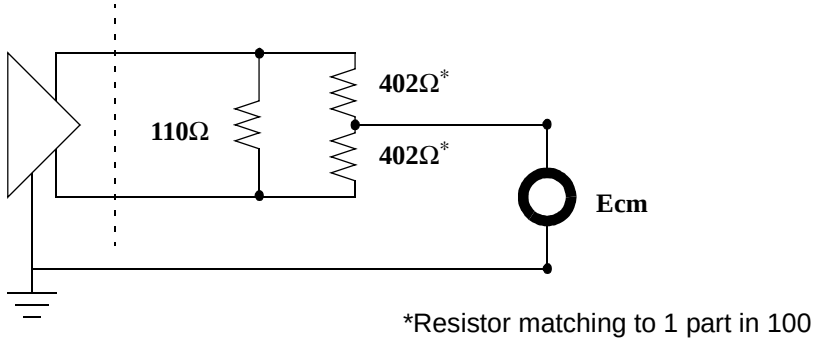


Figure 33–32—MDI fault tolerance test circuit

33.4.3 Impedance balance

Impedance balance is a measurement of the common-mode-to-differential-mode impedance balance of the MDI port. The common-mode-to-differential-mode impedance balance for the transmit and receive pairs shall exceed:

$29\text{-}17\log_{10}(f/10)\text{dB}$ (33–2)

from 2.0-20 MHz for a 10 Mbit/s PHY, and

$34\text{-}19.2\log_{10}(f/10)\text{dB}$ (33–3)

from 1.0-100 MHz for a 100 Mbit/s or greater PHY, where f is the frequency in MHz.

The impedance balance is defined as

$20\log_{10}(\text{Ecm/Edif})$ (33–4)

where Ecm is an externally applied AC voltage as shown in Figure 33–33 and Edif is the resulting waveform due only to the applied sine wave.

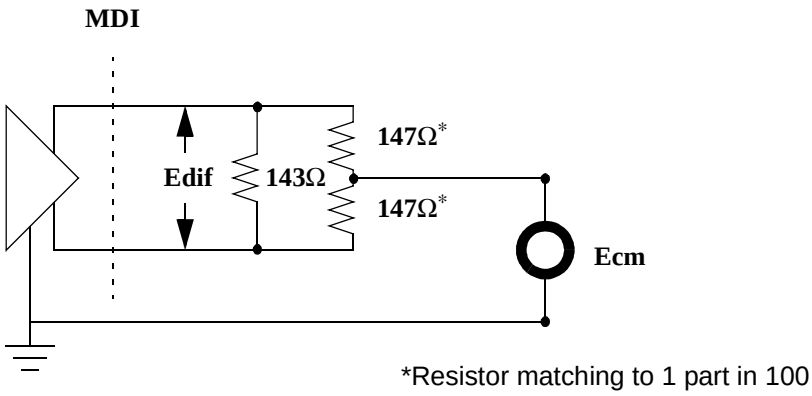


Figure 33–33—MDI impedance balance test circuit

33.4.4 Resistance balance

Resistance balance is a measure of the difference in resistance between the two conductors in the differential cabling. When conductor 1 is looped back to conductor 3 and conductor 2 is looped back to conductor 6 at the PD, the absolute difference in resistance at the PSE connector shall be less than 3.5 percent.

Editor's Note: *To be removed prior to final publication.*

A request has been made to add these specifications to ISO cable specifications. This subclause should be replaced with a reference when the specifications are included in ISO 11801 2002.

33.4.5 Common-mode output voltage

The magnitude of the total common-mode output voltage measured according to Figure 33–34 at the transmit port while transmitting data and with power applied, Ecm_out, shall not exceed 50 mV peak when operating at 10Mbit/s and 50 mV peak-to-peak when operating at 100Mbit/s or greater. The magnitude of the

common-mode AC voltage shall not exceed 50 mV peak-to-peak measured at all other ports. The frequency of the measurement shall be from 1 MHz to 100 MHz.

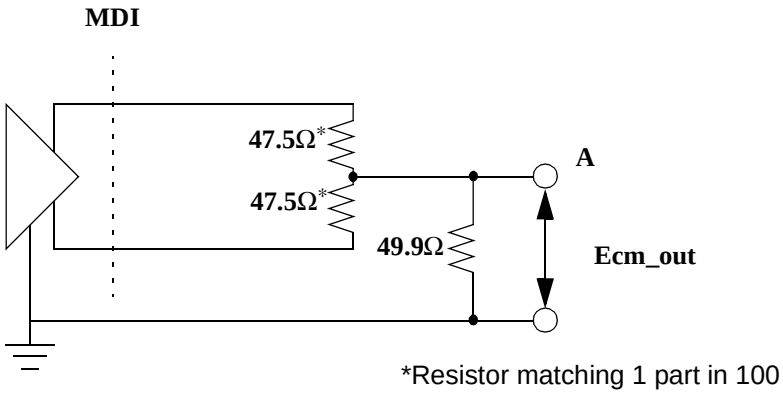


Figure 33–34—Common-mode output voltage test

NOTE - The implementor should consider any applicable local, national, or international regulations that may require more stringent specifications. One such specification can be found in the European Standard EN 55022:1998.

33.4.6 Common mode pair to pair output voltage

The common (A in Figure 33–35) to common differential AC voltage between any two pairs will be limited by the resulting electromagnetic interference due to this AC voltage. This AC voltage can be ripple from the

power supply or any other source. A system integrating a PSE shall comply with applicable local and national codes for the limitation of electromagnetic interference.

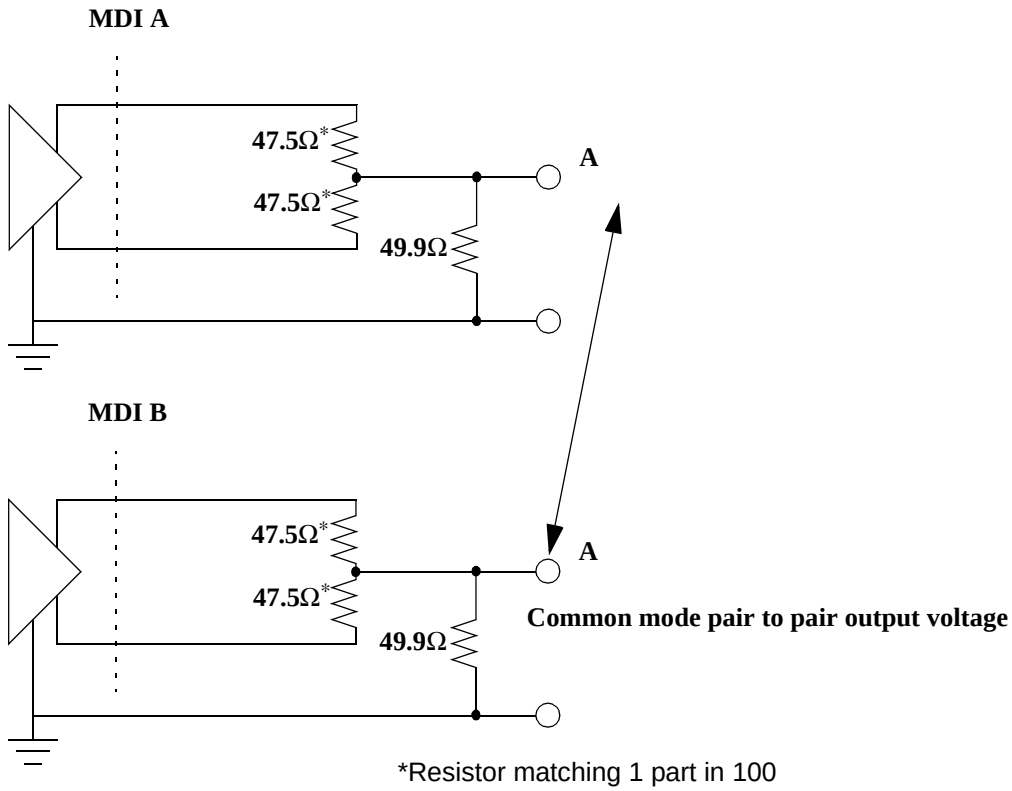


Figure 33–35—Common mode pair to pair output voltage test

33.4.7 Differential noise voltage

The noise coupled from an operating PSE to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak measured from 1 MHz to 100 MHz, when the PHY, if present, is in the condition equivalent to power-down mode of 40.8.3.

33.4.8 Return loss

While power is being applied, the differential impedance of the transmit and receive pairs at the PHY's MDI shall be such that any reflection shall meet the return loss requirements as specified in sub-clause 14.3.1.3.4 for a 10 Mbit/s PHY and sub-clause 40.8.3.1 for a 100 MBit/s or greater PHY. In addition while power is being applied all pairs terminated at a MDI should maintain a nominal common mode impedance of 75 Ω.

33.4.9 Midspan PSE device additional requirements

The cabling specifications for 100 Ω balanced cabling are described in ISO/IEC 11801-2000. The configuration of “channel” and “permanent link” is defined in Figure 33–36.

Editor’s Note: *To be removed prior to final publication.*

Some references to ISO 11801 in this clause require additions proposed for the revision underway. Other requirements are addressed by ISO 11801: 2000. If ISO 11801: 2002 is available at publication, The Clause 1 reference should be updated to the 2002 version. If the revision is not approved at publication, the reference should be replaced by ANSI/TIA/EIA 568-B.2.

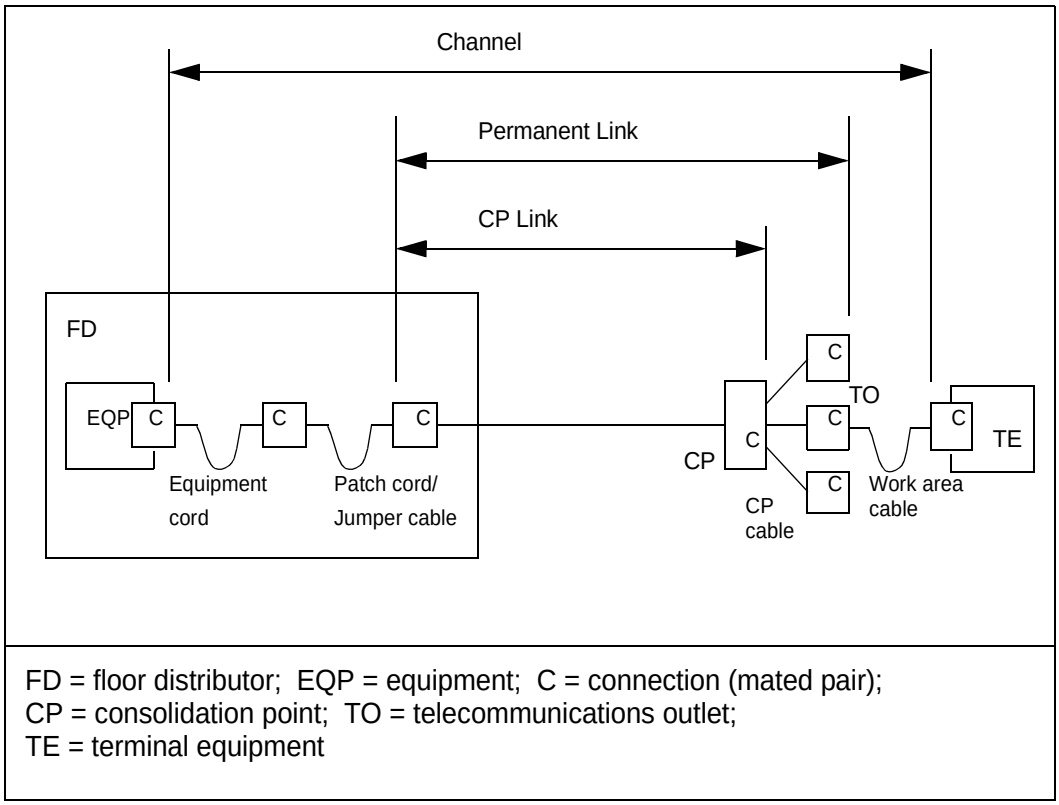


Figure 33–36—Channel configuration

The ISO/IEC 11801 defines in Para. 5.6.1 two types of Equipment interface to the cabling system: “Interconnect model” and the “cross-connect model”, see Figure 33–37.

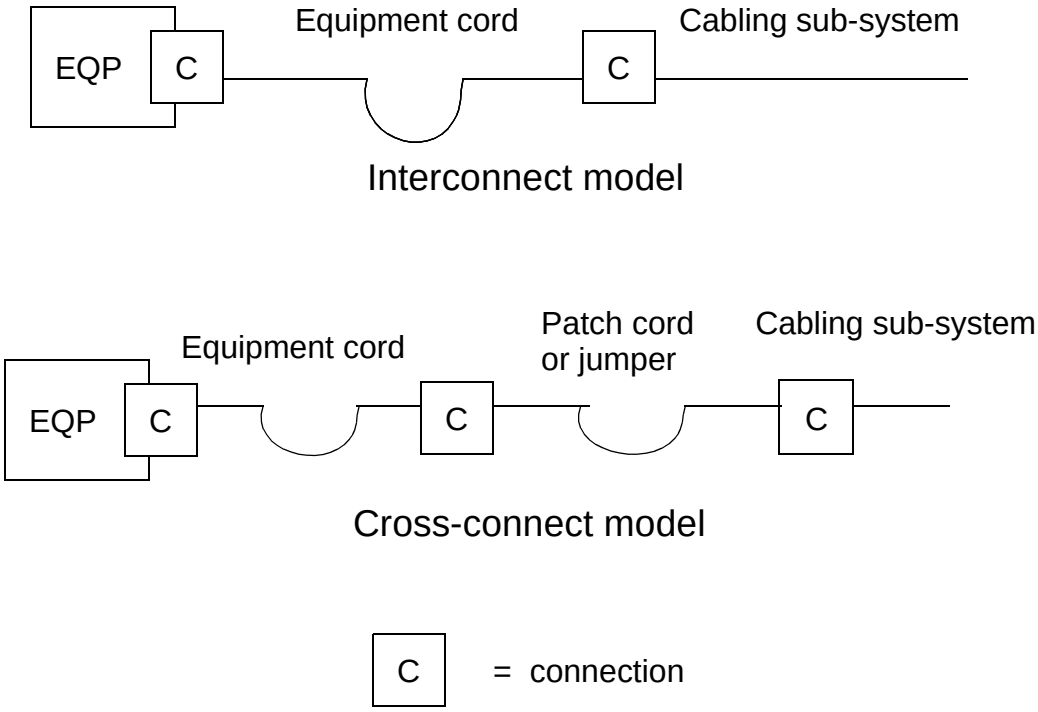


Figure 33–37—Interconnect and cross-connect models

The insertion of a PSE at the FD (Floor Distributor) shall comply with the following guidelines:

a) If the existing FD configuration is of the "Interconnect model" type, the PSE can be added, provided it does not increase the length of the resulting "channel" to more than specified 100 meters as defined in ISO/IEC 11801.
b) If the existing FD configuration is of the "channel" interconnect model, the PSE needs to be installed instead of one of the connection pairs in the FD. In addition, the installation of the PSE shall not increase the length of the resulting "channel" to more than specified 100 meters as defined in ISO/IEC 11801.

Configurations with the PSE in the cabling channel shall not alter the transmission requirements of the "permanent link". The inclusion of the PSE in the channel may reflect in channel continuity for the signal pairs only, as spare pairs on which power is injected may be discontinued at the PSE.

The requirements for the two pair category 5 channel are found in 25.4.6.

Note: Appropriate terminations should be applied to the interrupted pairs on both sides of the midspan device.

33.4.9.1 "Connector" or "Telecom outlet" PSE Transmission requirements

The PSE equipment to be inserted, as "Connector "or" Telecom outlet" shall meet the following transmission parameters.

33.4.9.1.1 NEXT (Near End Cross-Talk)

NEXT loss is a measure of the unwanted signal coupling from a transmitter at the near-end into neighboring pairs measured at the near-end. NEXT loss is expressed in dB relative to the received signal level. NEXT loss shall be measured for midspan PSE devices for all transmit and receive pair combinations from 1 MHz to 100 MHz and shall meet the values determined by Equation 33-5. However, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB.

$$NEXT_{conn} > 40 - 20\log(f/100)\text{dB} \qquad (33\text{–}5)$$

33.4.9.1.2 Insertion loss

Insertion loss is a measure of the signal loss between the transmitter and receiver, expressed in dB relative to the received signal level. Insertion loss shall be measured for midspan PSE devices for all transmit and receive pairs from 1 MHz to 100 MHz, and shall meet the values determined by Equation 33-6. However, for frequencies that correspond to calculated values less than 0.1 dB, the requirement reverts to the maximum requirement of 0.1 dB.

$$Insertion\_loss_{conn} < 0.04\ SQRT(f)\ \text{dB} \qquad (33\text{–}6)$$

33.4.9.1.3 Return loss

Return loss is a measure of the reflected energy caused by impedance mismatches in the cabling system and is expressed in dB relative to the reflected signal level. Return loss shall be measured for midspan PSE devices for all transmit and receive pairs from 1 MHz to 100 Mhz and shall meet or exceed the values specified in Table 33–15.

Table 33–15—Cross-connect return loss

Frequency	Return Loss
1 MHz <f <20 MHz	23 dB
20 MHz <f <100 MHz	14 dB

33.4.9.1.4 Work area or equipment cable PSE

Replacing the work area or equipment cable with a cable that includes a PSE should not alter the requirements of the cable. This cable shall meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801-2002 for insertion loss, NEXT, FEXT, return loss, and delay for all transmit and receive pairs.

33.5 Environmental

33.5.1 General safety

All equipment meeting this standard shall conform to IEC publication 60950.

Equipment shall comply with all applicable local and national codes related to safety.

33.5.2 Network safety

This clause sets forth a number of recommendations and guidelines related to safety concerns. The list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements. LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification of an existing network.

33.5.3 Installation

It is a mandatory functional requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

33.5.4 Patch Panel Considerations

It is possible that the current carrying capability of a cabling cross-connect may be exceeded by a PSE. The designer should consult the manufacturers specifications to ensure compliance with the appropriate requirements.

33.5.5 Installation and maintenance guidelines

It is a mandatory functional requirement that, during installation of the cabling plant, care be taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

33.5.6 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to a PSE or PD. Other than voice signals, the primary voltages that may be encountered are the ‘battery’ and ringing voltages. Although there is no universal standard, the following maximums generally apply:

Battery voltage to a telephone line is generally 56 Vdc, applied to the line through a balanced 400 Ω source impedance. Ringing voltage is a composite signal consisting of an AC component and a DC component. The AC component is up to 175 V peak at 20 Hz to 60Hz with a 100 Ω source resistance. The DC component is 56 VDC with 100-600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Application of any of the above voltages to a PSE or a PD shall not result in any safety hazard.

33.5.7 Electromagnetic emissions

The PD and PSE powered cabling link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

33.5.8 Temperature and humidity

The PD and PSE powered cabling link segment is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling. Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

33.5.9 Labeling

It is recommended that the PSE (and supporting documentation) or PD be labeled in a manner visible to the user with at least the following parameters:

a) Power level in terms of maximum current drain at nominal voltage,
b) Port type (e.g. 100BASE-TX, TIA Category or ISO Class),
c) Any applicable safety warnings, and
d) “PSE” or “PD” as appropriate.

33.6 Management function requirements

The MII Management Interface (see 22.2.4) is used to communicate PSE and PD information to the management entity. If a Clause 22 MII or a Clause 35 GMII is physically implemented, then management access is via the MII Management interface. Where no physical embodiment of the MII or GMII exists, equivalent management capability must be provided.

33.6.1 PHY specific registers for PSE and PD

Some of the extended registers (registers with addresses 2 to 15) are used as PHY specific registers as described in 22.2.4.3. A PSE shall use register address 11 for its control and register address 12 for its status functions. A PD shall use register address 12 for its status functions.

Some of the bits within registers are defined as latching high (LH). When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

33.6.1.1 PSE control register (Register 11) (R/W)

The assignment of bits in the PSE Control register is shown in Table 33–16 below. The default value for each bit of the PSE Control register should be chosen so that the initial state of the PSE upon power up or reset is a normal operational state without management intervention.

33.6.1.1.1 Reserved bits (11.15:5)

Bits 11.15:5 are reserved for future standardization. They shall not be affected by writes and shall return a value of zero when read. To ensure compatibility with future use of reserved bits and registers, the Management Entity should write to reserved bits with a value of zero and ignore reserved bits on read.

33.6.1.1.2 Detection Control (11.4)

Bit 11.4 controls the current mode of operation of the PD Detection function specified in 33.2.3. Setting bit 11.4 to ‘0’ enables the PD Detection function to operate normally. Setting bits 11.4 to ‘1’ places the PD Detection function in a test mode. When placed in this test mode the PD function shall operate normally with the exceptions that power shall not be supplied if a valid PD is detected and power shall be remove from a valid PD that has already been detected.

Table 33–16—PSE Control register bit definitions

Bit(s)	Name	Description	R/W[a]
11.15:5	Reserved	Ignore when read	RO
11.4	Detection Control (11.4)	1 = PD Detection test mode 0 = PD Detection normal	R/W
11.3:2	Pair Control (11.3:2)	11.3 11.2 1 1 = Reserved 1 0 = PSE pinout alternative B 0 1 = PSE pinout alternative A 0 0 = Reserved	R/W
11.1	PSE Pwr Force On - Test (11.1)	1 = Test mode enabled to force power sourcing 0 = Normal operation	R/W
11.0	Power Enable (11.0)	1 = Enable PSE functions 0 = Disable PSE functions	R/W

[a]R/W = Read/Write, RO = Read Only, LH = Latching High

33.6.1.1.3 Pair Control (11.3:2)

Bits 11.3:2 report the supported PSE Pinout Alternative specified in 33.2.1. A PSE may also provide the option of controlling the PSE Pinout Alternative through these bits. Provision of this option is indicated through the Pair Control Ability (12.1) bit. A PSE that does not support this option shall ignore writes to these bits and shall return the value that reports the supported PSE Pinout Alternative.

When read as ‘01’ bits 11.3:2 indicates that only PSE Pinout Alternative A is supported by the PSE. When read as ‘10’ bits 11.3:2 indicates that only PSE Pinout Alternative B is supported by the PSE.

Where the option of controlling the PSE Pinout Alternative through these bits is provided setting bits 11.3:2 to ‘01’ shall force the PSE to use only PSE Pinout Alternative A and setting bits 11.3:2 to ‘10’ shall force the PSE to use only PSE Pinout Alternative B.

The combinations ‘00’ and ‘11’ have been reserved for future use.

33.6.1.1.4 PSE Pwr Force On - Test (11.1)

When set to a logic one, bit 11.13 enables a test mode which supplies power without regard to detection. When set to a logic zero, normal operation is selected and detection mode controls the sourcing of power.

33.6.1.1.5 Power Enable (11.0)

The PSE function shall be enabled by setting bit 11.0 to a logic one. The PSE function shall be disabled by setting bit 11.0 to logic zero. When the PSE function is disabled by this bit the MDI shall function as it would if it had no PSE function.

Note - This bit can not be used to force power onto the MDI, merely to enable the PSE to provide power onto the MDI if a valid PD is detected.

33.6.1.2 PSE/PD status register (Register 12) (R/W)

The assignment of bits in the PSE/PD Status register is shown in Table 33–17 below.

Table 33–17—PSE/PD Status register bit definitions

Bit(s)	Name	Description	R/W[a]
12.15:10	Reserved	Ignore when read	RO
12.9	Overcurrent (12.9)	1 = Overcurrent condition detected 0 = No overcurrent condition detected	RO/ LH
12.8	Undercurrent (12.8)	1 = Undercurrent condition detected 0 = No undercurrent condition detected	RO/ LH
12.7:5	PD Class (12.7:5)	12.7 12.6 12.5 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Reserved 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Class 0	RO
12.4:2	Detection Status (12.4:2)	12.4 12.3 12.2 1 1 1 = Reserved 1 1 0 = Test mode 1 0 1 = Invalid PD 1 0 0 = Fault 0 1 1 = Delivering powering 0 1 0 = Detected 0 0 1 = Searching 0 0 0 = Disabled	RO
12.1	Pair Control Ability (12.1)	1 = PSE pinout controllable by Pair Control bits 0 = PSE pinout alternative fixed	RO
12.0	Power Pair Status (12.0)	1 = PD sinking power 0 = PD not sinking power	RO

[a]RO = Read Only

33.6.1.2.1 Reserved bits (12.15:10)

Bits 12.15:10 are reserved for future standardization. They shall not be affected by writes and shall return a value of zero when read. To ensure compatibility with future use of reserved bits and registers, the Management Entity should write to reserved bits with a value of zero and ignore reserved bits on read.

33.6.1.2.2 Overcurrent (12.9)

When read as a logic one, bit 12.9 indicates that an overcurrent condition has been detected. An overcurrent condition shall be detected when the current drawn from the PSE at the MDI is greater than the overload current limit for a duration greater than the overload time limit (see Table 33–5).The Overcurrent bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.3 Undercurrent (12.8)

When read as a logic one, bit 12.8 indicates that an undercurrent condition has been detected. An undercurrent condition shall be detected when the current drawn from the PSE at the MDI is less than I_{UDL} for a

duration greater than T_{PMDO} (see Table 33–5). The Undercurrent bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.4 PD Class (12.7:5)

Bits 12.7:5 report the PD Class classification of a detected PD as specified in 33.2.5 and 33.2.6. The value in this register is valid only when the Detection Status (12.4:2) bits are reporting that a valid PD has been detected.

The combinations ‘101’, ‘110’ and ‘111’ have been reserved for future use.

33.6.1.2.5 Detection Status (12.4:2)

Bits 12.4:2 report the current state of the PD Detection function specified in 33.2.3. When read as ‘000’ bits 12.4:2 indicates that the PD Detection function has been disabled. When read as ‘001’ bits 12.4:2 indicates that the PD Detection function is enabled and is searching for a valid PD. When read as ‘010’ bits 12.4:2 indicates that the PD Detection function has detected a valid PD but the PSE is not supplying power. When read as ‘011’ bits 12.4:2 indicates that the PD Detection function has detected a valid PD and the PSE is supplying power. When read as ‘100’ bits 12.4:2 indicates that the PD Detection function has detected a fault, faults detected are implementation-specific. When read as ‘101’ bits 12.4:2 indicates that the PD Detection function has detected an invalid PD. When read as ‘110’ bits 12.4:2 indicates that the PD Detection function has been placed in test mode

The combination ‘111’ has been reserved for future use.

33.6.1.2.6 Pair Control Ability (12.1)

When read as a logic one, bit 12.1 indicates that the PSE supports the option to control which PSE Pinout Alternative (see 33.2.1) is used for PD detection and power through the Pair Control (11.3:2) bits. When read as a logic zero, bit 12.1 indicates that the PSE lacks support of the option to control which PSE Pinout Alternative is used for PD detection and power through the Pair Control (11.3:2) bits.

33.6.1.2.7 Power Pair Status (12.0)

When read as a zero, bit 12.0 indicates that the PD is drawing a current less than I_{Port} as specified in Table 33–11. When read as a logic one, bit 12.0 indicates that the PD is drawing a current greater than the minimum value of I_{Port} as specified in Table 33–13.

33.7 Protocol Implementation Conformance Statement (PICS) proforma for Clause 33, DTE Power via MDI

33.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3af-200x, DTE Power via MDI, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

33.7.2 Identification

33.7.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

33.7.2.2 Protocol Summary

Identification of protocol standard	IEEE Std 802.3af-200x, Clause 33, DTE Power via MDI
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to the standard.)	
Date of Statement	

33.7.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
CL	Implementation supports classification	33.2.7	N/A	O	Yes [ ] No [ ]
MC	Classification uses the measured Current method	33.2.7.2	N/A	O	Yes [ ] No [ ]
MV	Classification uses the measured Voltage method	33.2.7.3	N/A	O	Yes [ ] No [ ]
PA	Implement a PSE which does not contain a power supply capable of supplying maximum power to all the devices that could possibly connect to it.	33.2.10	N/A	O	Yes [ ] No [ ]
PCA	Pair control ability - PSE supports the option to control which PSE Pinout is used	33.6.1.1.3	N/A	O	Yes [ ] No [ ]

33.7.3 PICS proforma Tables for DTE Power via MDI

33.7.3.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	Compatible at MDI	33.1	All implementations of twisted-pair link.	M	Yes [ ]
G2	Support PHYs defined in Clauses 14, 25 and 40	33.1	Only supports the use of the twisted pair PHYs defined by these clauses.	M	Yes [ ]
G3	Power source	33.1	To add power to the 100 Ω balanced cabling system,	M	Yes [ ] N/A [ ]
G4	Detection	33.1	Detecting a device that requires power.	M	Yes [ ] N/A [ ]
G5	Classification	33.1	Classify devices based on their power needs.	O	Yes [ ] N/A [ ]
G6	Any MDI compliant with clauses 14, 25 and 40 is allowed	33.1.1	Defined as a PD if sinking power and a PSE of sourcing power.	M	Yes [ ]
G7	Connection	33.1.2	No additional connection other that the MDI	M	Yes [ ]
G8	SELV	33.1.2	PSE designed to the standard will not introduce non-SELV (safety extra low voltage) power into the wiring plant.	M	Yes [ ]
G9	MDI	33.1.2	Use MDI for clauses 14, 25 and 40 without modification	M	Yes [ ]
G10	Simplicty	33.1.2	No more burdensome on the end users than the requirements of 10BASE-T, 100BASE-TX, or 1000BASE-T.	M	Yes [ ]

33.7.3.2 Power sourcing equipment

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	Implement alternative A, alternative B, or both	33.2.1	No preference on alternative.	M	Yes [ ]
PSE2	Alternative A and alternative B	33.2.1	Not operate on same link segment simultaneously	M	Yes [ ]
PSE3	Midspan PSE and Endpoint PSE	33.2.2	The requirements of this document shall apply equally to both unless the specified otherwise.	M	Yes [ ]
PSE4	Midspan PSE use alternative B	33.2.2	Limited to operation with 10BASE-T and 100BASE-TX systems.	M	Yes [ ]
PSE5	Apply power.	33.2.4	Only after PD detection	M	Yes [ ]
PSE6	PD detection	33.2.4	Operate without regard to the data link status	M	Yes [ ]
PSE7	Detect PD	33.2.5	Executed by probing via the PSE MDI interface	M	Yes [ ]
PSE8	Open circuit voltage	33.2.5	Less than 30V	M	Yes [ ]
PSE9	Short circuit current	33.2.5	Less than 5mA	M	Yes [ ]
PSE10	Output capacitance	33.2.5	520nF maximum during detection.	M	Yes [ ]
PSE11	Exhibit Thevenin equivalence to one of the detection circuits in all detection states	33.2.5	Figure 33–6 or Figure 33–7.	M	Yes [ ]
PSE12	Detection voltage V_{detect} with a valid PD signature connected	33.2.5.1	2.8 to 10 V	M	Yes [ ]
PSE13	Two measurements with V_{detect}	33.2.5.1	At least 1 V difference between the two measurements	M	Yes [ ]
PSE14	Control slew rate when switching detection voltages	33.2.5.1	Less than 0.1V/µs	M	Yes [ ]
PSE15	Polarity of V_{detect}	33.2.6	Match polarity of V_{Port} defined in 33.2.1	M	Yes [ ]
PSE16	Probe link to detect all PDs which present a valid signature	33.2.6.1	(19KΩ to 26.5KΩ DC resistance) * (120nF capacitance or less) * (Voltage offset of at least 2.0 volts DC) * (Current offset of a least 12µA)	M	Yes [ ]
PSE17	Reject PDs which present an invalid signature	33.2.6.2	(Less than 15 KΩ DC resistance) + (More than 33 KΩ DC resistance) + (More than 10µF capacitive load)	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE18	Turn on power	33.2.6.3	Only on the same pairs as those used for detection.	M	Yes [ ]
PSE19	Provide V_{Class}	33.2.7.2	Between 15 and 20 volts, limited to 100 mA or less with the same polarity as V_{Port}.	MC:M	Yes [ ] N/A [ ]
PSE20	Measure I_{Class}	33.2.7.2	Classify PD according to Table 33–3	MC:M	Yes [ ] N/A [ ]
PSE21	Provide I_{Class}	33.2.7.3	Limited to less that 47mA, with V_{Class} limited to less than 30 volts with the same polarity as V_{Port}.	MV:M	Yes [ ] N/A [ ]
PSE22	Measure V_{Class}	33.2.7.3	Classify PD according to Table 33–4.	MV:M	Yes [ ] N/A [ ]
PSE23	Class 1-4 measured voltage	33.2.7.3	Meet requirement in each of the two current ranges	MV:M	Yes [ ] N/A [ ]
PSE24	Time limit before PSE is to apply power if PSE is going to apply power	33.2.8	Within T_{tot} after start of detection / classification cycle.	M	Yes [ ]
PSE25	Detection and Classification timing	33.2.8	Meet specifications in Table 33–5	M	Yes [ ]
PSE26	Time to turn on power after a valid detection if power is to be applied	33.2.8	Less 400ms.	M	Yes [ ]
PSE27	Alternative B backoff.	33.2.8.1	Failing to detect a valid PD signature backoff no less than $T_{dbot.}$	M	Yes [ ]
PSE28	PSE output voltage during backoff period	33.2.8.1	Not greater than 1 volt.	M	Yes [ ]
PSE29	PSE source power to MDI	33.2.9	According to Table 33–5	M	Yes [ ]
PSE30	Absence of PD power maintenance signal	33.2.9	PSE remove power within 400 ms (Table 33–5, item7).	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE31	Time to remove power upon detection of an overload current condition	33.2.9	After time duration of T_{ovld} the PSE shall disconnect power from the port. (Table 33–5, item 8).	M	Yes [ ]
PSE32	Overload time limit (T_{ovld})	33.2.9	350mA < I_{CUT} < 400mA for 50ms <T_{ovld} < 75ms (Table 33–5, item 9).	M	Yes [ ]
PSE33	Open current or short circuit condition.	33.2.9	The power must be disconnected from the port within 50ms <= T_{LIM} <= 75ms (Table 33–5, item 10)	M	Yes [ ]
PSE34	Safety	33.2.9	PSE comply with applicable local and national codes.	M	Yes [ ]
PSE35	PSE port parameters for AC disconnect-detection function	33.2.9	Table 33–6	M	Yes [ ]
PSE36	AC power maintenance signature	33.2.9	Values for Z_{ac}: If Zac = 33KΩ do not remove power, if Zac = 500KΩ remove power.	M	Yes [ ]
PSE37	Power provision	33.2.10	Do not initiate if PSE is unable to provide maximum power level requested by PD based on PD's classification.	PA:M	Yes [ ] N/A [ ]
PSE38	Power removal	33.2.11	When PD is removed or no longer maintains the power maintenance signature	M	Yes [ ]
PSE 39	Monitor power maintenance signature	3322.11	DC current (Table 33–5, item 6) and/or AC impedance (Table 33–6).	M	Yes [ ]
PSE40	Remove power.	33.2.11	Within limits of T_{PMDO} (Table 33–5)	M	Yes [ ]

33.7.3.3 Powered Devices

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Accept power	33.3.1	On either set of MDI conductors.	M	Yes [ ]
PD2	Source power	33.3.1	The PD will not source power on its MDI	M	Yes [ ]
PD3	PD pinout	33.3.1	Support at least one Mode-A column and Mode-B defined in Table 33–7.	M	Yes [ ]
PD4	Auto-MDI-X PD	33.3.1	Polarity insensitive.	M	Yes [ ]
PD5	Valid detection signature	33.3.3	Presented on each set of pairs defined in 33.3.1 if not powered via the MDI.	M	Yes [ ]
PD6	Invalid detection signature	33.3.3	Presented on each set of pairs defined in 33.3.1 if not powered via the MDI and will not accept power via the MDI.	M	Yes [ ]
PD7	Invalid detection signature	33.3.3	When powered present an invalid signature on the set of pairs not drawing power	M	Yes [ ]
PD8	Valid detection signature	33.3.3	Characteristics defined in Table 33–8.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PD9	PD current	33.3.3	Monotonically increase with voltage at all voltages below 28V.	M	Yes [ ]
PD10	Invalid detection signature	33.3.3	Exhibit one or both of the characteristics described in Table 33–9	M	Yes [ ]
PD11	Return Class 1 to 3 classification	33.3.4	Implement classification selection according to maximum power draw specified in Table 33–10	CL:M	Yes [ ] N/A [ ]
PD12	Classification	33.3.4	Provide both the current characteristics and the voltage characteristics of a classification signature as specified in Table 33–11 and Table 33–12.	CL:M	Yes [ ] N/A [ ]
PD13	Classification presentation	33.3.4	One and only one set of classification characteristics during classification and the classification shall be the same for both modes of PSE classification.	CL:M	Yes [ ] N/A [ ]
PD14	Classification characteristics	33.3.4	Implement identical classification for each PSE mode	CL:M	Yes [ ] N/A [ ]
PD15	PD power	33.3.5	Operate within the characteristics in Table 33–13.	M	Yes [ ]
PD16	Input current range (startup mode)	33.3.5	Limited by PSE for 50mS if C_{port} < 180µF. Limited by PD if C_{port} > 180µF	M	Yes [ ]
PD17	Power maintenance signature	33.3.6	(current draw) * (AC impedance) defined in Table 33–14	M	Yes [ ]
PD18	No longer require power	33.3.6	Remove both components of the power maintenance signature.	M	Yes [ ]

33.7.3.4 Electrical Specifications

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Electrical isolation (PD and PSE)	33.4.1	Provided between port device circuits, frame ground and MDI leads	M	Yes [ ]
EL2	Strength tests for electrical separation	33.4.1	Withstand at least one electrical strength tests specified in 33.4.1	M	Yes [ ]
EL3	Insulation breakdown during electrical strength tests	33.4.1	None.	M	Yes [ ]
EL4	Resistance after electrical strength test	33.4.1	>= 2MΩ, measured at 500 Vdc	M	Yes [ ]
EL5	Safety (PD and PSE)	33.4.1.1	Comply with applicable local and national codes.	M	Yes [ ]
EL6	Environment A requirements for multiple instances of PSE and/or PD	33.4.1.1.1	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated.	M	Yes [ ] N/A [ ]
EL7	Environment B requirements for multiple instances of PSE and/or PD	33.4.1.1.2	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated.	M	Yes [ ] N/A [ ]
EL8	Fault tolerance	33.4.2	Any wire pair will withstand any short circuit to any other pair for an infinite amount of time	M	Yes [ ]
EL9	Magnitude of short circuit current	33.4.2	Not to exceed I_{limmax}	M	Yes [ ]
EL10	Fault tolerance	33.4.2	Each wire pair will withstand a 1000V common-mode impulse applied at Ecm of either polarity without damage	M	Yes [ ]
EL11	The shape of the impulse for item EL10	33.4.2	0.3/50 µs (300 nS virtual front time, 50 µs virtual time of the half value)	M	Yes [ ]
EL12	Impedance balance for transmit and receive pairs:	33.4.3	Exceed: - 29-17 log 10 (f/10)dB from 2.0 to 20MHz for 10Mbit/s PHYs - 34-19.2 log 10 (f/10)dB from 1.0 to 100MHz for 100Mbits/s or greater PHYs.	M	Yes [ ]
EL13	Resistance balance	33.4.4	When pair (1,2) is looped back to pair (3,6) at the PD the absolute resistance at the PSE connector will be less than 3.5%.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
EL14	Common-mode output voltage	33.4.5	Magnitude while transmitting data and with power applied will not exceed 50mV peak when operating at 10Mbits/s and 50mV peak-to-peak when operating at 100Mbits/s or greater	M	Yes [ ]
EL15	Common-mode AC voltage	33.4.5	Magnitude at all other ports will not exceed 50mV peak-to-peak	M	Yes [ ]
EL16	Frequency range for common-mode AC voltage measurement	33.4.5	At all other ports will be from 0.15 MHz to 100MHz	M	Yes [ ]
EL17	Limitation of electromagnetic interference	33.4.6	PSE will comply with applicable local and national codes.	M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
EL18	Noise from an operating PSE to the differential transmit and receive pairs	33.4.7	Will not exceed 10mV peak-to-peak measured from 0.15MHz to 100MHz	M	Yes [ ]
EL19	Return loss requirements	33.4.8	Specified in subclause 14.3.1.3.4 for a 10 Mbit/s PHY and sub-clause 40.8.3.1 for a 100 MBit/s or greater PHY.	M	Yes [ ]
EL20	Insertion of a PSE at the FD (Floor Distributor)	33.4.9	See subclause 33.4.9 bullets a) and b).	M	Yes [ ] N/A [ ]
EL21	Resulting “channel”	33.4.9	Installation of a PSE not increase the length to more than 100 meters as defined in ISO/IEC 11801.	M	Yes [ ] N/A [ ]
EL22	PSE in the cabling channel	33.4.9	Not alter transmission require-ments of "permanent link"	M	Yes [ ]
EL23	PSE inserted as a "Connector" or "Telecom outlet"	33.4.9.1	Meet transmission parameters NEXT, insertion loss and return loss	M	Yes [ ] N/A [ ]
EL24	PSE NEXT	33.4.9.1.1	$NEXT_{conn} > 40 - 20\log(f/100)$dB (equation 33–5) but not greater than 65 dB from from 1 MHz to 100 MHz,.	M	Yes [ ] N/A [ ]
EL25	PSE Insertion Loss	33.4.9.1.2	$Insertion\_loss_{conn} < 0.04$ SQRT(f) dB (equation 33–6) but not less than 0.1 dB from from 1 MHz to 100 MHz,.	M	Yes [ ] N/A [ ]
EL26	PSE Return Loss	33.4.9.1.3	1 MHz $< f <$20 MHz 23 dB 20 MHz $< f <$100 MHz 14 dB (Table 33–15)	M	Yes [ ] N/A [ ]
EL27	Work area or equipment cable PSE	33.4.9.1.4	Meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801-2002 for insertion loss, NEXT, FEXT, return loss, and delay for all transmit and receive pairs.	M	Yes [ ] N/A [ ]

33.7.3.5 Environmental Specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Safety	33.5.1	Conform to IEC publication 60950.	M	Yes [ ]
ES1	Safety	33.5.1	Comply with all applicable local and national codes.	M	Yes [ ]
ES2	Telephony voltages	33.5.5	Application thereof described in 33.5.6 not result in any safety hazard	M	Yes [ ]
ES3	Limitation of electromagnetic interference	33.5.6	Comply with applicable local and national codes	M	Yes [ ]

33.7.3.6 Management function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	PSE register address 11	33.6.1	Control functions.	M	Yes [ ] No [ ] N/A [ ]
MF2	PSE register address 12	33.6.1	Status functions.		Yes [ ] No [ ] N/A [ ]
MF3	PD Register address 12	33.6.1	Status functions.	M	Yes [ ] No [ ] N/A [ ]
MF4	Register bits latching high (LH)	33.6.1	Remain high until read via the management interface. Once read, the bit assumes a value based on the current state of the condition it monitors.	M	Yes [ ] No [ ]
MF5	Register bits read	33.6.1	Bit assumes a value based on the current state of the condition it monitors.	M	Yes [ ] No [ ]
MF6	PSE Control register reserved bits (11.15:5)	33.6.1.1.1	Not affected by writes and return a value of zero when read.	M	Yes [ ] No [ ] N/A [ ]
MF7	PSE detection control bit (11.4)	33.6.1.1.2	Set to '1' allows normal operation except power not applied to valid detected PDs and causes power to be removed if applied to a valid PD previously detected.	M	Yes [ ] No [ ] N/A [ ]
MF8	Pair Control Ability not supported	33.6.1.1.3	Ignore writes to bits 11.3:2	!PCA:M	Yes [ ] No [ ] N/A [ ]
MF9	Writes to 11.3:2 when Pair Control Ability not supported	33.6.1.1.3	Return the value that reports the supported PSE Pinout Alternative.	!PCA:M	Yes [ ] No [ ] N/A [ ]
MF10	Bits 11.3:2 set to '01'	33.6.1.1.3	Forces the PSE to use Alternative A.	PCA:M	Yes [ ] No [ ] N/A [ ]
MF11	Bits 11.3:2 set to '10'	33.6.1.1.3	Forces the PSE to use Alternative B.	PCA:M	Yes [ ] No [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MF12	Setting power enable bit 11.0 to a logic one	33.6.1.1.5	PSE function enabled.	M	Yes [ ] No [ ] N/A [ ]
MF13	Setting power enable bit 11.0 to a logic zero	33.6.1.1.5	PSE function disabled.	M	Yes [ ] No [ ] N/A [ ]
MF14	Power enable bit 11.0 set to logic zero	33.6.1.1.5	MDI to function as if there was no PSE function	M	Yes [ ] No [ ] N/A [ ]
MF15	Reserved bits (12.15:10)	33.6.1.2.1	Not be affected by writes and shall return a value of zero when read.	M	Yes [ ] No [ ] N/A [ ]
MF16	Overcurrent bit (12.9)	33.6.1.2.2	Read as logic 1 indicates an overcurrent condition specified in Table 33–5	M	Yes [ ] No [ ] N/A [ ]
MF17	Overcurrent condition detected	33.6.1.2.2	When the current drawn from the PSE at the MDI is greater than the overload current limit for a duration greater than the overload time limit (see Table 33–5).	M	Yes [ ] No [ ] N/A [ ]
MF18	Overcurrent bit implementation	33.6.1.2.2	With latching high behavior as defined in 33.6.1.	M	Yes [ ] No [ ] N/A [ ]
MF19	Undercurrent bit (12.8)	33.6.1.2.3	Read as logic 1 indicates an undercurrent condition specified in Table 33–5	M	Yes [ ] No [ ] N/A [ ]
MF20	Undercurrent condition detected	33.6.2.3	When the current drawn from the PSE at the MDI is less than I_{UDL} for a duration greater than T_{PMDO} (see Table 33–5).	M	Yes [ ] No [ ] N/A [ ]
MF21	Undercurrent bit implementation	33.6.1.2.3	With latching high behavior as defined in 33.6.1.	M	Yes [ ] No [ ] N/A [ ]

Annex A

(informative)

PSE Detection of Class 0 PDs

The capacitance of the maximum cabling plant and maximum PD signature is included in the PSE detection requirement. The following circuit is recommended for test purposes.

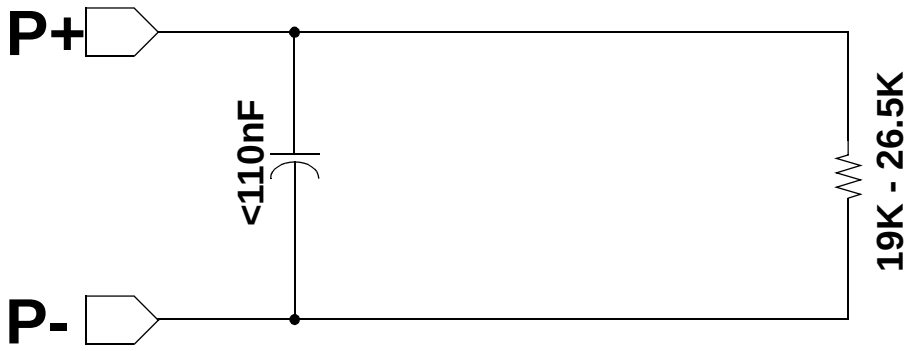


Figure A.1—PD detection signature

PDs may contain a polarity guard in front of the signature which may result in a DC offset in the signature, as illustrated below.

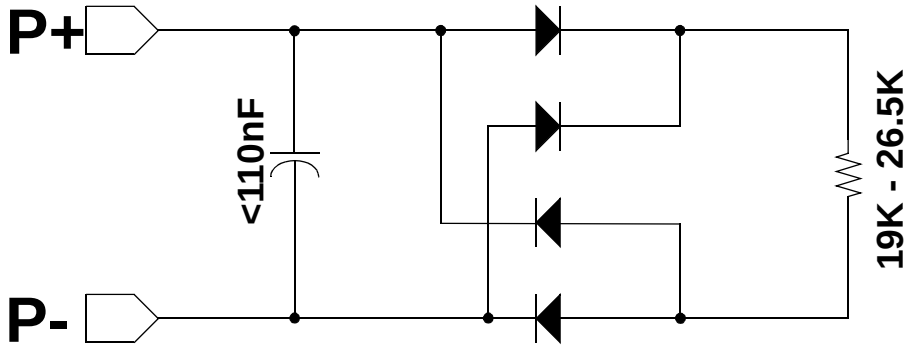


Figure A.2—PD detection signature with polarity guard

The following three circuits are recommended as test benchmarks for rejection by a compliant PSE.

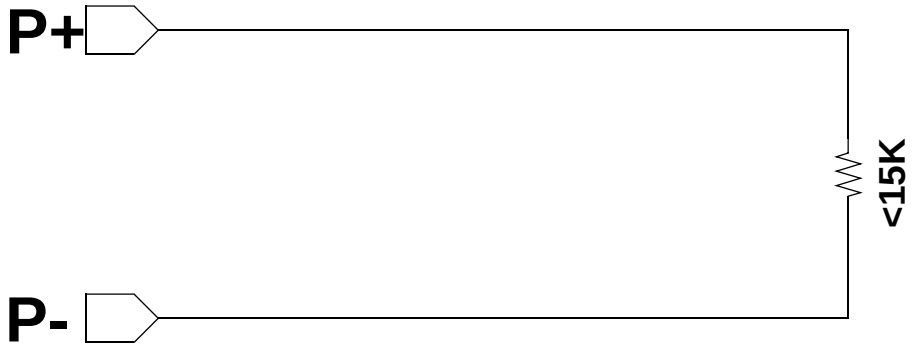


Figure A.3—Invalid detection signature, impedance low

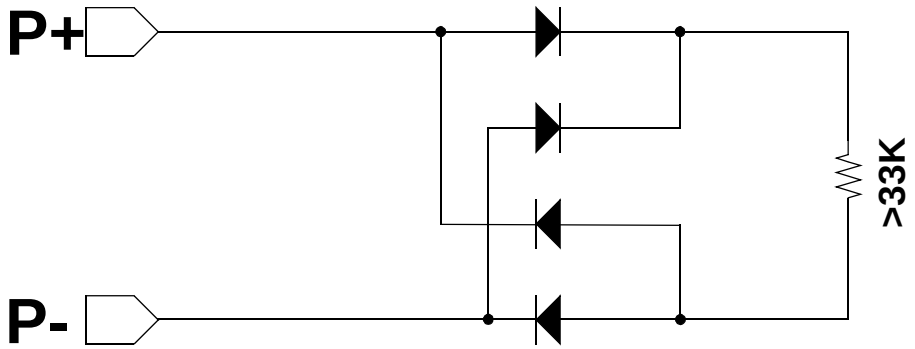


Figure A.4—Invalid detection signature, impedance high

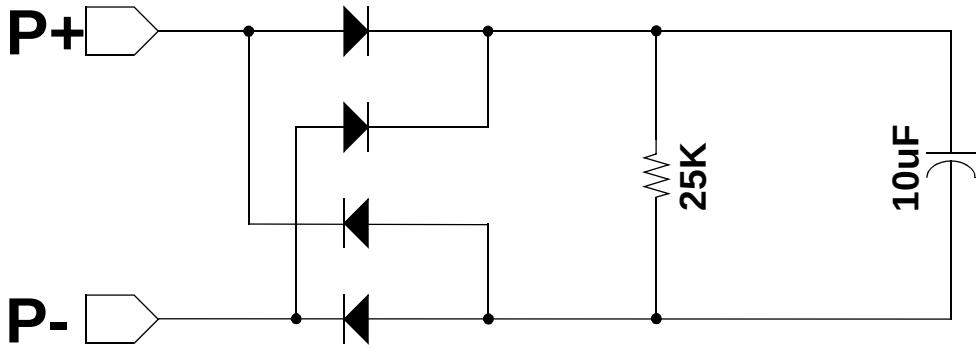


Figure A.5—Invalid detection signature, capacitance high

Annex B

(informative)

Cabling Guidelines

DTE power via MDI is intended to operate over a 4-pair unshielded twisted-pair (UTP) balanced cabling infrastructure as described in ISO/IEC 11801-2000. Although initial implementations are expected to make use of this clause to provide powered IP telephones, the clause is intended to address a much larger family of low power devices whose applications require connection to local area networks.

It is expected that in the future as building cabling infrastructures begin to support more building automation systems (BAS), additional cabling guidelines will be implemented. BAS systems are used for controlling building systems such as fire alarm, security and access control (e.g., closed circuit television), and energy management systems (e. g., heating, ventilation and air conditioning and lighting control). One such standard that is to be published to support these systems with a cabling infrastructure in EIA/TIA is the Building Automation Cabling Standard for Commercial Buildings. This Standard will specify a generic cabling system for building automation systems used in commercial buildings for a multi-product, multi-vendor environment. The purpose of the Standard is to enable the planning and installation of a structured cabling system for building automation system applications that are required for use in new or renovated construction of commercial buildings. It is significantly less expensive to integrate all of the major voice, data, and BAS applications by utilizing a fully integrated structured cabling infrastructure.

For planning purposes, a sufficient number of horizontal cabling links should be provided for voice, data, and building automation services over the average floor space. It is recommended that a minimum of two 4-pair outlets be provided per work area as specified in the current standards in ISO/IEC and TIA/EIA.