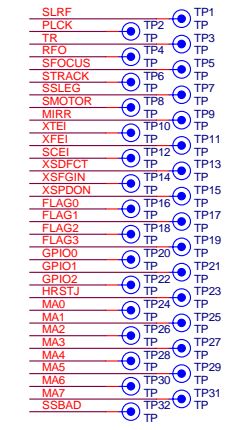
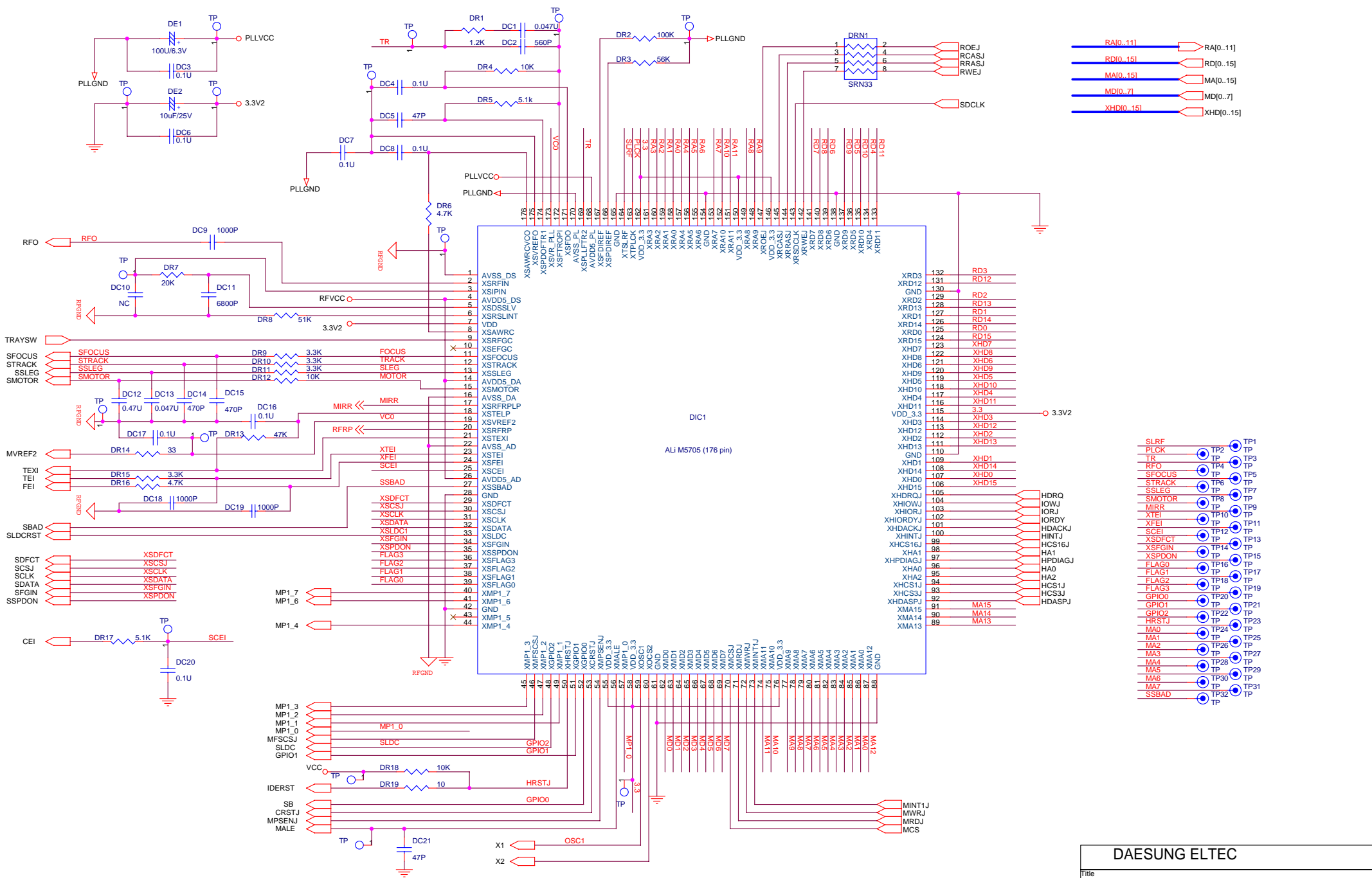
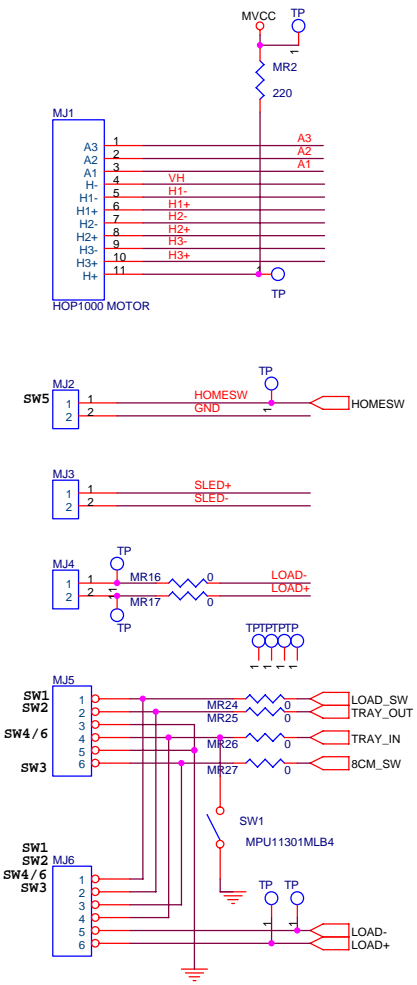
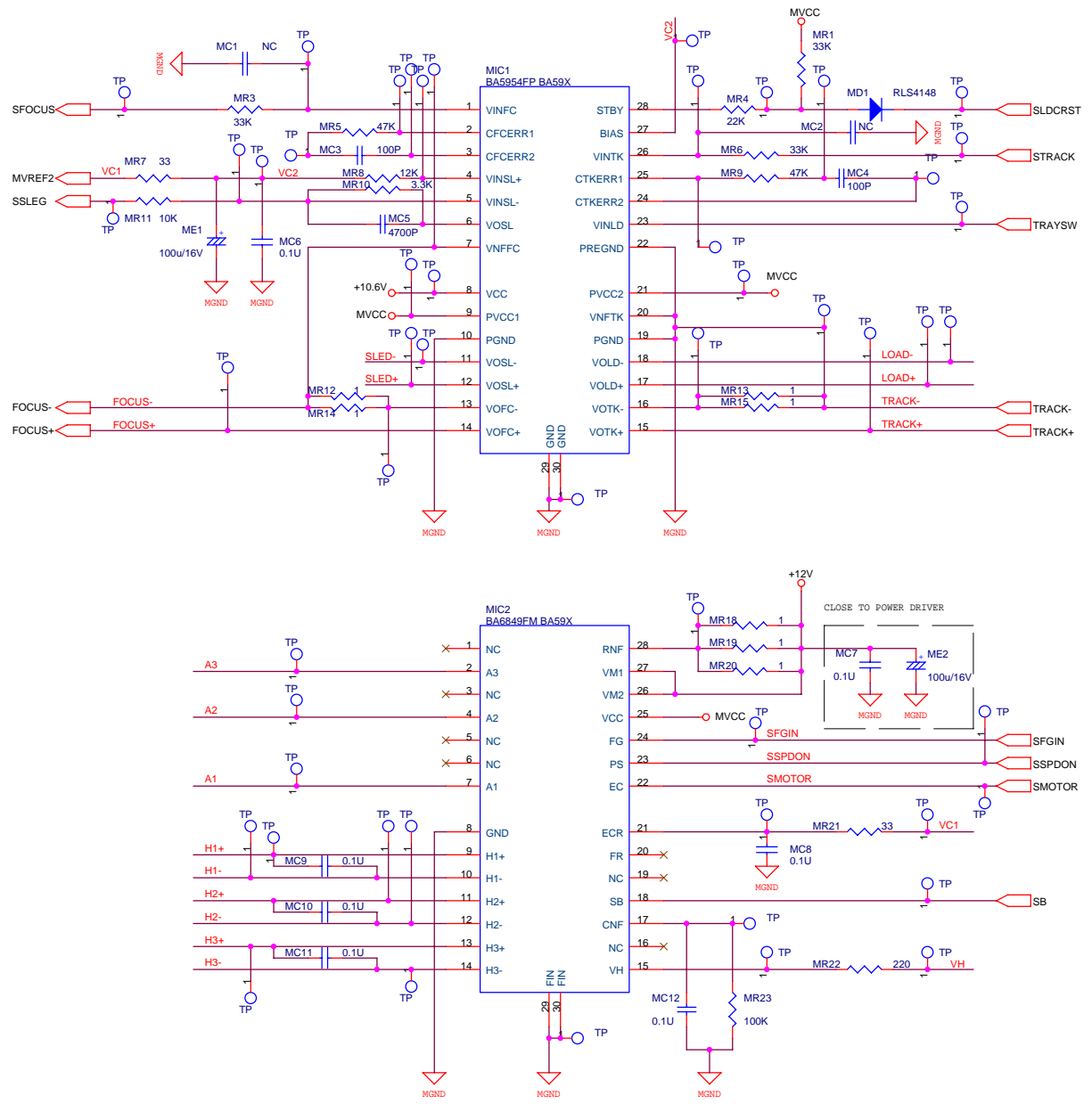


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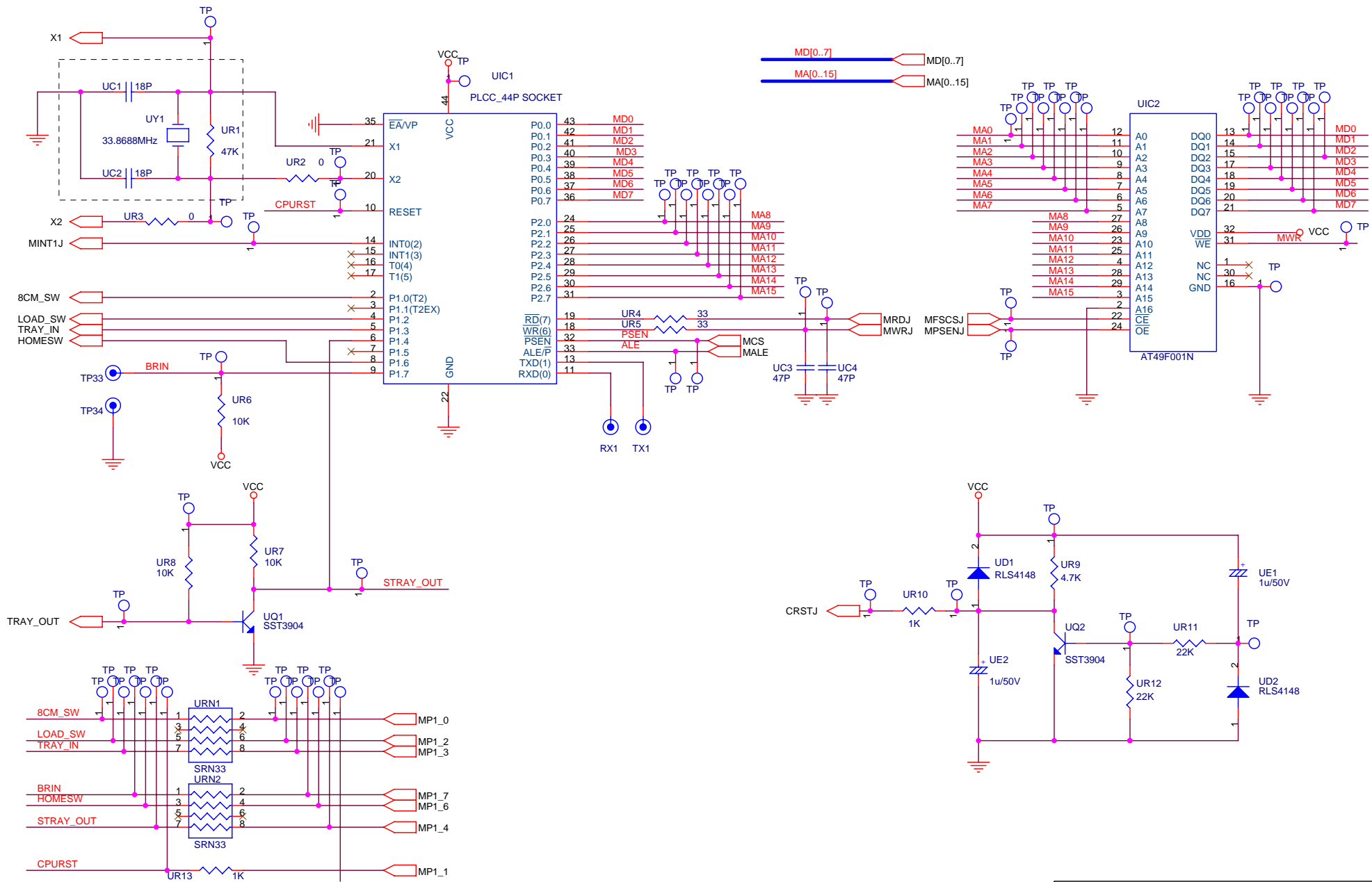




NOTE: SW1=LOAD_SW
 SW2=8/12CM SW
 SW3=8CM SW
 SW5=HOME_SW
 SW4/6=CHUCK SW

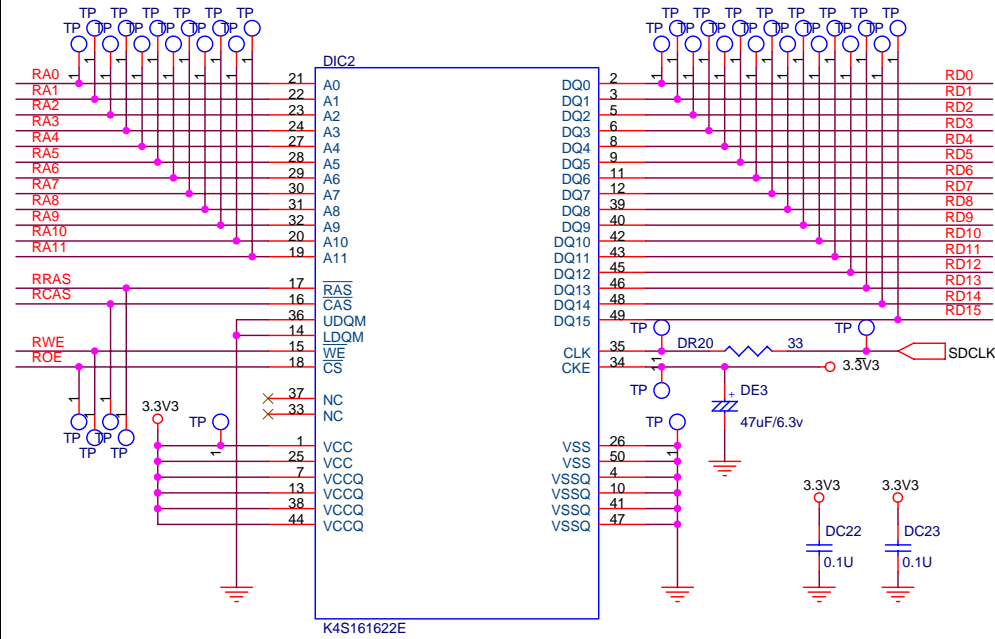
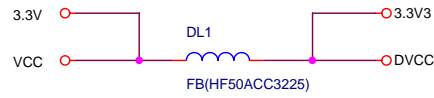


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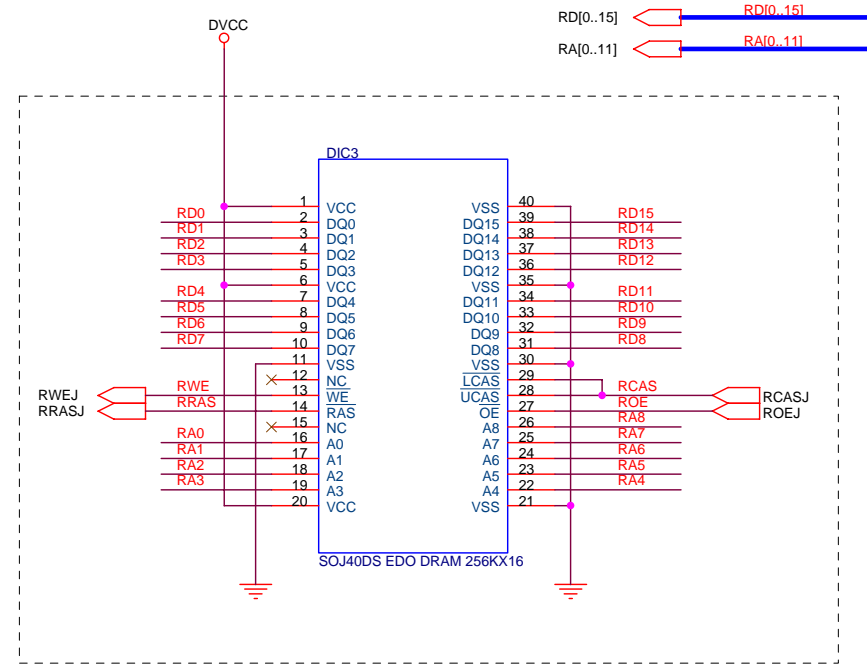
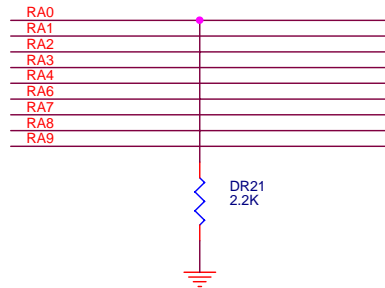


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CPU		
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NOTE: 4M DRAM USE 5V
16M SDRAM USE 3.3V



HARDWARE SETTING

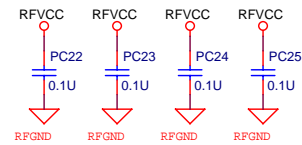
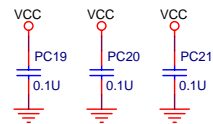
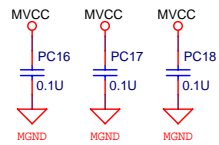
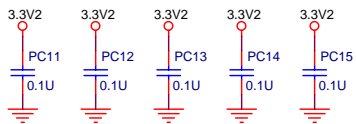
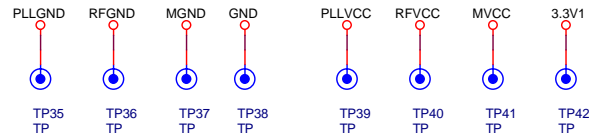
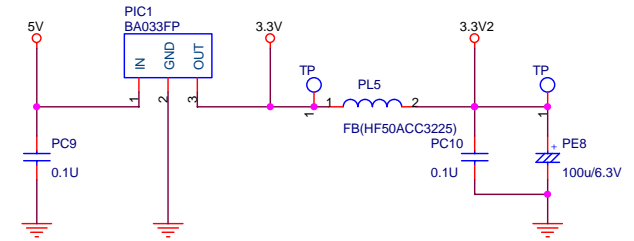
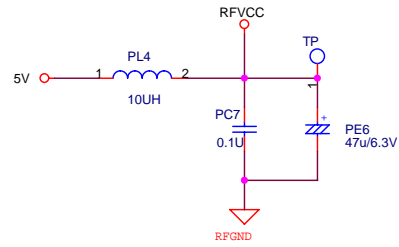
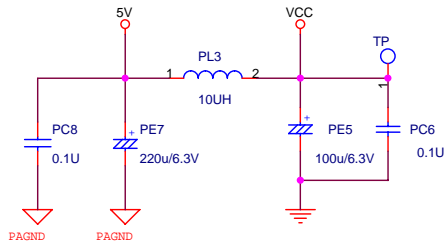
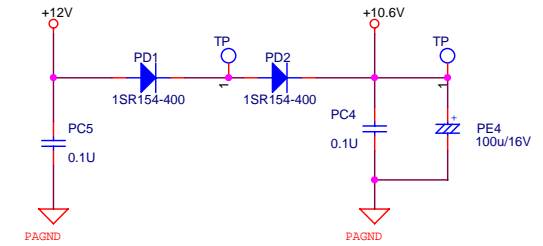
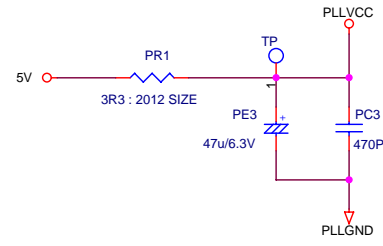
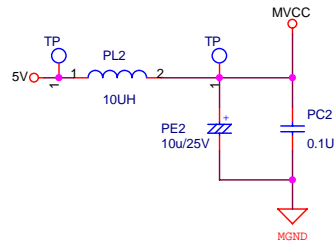
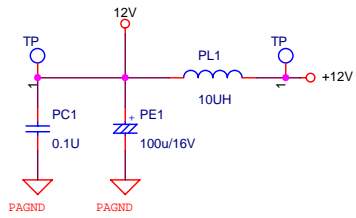


HARDWARE SETTING:

- RA[9] : Flash ROM Type
 - 1 : Now is using 64K Flash, so that XMP1[0] can be used as GPIO. (Default)
 - 0 : Now is using 128K Flash, so that XMP1[0] is used as A16
- RA[8] : MP Type
 - 1 : MP type is Intel 8032.
 - 0 : MP type is H8
- RA[7] : Microprocessor programmable I/O port 1 pin control
 - 1 : By internal microprocessor
 - 0 : By registers to decided input/output
- RA[6] : System testpin output
 - 1 : Normal operation
 - 0 : System test pin output
- RA[4] : IDE Master/Slave
 - 1 : Slave
 - 0 : Master
- RA[3] : Microprocessor I/F pins configuration (For Testing Only)
 - 1 : Normal mode
 - 0 : M5701 compatible mode
- RA[2] : Clock source selection (For Testing Only)
 - 1 : Select internal clock
 - 0 : Select external clock
- RA[1-0] : MCU Mode selection
 - 11 : Normal Mode (internal uP, internal address latch)
 - 10 : Output uP Mode (ICE Mode)
 - 01 : Test mode for internal uP testing
 - 00 : internal uP mode with external address latch

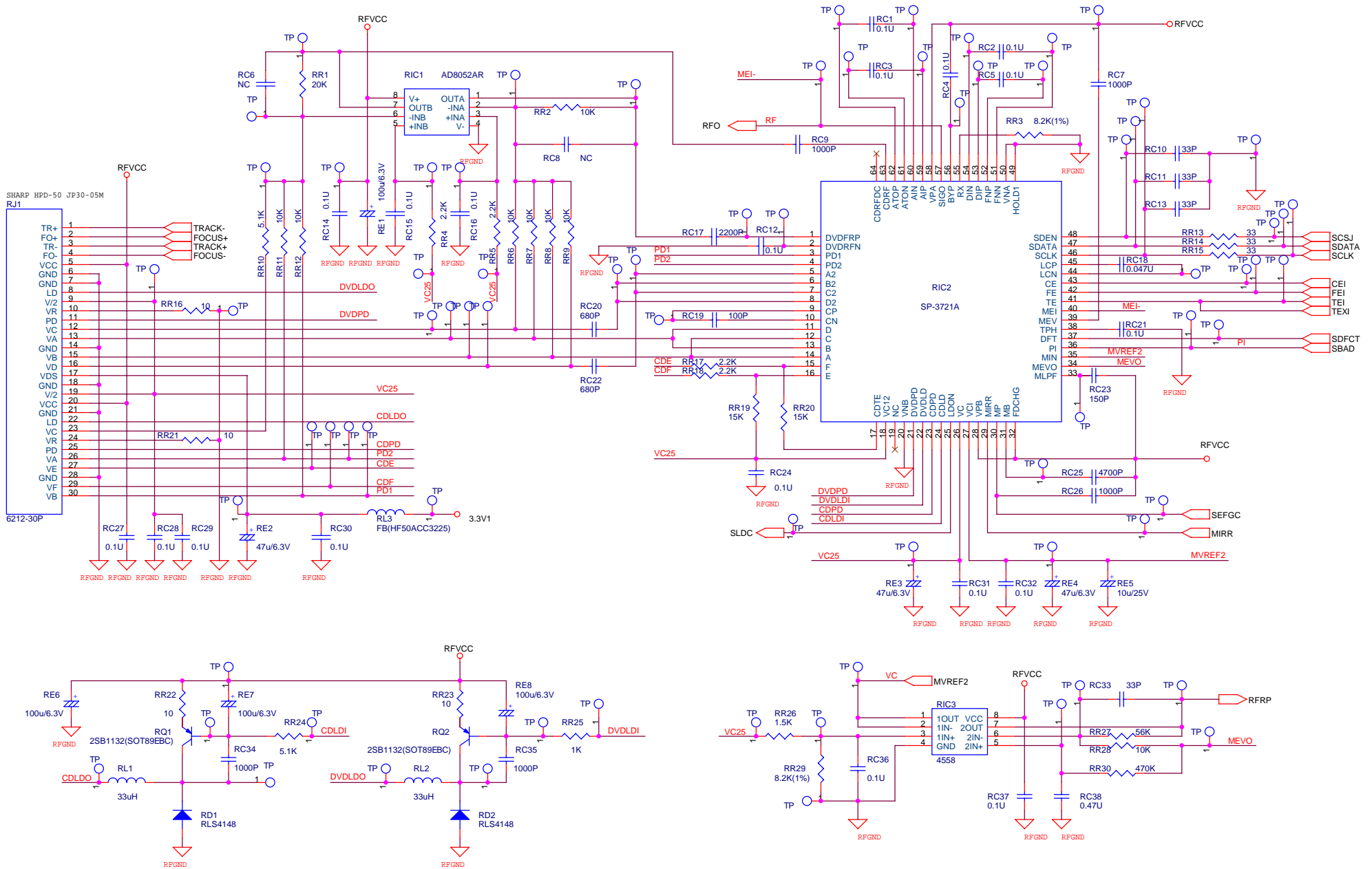
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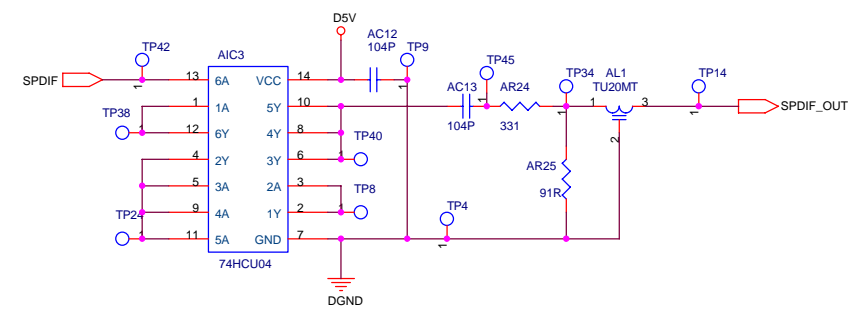
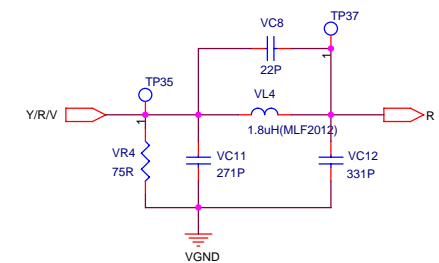
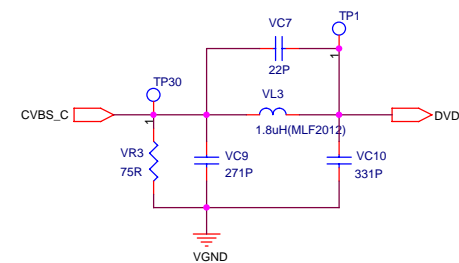
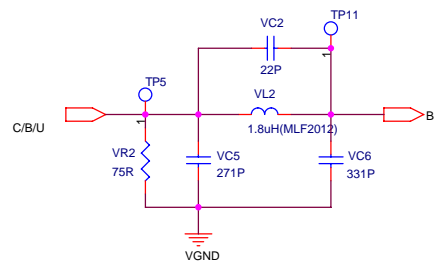
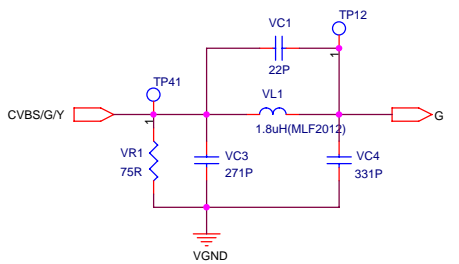
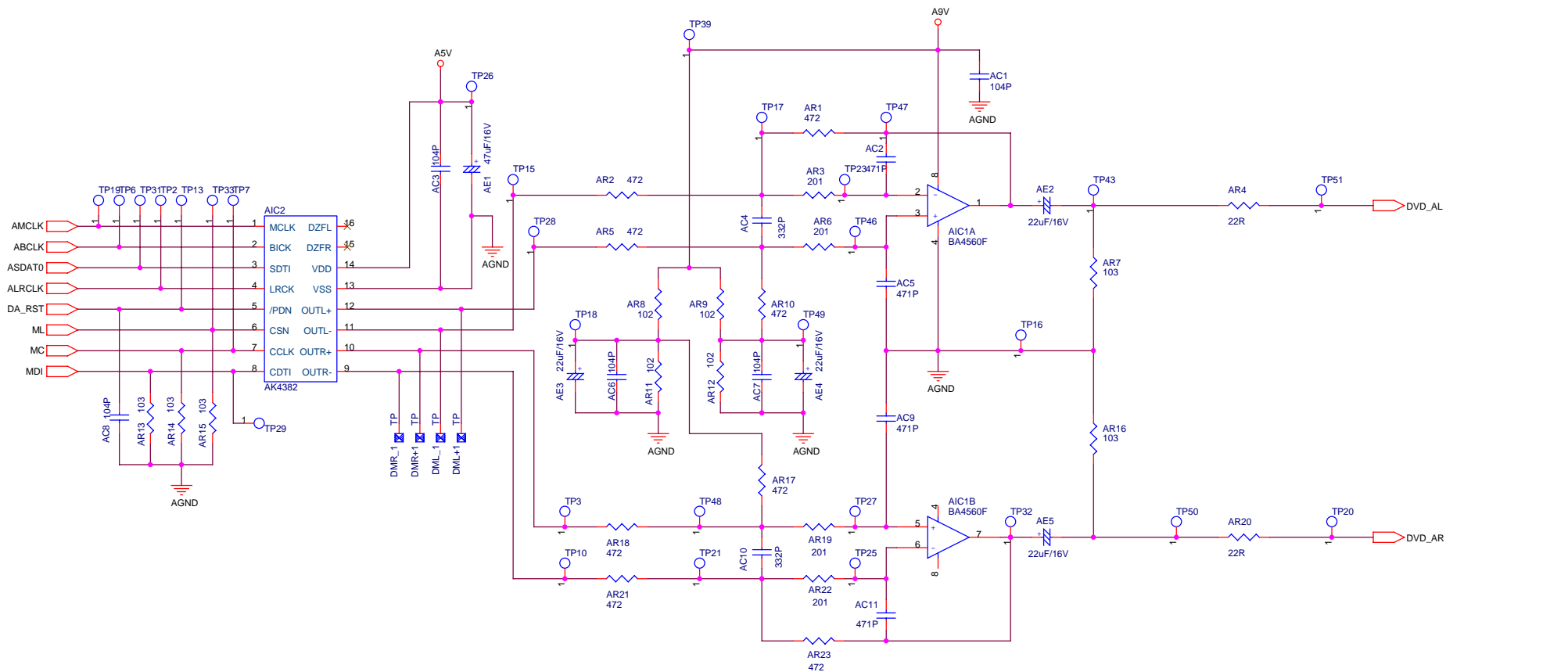


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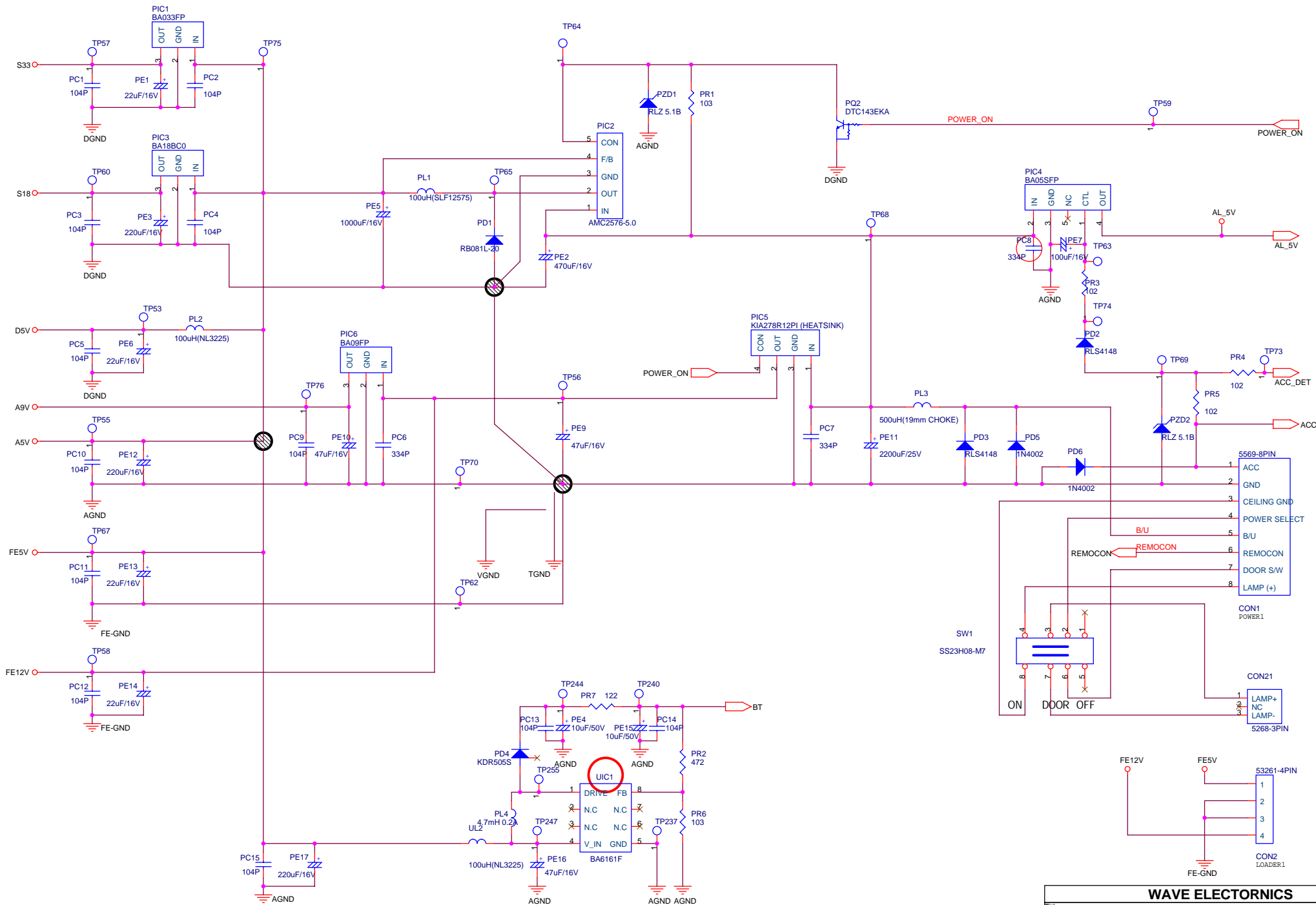
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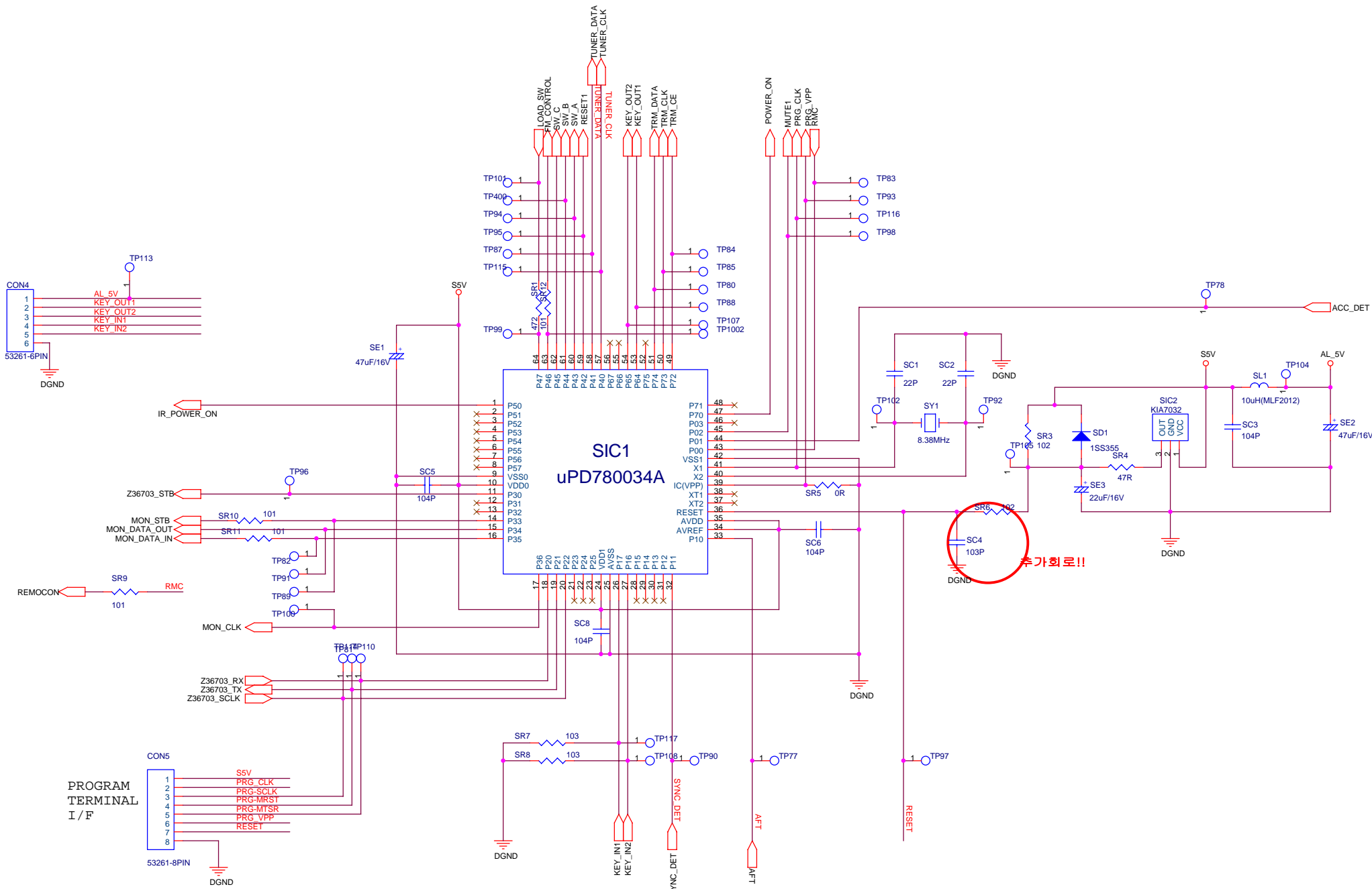
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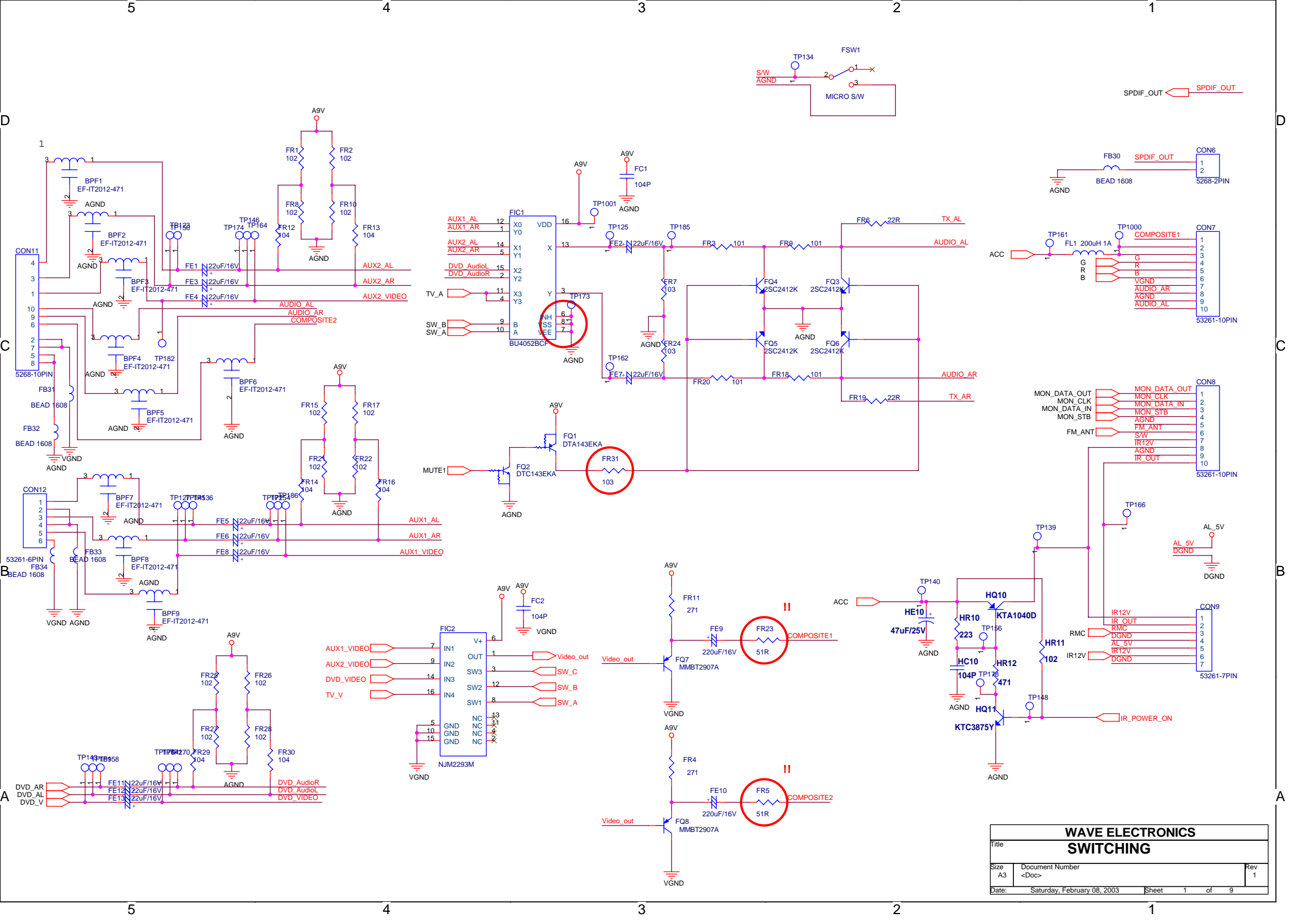
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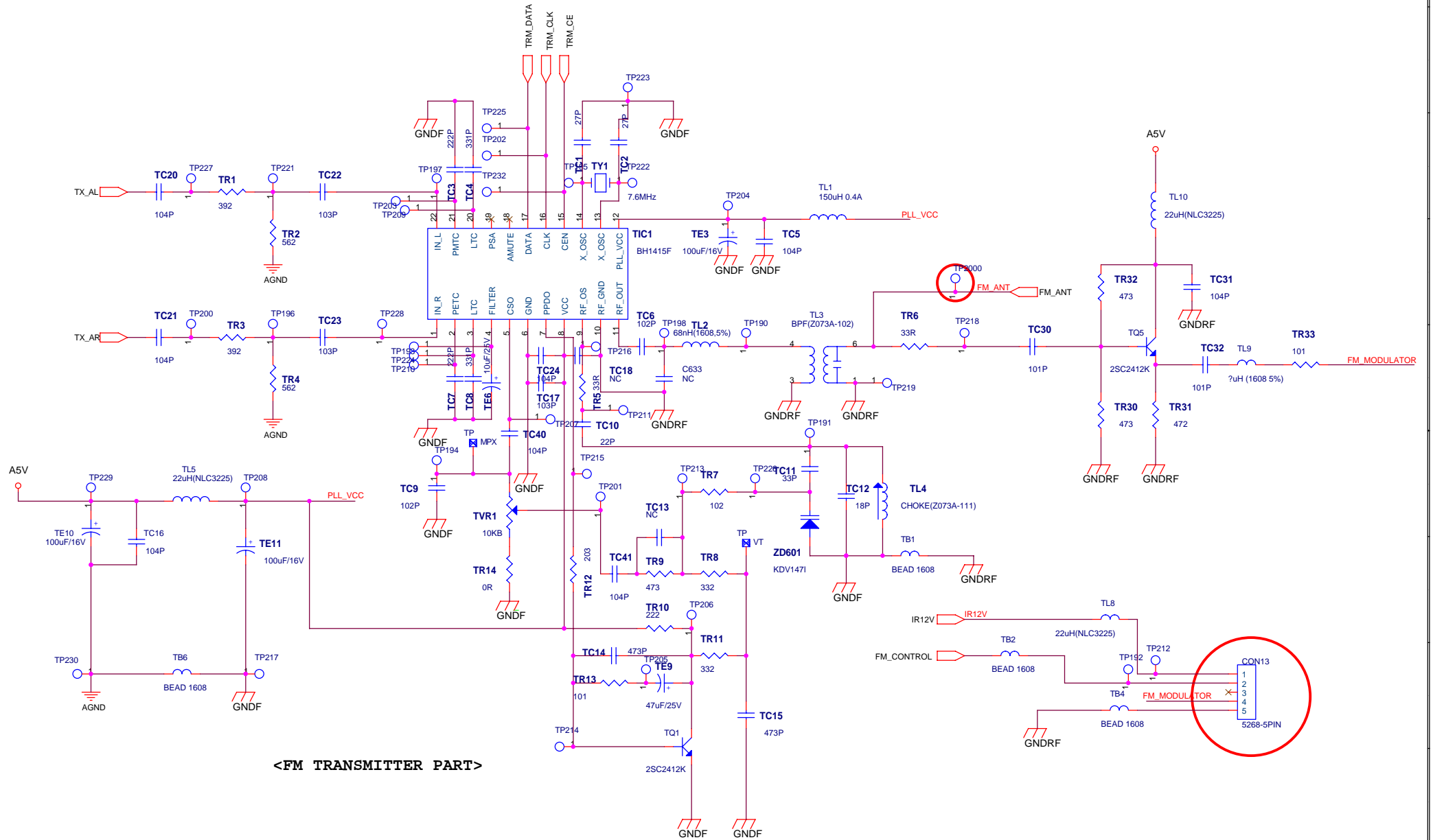
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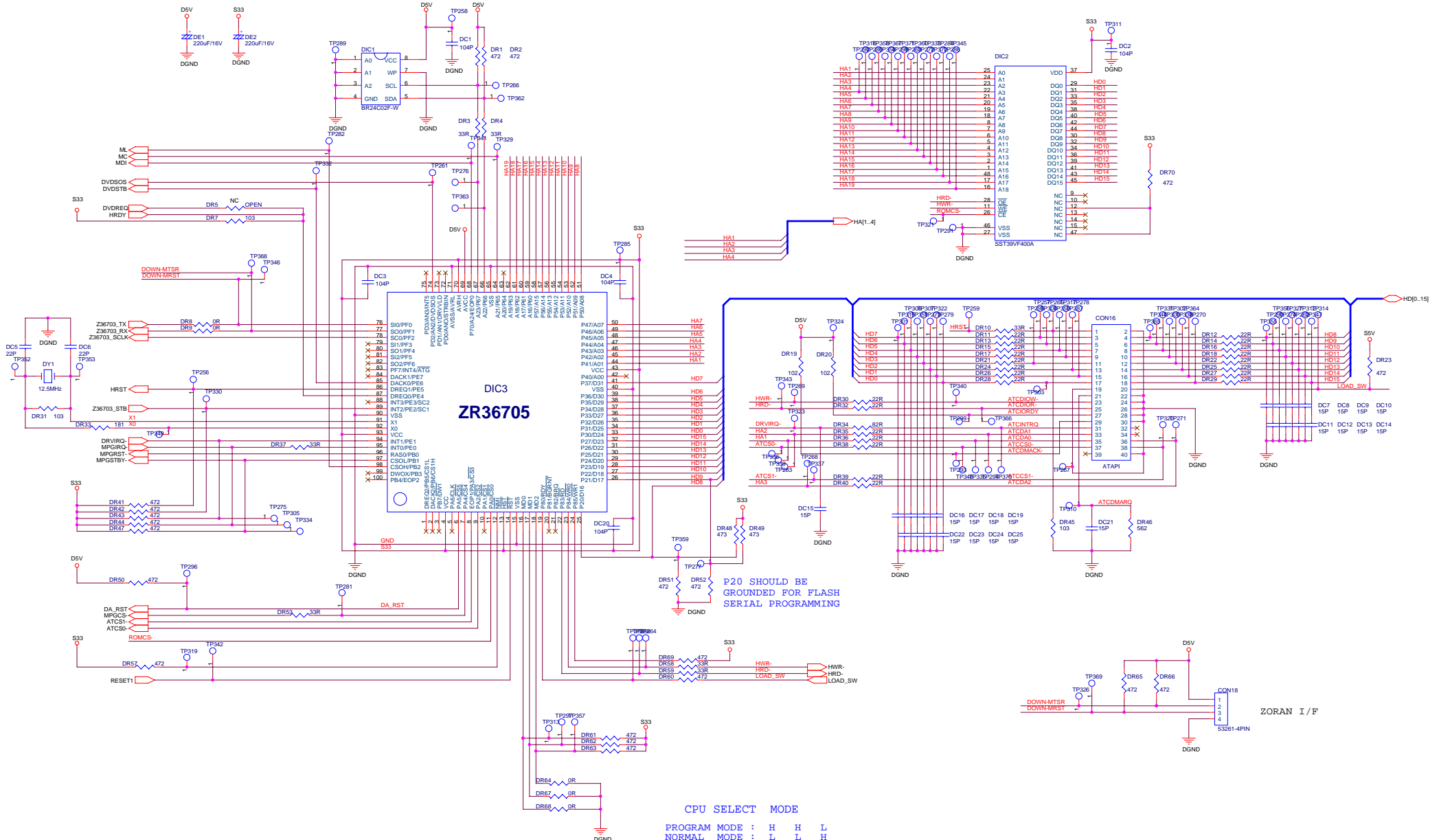
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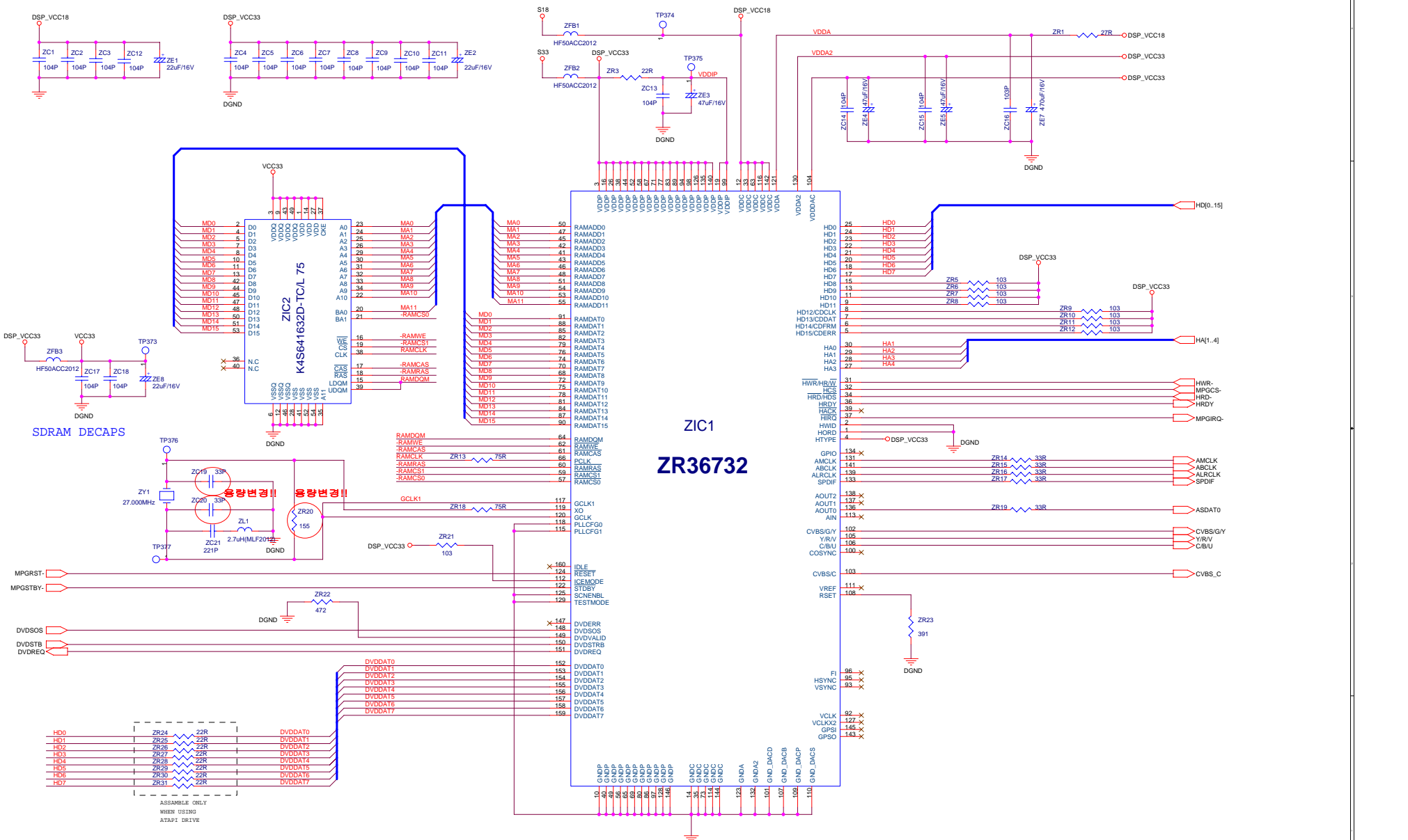


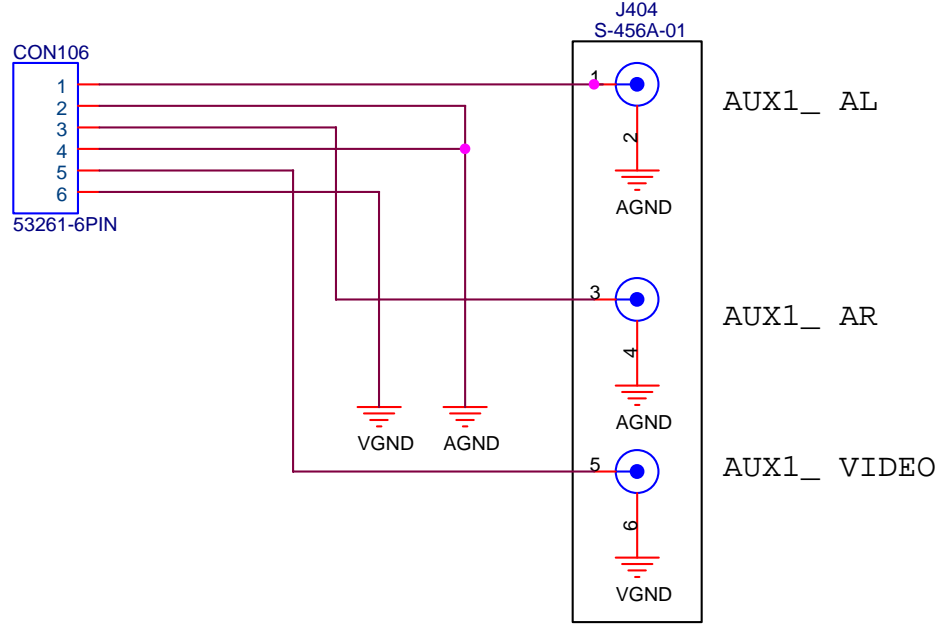
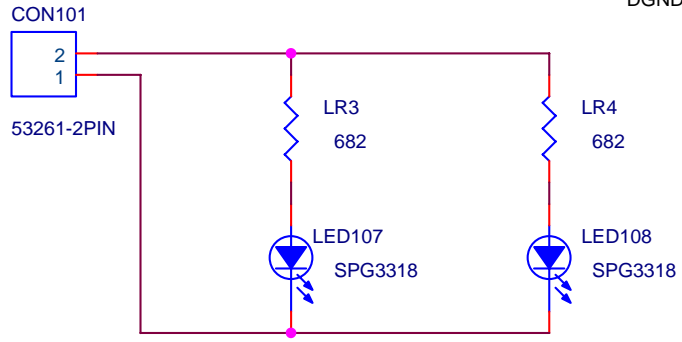
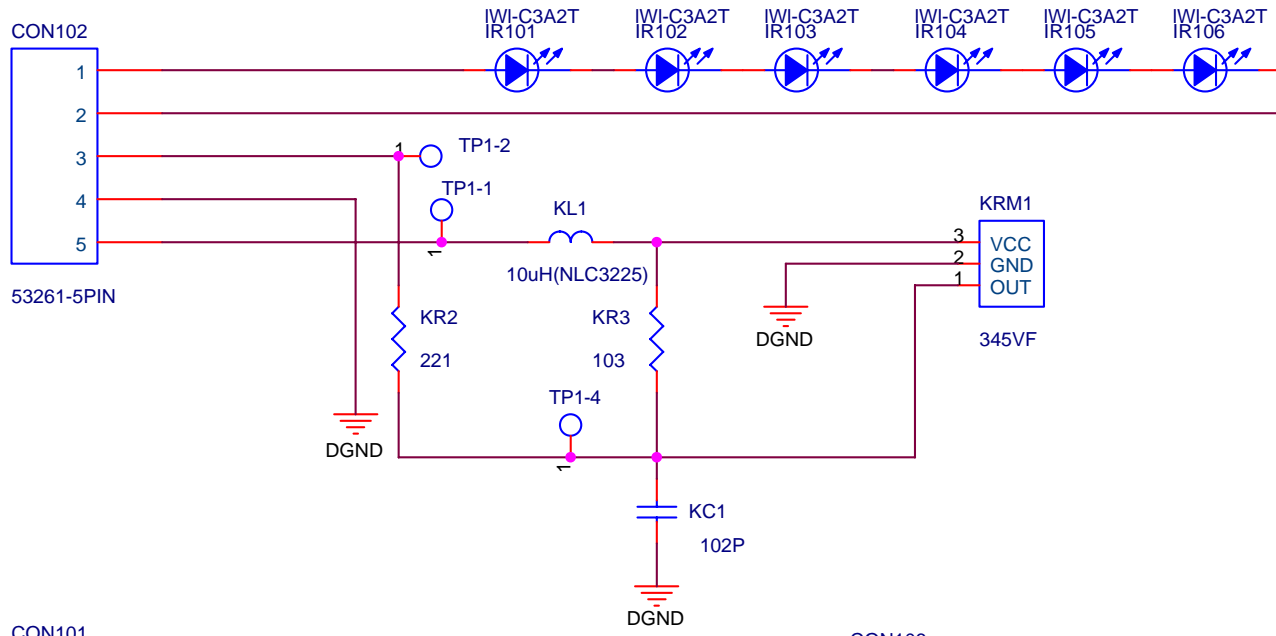
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		Rev	A



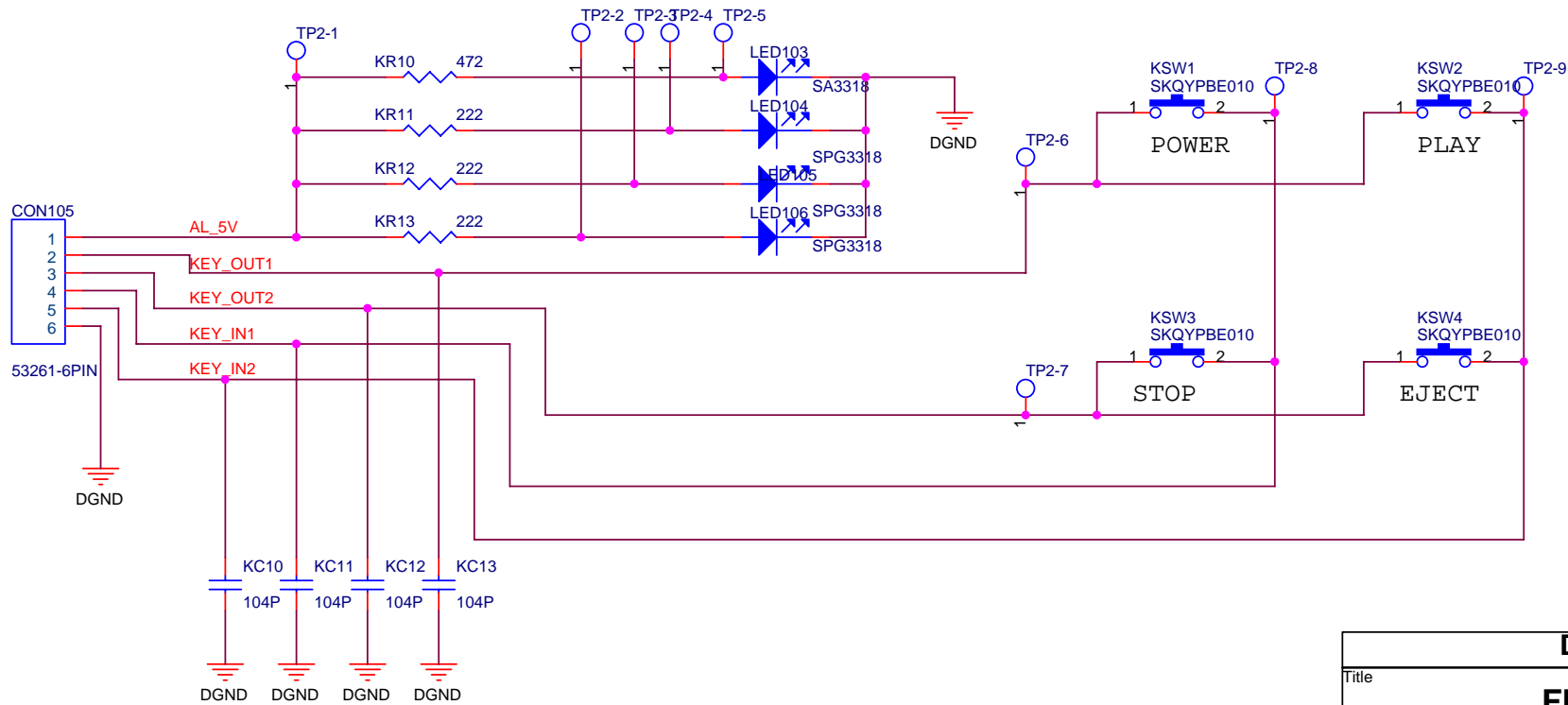
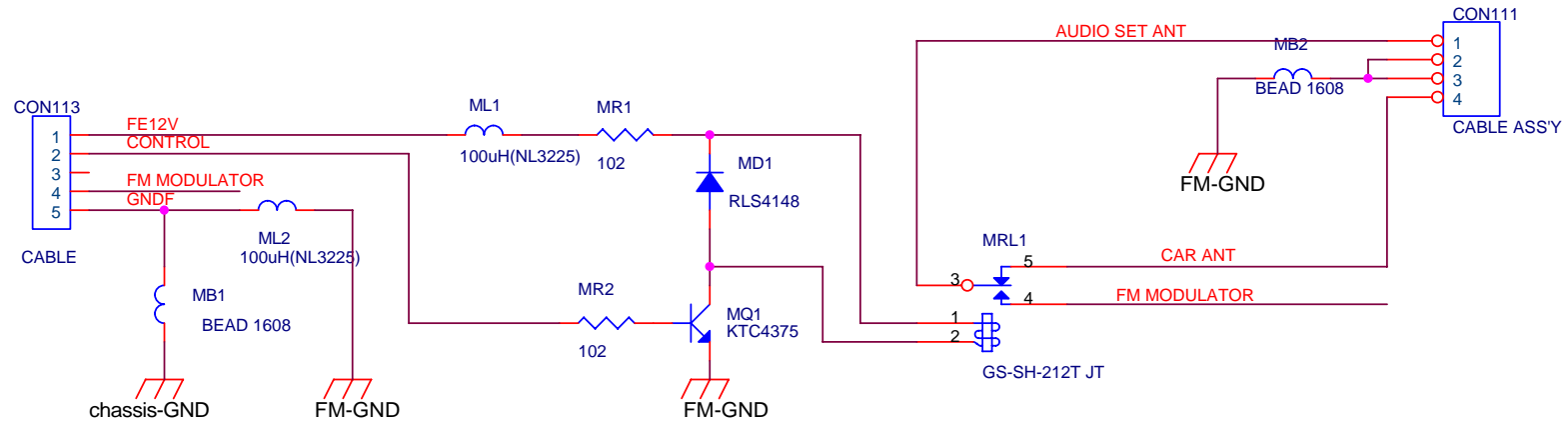
P20 SHOULD BE GROUNDED FOR FLASH SERIAL PROGRAMMING

CPU SELECT MODE
 PROGRAM MODE : H H L
 NORMAL MODE : L L H





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DAESUNGELTEC		
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Size A4	Document Number <Doc>	Rev 1
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