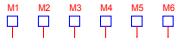
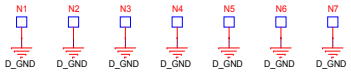
HOLE:

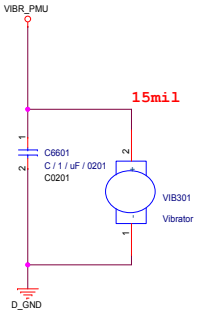
MARK POINT:

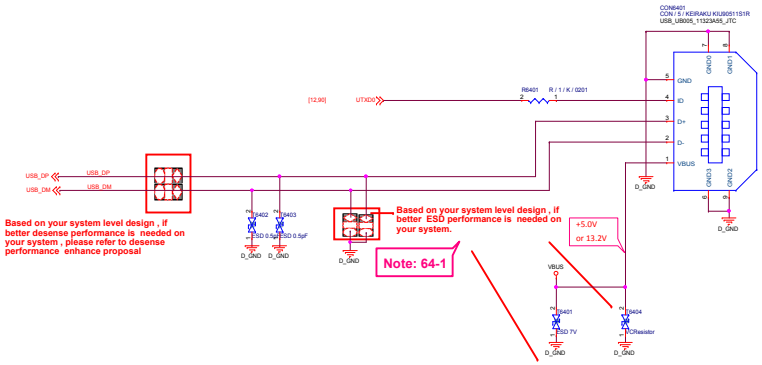


LUOMU:



VIBRATOR


VIBR_PMU
15mil
1
2
C6601
C / 1 / uF / 0201
C0201
2
1
VIB301
Vibrator
D_GND

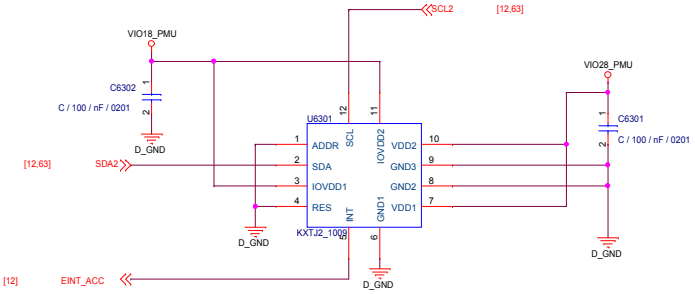


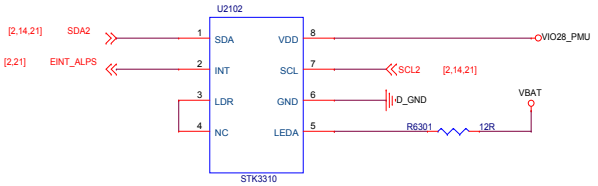
DOWNLOAD PAD

VBAT PAD

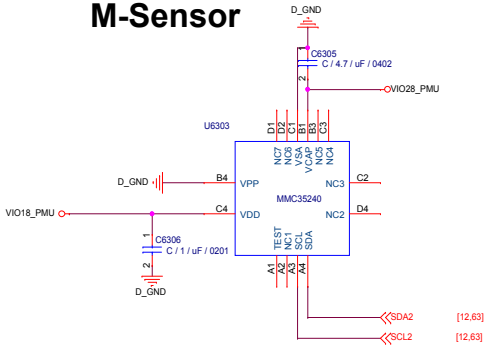
SUBBOARD CONN

Accerometer

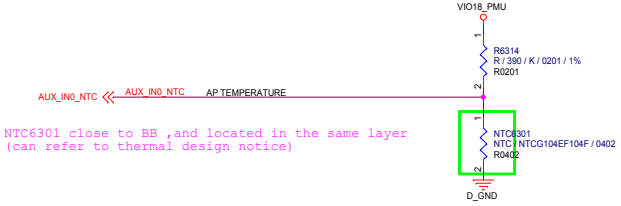




M-Sensor

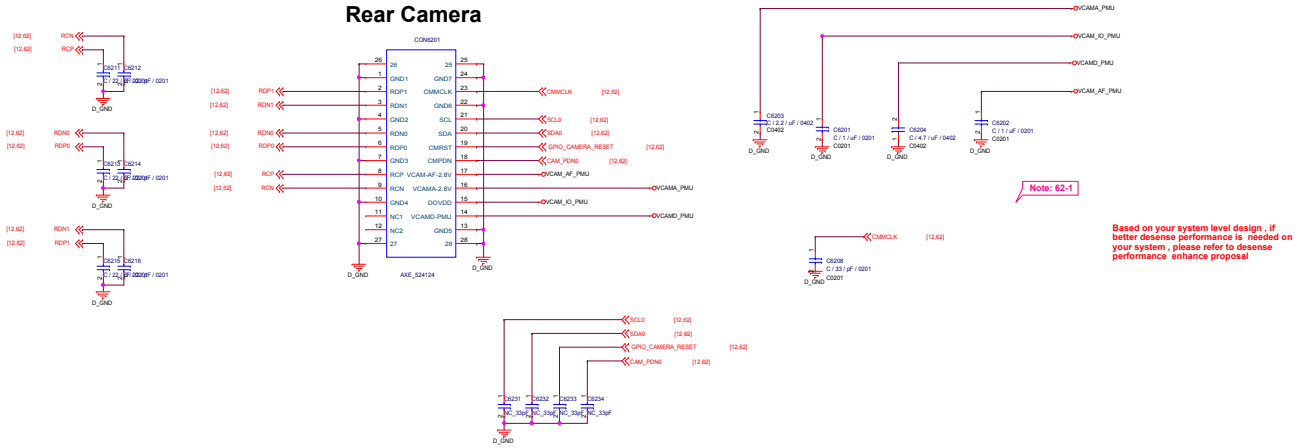


Thermistor / To sense board level temperature



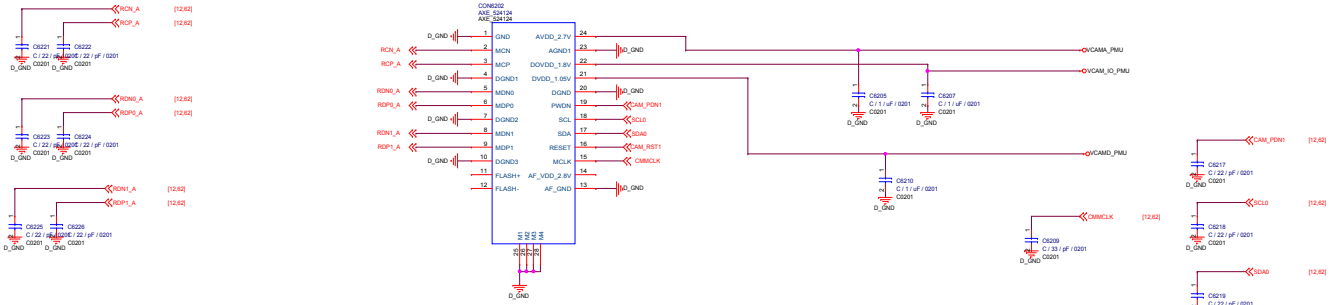
	PCB	Note
AUX_IN0_NTC	AP	Keep 5-8 mm to AP, and far to other heat source

Rear Camera



Front Camera

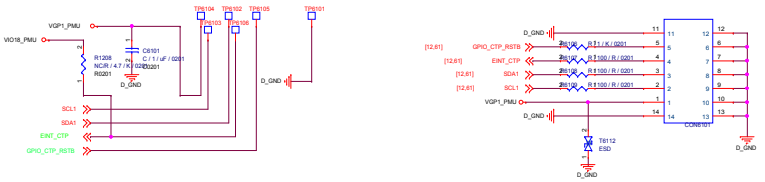
Front camera (GC2355) I2C address: 0x3C (Write:0x78, Read:0x79)



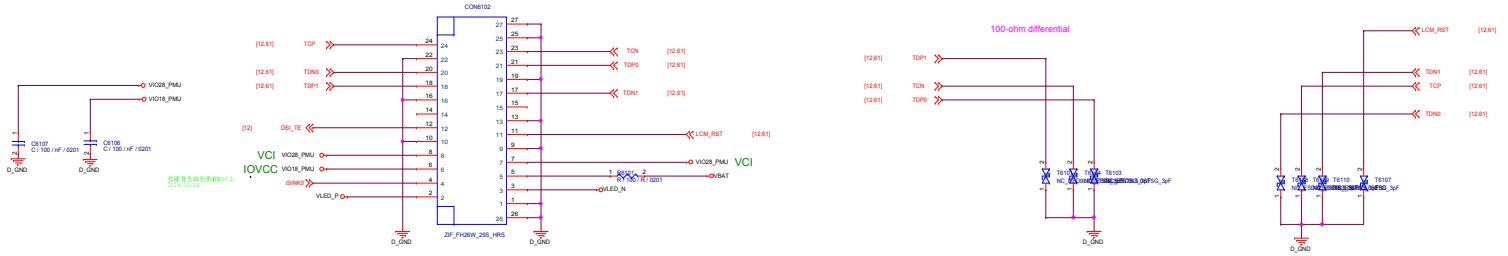
Schematic design notice of "62_PERI_CAMERA" page.

Note 62-1: If your project needs PIP function, please refer to MT6735 design notice for the connection of MCLK / I2C / AVDD & DVDD

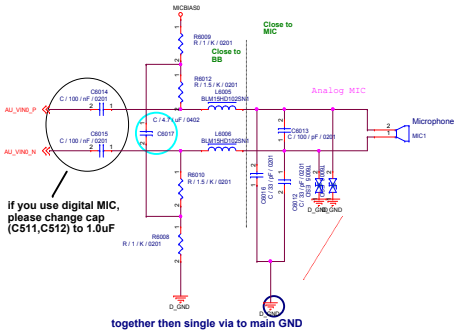
CTP Connector



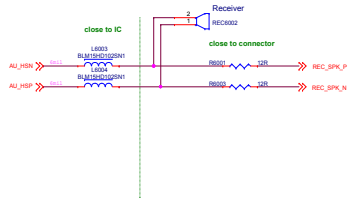
Main LCM



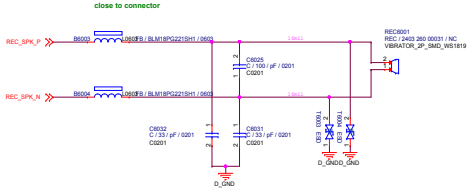
Handset Microphone 1



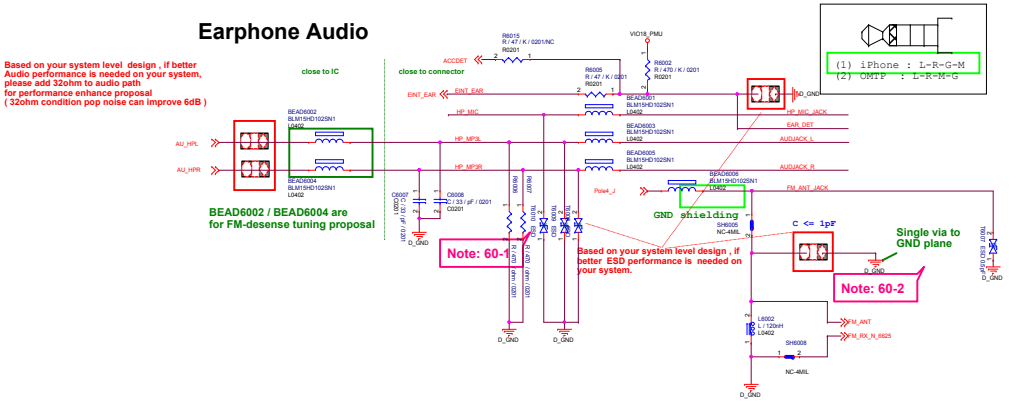
Receiver



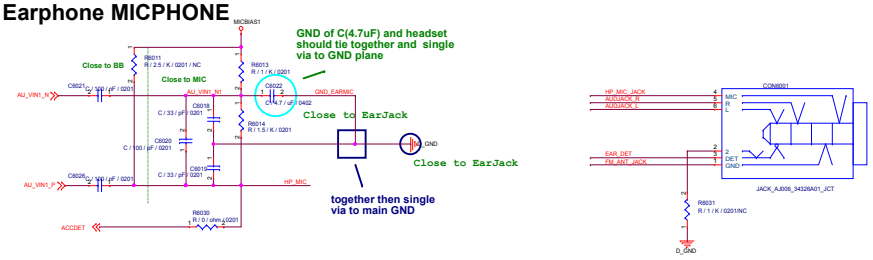
Receiver and Speeker 2 in 1



Earphone Audio



Earphone MICPHONE



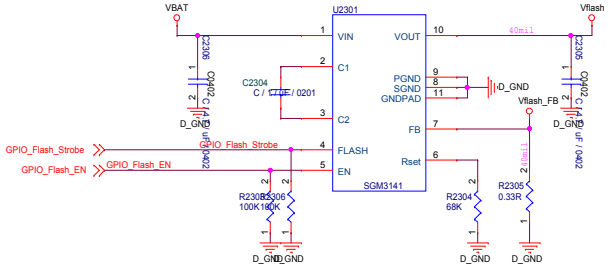
Earphone Detection Circuit				
Mode	R6002	R6005	R6015	R6030
Low Cost Mode	NC	NC	47K	NC
Traditional Mode (ACC)	470K	47K	NC	0R

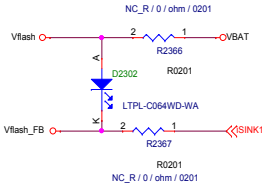
Shall be working in class AB mode

Speaker

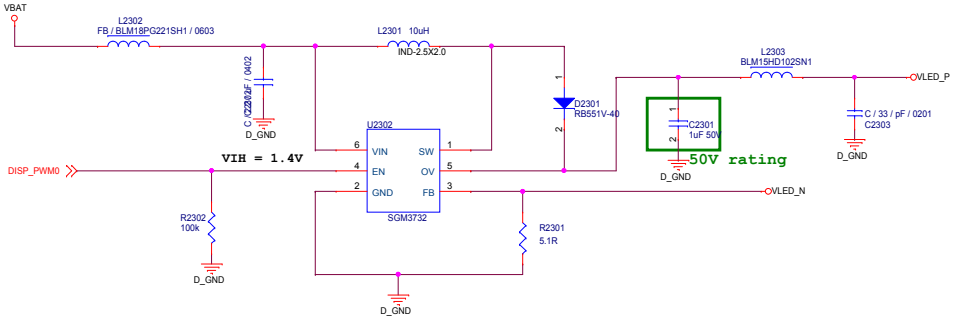
Schematic design notice of "60_PERI_AUDIO_IO" page.	
Note 60-1:	The equivalent capacitance of audio and speech ESD protection device must be <=330pF. choose bi-directional device only
Note 60-2:	The equivalent capacitance of FM ANT. ESD protection device must be <=1pF.
Note 60-3:	TVS Stand off voltage for speaker should >=5V

Flash LED 5V Boost

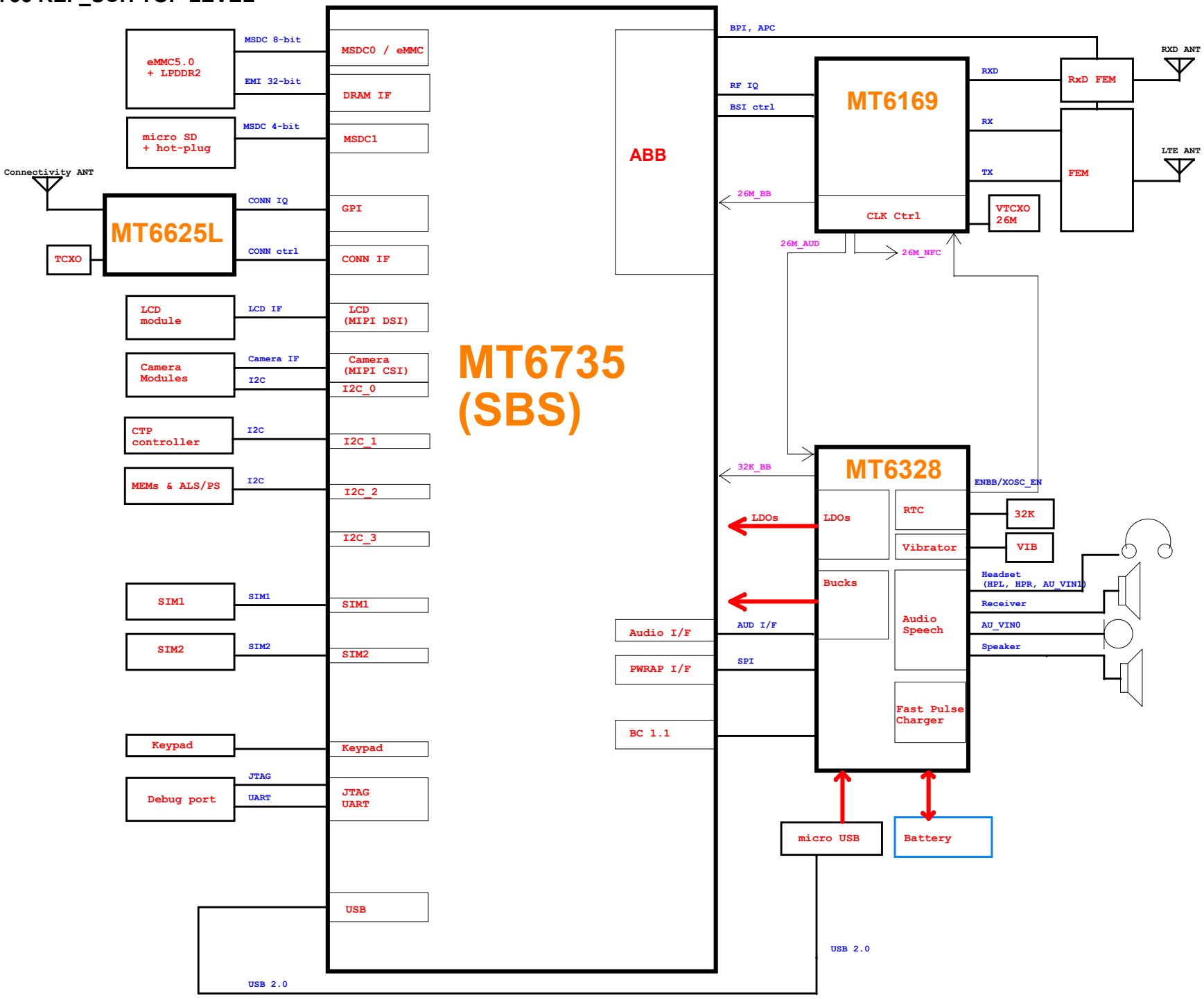




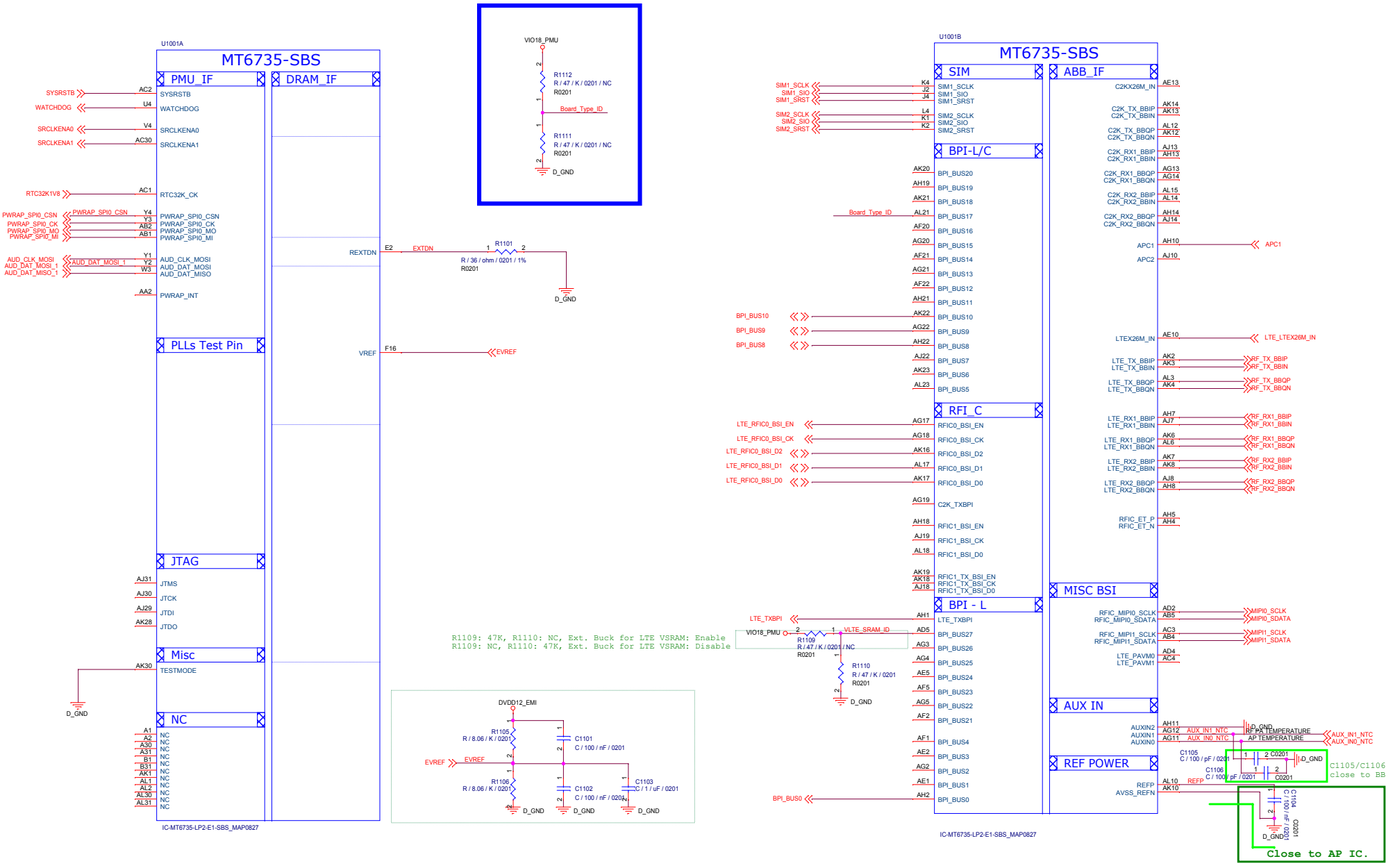
LCM Backlight LED Driver

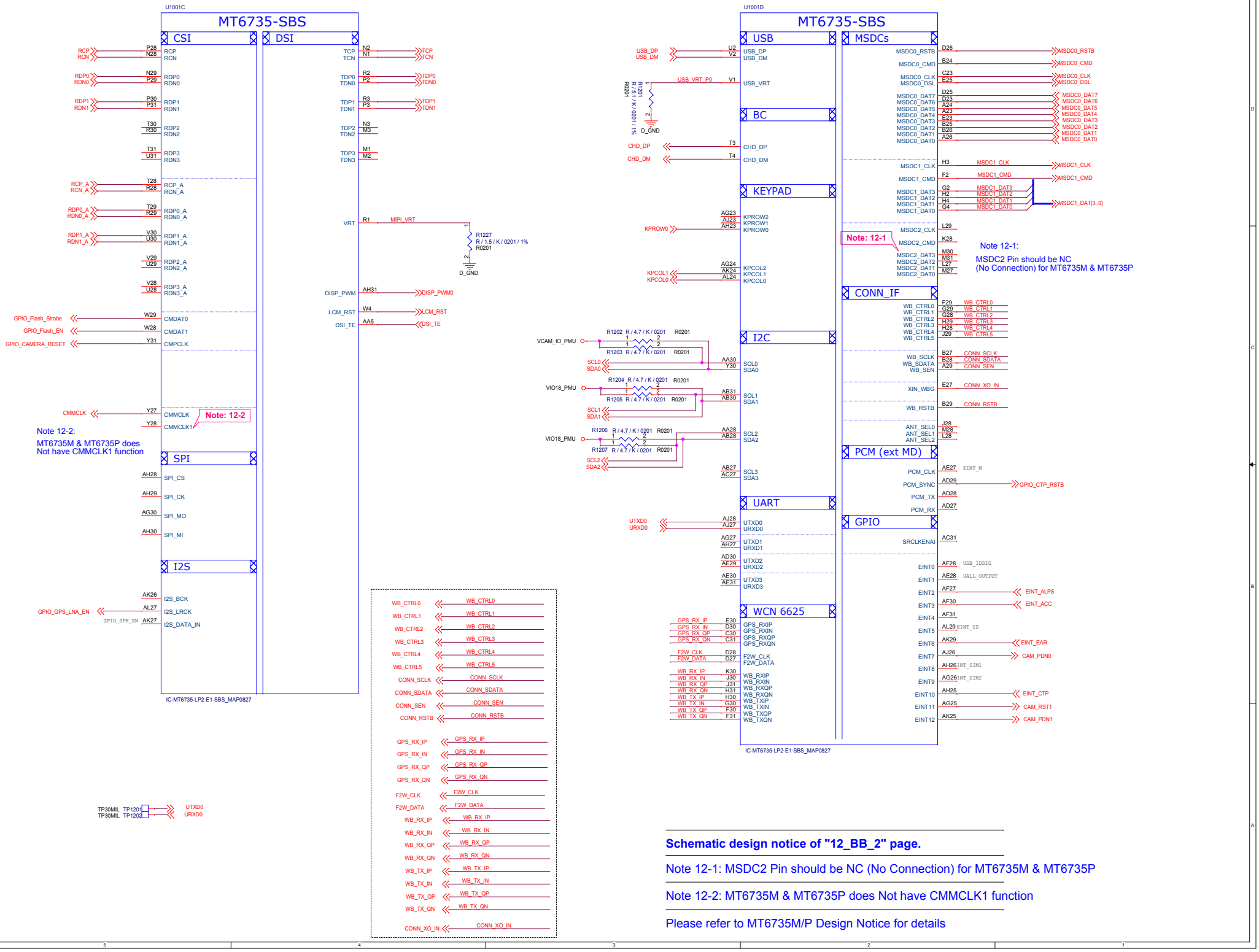


Project : MT6735 REF_SCH TOP LEVEL



This circuit muse be reserved



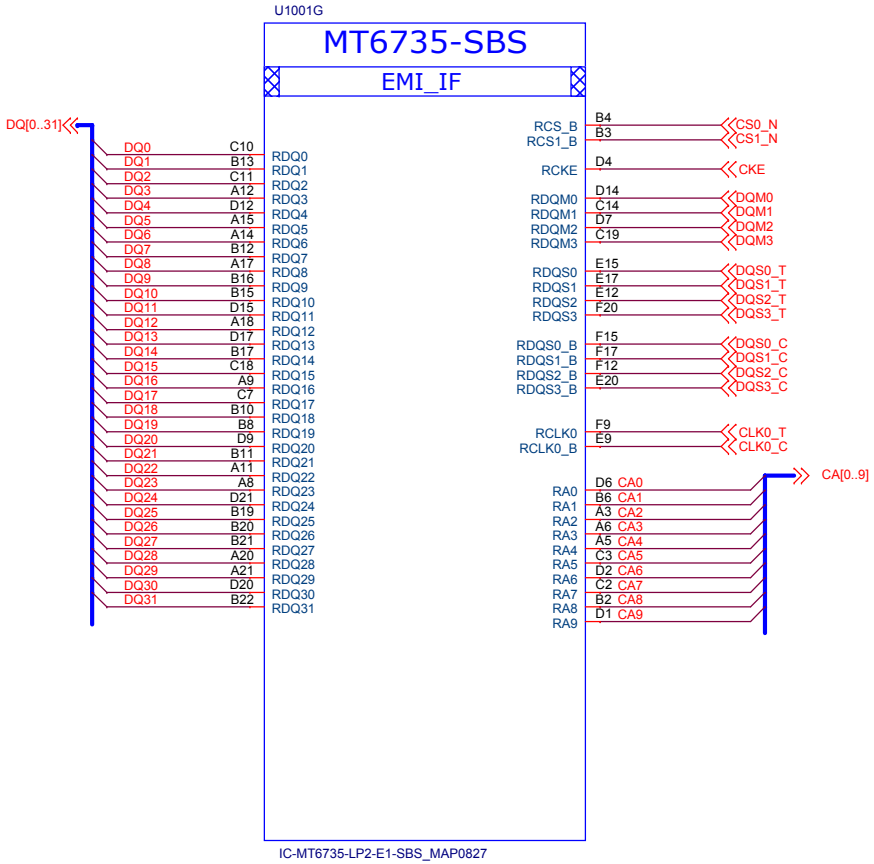


Schematic design notice of "12_BB_2" page.

Note 12-1: MSDC2 Pin should be NC (No Connection) for MT6735M & MT6735P

Note 12-2: MT6735M & MT6735P does Not have CMMCLK1 function

Please refer to MT6735M/P Design Notice for details


U1001G
MT6735-SBS
EMI_IF
DQ[0..31]
DQ0 C10 RDQ0
DQ1 B13 RDQ1
DQ2 C11 RDQ2
DQ3 A12 RDQ3
DQ4 D12 RDQ4
DQ5 A15 RDQ5
DQ6 A14 RDQ6
DQ7 B12 RDQ7
DQ8 A17 RDQ8
DQ9 B16 RDQ9
DQ10 B15 RDQ10
DQ11 D15 RDQ11
DQ12 A18 RDQ12
DQ13 D17 RDQ13
DQ14 B17 RDQ14
DQ15 C18 RDQ15
DQ16 A9 RDQ16
DQ17 C7 RDQ17
DQ18 B10 RDQ18
DQ19 B8 RDQ19
DQ20 D9 RDQ20
DQ21 B11 RDQ21
DQ22 A11 RDQ22
DQ23 A8 RDQ23
DQ24 D21 RDQ24
DQ25 B19 RDQ25
DQ26 B20 RDQ26
DQ27 B21 RDQ27
DQ28 A20 RDQ28
DQ29 A21 RDQ29
DQ30 D20 RDQ30
DQ31 B22 RDQ31
RCS_B B4 CS0_N
RCS1_B B3 CS1_N
RCKE D4 CKE
RDQM0 D14 DQM0
RDQM1 C14 DQM1
RDQM2 D7 DQM2
RDQM3 C19 DQM3
RDQS0 E15 DQS0_T
RDQS1 E17 DQS1_T
RDQS2 E12 DQS2_T
RDQS3 F20 DQS3_T
RDQS0_B F15 DQS0_C
RDQS1_B F17 DQS1_C
RDQS2_B F12 DQS2_C
RDQS3_B E20 DQS3_C
RCLK0 F9 CLK0_T
RCLK0_B E9 CLK0_C
CA[0..9]
RA0 D6 CA0
RA1 B6 CA1
RA2 A3 CA2
RA3 A6 CA3
RA4 A5 CA4
RA5 C3 CA5
RA6 D2 CA6
RA7 C2 CA7
RA8 B2 CA8
RA9 D1 CA9
IC-MT6735-LP2-E1-SBS_MAP0827

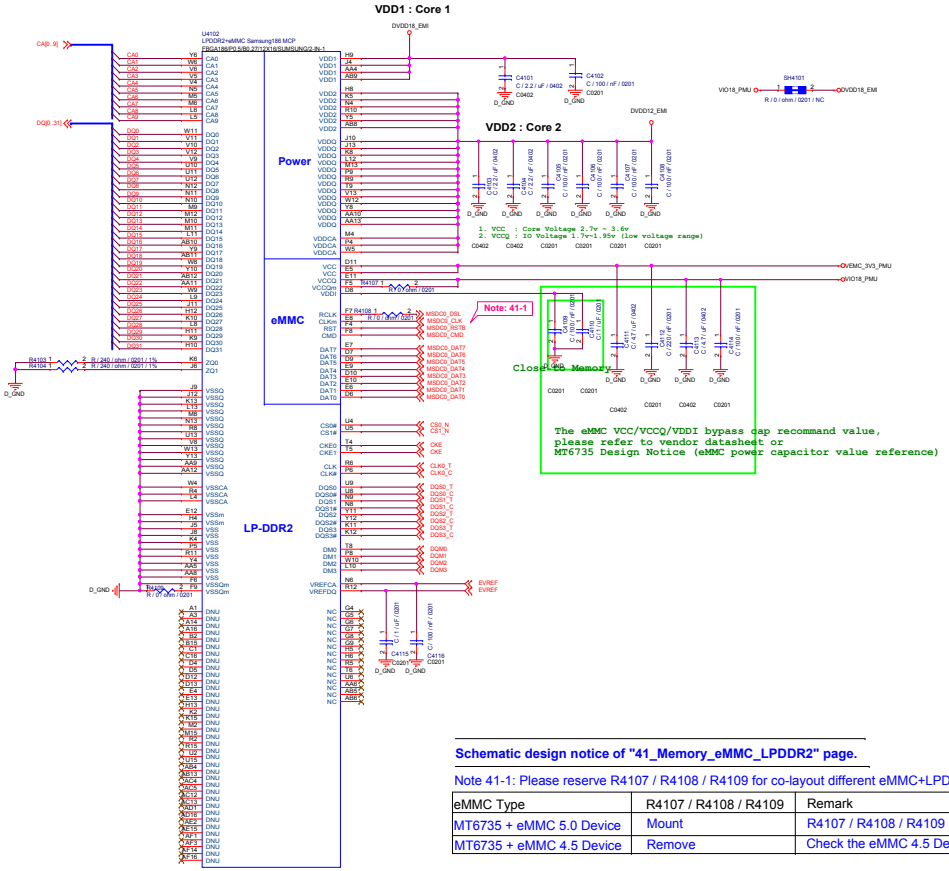
Connect to AP	
DQ[0..31]	DQ[0..31]
CA[0..9]	CA[0..9]
CS0_N	CS0_N
CS1_N	CS1_N
CKE	CKE
DQM0	DQM0
DQM1	DQM1
DQM2	DQM2
DQM3	DQM3
DQS0_C	DQS0_C
DQS1_C	DQS1_C
DQS2_C	DQS2_C
DQS3_C	DQS3_C
DQS0_T	DQS0_T
DQS1_T	DQS1_T
DQS2_T	DQS2_T
DQS3_T	DQS3_T
CLK0_T	CLK0_T
CLK0_C	CLK0_C
VREF_CA	VREF_CA
VREF_DQ	VREF_DQ
MSDC0_RSTB	MSDC0_RSTB
MSDC0_CMD	MSDC0_CMD
MSDC0_CLK	MSDC0_CLK
MSDC0_DSL	MSDC0_DSL
MSDC0_DAT0	MSDC0_DAT0
MSDC0_DAT1	MSDC0_DAT1
MSDC0_DAT2	MSDC0_DAT2
MSDC0_DAT3	MSDC0_DAT3
MSDC0_DAT4	MSDC0_DAT4
MSDC0_DAT5	MSDC0_DAT5
MSDC0_DAT6	MSDC0_DAT6
MSDC0_DAT7	MSDC0_DAT7

Power I/F	
VIO18_PMU	VIO18_PMU
VEMC_3V3_PMU	VEMC_3V3_PMU
DVDD12_EMI	DVDD12_EMI

eMMC+LPDDR2

162/186 Ball, 0.5mm pitch

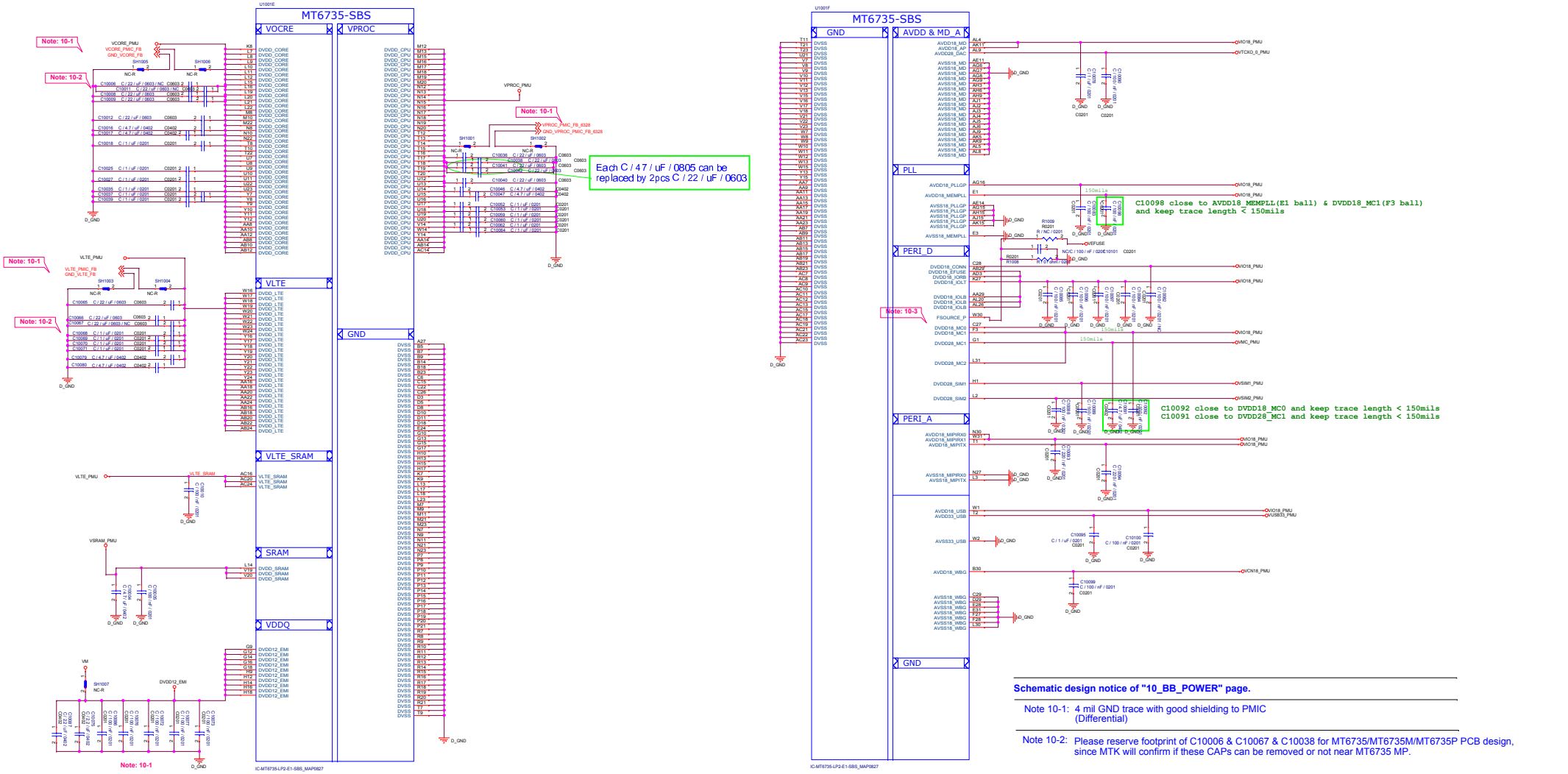
VDD1=1.8V
VDD2=1.20V
VDDCA=1.2V
VDDQ= 1.20V



Schematic design notice of "41_Memory_eMMC_LPDDR2" page.

Note 41-1: Please reserve R4107 / R4108 / R4109 for co-layout different eMMC+LPDDR2 Type

eMMC Type	R4107 / R4108 / R4109	Remark
MT6735 + eMMC 5.0 Device	Mount	R4107 / R4108 / R4109
MT6735 + eMMC 4.5 Device	Remove	Check the eMMC 4.5 Device, if the F5/F7/F9 Ball are real NC, the resistor cam be mounted



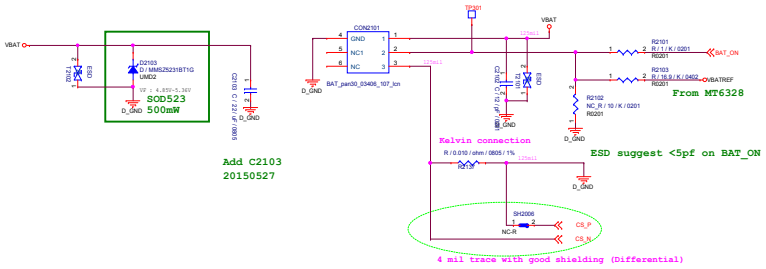
Schematic design notice of "10_BB_POWER" page.

Note 10-1: 4 mil GND trace with good shielding to PMIC (Differential)

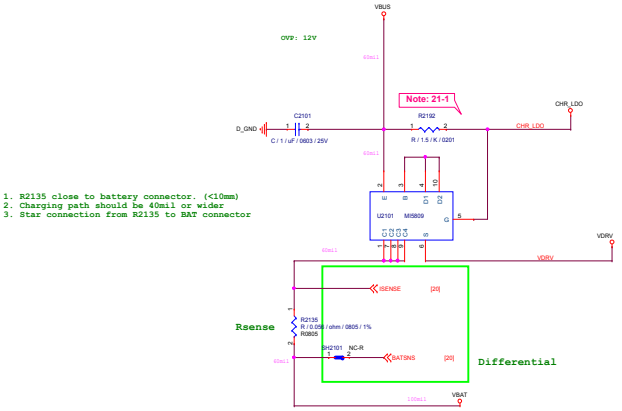
Note 10-2: Please reserve footprint of C10006 & C10067 & C10038 for MT6735/MT6735M/MT6735P PCB design, since MTK will confirm if these CAPs can be removed or not near MT6735 MP.

Note 10-3: FSOURCE_P(EFUSE)
(1)FSOURCE_P EFUSE power(VEFUSE) should be only for EFUSE usage(not share with other application)
(2)W/I EFUSE program, VEFUSE need 1uF bypass cap (pls refer to "LDO output voltage/current table")
(3)W/O EFUSE program, VEFUSE bypass cap should be NC.

BATTERY CONNECTOR



Pulse Charger



1. R2135 close to battary connector. (<10mm)
2. Charging path should be 40mil or wider
3. Star connection from R2135 to BAT connector

Schematic design notice of "21_POWER_TBD" page.

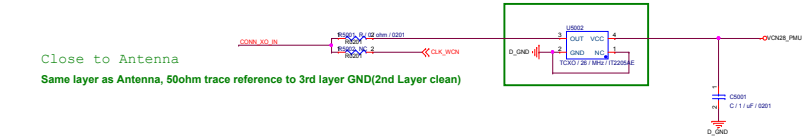
Note 21-1: Connect VBUS to MT6328.P3 by series connection with a 1.5K resistor for internal or external charger design.

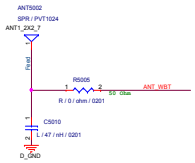
GPS co-VCTCXO: Suggest to reserve this option circuit,
since MTK will confirm if it's ok to implement this near MT6735 MP

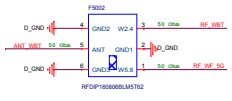
Reserve Keep out region from L1 to Main GND layer

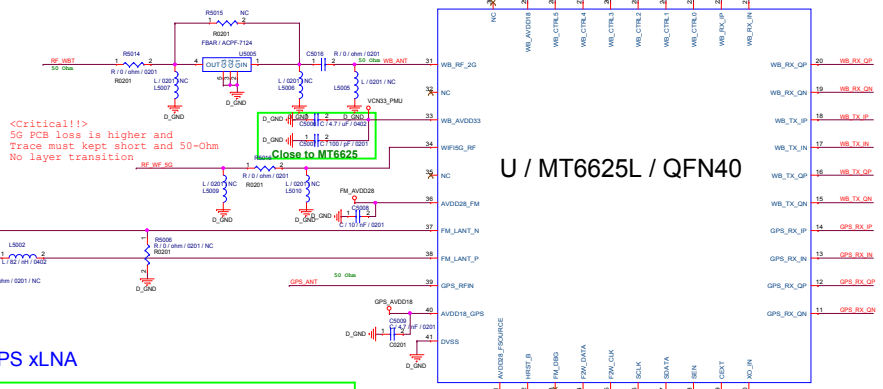
Close to Antenna

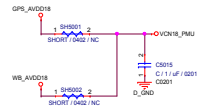
Same layer as Antenna, 50ohm trace reference to 3rd layer GND(2nd Layer clean)

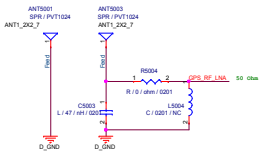






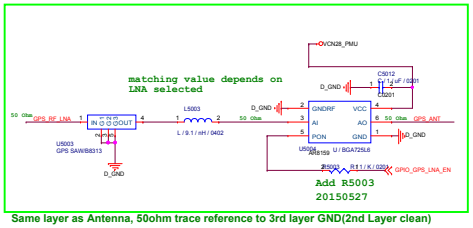






Close to ANT

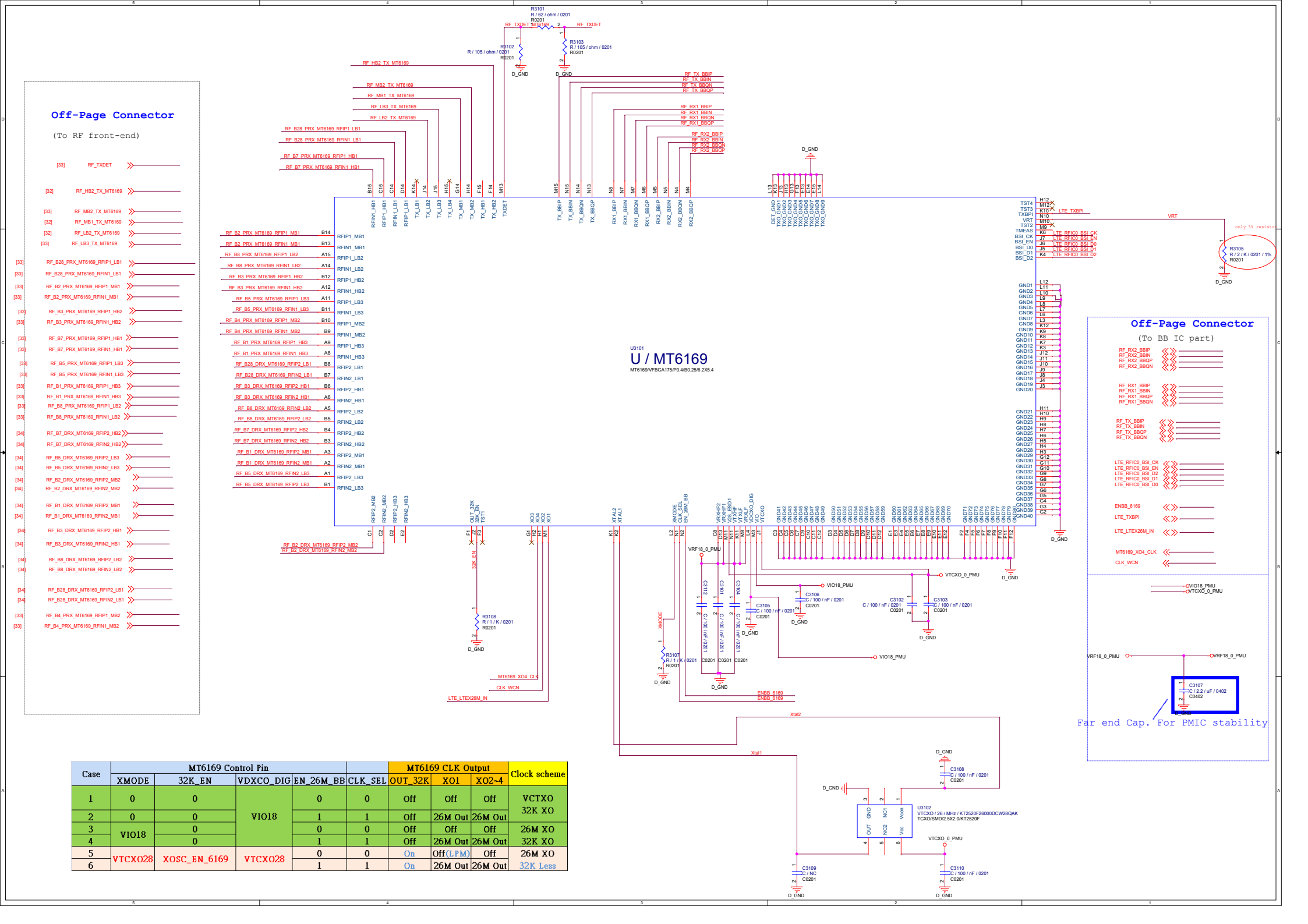
GPS xLNA



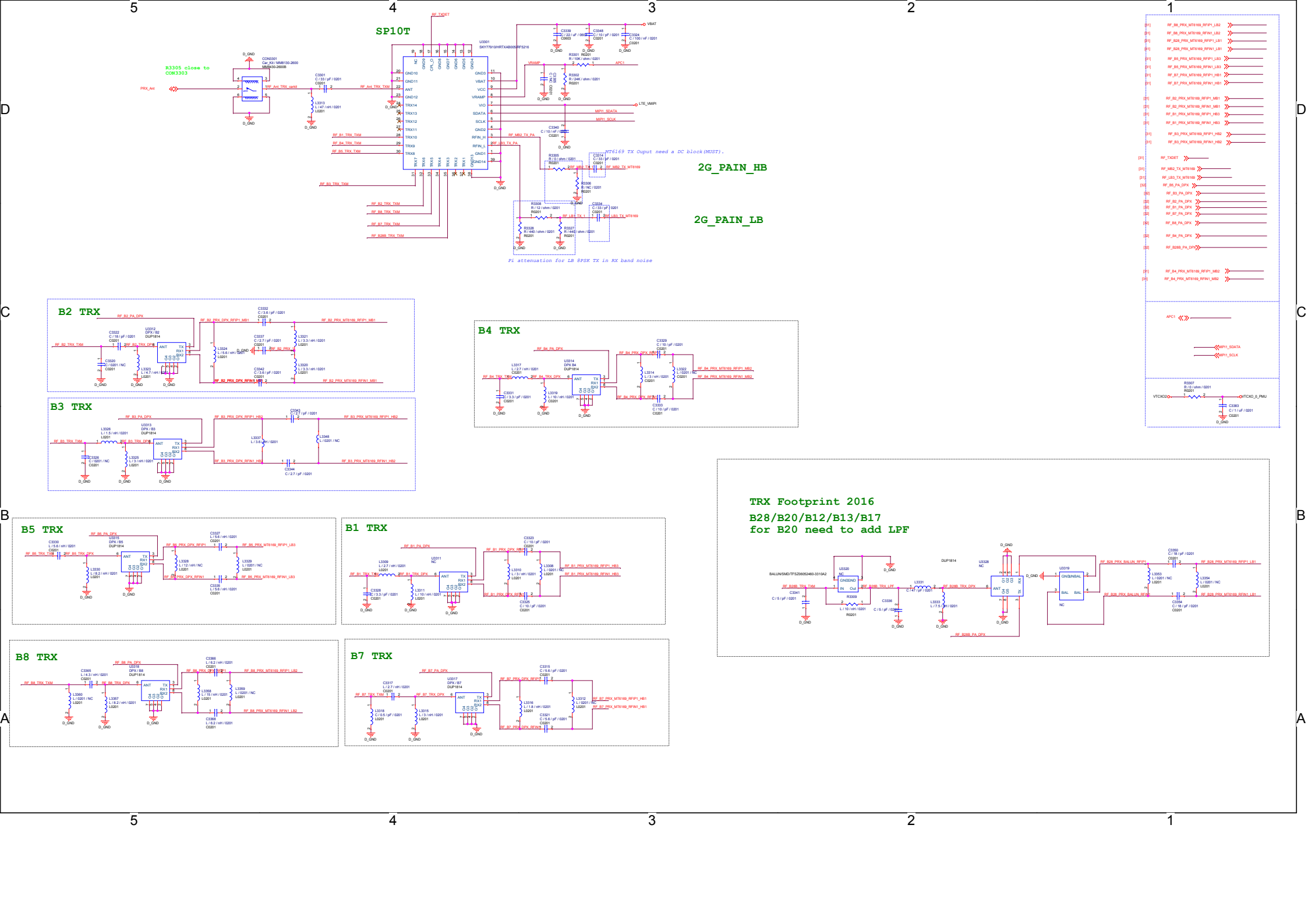
Same layer as Antenna, 50ohm trace reference to 3rd layer GND(2nd Layer clean)

WB_CTRL0 WB_CTRL1 WB_CTRL2 WB_CTRL3 WB_CTRL4 WB_CTRL5 CONN_SCLK CONN_SDATA CONN_SEN CONN_RSTB

GPS_RX_IP GPS_RX_IN GPS_RX_QP GPS_RX_QN F2W_CLK F2W_DATA WB_RX_IP WB_RX_IN WB_RX_QP WB_RX_QN WB_TX_IP WB_TX_IN WB_TX_QP WB_TX_QN CONN_XO_IN



Case	MT6169 Control Pin					MT6169 CLK Output			Clock scheme
	XMODE	32K_EN	VDXCO_DIG	EN_26M_BB	CLK_SEL	OUT_32K	XO1	XO2~4	
1	0	0	VIO18	0	0	Off	Off	Off	VCTXO 32K XO
2	0	0		1	1	Off	26M Out	26M Out	
3	VIO18	0		0	0	Off	Off	Off	26M XO
4		0		1	1	Off	26M Out	26M Out	32K XO
5	VTCXO28	XOSC_EN_6169	VTCXO28	0	0	On	Off(LPM)	Off	26M XO
6				1	1	On	26M Out	26M Out	32K Less


SP10T
2G_PAIN_HB
2G_PAIN_LB
MT6169 TX Ouput need a DC block(MUST).
P1 attenuation for LB 8PSK TX in RX band noise
B2 TRX
B4 TRX
B3 TRX
B5 TRX
B1 TRX
B8 TRX
B7 TRX
TRX Footprint 2016
B28/B20/B12/B13/B17
for B20 need to add LPF

DRX ANT: 1805-2690MHz

SP6T

DRX Car Kit

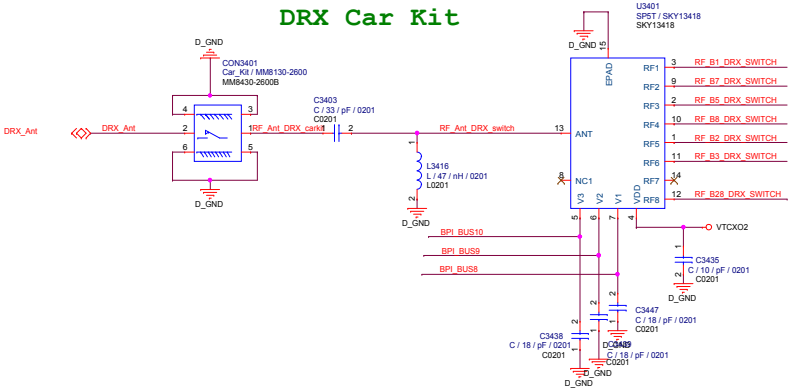
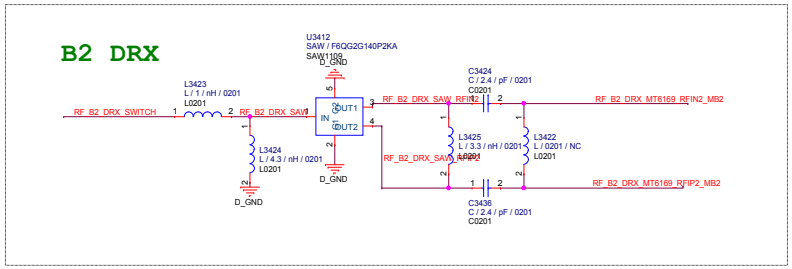


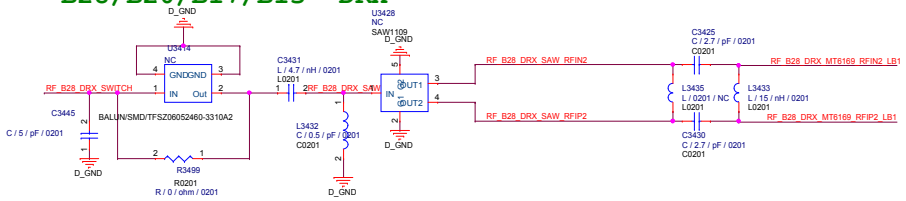
Table 4. SKY13415-485LF Control Logic

Control Pins			Switched RF Outputs					
V1 (Pin 7)	V2 (Pin 6)	V3 (Pin 5)	RF1 (Pin 3)	RF2 (Pin 9)	RF3 (Pin 2)	RF4 (Pin 10)	RF5 (Pin 1)	50 Ω
0	0	0	**Insertion Loss**	Isolation	Isolation	Isolation	Isolation	Isolation
0	0	1	Isolation	**Insertion Loss**	Isolation	Isolation	Isolation	Isolation
0	1	0	Isolation	Isolation	**Insertion Loss**	Isolation	Isolation	Isolation
0	1	1	Isolation	Isolation	Isolation	**Insertion Loss**	Isolation	Isolation
1	0	0	Isolation	Isolation	Isolation	Isolation	**Insertion Loss**	Isolation
1	0	1	Isolation	Isolation	Isolation	Isolation	Isolation	**50 Ω**
1	1	0	Isolation	Isolation	**Insertion Loss**	Isolation	**Insertion Loss**	Isolation
1	1	1	Shutdown mode					

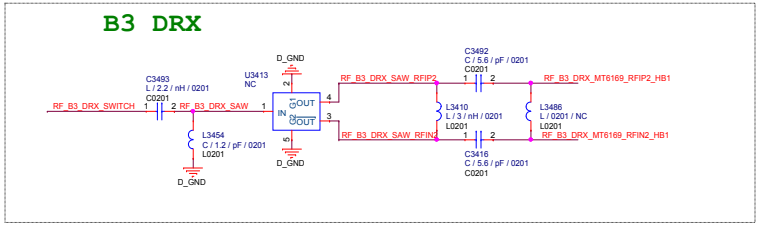
B2 DRX



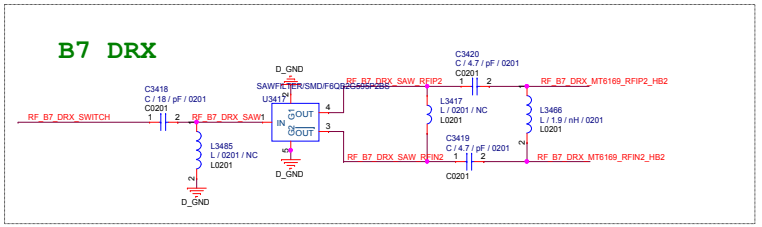
B28/B20/B17/B13 DRX



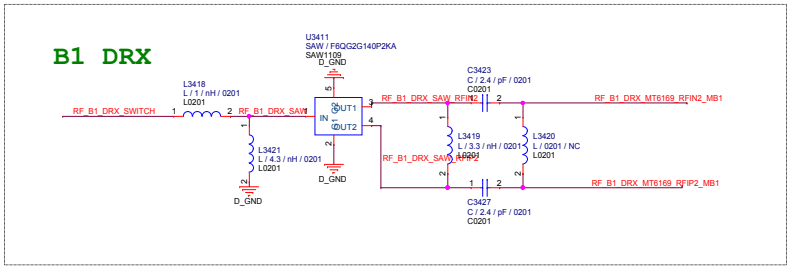
B3 DRX



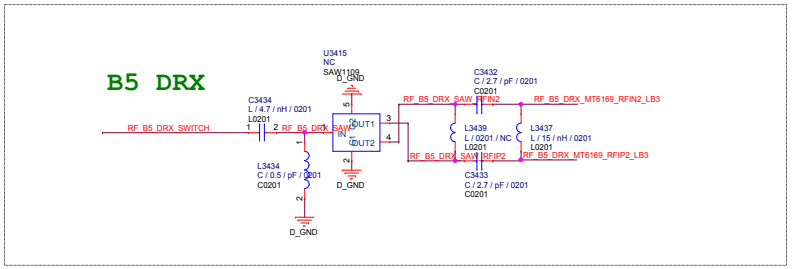
B7 DRX



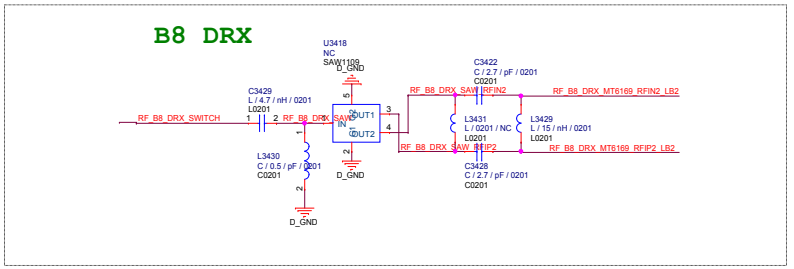
B1 DRX

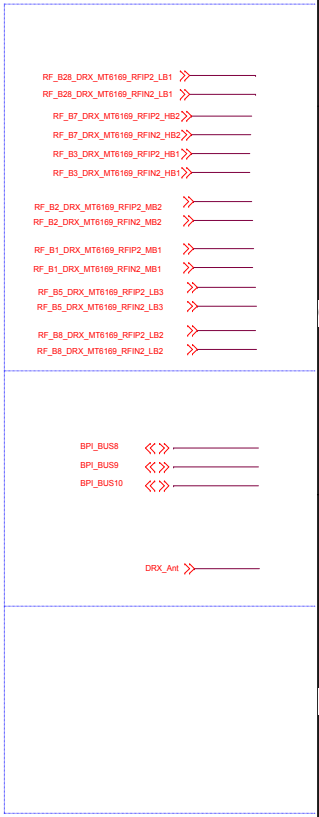


B5 DRX

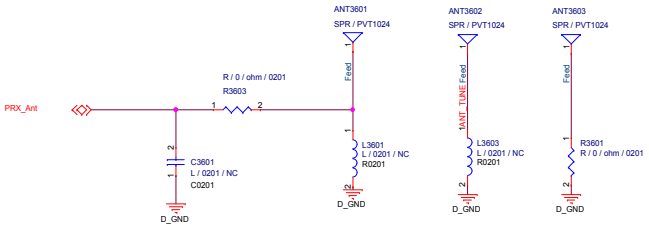


B8 DRX

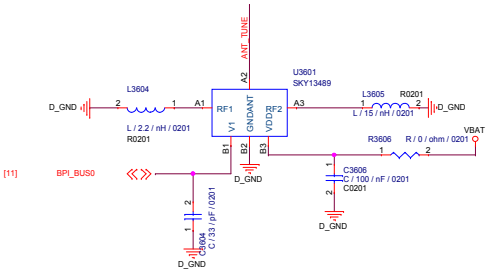




LTE Antenna

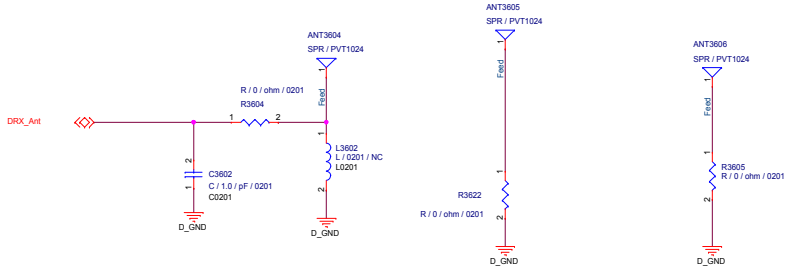


Antenna Tuner

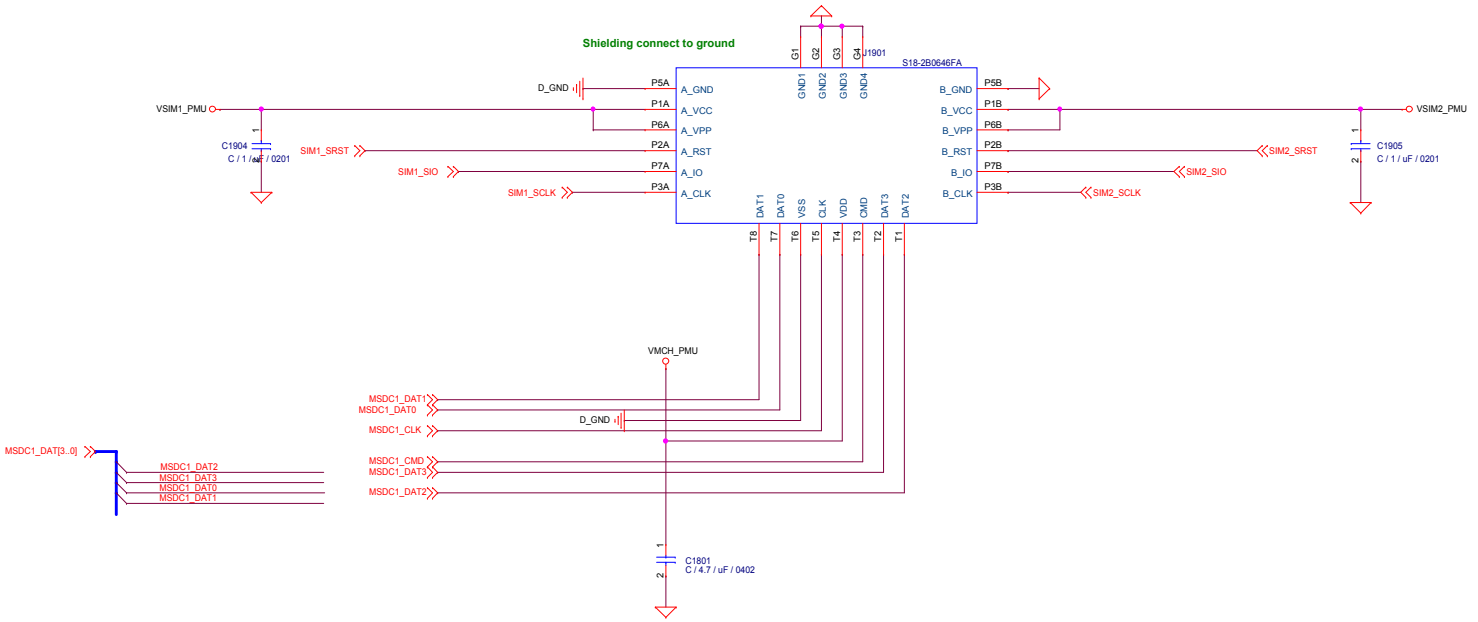


[Optional] Please Note That:
1. MT6735 can support GPIO Switch for antenna design, and it is optional function. Please decide to use it or not by each project consideration.
2. Please modify matching topology or GPIO Switch components position for diffetent antenna concepts.
3. Please fine ANT design guideline for details.

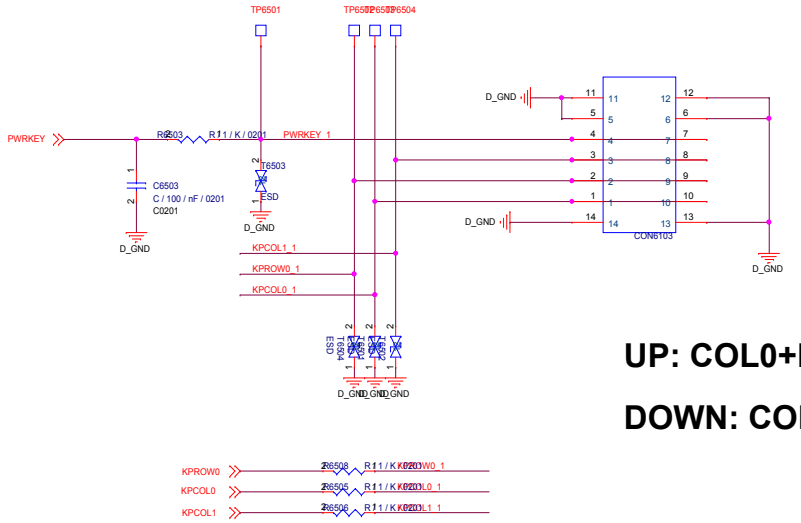
C2K/RxD Antenna



SIM1 & SIM2 & TFLASH



MC1CK with GND shield



Power Key / Key Pad

DO NOT put pull-up resistor on PWRKEY

Long press to shutdown (Force shutdown PMIC)	R6508	R6509	R6510
PWRKEY + HOMEKEY (default setting)	ON	NC	NC
	NC	ON	ON
PWERKEY only (setting by register)	NC	ON	NC

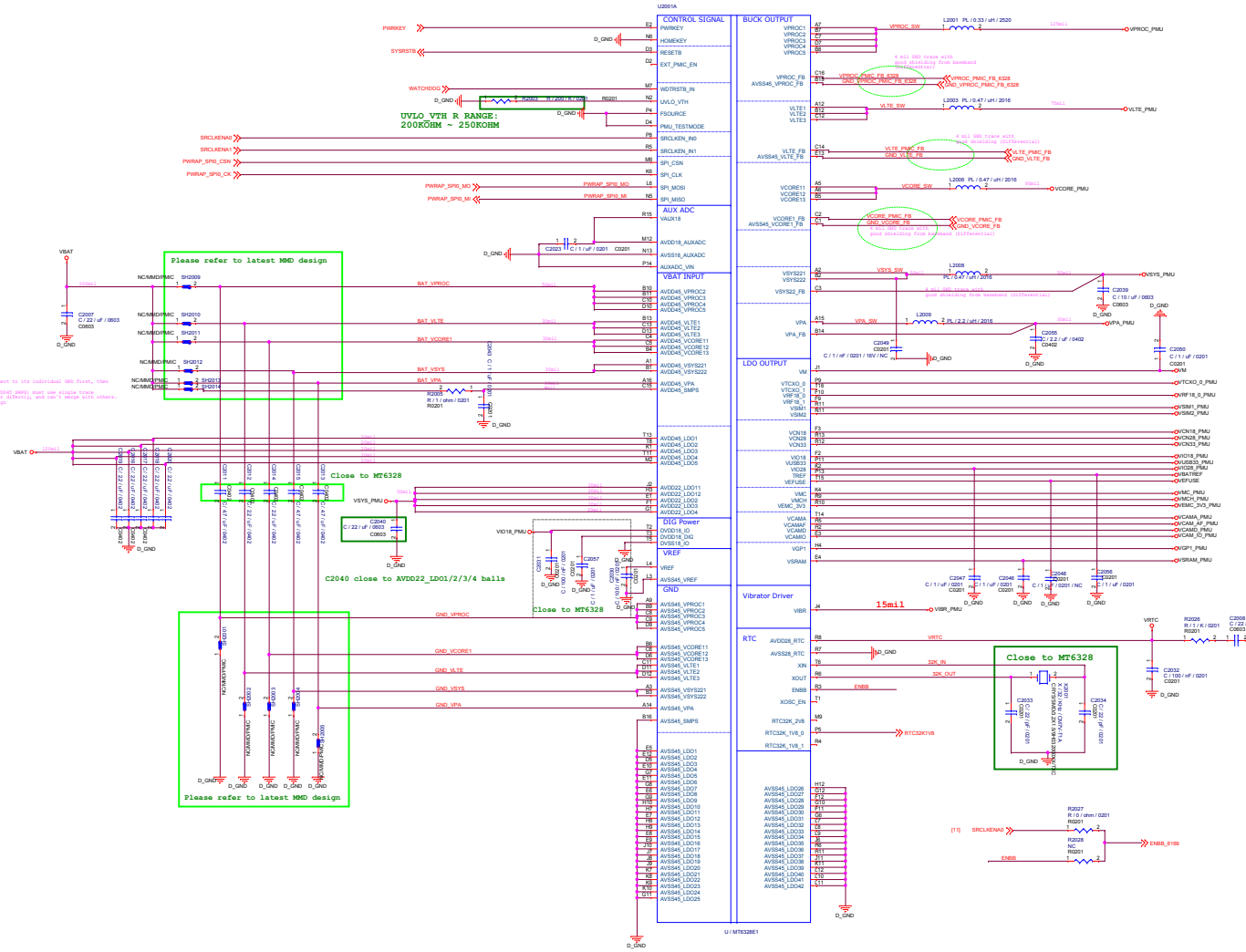
UP: COL0+ROW0

DOWN: COL1+ROW0

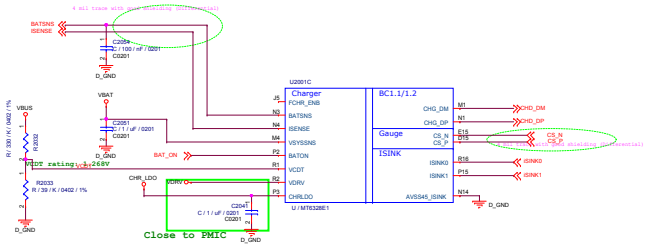
Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.

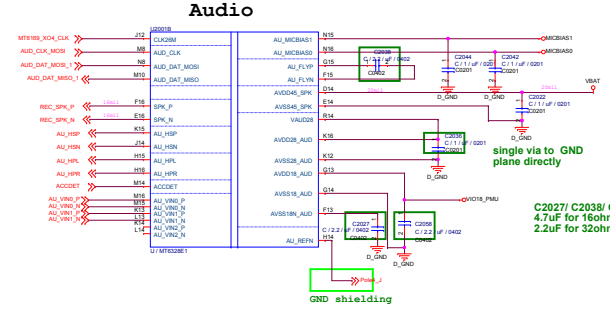
Note 65-1: DO NOT put pull-up resistor on PWRKEY

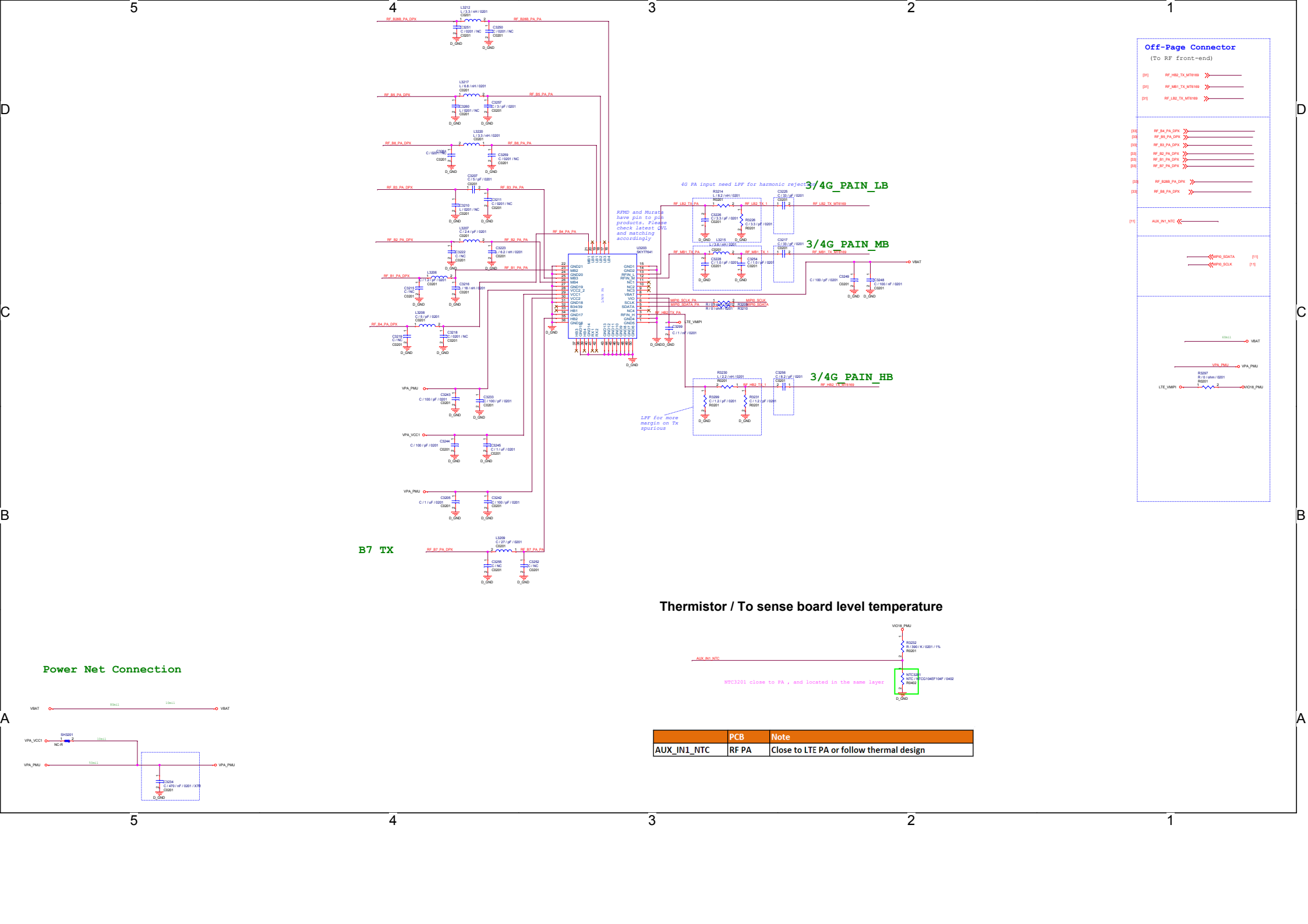
Note 65-2: Volume Up : KPROW0/KPCOL0
Volume Down : KPROW0/KPCOL1



Regulator	Output Voltage Range(V)	Output Current(mA)	Input Decoupling Cap	Output Decoupling	Note
VPROC	0.6~1.31	5000	>2.2uF	0.33uH+47uF*2+22uF	≧125mil
VCORE	0.6~1.31	3500	>2.2uF	0.47uH+47uF*2	≧88mil
VLTE	0.6~1.31	2800	>2.2uF	0.47uH+22uF*3	≧63mil
VSYS	2	1900	>2.2uF	0.47uH+22uF+10uF	≧48mil
VPA	0.5~3.4	600	>4.7uF	2.2uH+2.2uF+2.2uF	≧30mil
VM	1.24/1.39/1.54	1000		9.4uF~10uF	L/W=1500mil/25mil
VTCXO_0	2.8	40		1uF~3uF	L/W=2800mil/6mil
VTCXO_1	2.8	40		1uF~3uF	L/W=2800mil/6mil
VRF18_0	1.825	350		2.2uF~`3.3uF	L/W=2800mil/10mil
VRF18_1	1.2/1.3/1.5/1.825	300		2.2uF~`3.3uF	L/W=2800mil/10mil
VSIM1	1.7/1.8/1.86/2.76/3.0/3.1	50		1uF~3uF	L/W=2800mil/6mil
VSIM2	1.7/1.8/1.86/2.76/3.0/3.1	50		1uF~3uF	L/W=2800mil/6mil
VCN18	1.8	150		1uF~3uF	L/W=2800mil/10mil
VCN28	2.8	40		1uF~3uF	L/W=2800mil/6mil
VCN33	3.0/3.1/3.2/3.3/3.4/3.5/3.6	350		4.7uF~5uF	L/W=2800mil/12mil
VIO18	1.8	600		2.2uF~14uF	L/W=2800mil/20mil
VUSB33	3.3	20		1uF~3uF	L/W=2800mil/6mil
VIO28	2.8	200		2.2uF~6.6uF	L/W=2800mil/10mil
VEFUSE	1.8/1.9/2.0/2.1/2.2	200		1uF~3uF	L/W=2800mil/10mil
VMC	1.8/2.9/3.0/3.3	200		1uF~4.7uF	L/W=2800mil/10mil
VMCH	2.9/3.0/3.3	800		4.7uF~7uF	L/W=2800mil/20mil
VEMC_3V3	2.9/3.0/3.3	400		4.7uF~7uF	L/W=2800mil/12mil
VCAMA	1.5/1.8/2.5/2.8	200		2uF~3.3uF	L/W=2800mil/10mil
VCAMAF	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	200		2uF~3.3uF	L/W=2800mil/10mil
VCAMD	0.9/1.0/1.1/1.22/1.3/1.5	500		4.4uF~13.2uF	L/W=2800mil/16mil
VCAMIO	1.2/1.3/1.5/1.8	200		1uF~3uF	L/W=2800mil/10mil
VGP1	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200		1uF~3uF	L/W=2800mil/10mil
VSRAM	0.6~1.31	400		4.7uF~7uF	L/W=2800mil/12mil
VIBR	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	100		1uF~3uF	L/W=2800mil/8il
VAUX18	1.8	40		1uF~3uF	L/W=2800mil/6il
VAUD28	2.8	40		1uF~3uF	L/W=2800mil/6il
DVDD18_DIG	1.8	20		1uF	L/W=800mil/4il
VRTC	2.8	2		0.1uF	L/W=800mil/4il







	PCB	Note
AUX_IN1_NTC	RF PA	Close to LTE PA or follow thermal design