WLAN6060 Embedded Module
Data Sheet

09/27/2002
(Preliminary)

Confidential Information

WLAN6060 Embedded Module Document Revision Control

Revision	Date	Author	Engineering Approval	Marketing Approval	Operation Approval	Mark
Preliminary	09/27/2002	PG	KS	AM	RC	

WLAN6060 Product Series

Product	**Footprint**	**I/O to Host**	**I/O to RF**	**Antenna**
WLAN6060BB Embedded Module	BGA/SMT	CF/PCMCIA	Coaxial Connector	External antenna required
WLAN6060EB Embedded Module	60 pin interboard connector	CF/PCMCIA	Coaxial Connector	External antenna required
WLAN6060SD Network Interface Card	SDIO	SDIO	Internal	No external antenna required

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1. Architecture

Block Diagram

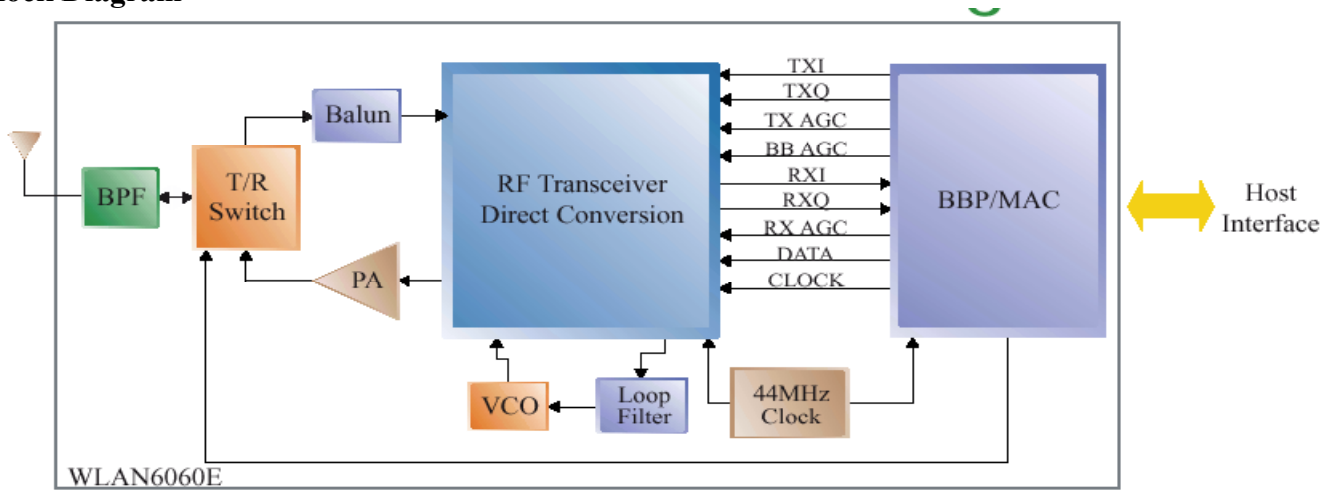


Figure 1. WLAN6060BB(EB) Block Diagram

The design is robust. Utilizing separate chips for the Radio, Base band, and VCO functions enables SyChip to deliver a reliable, consistent product.

The RF Transceiver integrated circuit includes an LNA, transmit pre-amplifier, quadrature up/down converter, synthesizer, low pass filter, and RX amplifier. It utilizes Direct Conversion technology, eliminating the need for intermediate-frequency mixer(s), amplifier and filter components.

The versatile design of the WLAN6060BB(EB) enables programming of the RF channel frequency from 2.4 GHz to 2.5 GHz in steps of 1 MHz. This covers all of the RF channels frequencies specified in 802.11b standard.

The Baseband Processor is a highly integrated Baseband/MAC . The host interface supports PCMCIA, and CF card applications.

2. Functional Description

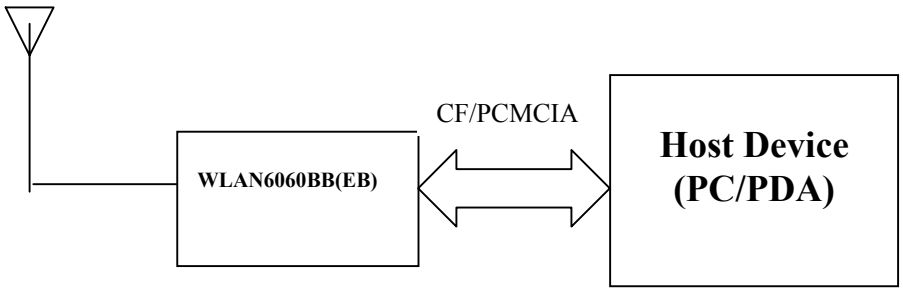


Figure 2. WLAN6060BB(EB) Functional Interface Diagram

WLAN6060BB(EB) is a completed WLAN(802.11b) system and only an external antenna needs to be implemented as a standalone unit or as a plug-and-play module in different applications.

The RF function provides programming of the RF channel frequency from 2.4 GHz to 2.5 GHz in steps of 1 MHz. This covers all of the RF channels frequencies specified in 802.11b standard.

The RF channel frequency for transmission and reception is stable with 25kHz of its final value, 0.75ms after reprogramming or switching from sleep mode to receive mode.

WLAN6060BB(EB) delivers the wireless connection with data rates of 1Mbps, 2Mbps, 5.5Mbps, and 11Mbps in various environments. A control circuit within the module selects the data rate and power level ensuring optimum performance at the lowest possible power levels at all times.

WLAN6060BB(EB) supports 802.11 WEP 64/128 bit security standard. Future versions will support LEAP and 802.1x.

WLAN6060BB(EB) currently supports Windows 2000/NT/XP and Win CE3.0 Operating System. Future versions will include Win CE.NET and Palm OS.

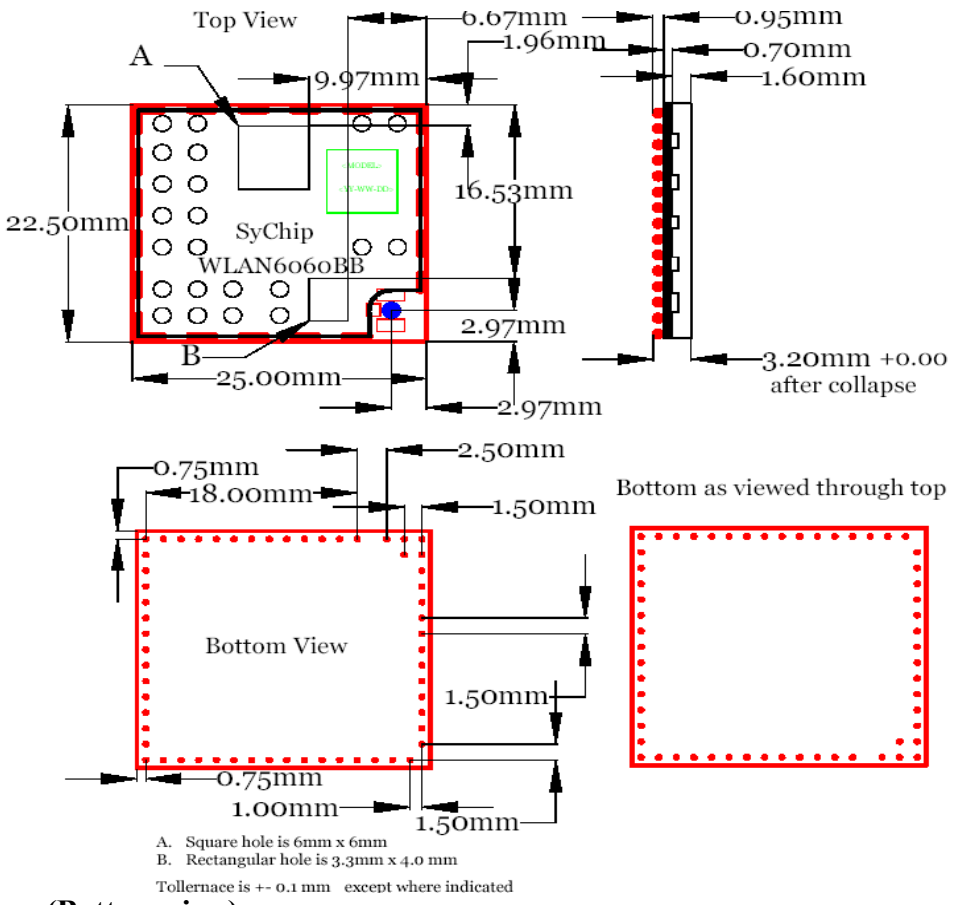
3. Specifications

DC Electrical Specifications					
Parameter	Condition	Min	Typical	Max	Units
Supply Voltage(Vcc)		3.0	3.3	3.6	V
Current (Receiving)	3.3V		TBD		mA
Current (Transmitting)	Pout = 12.5dBm @3.3V		TBD		mA
Current (Standby)	3.3V		TBD		mA
Current (Sleep)	3.3V		TBD		µA
Logic high input		0.7Vcc			V
Logic low input				0.3Vcc	V
Logic high output		Vcc – 0.2			V
Logic low output			0.1	0.2	V
Operating Temperature		-30		+70	°C
Storage Temperature		-40		+85	°C
I/O Interface	PCMCIA/CF				
RX/TX Specifications					
Physical Layer Data Rate			1		Mbps
			2		Mbps
			5.5		Mbps
			11		Mbps
Frequency Range		2400		2500	MHz
Step Size			1		MHz
Output Power	3.3V, 25°C	12.5			dBm
Transmit Spectral Mask	1st Side-lobe, 3.3V	-30			dBc
Transmit Spectral Mask	2nd Side-lobe, 3.3V	-50			dB
Sensitivity	1Mbps, FER 8%, 3.3V	-80*	-90		dBm
	2Mbps, FER 8%, 3.3V	-80*	-88		dBm
	5.5Mbps, FER 8%, 3.3V	-76*	-87		dBm
	11Mbps, FER 8%, 3.3V	-76*	-83		dBm

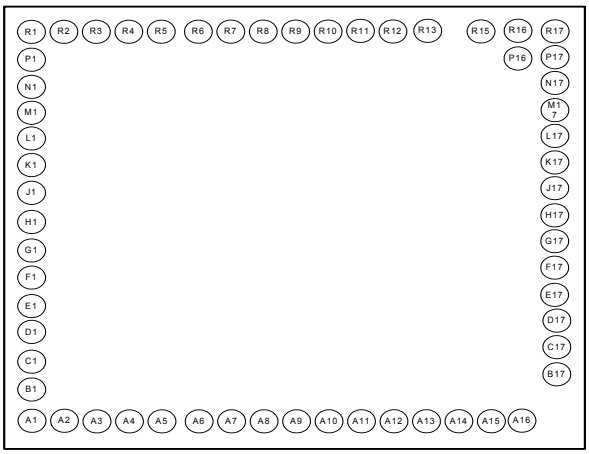
* IEEE802.11 compliant

Dimension

a) BGA version WLAN6060BB



Pin Definitions (Bottom view)

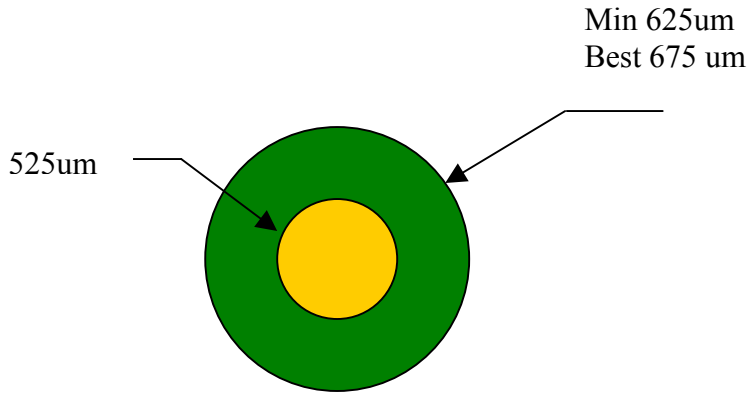


Pin Number	Pin Name	Description
R4	HD0	PC Card data bus
R5	HD1	PC Card data bus
R6	HD2	PC Card data bus
R7	HD3	PC Card data bus
R8	HD4	PC Card data bus
R9	HD5	PC Card data bus
R10	HD6	PC Card data bus
R11	HD7	PC Card data bus
R12	HD8	PC Card data bus
K17	HD9	PC Card data bus
J17	HD10	PC Card data bus
H17	HD11	PC Card data bus
G17	HD12	PC Card data bus
F17	HD13	PC Card data bus
E17	HD14	PC Card data bus
D17	HD15	PC Card data bus
A7	HA0	PC Card address bus
A8	HA1	PC Card address bus
A9	HA2	PC Card address bus
A10	HA3	PC Card address bus
A11	HA4	PC Card address bus
A13	HA5	PC Card address bus
A14	HA6	PC Card address bus
A15	HA7	PC Card address bus
B17	HA8	PC Card address bus
C17	HA9	PC Card address bus
A5	HCE1_N	PC Card select, low byte
A4	HCE2_N	PC Card select, high byte
A3	HOE_N	PC Card output enable
A2	HIORD_N	PC Card I/O space read strobe
C1	HIOWR_N	PC Card I/O space write strobe
D1	HWE_N	PC Card memory attribute space write enable
E1	HIREQ_N	PC Card interrupt request
L1	RESET_N	Hardware reset. Self-asserted by internal pull-up at power-on. Clock signal CLKIN or XTALIN must be available before negation of reset. Value of MD[15:0] copied to MDIR[15:0] and various control register bits on the first MCLK following release of Reset.
F1	HWAIT_N	Host wait, asserted to indicate data transfer not completed and to force host bus wait states.
H1	HIMPACK_N	PC Card I/O decode confirmation
J1	HREG_N	PC Card attribute space select
K1	HSTSCHG_N	PC Card status change
B1	LED	LED Input
A1	GND	Ground
A6	GND	Ground
A12	GND	Ground
A16	GND	Ground
L17	GND	Ground
G1	GND	Ground
N17	GND	Ground
M17	GND	Ground
R16	GND	Ground

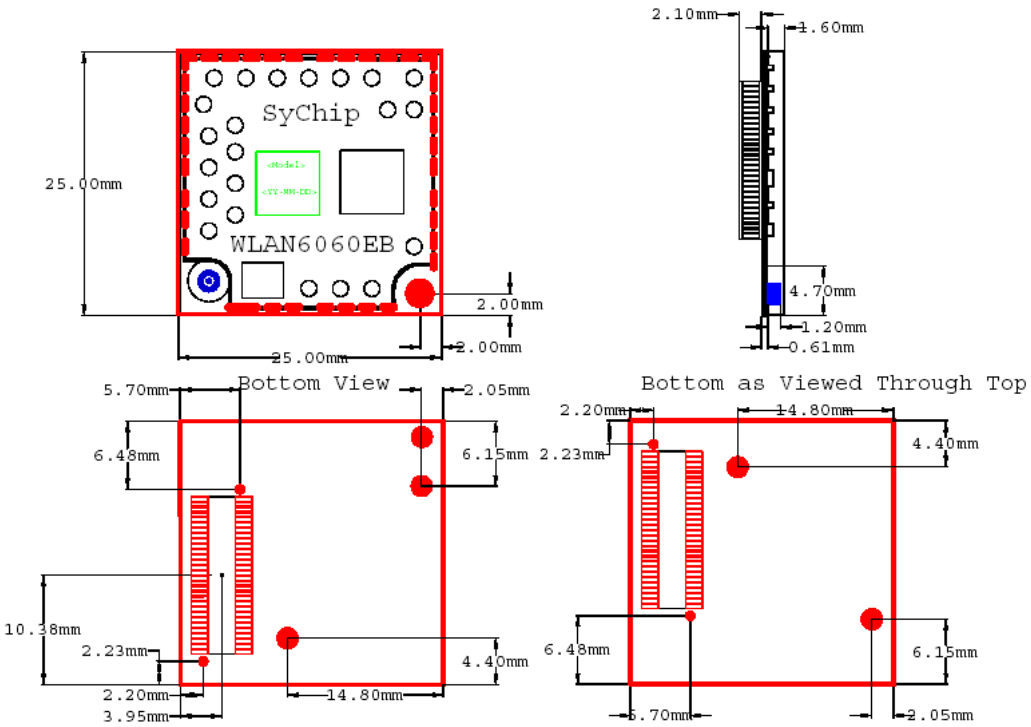
R17	GND	Ground
P16	GND	Ground
P17	GND	Ground
M1	GND	Ground
N1	GND	Ground
R3	GND	Ground
R13	GND	Ground
R15	GND	Ground
P1	VCC	Power Input (3.3V)
R1	VCC	Power Input (3.3V)
R2	VCC	Power Input (3.3V)

Suggested PCB PAD for WLAN6060BB module

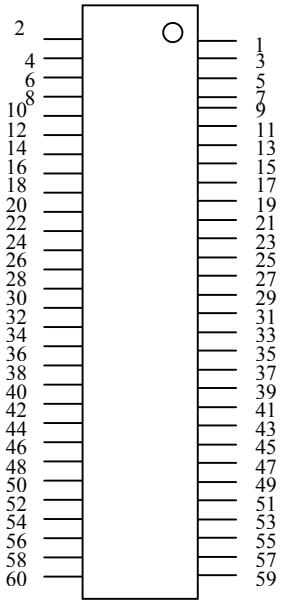
1. Solder mask defined PAD.
2. Copper pad: Min 625 um, best 675 um
3. Solder mask opening: 525 um
4. For Solder Mask:
    a. Very thin (Taiyo PSR4000)
    b. No solder mask undercut
5. Solder mask registration tolerance: 50um maximum



b) 60-pin connector version WLAN6060EB



Pin Definitions



Pin Number	Pin Name	Description
1	GND	Ground
2	GND	Ground
3	HD3	PC Card data bus
4	HD11	PC Card data bus
5	HD4	PC Card data bus
6	HD12	PC Card data bus
7	HD5	PC Card data bus
8	HD13	PC Card data bus
9	HD6	PC Card data bus
10	HD14	PC Card data bus
11	HD7	PC Card data bus
12	HD15	PC Card data bus
13	HCE1_N	PC Card select, low byte
14	HCE2_N	PC Card select, high byte
15	NC	Not Connected
16	GND	Ground
17	HOE_N	PC Card output enable
18	HIORD_N	PC Card I/O space read strobe
19	HA9	PC Card address bus
20	HIOWR_N	PC Card I/O space write strobe
21	HA8	PC Card address bus
22	HWE_N	PC Card memory attribute space write enable
23	HA7	PC Card address bus
24	HIREQ_N	PC Card interrupt request
25	VCC	Power Input (3.3V)
26	VCC	Power Input (3.3V)
27	HA6	PC Card address bus
28	NC	Not Connected
29	HA5	PC Card address bus
30	NC	Not Connected
31	HA4	PC Card address bus
32	RESET_N	Hardware reset. Self-asserted by internal pull-up at power-on. Clock signal CLKIN or XTALIN must be available before negation of reset. Value of MD[15:0] copied to MDIR[15:0] and various control register bits on the first MCLK following release of Reset.
33	HA3	PC Card address bus
34	HWAIT_N	Host wait, asserted to indicate data transfer not completed and to force host bus wait states.
35	HA2	PC Card address bus
36	HINPACK_N	PC Card I/O decode confirmation
37	HA1	PC Card address bus
38	HREG_N	PC Card attribute space select
39	HA0	PC Card address bus
40	NC	Not Connected
41	HD0	PC Card data bus
42	HSTSCHG_N	PC Card status change
43	HD1	PC Card data bus
44	HD8	PC Card data bus
45	HD2	PC Card data bus
46	HD9	PC Card data bus
47	GND	Ground
48	HD10	PC Card data bus

49	GND	Ground
50	GND	Ground
51	GND	Ground
52	GND	Ground
53	GND	Ground
54	GND	Ground
55	NC	Not Connected
56	NC	Not Connected
57	NC	Not Connected
58	NC	Not Connected
59	NC	Not Connected
60	NC	Not Connected

4. Technical Support

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